Monolayer Etching with Soft Plasmas

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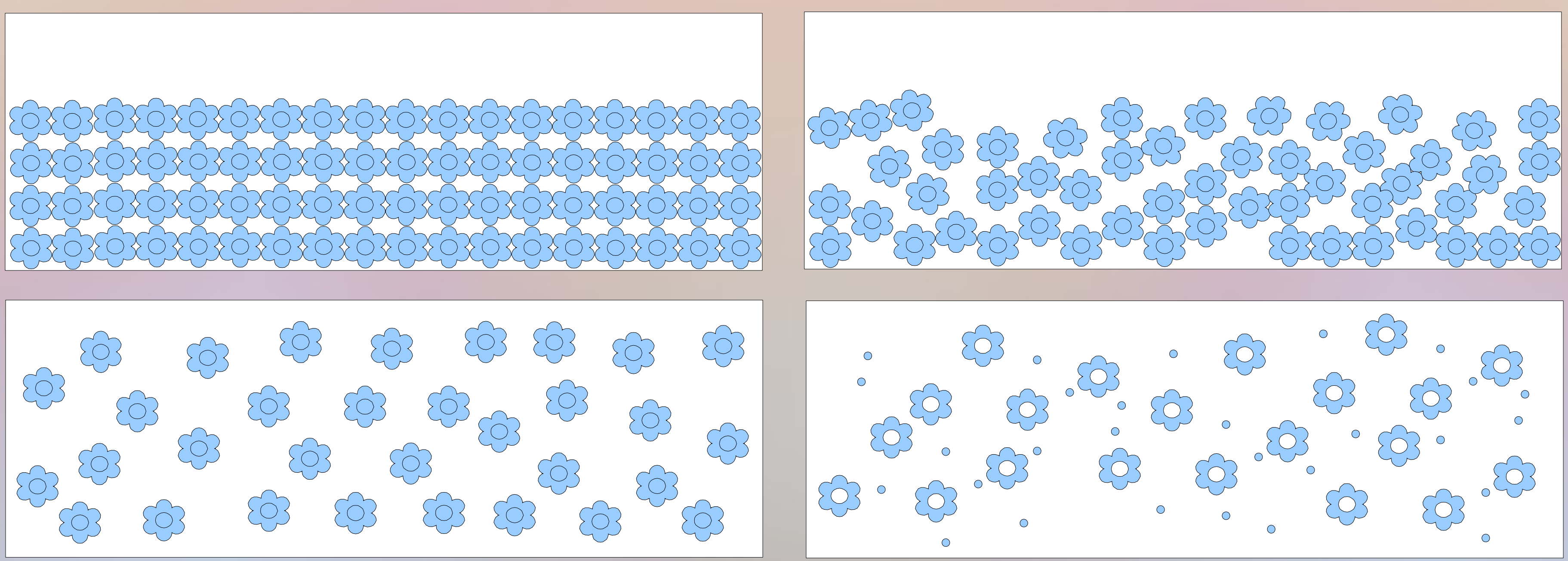
Monolayer Etching with Soft Plasmas

- Review of plasma technology and applications
- History of plasma etch in IC fabs
- Dennard Scaling leads to critical monolayers
- Chemistry provides selectivity
- Radial Line Slot Antenna (RLSA) source
- ICP source with source/bias sync
- Conclusions

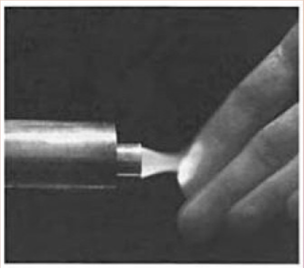
Plasma Technology and Applications

- Plasma is 4th state of matter
  - Free electrons and energetic ions
  - Interactions with surfaces inherent



Plasma Technology and Applications

- Free electrons, ions, radicals chemically active
- Plasmas for general lighting, industrial cleans, surface treatments



- Simple isotropic tools
- Early use in semiconductor fabs to remove residues and strip photoresist (a.k.a. "ash")
- "Barrel" batch reactors used up to 4" wafers

Plasma Etch History in IC Fabs

- Etching once was exclusively wet
  - Purely isotropic
  - Chemical sourcing and disposal costs
- Plasma etch explored at IDMs in 1970s
- OEMs start to provide new capabilities
  - 1979 Tegal releases single-wafer tool
  - 1981 Lam load-locks & automated recipes
- Rapid growth of applications in 1980s

Plasma Etch History in IC Fabs

- Single-wafer etchers, competing with batch, designed for high etch rates and throughput
- 1980s etch geometries 1-10 microns
- Single-wafer etch chambers designed with large vacuum pumps, showerheads, power supplies
- 2000s etch geometries 0.010-1 microns
  - Cluster tool robotics 100-200 wafers/hour
  - Retain ~1 μm/min. rates

Dennard Scaling led to Monolayers

- Moore's Law (#XDCRs/chip)...marketing
  - Larger chips
  - Design cleverness (e.g., DRAM 6T to 4T)
  - 2D shrinks (as per ITRS "nodes")
- Denard Scaling for 2D shrinks...engineering
  - 45 and 32nm IC nodes use monolayers
  - Legacy materials limits
- Monolayer etching with extreme selectivity critical

Dennard Scaling led to Monolayers

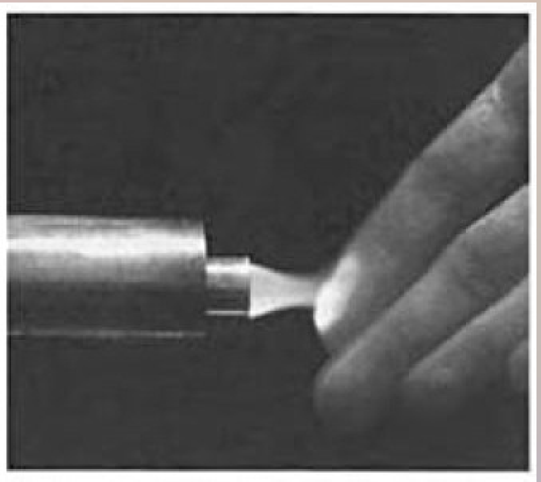
- Chamber architectures fine-tuned to PORs
- High etch-rate chambers and sub-systems limited in low etch-rates
- Neutral ion-beams limited in selectivity
- Etch isotropy essential
- Extensions of proven chambers and sub-systems (valves, pumps, chucks, etc.)

Dennard Scaling led to Monolayers

- Atomic-layer etch (ALE) processes explored by labs for R&D
- Comparable to atomic-layer deposition (ALD)
- Adsorb a precursor, then ΔT or ΔP or UV or ...
- Purely chemical reactions without ion bias
- Perhaps needed some year...
- ...fortunately not yet

Chemistry Provides Selectivity

- Downstream plasmas in cluster tools
  - Pre-clean chambers
  - Surface treatments
- Plasma ashers POR for resist removal
- Minimal directionality without bias

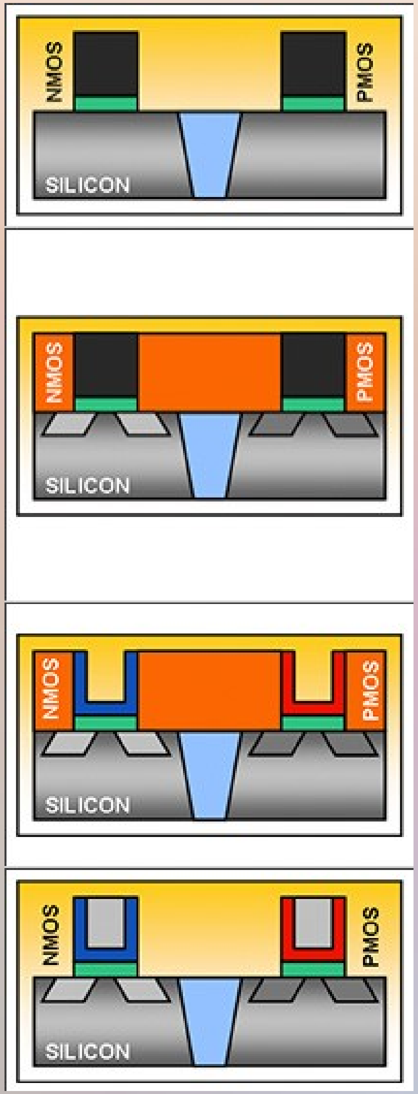


Chemistry Provides Selectivity

- Gate etch very complex even without HKMG
  - Si to SiNx, then to SiO2
  - SiO2 to Si, then to SiNx
  - SiNx to Si, then to SiO2
  - Organic to Si, then to SiNx, then to SiO2
- HKMG only adds more complexity in selectivity
- Active structures extraordinarily sensitive to topographic variability

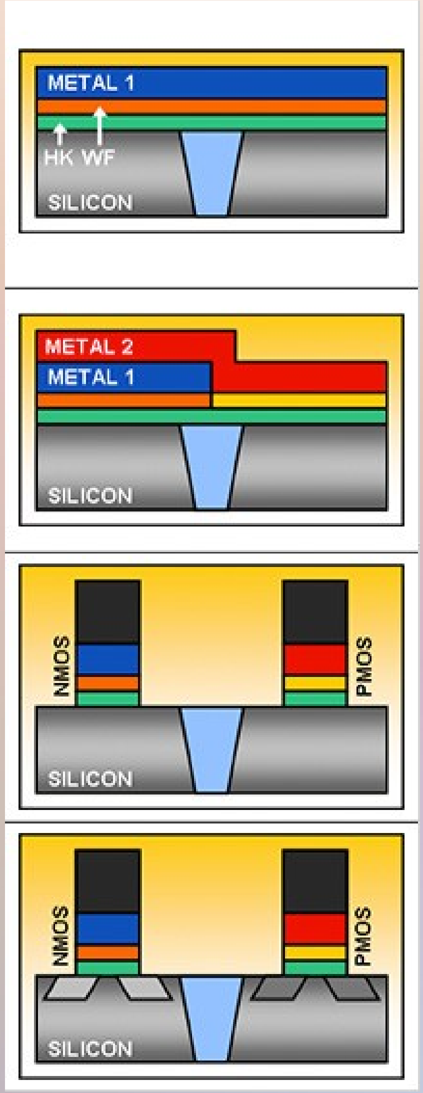
Chemistry Provides Selectivity

- HKMG "gate-last"
- Etch out dummy gate
- Selectivity control key



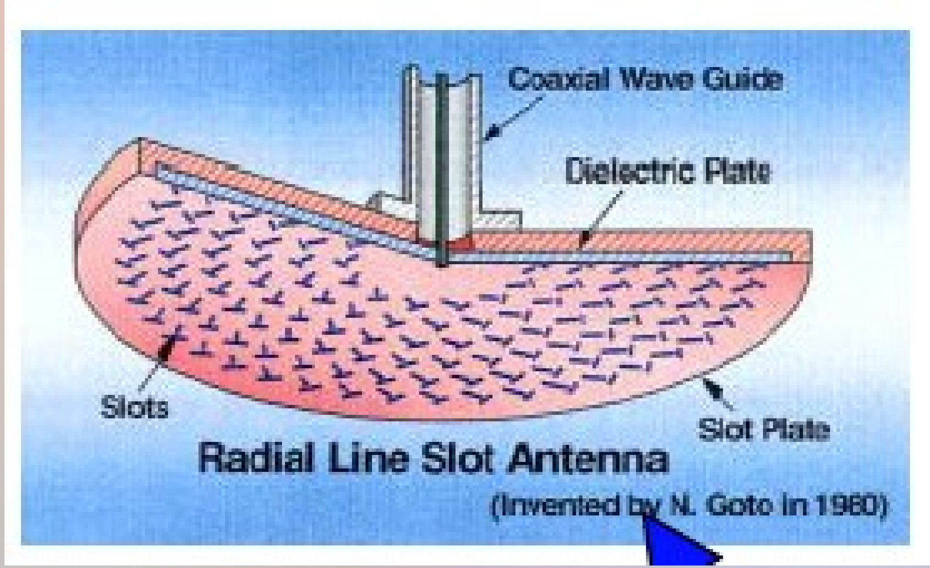
Chemistry Provides Selectivity

- HKMG “gate first”
- Etch Metal1 & WF1
- Etch gates with poly mask
- Serious selectivities
- Unforgiving precision needed
- WF thickness <1 nm



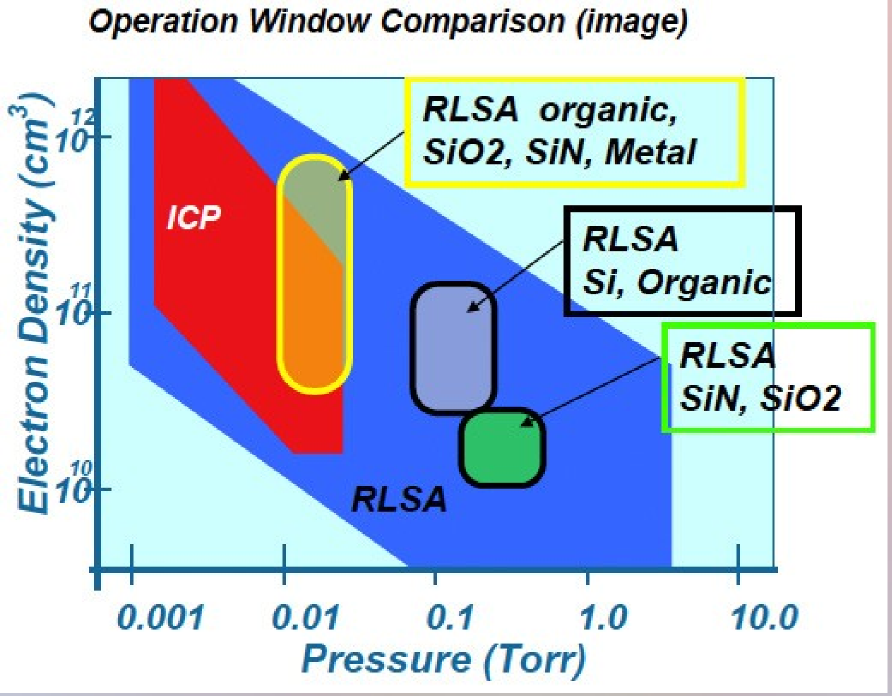
RLSA Plasma Source

- Radial Line Slot Antenna (RLSA) 2.45GHz source developed for various applications
- High Density and low electron temperature



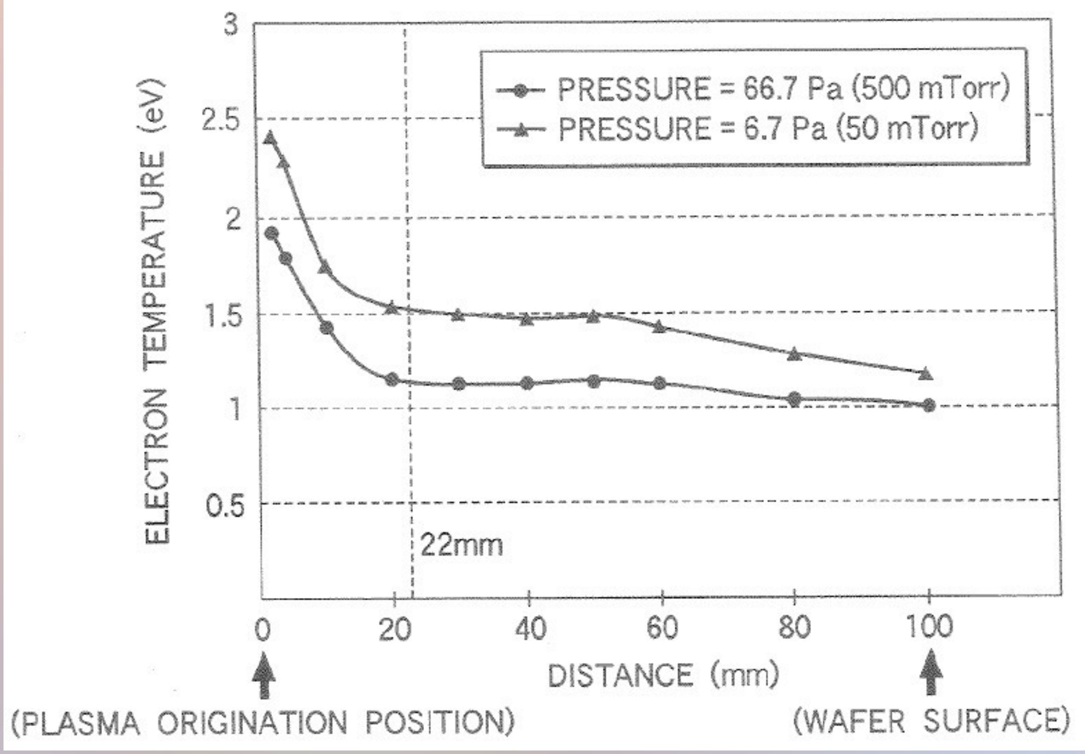
RLSA Plasma Source

- US Patent App. Pub. No.: US 2008/0142159 A1 Masaru Sasaki assigned to Tokyo Electron Ltd.
- High Density and low electron temperature



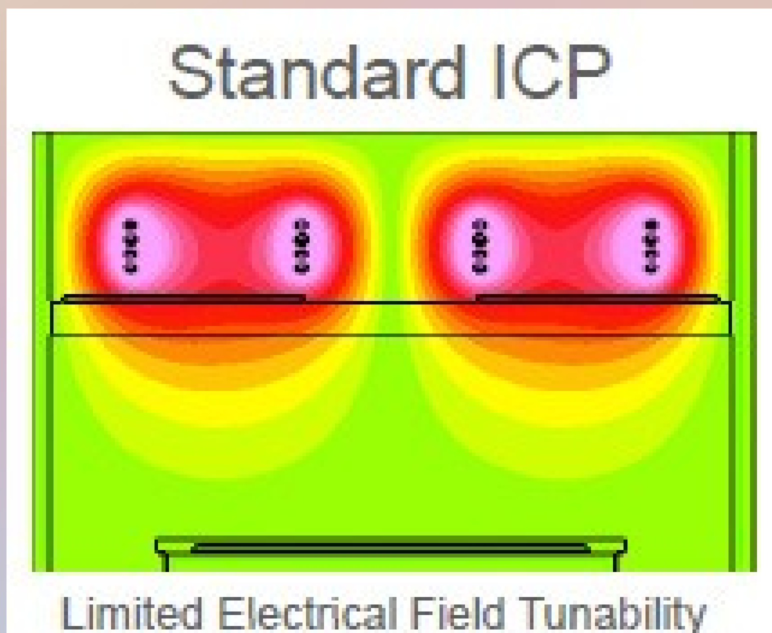
RLSA Plasma Source

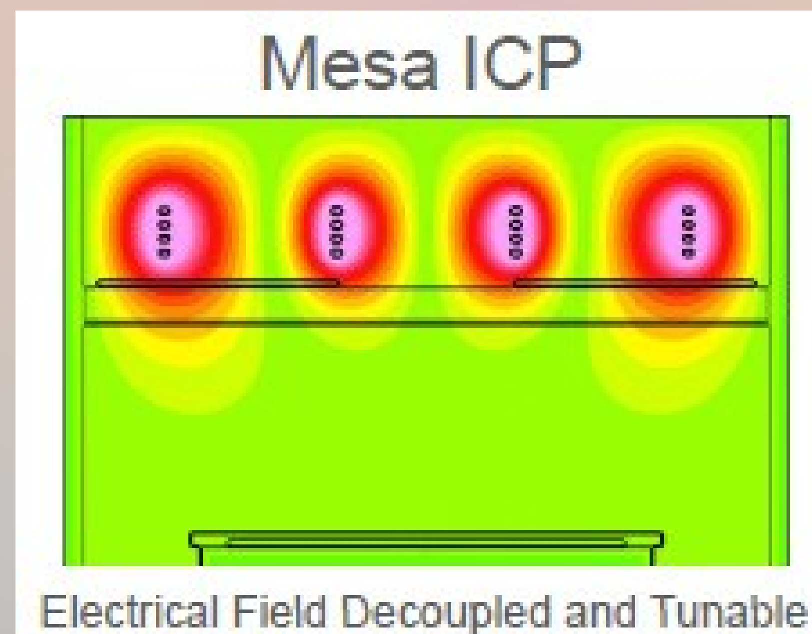
- Chemical dominance with many reactants
- Not “downstream” yet low ion bombardment
- “Soft” effects
- Low Te
- Bias possible



ICP with Source-Bias Sync

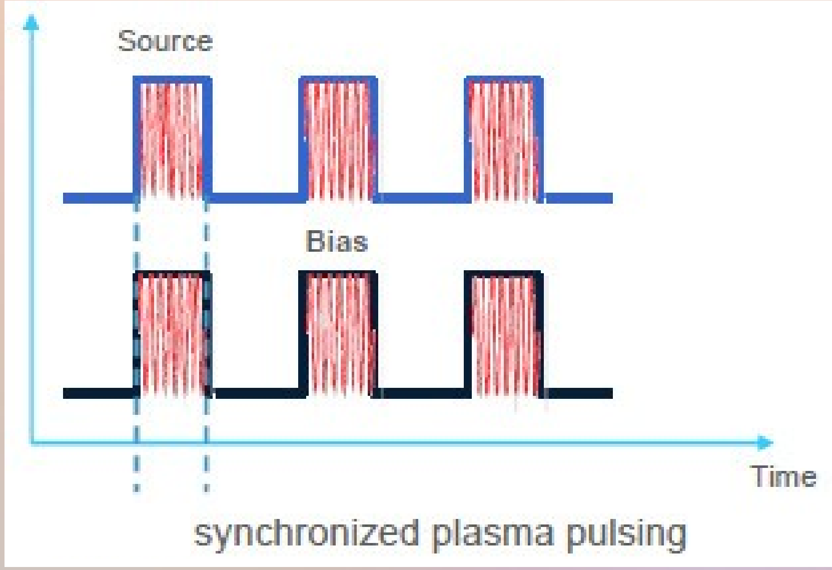
- ICP source coils for within wafer uniformity
- New "knob" to turn
- 1 nm etch control across 300,000,000 nm





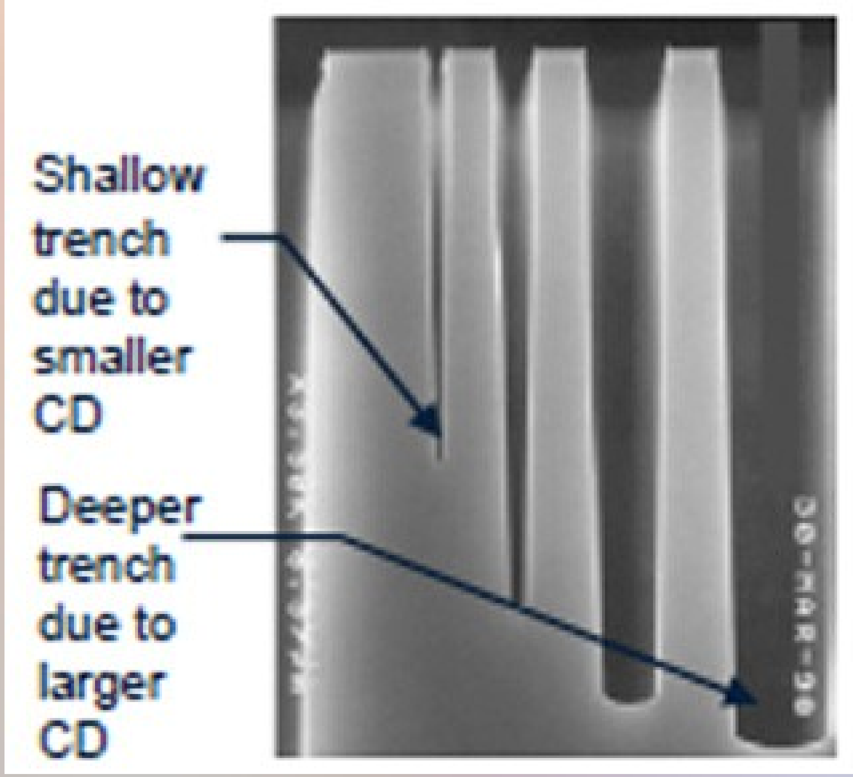
ICP with Source-Bias Sync

- Sync of source and bias neutralizes mask
- Byproduct removal
- Precursor refreshing
- Etch rate tuning
  - 0.1nm/min
  - 2 atomic layers
  - 0.8nm overetch shown compared to 4nm POR



ICP with Source-Bias Sync

- Sync of source and bias neutralizes mask
- Byproduct removal
- Precursor refreshing
- Minimizing → variability to CD
- 3X improvement claimed by OEM



Results without Source-Bias sync.

ICP with Source-Bias Sync

- New ICP source combined with source-bias sync improves depth uniformity
- STI and buried wordline etches have no “stop”
- Within die & wafer uniformity claims
  - <1nm 3σ CD for line/spaces
  - <1nm gate oxide recess
  - 1% etch-depth across 300mm

Conclusions

- New sources replace legacy tools
- New knobs provide new capabilities
  - Monolayers and few layers of new materials
  - Iso/Dense bias reduction
  - Aspect-ratio dependent etch effects minimized
  - End-users will explore new process spaces
- Major OEMs claim fabs pull for technology
- Difficult to predict limits of applications

Acknowledgments

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Thank You

Ed Korczynski, Founder and Editor

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