Niche Market Opportunities for Small and Mid-sized Companies

Dr. Robert N. Castellano
President
The Information Network
8740 Lyon Valley Road
New Tripoli, PA 18066
610-285-4548
www.theinformationnet.com
tinn@enter.net
• A joke told by Warren Buffett comes to mind: a patient, after hearing from a doctor that he has cancer, tells the doctor, “Doc, I don’t have enough money for the surgery, but maybe could I pay you to touch up the x-ray?”

• Hope and self-deception are not a strategy.

• We at The Information Network are neither a pessimist nor an optimist, we are a realist.
And The Reality Is That Things Are Not Very Good Out There
Industrial Production Worldwide Is Waning

![Graph showing industrial production worldwide over time.](image-url)

Source: www.econgrapher.com
We Can’t Readily Get Credit
Unemployment Is Obscene

Civilians Unemployed for 27 Weeks and Over (UEMP27OV)

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What Did That $750 Billion Stimulus Package Do For Jobs?

![Bar chart showing civilian unemployment rate (UNRATE) from 2007-12 to 2010-06.](research.stlouisfed.org)
But There Are Glimmers of Hope
The Business Climate in Germany is Improving

Ifo Business Climate in Germany
Ifo Business Survey June 2010

Index, 2000 = 100, seasonally adjusted

1) Manufacturing, construction, wholesaling and retailing.
Source: Ifo Business Survey.

22/06/2010 © ifo
Without A Strong Economy
Sales Are In the Toilet
This Is Why We Utilize Our Proprietary Leading Indicators
Competing Against Large Companies Exasperates Problems
The small business even with its limited resources can better serve these market segments by customized offerings, because the products of the big business will often be too generic to suit the needs of a niche market audience.
Niche Applications by Wafer Size

- High-tech applications that are fabricated on 300mm wafers
  - Packaging
  - MEMs
- High-tech applications that are built on non-300mm wafers.
  - Solar
  - LEDs
Packaging – WLP Gold Bump

Step 1: Incoming Wafer / PreClean

Step 2: Sputter

Step 3: Photo

Step 4: Expose

Step 5: Plating

Step 6: Resist Strip

Step 7: Etch
Packaging – WLP Solder Bump

Step 1: Incoming Wafer / PreClean
Step 2: Sputter
Step 3: Photo
Step 4: Expose
Step 5: Plating
Step 6: Resist Strip
Step 7: Etch & Reflow
## WLP Metallization Materials

<table>
<thead>
<tr>
<th>UBM STACK</th>
<th>BUMP</th>
<th>BUMP METALLURGY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti:W(N) / Au</td>
<td>Au</td>
<td>Au</td>
</tr>
<tr>
<td>Ti / Cu</td>
<td></td>
<td>Sn5Pb95 (high-Pb)</td>
</tr>
<tr>
<td>Ti:W / Cu</td>
<td></td>
<td>Sn37Pb63 (eutectic)</td>
</tr>
<tr>
<td>Al / NiV / Cu</td>
<td>Solder</td>
<td>Sn96.5 / Ag3.5 (Pb-free)</td>
</tr>
<tr>
<td>Ti / Ni</td>
<td></td>
<td>Sn99.3 / Cu0.7 (Pb-free)</td>
</tr>
<tr>
<td>Cr / Cr-Cu / Cu</td>
<td></td>
<td>Sn95.5 / Ag3.8 / Cu0.7 (Pb-free)</td>
</tr>
</tbody>
</table>
WLP Market by Bump Material

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Through Silicon Via (TSV) – A Solution To Extending Moore’s Law

Paradigm Shift in Chip Building Required

Single Layer          Stacked

2 Dimensional          3 Dimensional

Results

- Increased processing speed
- Decreased power requirements
- Smaller footprint
- Decreased heat output

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TSV Differences

- Via-First used for CIS which isn’t really a challenge

- Via after FEOL (transistor development post W-plug) and Via-Middle both called iTSV for ‘interconnect TSV’.
  - By far a majority of development is going into this area
Packaging – TSV Via Middle
(iTSV – interconnect TSV)

Key Via Middle TSV Process Steps

1. Via Etch
2. Oxide Dep
3. Seed Dep
4. Copper Plate
5. Copper CMP/Pattern
6. Wafer Backgrind
7. Bonding (W2W/D2W)

- Via depth, CD, profile Missing/incomplete via
- Dielectric/Seed thickness Pinholes/incomplete seed
- Thickness Plate block/contamination
- Thickness Uniformity Defectivity
- Remaining thickness/Uniformity, roughness, stress Scratches, via voids, chipping, microcracks
- Bonding alignment Edge inspection
iTSV – Via Formation and Fill Are Critical Steps

5μm x 50μm (10:1) TSV

Target 2μm/min Cu fill time
**TSV Differences**

- Via Before/after bonding called pTSV which is ‘Packaging TSV’ typically done by DRAM & Flash R&D

- Larger diameter via-last pTSV used in DRAM and interposers have significantly different challenges than the smaller diameter high aspect ratio iTSV structures
Packaging – TSV Via Last
(pTSV – packaging TSV)

Typical Via Last Process Control Steps

0. Finished wafer
1. Wafer backgrind
2. Via etch
3. Oxide dep
4. Anisotropic etch
5. Seed dep
6. Cu fill
7. Cu pattern/wet etch

- Roughness
- Macro defects
- Via depth, CD, profile
- Missing/incomplete via
- Dielectric/Seed thickness
- Pinholes/incomplete seed
- Dielectric/Seed thickness
- Pinholes/incomplete etch
- Thickness
- Plate block/contamination

Note: Cu fill may be conformal

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iTSV Equipment Breakdown

iTSV 5 x 30 um

- Etch/Strip: 19%
- Electroplate: 15%
- Dicing/CMP/Barrier/Seed: 13%
- Via Etch: 7%
- Lithography/Bonding: 35%

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Solar Cells – Thin Film and Crystalline

2009 Solar Cell Percentage Breakout by Type

- **poly c-Si**: 65.0%
- **mono c-Si**: 9.4%
- **ribbon c-Si**: 1.1%
- **a-Si**: 7.5%
- **CdTe**: 14.6%
- **CIS**: 2.2%
- **Other TF**: 0.2%

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a-Silicon Multijunction Stack Solar Cell

New development
Triple-junction thin-film solar cell

Conventional
Tandem thin-film solar cell

Amorphous silicon cell
Amorphous silicon cell
Microcrystalline silicon cell
Amorphous silicon cell
Microcrystalline silicon cell

Source: Sharp
a-Silicon Multijunction Stack Equipment
a-Silicon Multijunction Stack Solar Cell

Glass
TCO
a-Si:H cell
Intermediate layer
Poly-Si cell
Back reflector
CdTe Solar Cell

Diagram showing the CdTe Solar Cell with labels for Substrate and CdTe Source.
CIGS (Copper Indium Gallium Selenium) Solar Cell
CIGS (Copper Indium Gallium Selenium) Solar Cell

- ZnO, ITO - 2500 Å
- CdS - 700 Å
- CIGS 1-2.5 μm
- Mo - 0.5-1 μm
- Glass, Metal Foil, Plastics
Silicon Solar Cells

Cell Processing → Wafer Inspection → Texture Etch

Diffusion → PSG Etch → AR Coating / PECVD

Metallization → Co-Firing Furnace → Cell Test/Sort

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Types of Commercial ARC films

- Titanium Oxide, TiO$_2$
  - Atmospheric Pressure Chemical Vapor Deposition
- Indium Tin Oxide, ITO
  - Transparent conducting oxide
- Silicon Oxide, SiO$_2$
  - Thermal oxidation
  - High temperature
  - Passivates surface
- Silicon Nitride, SiN$_x$:H
  - Plasma Enhanced Chemical Vapor Deposition (PECVD)
  - Low Temperature
  - Passivates Surface and Bulk
Commercial ARC Film Deposition

- $\text{SiH}_4 + \text{N}_2\text{O}$
  - $\text{SiO}_x\text{N}_y\text{:H}$
  - $n = 1.46 - 1.9$
- $\text{SiH}_4 + \text{NH}_3 / \text{N}_2$
  - $\text{SiN}_x\text{:H}$
  - $n = 1.85 - 3.3$
- $\text{SiH}_4$
  - a-$\text{Si}:\text{H}$
  - $n = 4.2$
- Doping of a-$\text{Si}:\text{H}$
Silicon Solar Cells – Watch for Disrupting Technologies
Silicon Solar Cells – Or Look To Develop New Technology

- Eddy current sheet resistance measurements on multi-crystalline wafers
- A discontinuity was seen in a wafer that was later seen to have a crack
- Photos courtesy of Lehighton Electronics
Solar Cells – Equipment Leaders

2009 Solar Equipment Market Shares - Top 11 Vendors

- GT Solar: 12.4%
- Schmid Gruppe: 15.6%
- Applied Materials: 23.1%
- Centrotherm: 15.6%
- Manz Automation: 1.5%
- NPC: 4.3%
- Ulvac: 4.9%
- Roth & Rau AG: 6.1%
- Meyer Burger: 6.1%
- Oerlikon: 9.3%
- ALD Vacuum Technologies: 4.0%
Huge Solar Cells Market Forecast in MW Per Year
Conclusions

• Niche markets offer an opportunity for small to mid-sized companies to compete against the large equipment and materials suppliers

• Niche markets offer greater growth potential than standard semiconductor devices

• A win-win situation