Electrical Non-contact Characterization of Plasma Processing Induced Damage on Blanket Oxides and Patterned Low-k Dielectrics

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Several non-contact techniques have been developed for monitoring of plasma processing induced damage in both FEOL and BEOL applications.

Such approaches require no special test structures and allow for low cost, fast turnaround measurements, making them well suited to real time production monitoring. The following techniques will be discussed:

- Rapid non-contact technique for residual plasma charge mapping; non-contact corona based technique for leakage & SILC measurements on plasma CVD deposited dielectrics
- Near-field scanning microwave microscope for nondestructive characterization of processing induced sidewall plasma damage in patterned low-*k dielectrics.*

The presentation will explain the basic theory behind the measurements, and include example data of real production issues which have been observed.

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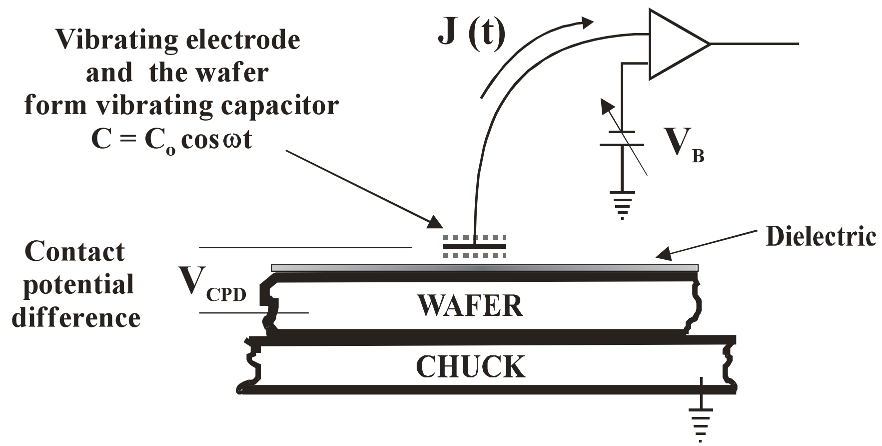
Non-Contact Voltage Measurements



- Contact Potential Difference, V_{CPD} and the bias V_B polarize vibrating capacitor inducing ac current

$$J\,(t) = (V_{CPD} + V_B)\, dC/dt$$

- The bias feedback loop automatically searches for J=0; then $V_{CPD} = -V_B$

$$Vcpd = \Phi_{MS} + V_{SB} + V_D$$

- Φ_{MS}: Metal semiconductor workfunction difference
- V_{SB}: Si surface barrier
- V_D: Dielectric voltage — Linear dependence on Qc, # T

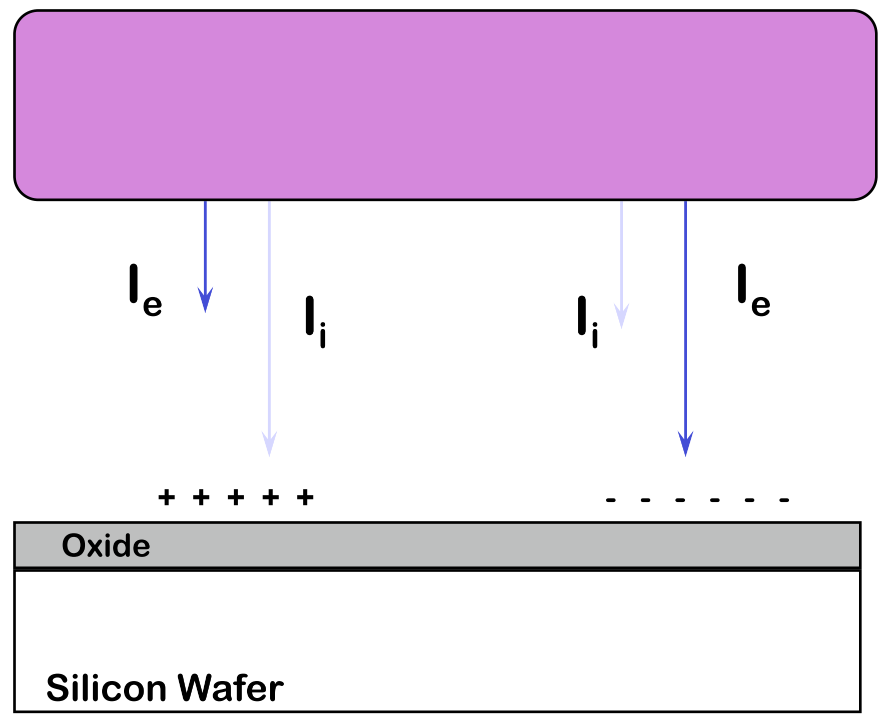
Plasma Damage Monitor (PDM)

residual charge mapping after plasma processing

<u>SDI measurement approach</u>:

- Non-contact / Non-destructive
- Preparation free
- Provide Full Wafer Imaging
- Give results in several minutes :

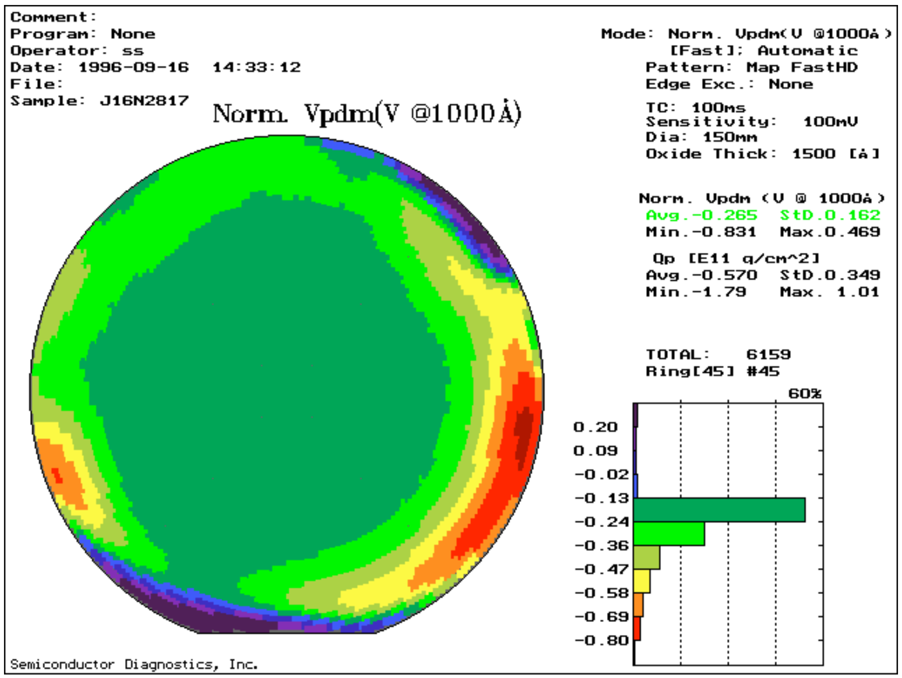
  picture charge / balance



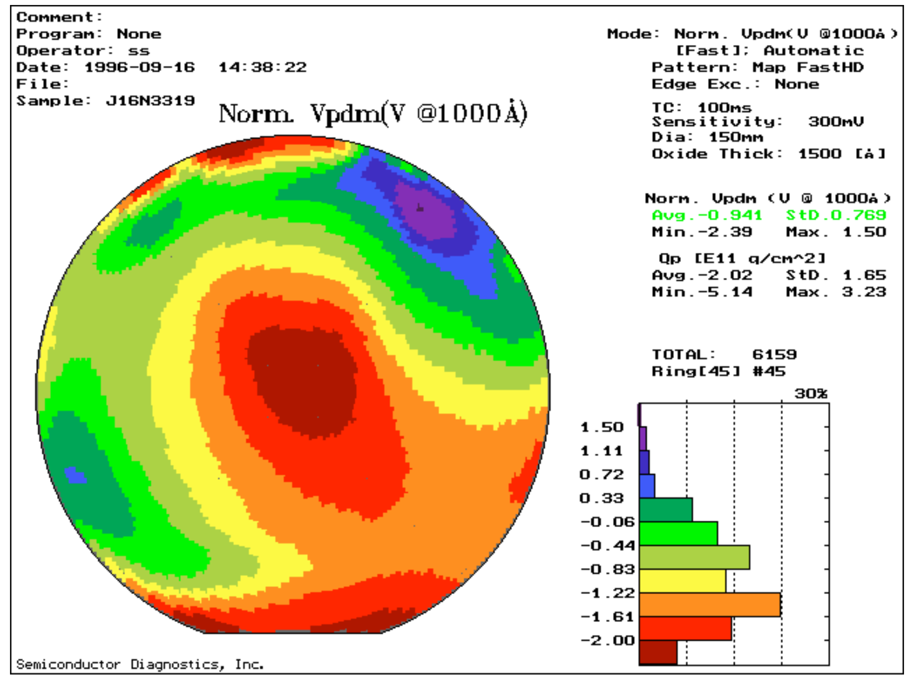
Recommended Oxide thickness >1000A

Comparison of ashers

CONTROL	R.F. BARREL ASHER



Average Vpdm: -0.266V
(max - min) Vpdm: 1.3V



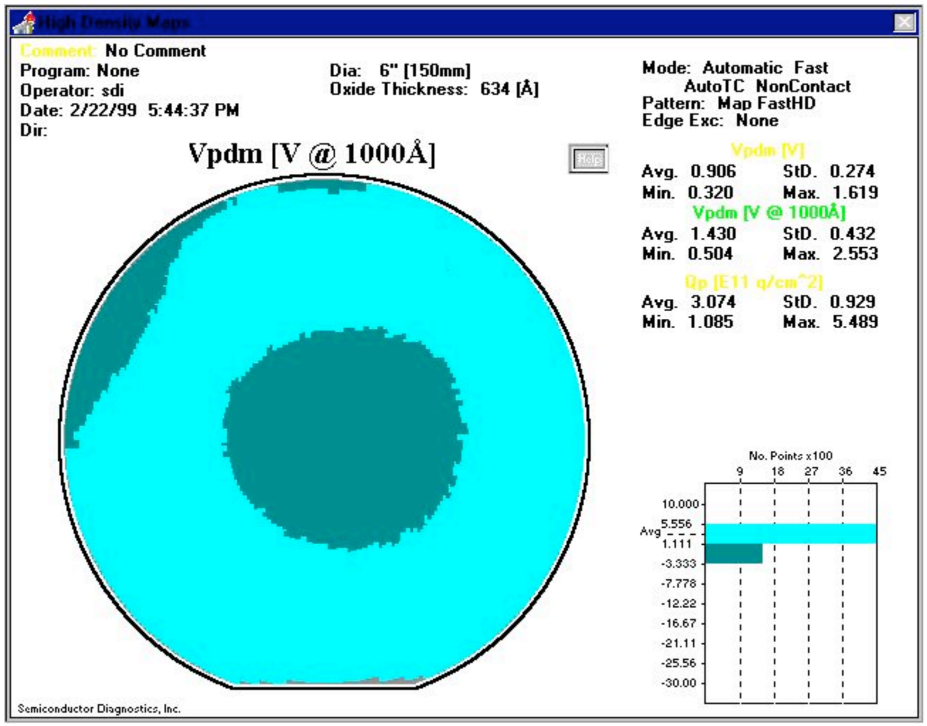
Average Vpdm: -0.941V
(max - min) Vpdm: 3.89V

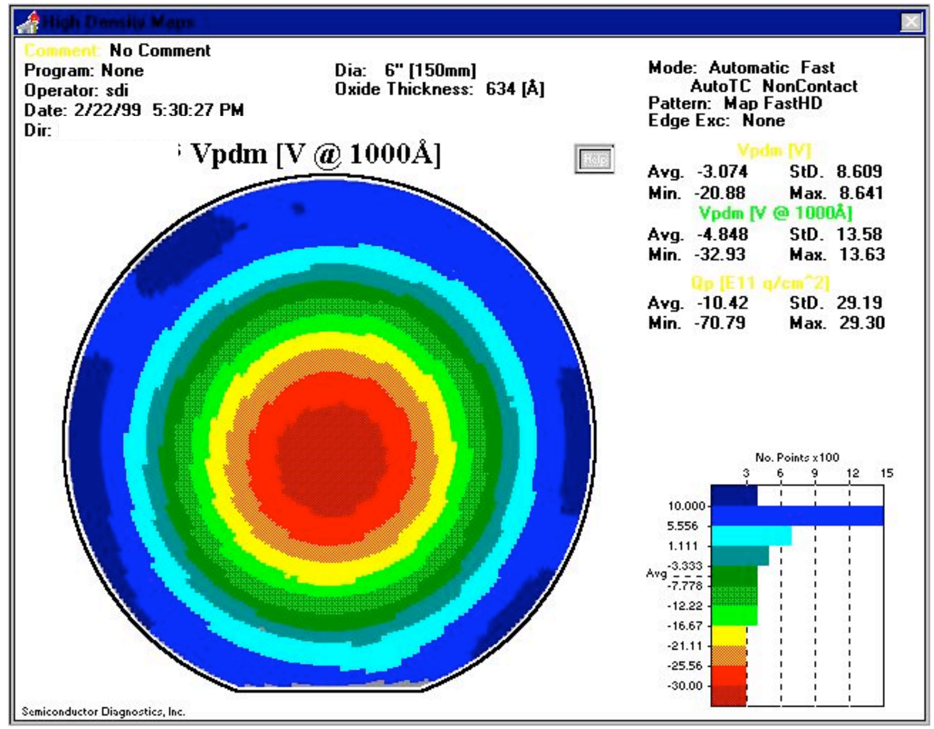
Power-Lift process

(Maps printed in the same scale)

Without Powerlift

With 75W Powerlift



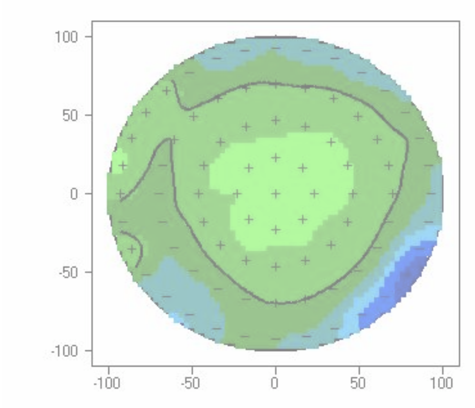


Average Vpdm: 1.43 V
(max - min) Vpdm: 2.05 V

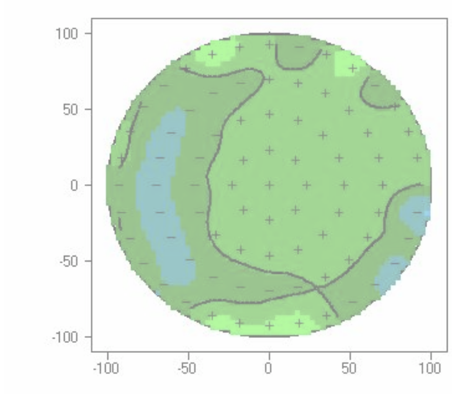
Average Vpdm: -4.85 V
(max - min) Vpdm: 46.5 V

~630A TEOS deposited on top of 1000A thermal oxide

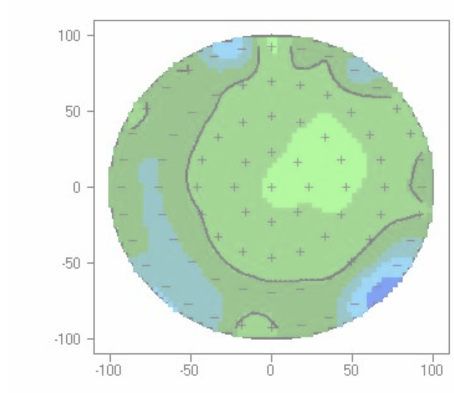
Plasma CVD example: PDM maps
Slots 1-3: chamber 1 / slots 4-6: chamber 2



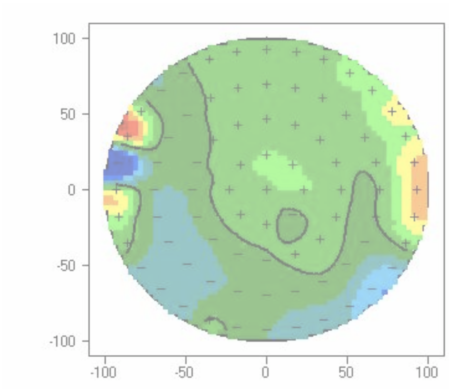
Wafer S01 – Vpdm



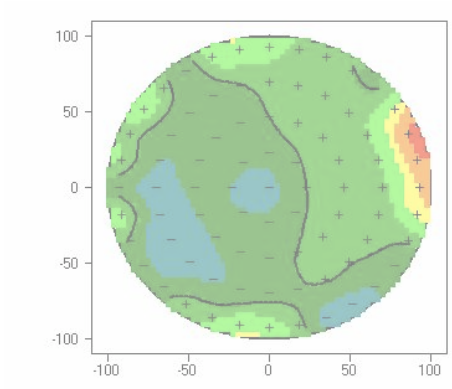
Wafer S02 – Vpdm



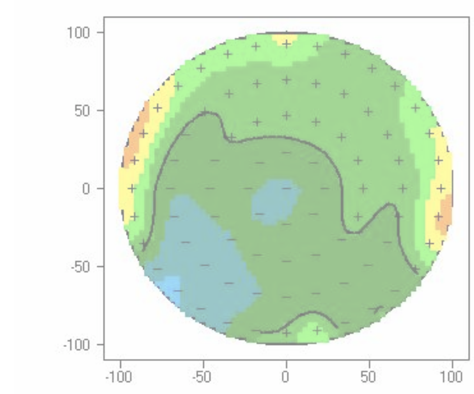
Wafer S03 – Vpdm



Wafer S04 – Vpdm



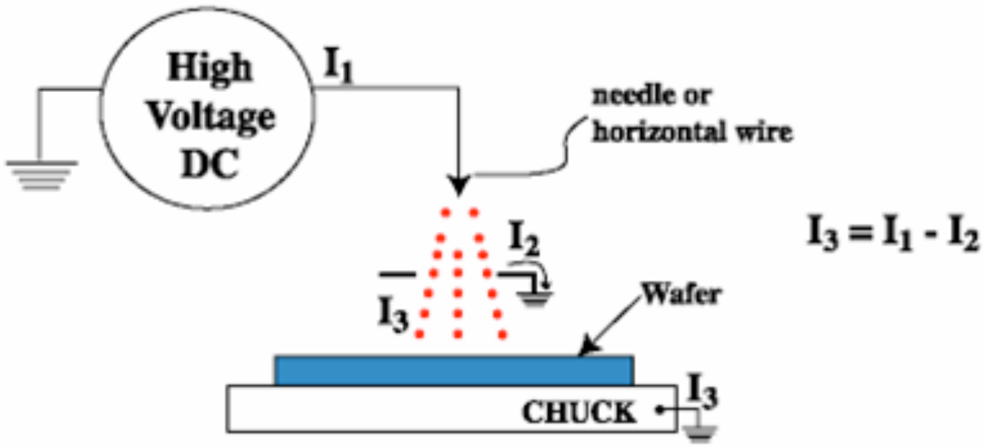
Wafer S05 – Vpdm



Wafer S06 – Vpdm

→ from residual charge measurements we can observe somewhat higher charging at the wafer edges, but magnitude of differences are small.

Corona Charging Technique



CORONA FLUX	$J_C = \frac{\text{NUMBER OF IONS}}{cm^2 \cdot s}$
CORONA DOSE	$\Delta Q_C = J_C \cdot \Delta t = \frac{\text{NUMBER OF IONS}}{cm^2}$
TOTAL CORONA CHARGE in n-doses	$Q_C = n \cdot \Delta Q_C$

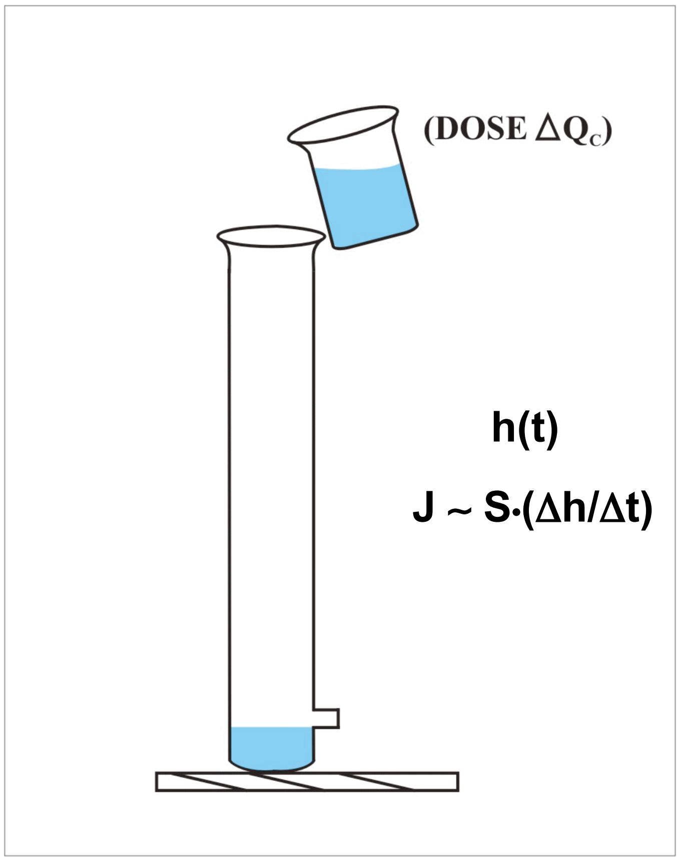
- Polarity controlled by the polarity of high voltage

  → ions: CO_3^- or $(H_2O)_nH^+$
- Low kinetic energy ion deposition on dielectric : non contact bias
- Amount of charge controlled by:
  1. Magnitude of high voltage
  2. Distance of corona source to the surface
  3. Time of corona charge deposition
  4. Coulombic interaction with the charge on the wafer alters deposition

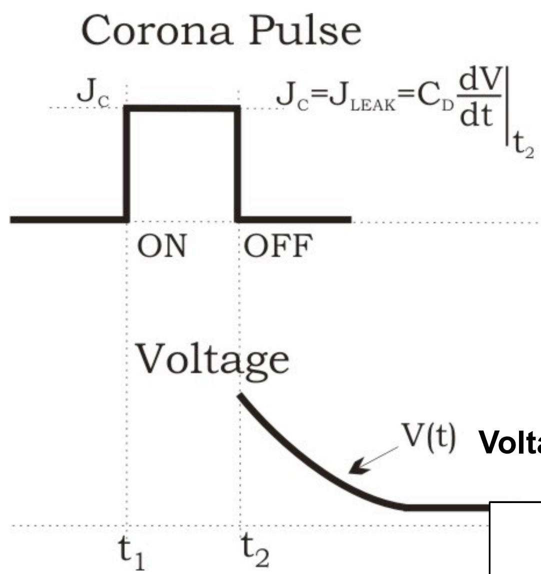
SASS I-V Technique

How to Measure Current Across a Dielectric Without Touching the Wafer? The Self Adjust Steady State I-V Technique

Water Analogy for Leakage



Dielectric Leakage Measurement



Voltage transient measured by cpd

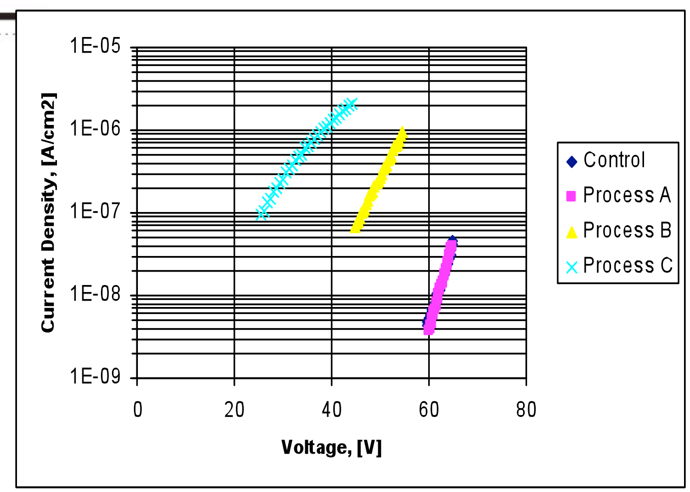
Q = CV

J = dQ/dt

= Cox dV/dt

I-V leakage curves

For 4ea **1000Å** deposited oxides



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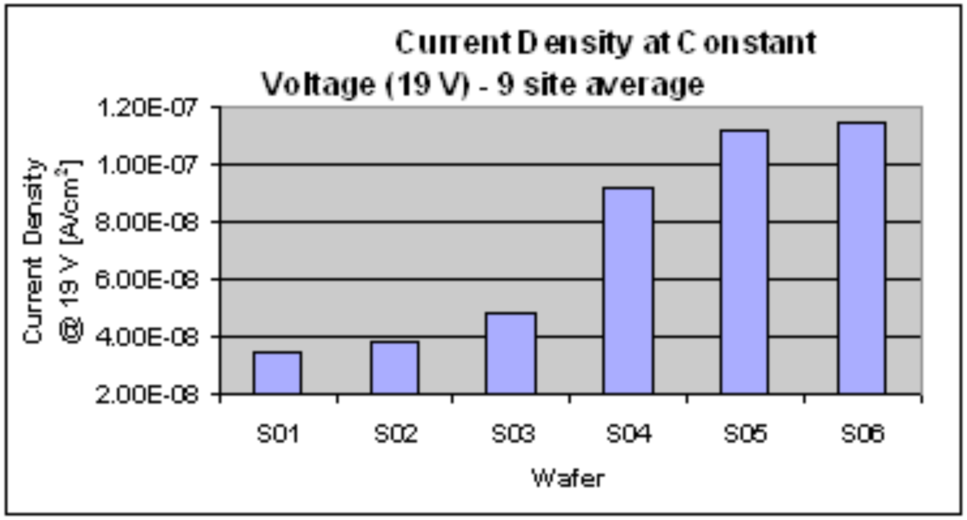
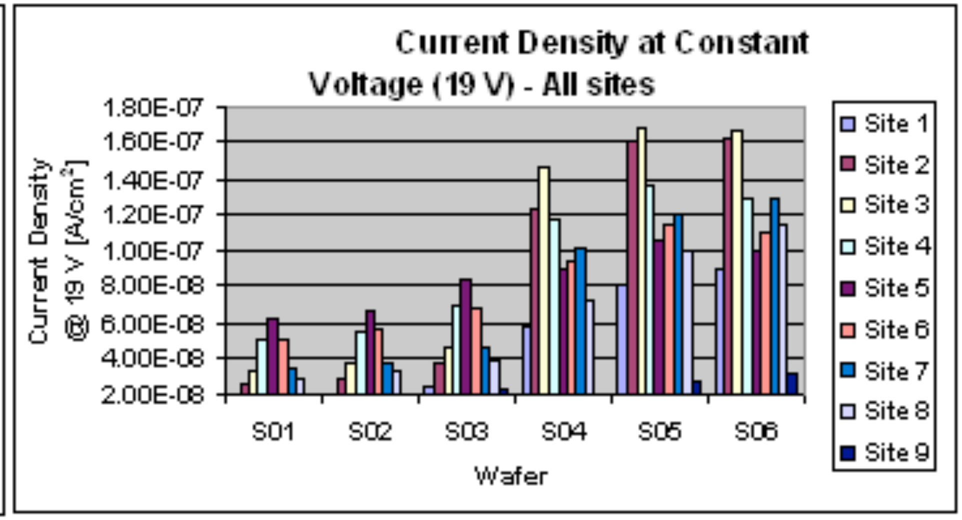
Plasma CVD example: I-V / leakage
Slots 1-3: chamber 1 / slots 4-6: chamber 2

We observe 2-3 times larger leakage for slots 4-6 (chamber 2) as compared to slots 1-3, as well as different within wafer characteristics.

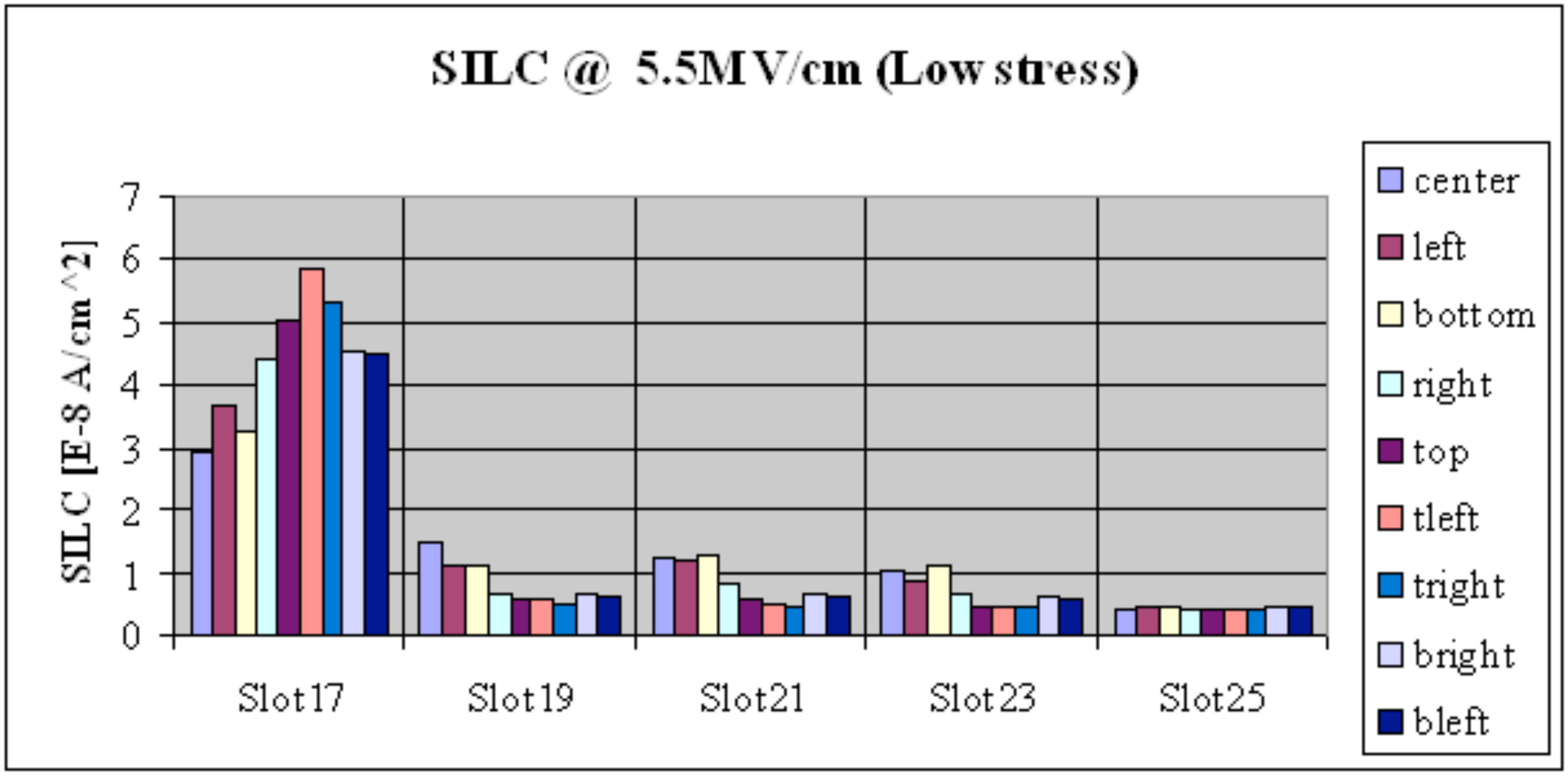




Chamber 1 & 2 were the same type / same manufacturer. The film was PMD (pre-metal dielectric), and device data from chamber 2 was showing higher leakage characteristics than from chamber 1.

SILC – stress induced leakage current Resist stripping problem

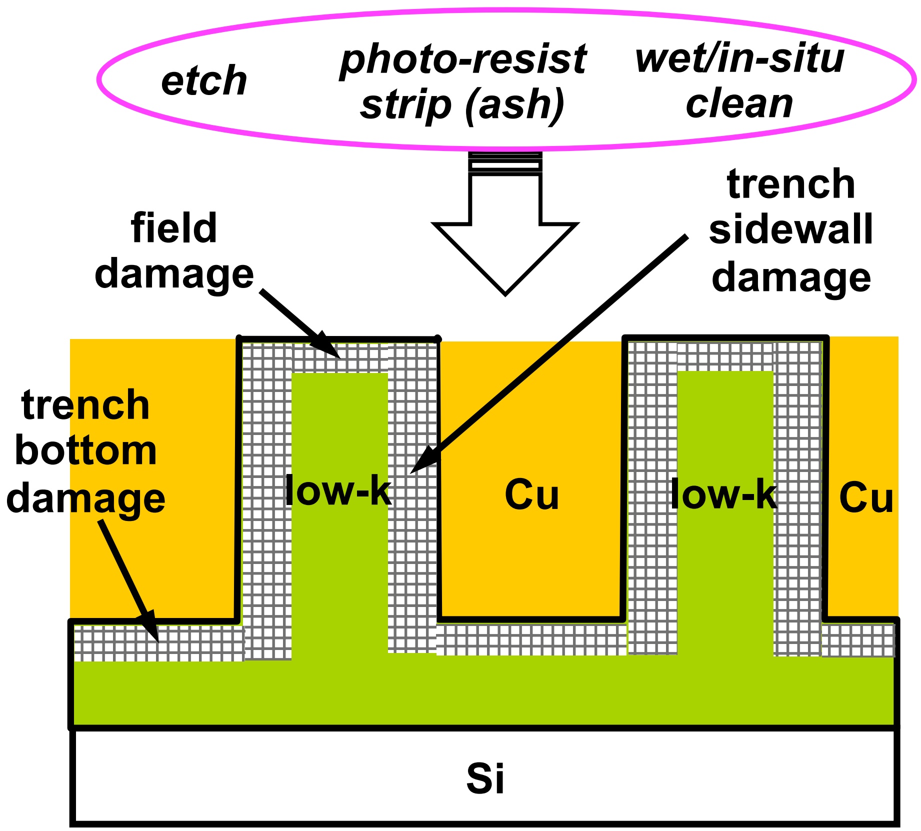
- Production Fab experienced Q_{bd} problem
- Splits run & tested on FAaST tool. Corona I-V / leakage was measured before and after corona stressing of the oxide.
- Slot 17 shows 3-5X higher leakage, highlighting issue with the new resist strip process
- Issue fully verified and resolved in ~7-10 days



SEMILAB SSM

Near-field scanning microwave microscope NeoMetriK™ for monitoring of plasma damage during interconnect processing

Processing induced low-k damage

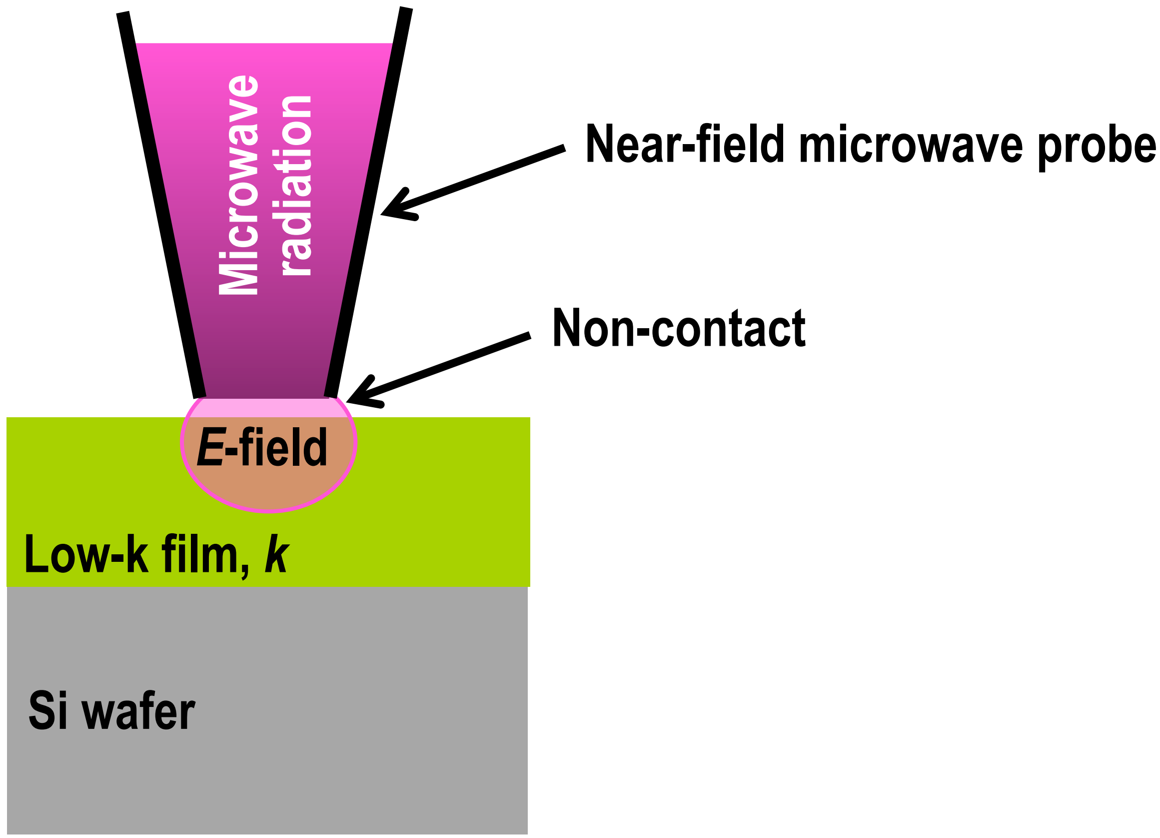


- Patterning creates chemical and physical low-k damage leading to increase in k-value due to:
  - Doping depletion → skeleton $k\uparrow$
  - Moisture uptake into pores → pore $k\uparrow$ since k_{H20}~80
- Plasma damage may increase k-value drastically, e.g. from 2 to 6 → interline capacitance increase

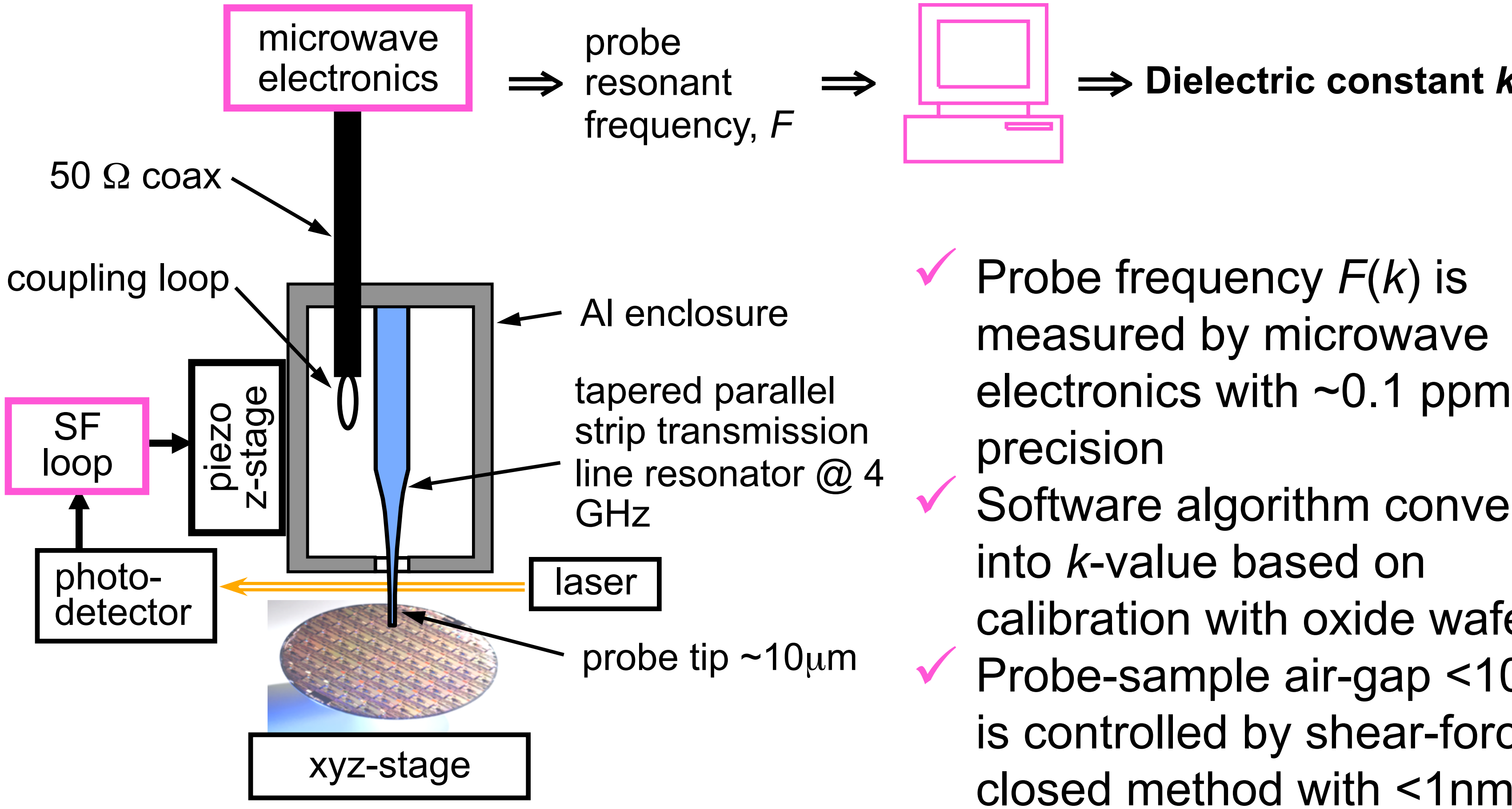
ITRS: Monitoring for <u>etching plasma damage</u> will be needed in production after 32nm node. But now need to study at R&D.

What NeoMetriK does?

- NeoMetriK measures dielectric constant *k* of interconnect, which influences interconnect response to electrical signal

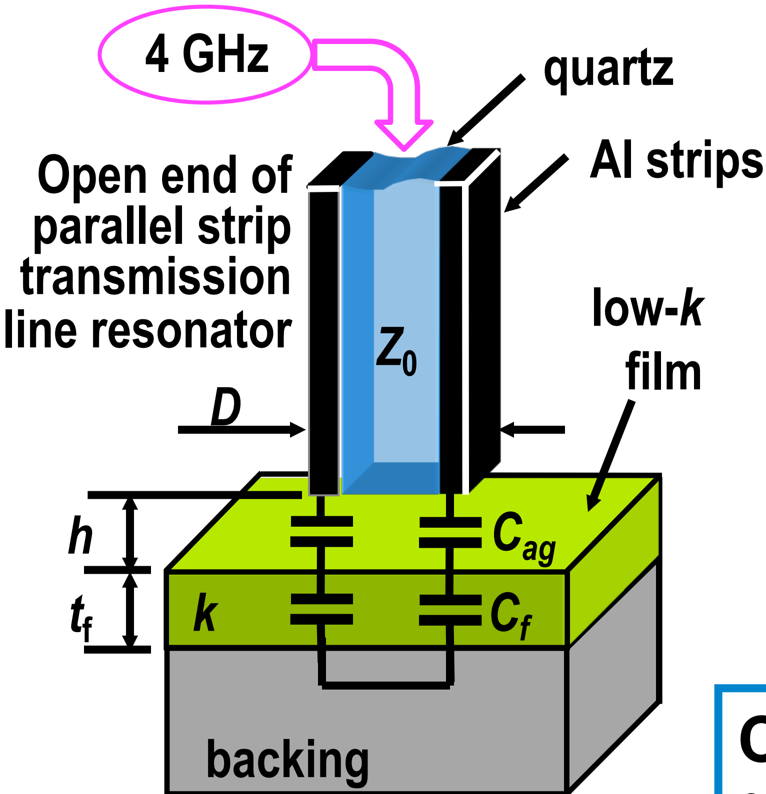


NeoMetriK operating principle



- Probe frequency *F*(*k*) is measured by microwave electronics with ~0.1 ppm precision
- Software algorithm converts *F* into *k*-value based on calibration with oxide wafers
- Probe-sample air-gap <100nm is controlled by shear-force closed method with <1nm repeatability

Probe-sample interaction



D ~ 10 µm
h < 0.1 µm
backing: low-ρ Si, Cu, Cu grid

Probe tip capacitance:

$$C_t = 1/(2C_f^{-1} + 2C_{ag}^{-1})$$

Probe resonant frequency shift $\Delta F = F_0 - F$:

$$\frac{\Delta F}{F} = -2FZ_0\Delta C_t[k, t_f, h]$$

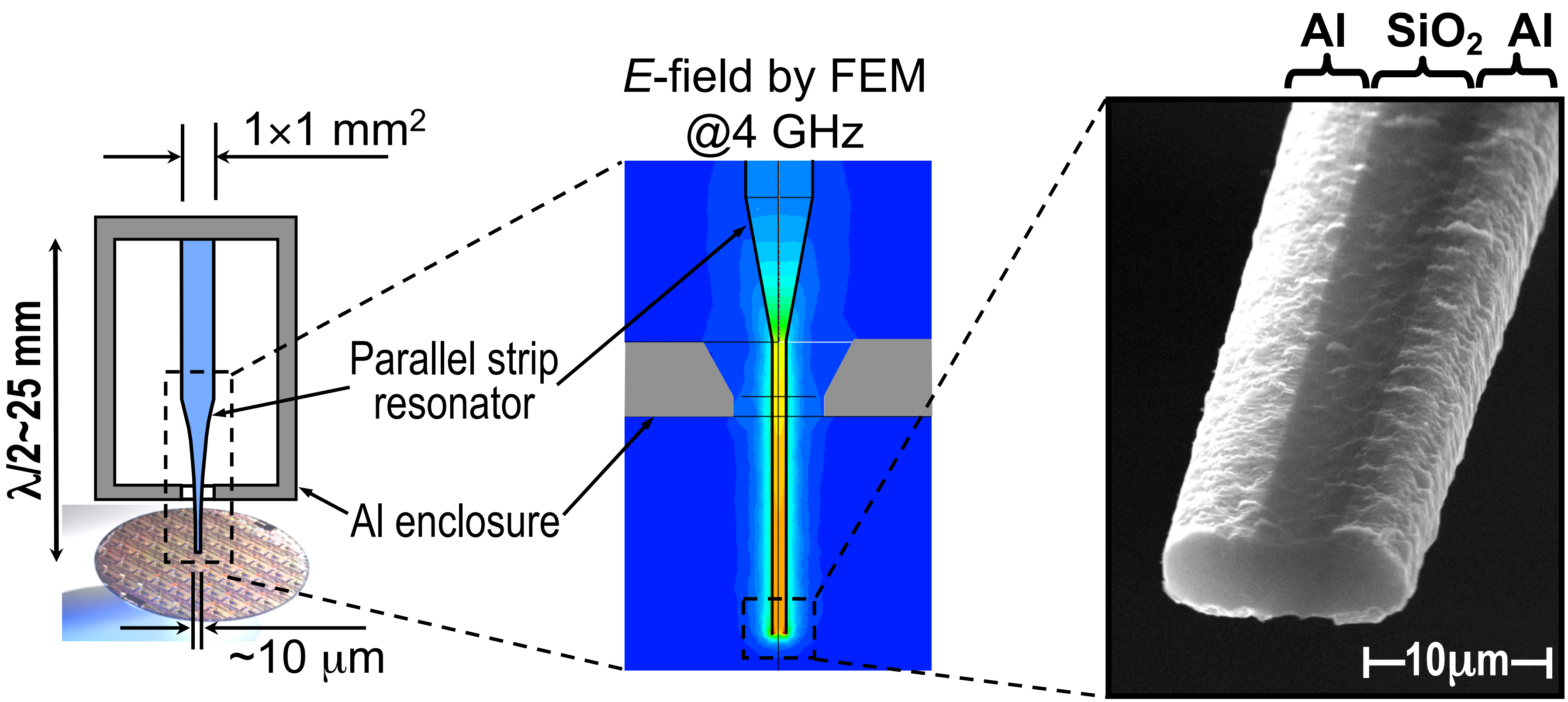
F_0 probe frequency w/o sample ~4 GHz
Z_0=100Ω transmission line characteristic impedance

Capacitance sensitivity
$\delta C_t \sim 10^{-18}$ F = 1 aF

→ **few µm^2 sampling area !!**

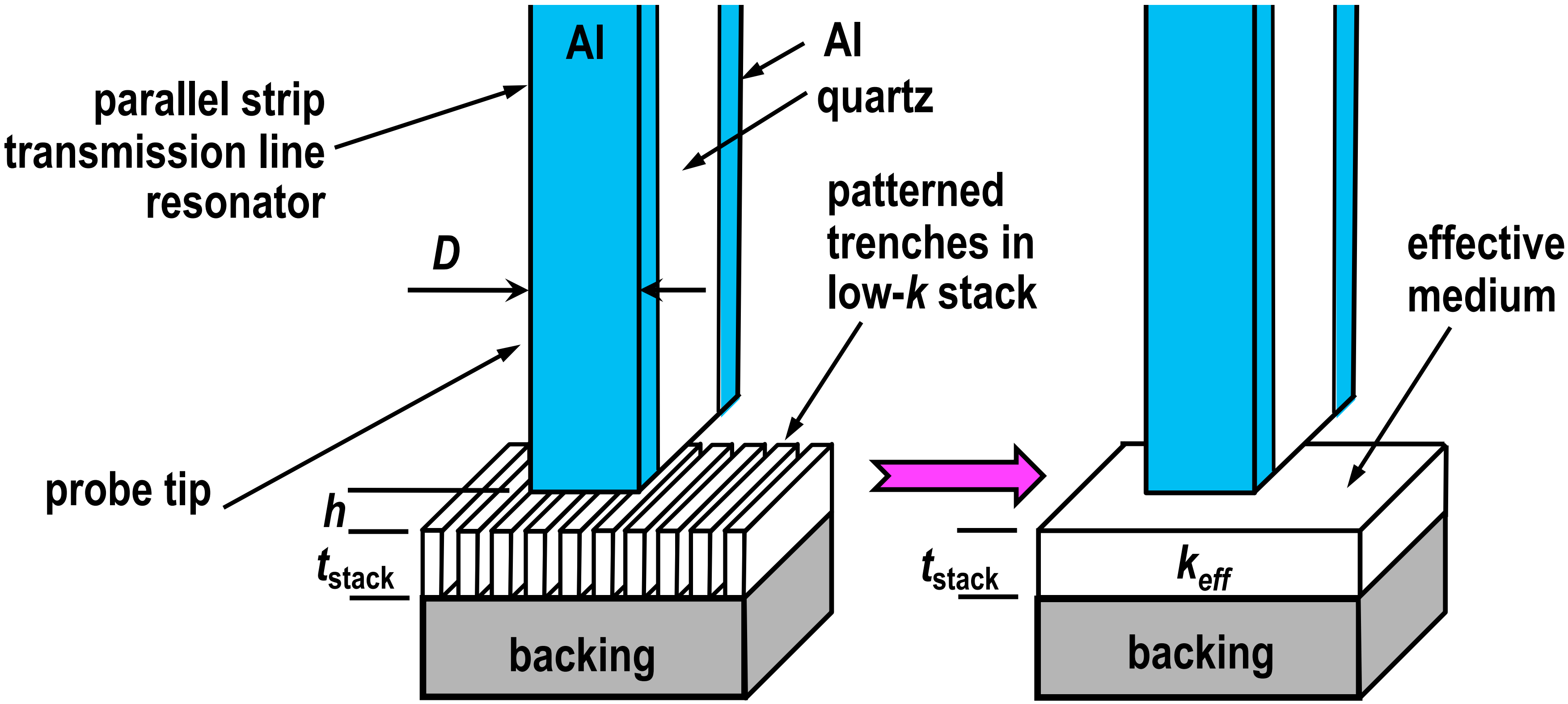
Probe design

- Probe is a tapered parallel strip transmission line resonator @ 4 GHz
- Electrically open tip end creates well confined sampling *E*-field similar to parallel plate capacitor fringe field



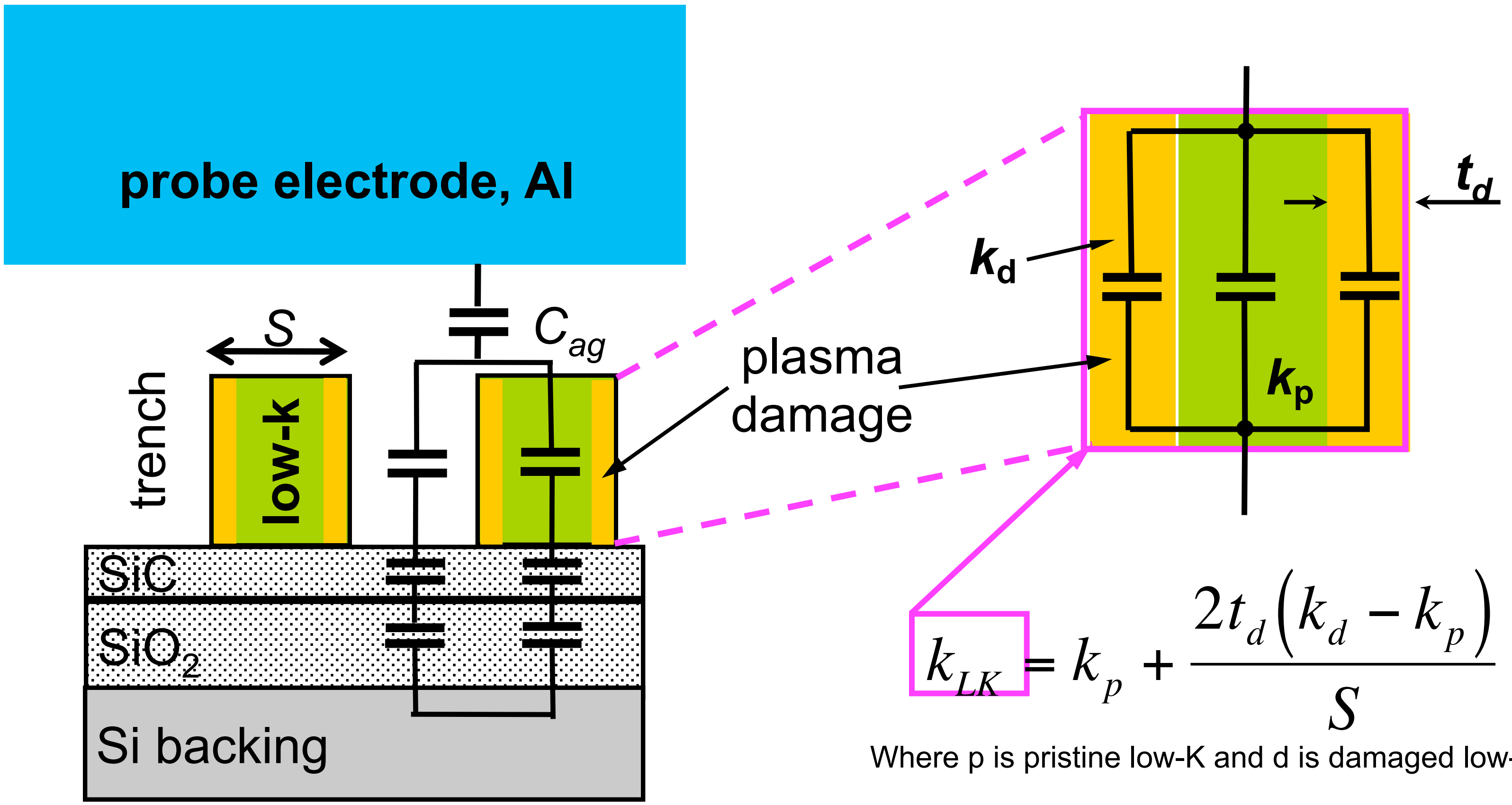
SEM image of probe tip

Effective medium approach



- Effective medium approach: probe size *D* >> pattern pitch
- Existing structures can be used: comb, MF, OCD, CD-SEM, etc.
- No Cu metallization
- No limitation on pitch! (e.g., 1 nm is Ok)

Lumped element model

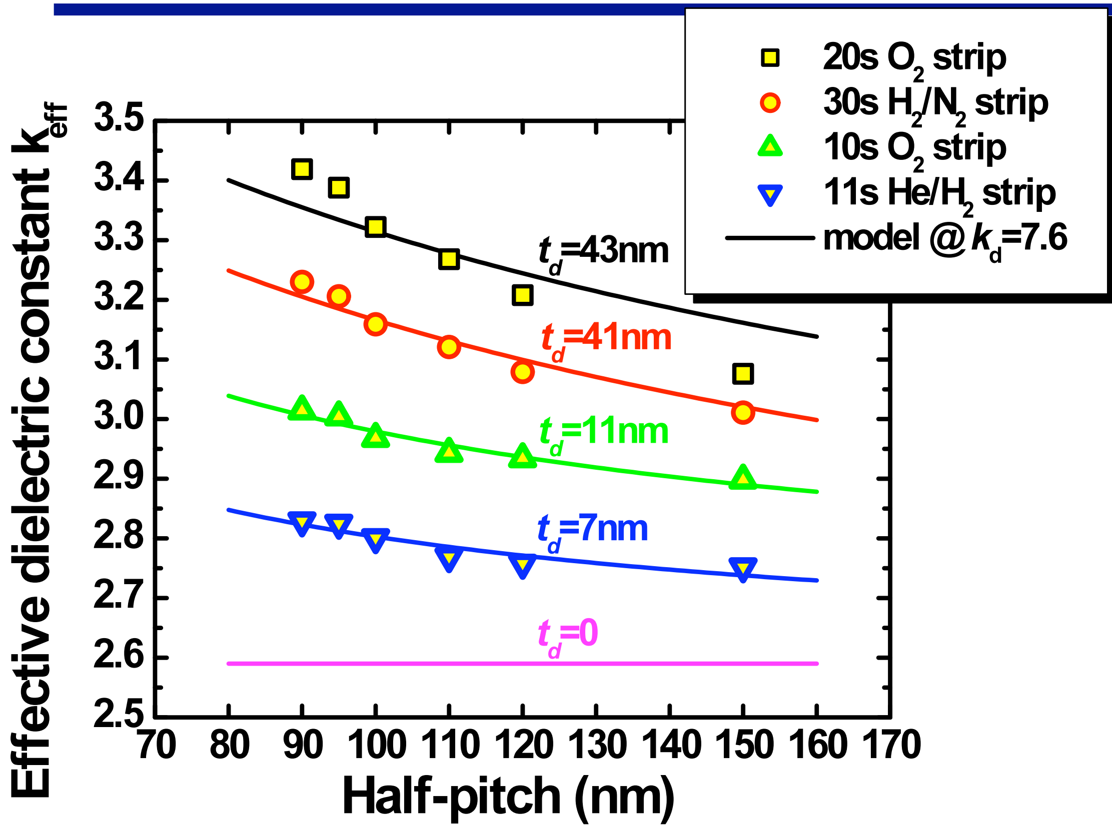


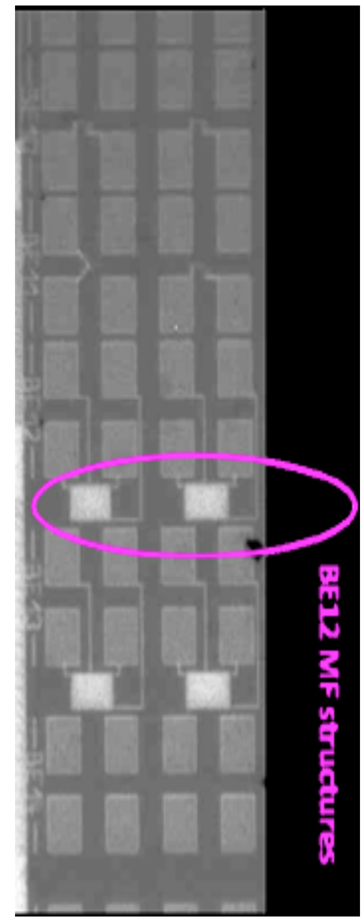
$$k_{LK} = k_p + \frac{2t_d(k_d - k_p)}{S}$$

Where p is pristine low-K and d is damaged low-K

- Sensitivity to the damaged layer thickness t_d is ~ 1 nm
- Analytic model accuracy was verified by finite element modeling

Side-wall damage vs. strip recipe

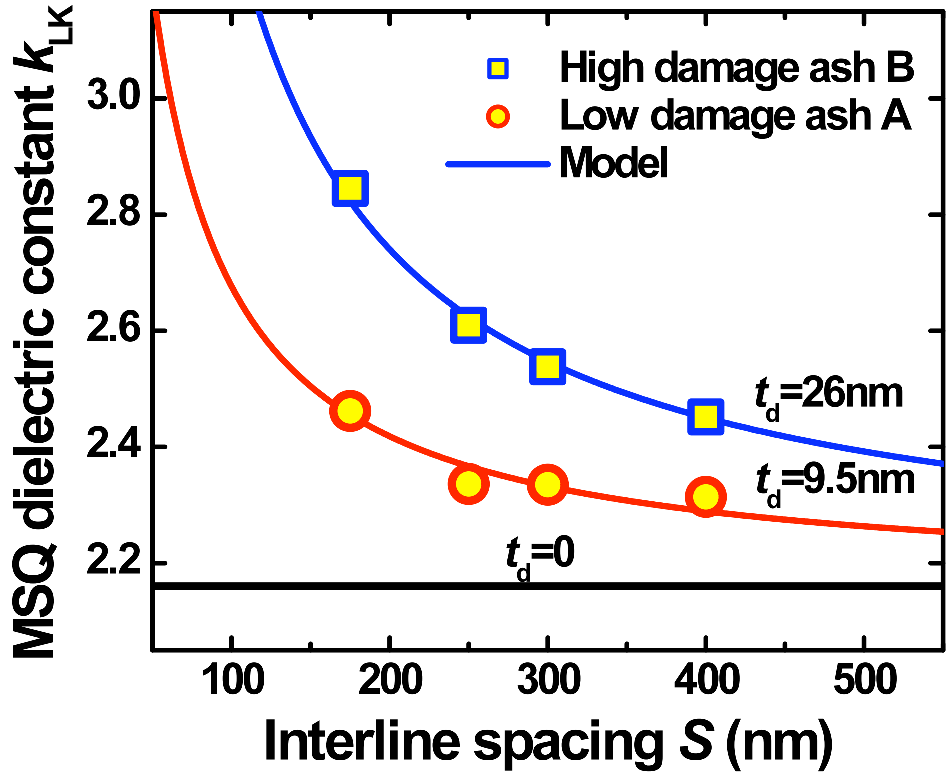


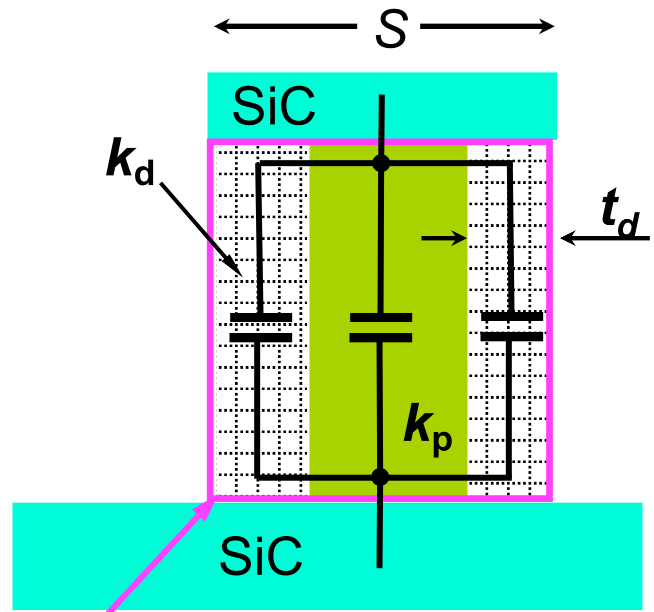


- 50% pattern density for all structures
- Solid lines are the fits to the parallel plate capacitor model using damaged layer thickness t_d as a free parameter.

Side-wall damage in MSQ

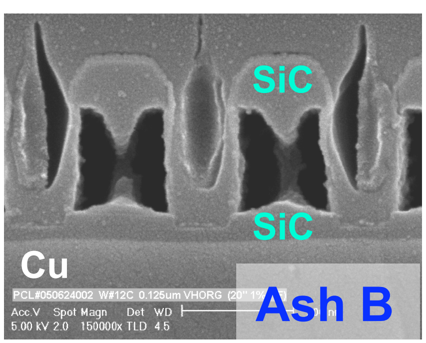
SEMILAB SSM

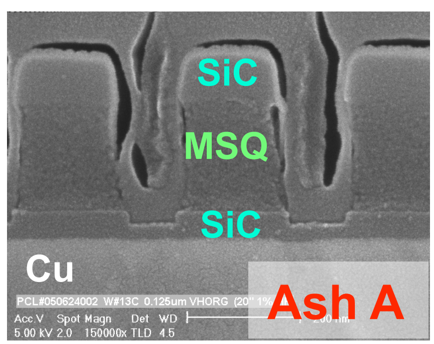




$$k_{LK} = k_p + \frac{2t_d\left(k_d - k_p\right)}{S}$$

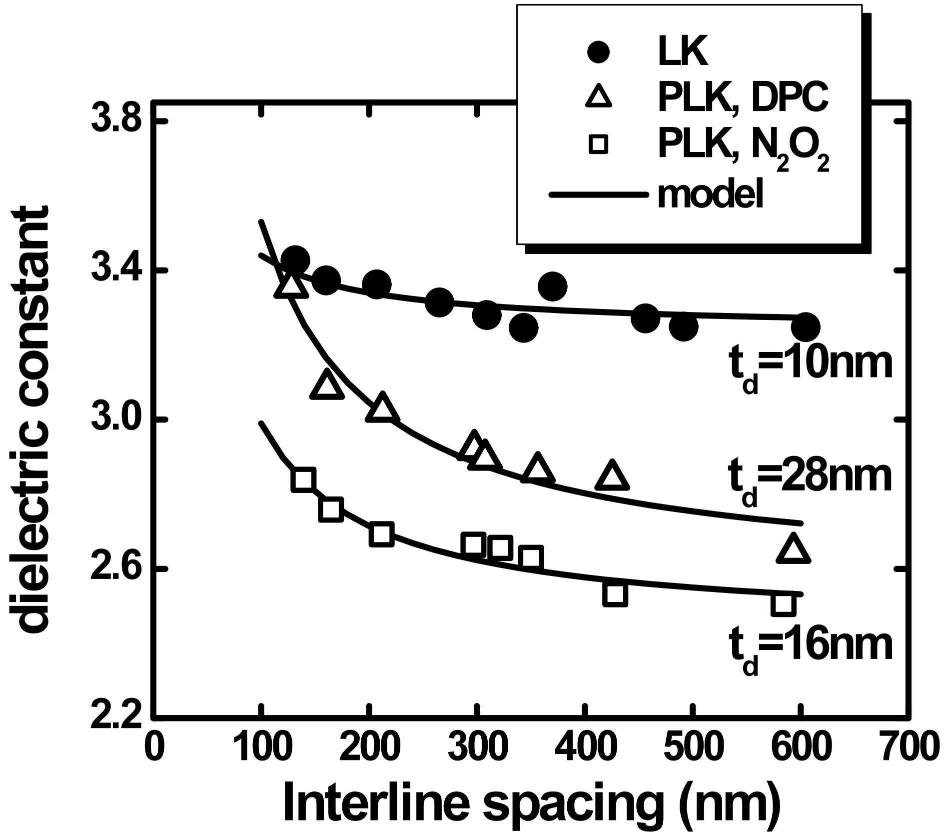
t_d sensitivity ~ 1 nm





SEM x-sections after HF decoration

Side-wall damage in PLK vs. LK



Dielectric constant of remaining after etch low-*k* dielectric extracted from experimental data for non-porous (LK) and porous (PLK) low-*k* materials. Solid lines are the fits to an analytical model for sidewall damage contribution. LK exhibits minimal processing induced damage, while PLK damage depends on processing. Dry preclean induces more damage than N_2O_2 ash.

Conclusion

Semilab offers a wide range of non contact electrical characterization techniques to monitor plasma damage:

- Residual charge measurements
- Leakage current measurements
- K measurement
- Direct, quantitative electrical measurement
- Non-contact, non-contaminating, non-invasive → Fab compatible
- Real time measurement and data analysis → in-line monitoring

NeoMetriK :

- On blanket and patterned wafers, no special structures needed
- 10 μm spatial resolution → fits into most test structures
- The only technique for side-wall damage measurement before Cu → all patterning stages can be characterized; plasma damage monitoring in production at/after 32 nm node
- Accuracy, precision are similar to established area capacitor methods
- unlike AFM, probe is not a consumable
- No wafer contact → measurement at any metal level