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DRIE Technology For MEMS

Plasma Etch Users Group, 26 February, 2009

ALCATEL Micro Machining Systems

Outline

- Introducing Tegal Products
- MEMS Feature Size Requirements
- The Bosch DRIE Process
- Silicon DRIE Technology
  - Scallop Control
  - Etch Rate
  - Angle deviation
  - Thermal Dissipation
  - Notching control
  - ARDE
  - SHARP
  - Process Stability
- Oxide DRIE

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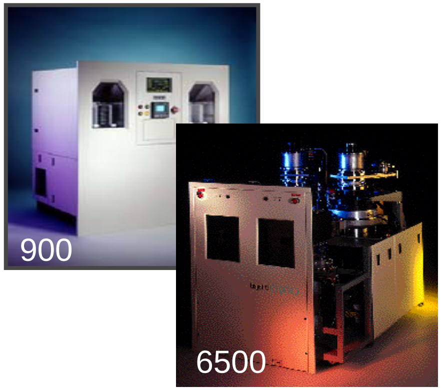
Tegal Products 1

ETCH



Diode, ICP and HRe$^-$ CCP Sources

- Non-volatile memory
- MEMS devices
- Thin-film head for disk drives
- Integrated Passives
- Compound Semiconductors

PVD

Sputtered Films Inc.

AMS

Endeavor AT
AMS SMT, MMT

- Advanced Packaging: Under-bump metallization
- Power device backside metallization
- MEMS devices – AlN BAW FBAR
- Integrated Passives : Thin film resistors and capacitors

NLD

Compact 360 NLD

- Thin film barrier
- Thin film seed
- Thin film electrode
- LED encapsulation
- MIM DRAM
- High-k dielectrics
- 300 mm

Tegal technology addresses Etch, PVD and CVD

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Tegal Products 2

AMMS technology is now part of Tegal, addressing Deep Silicon Etch and Oxide Etch

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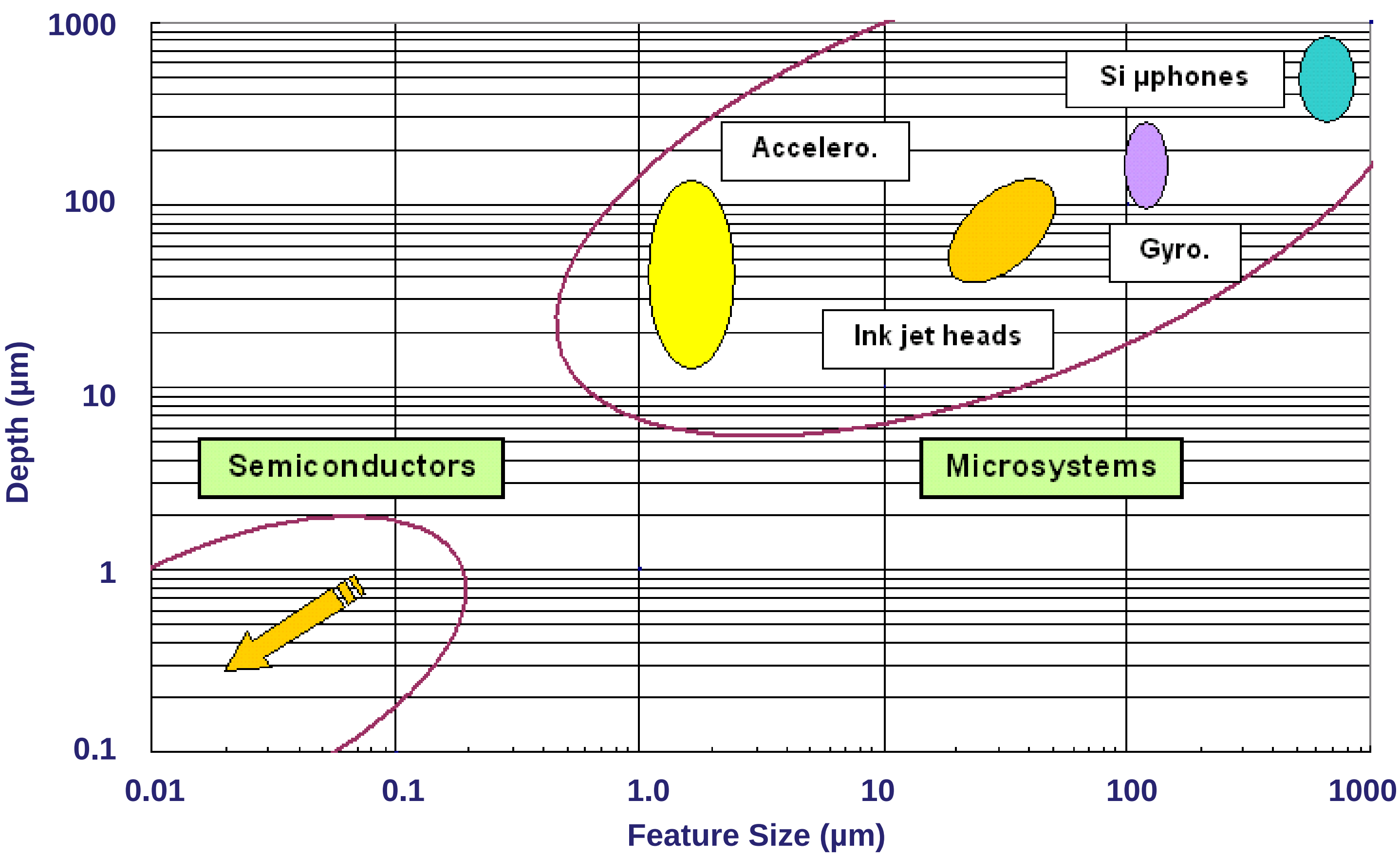
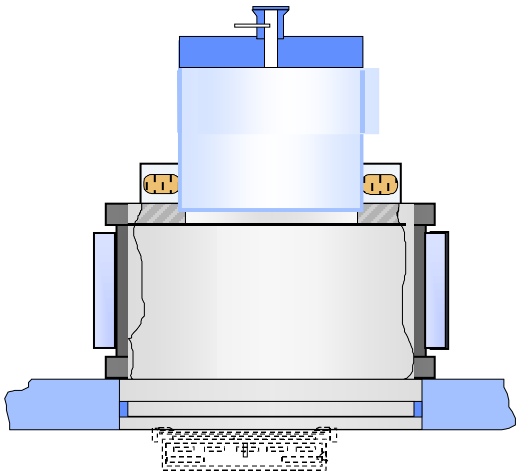
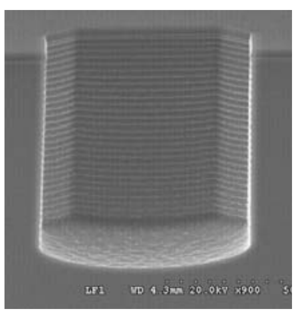
Microsystems & Semiconductors

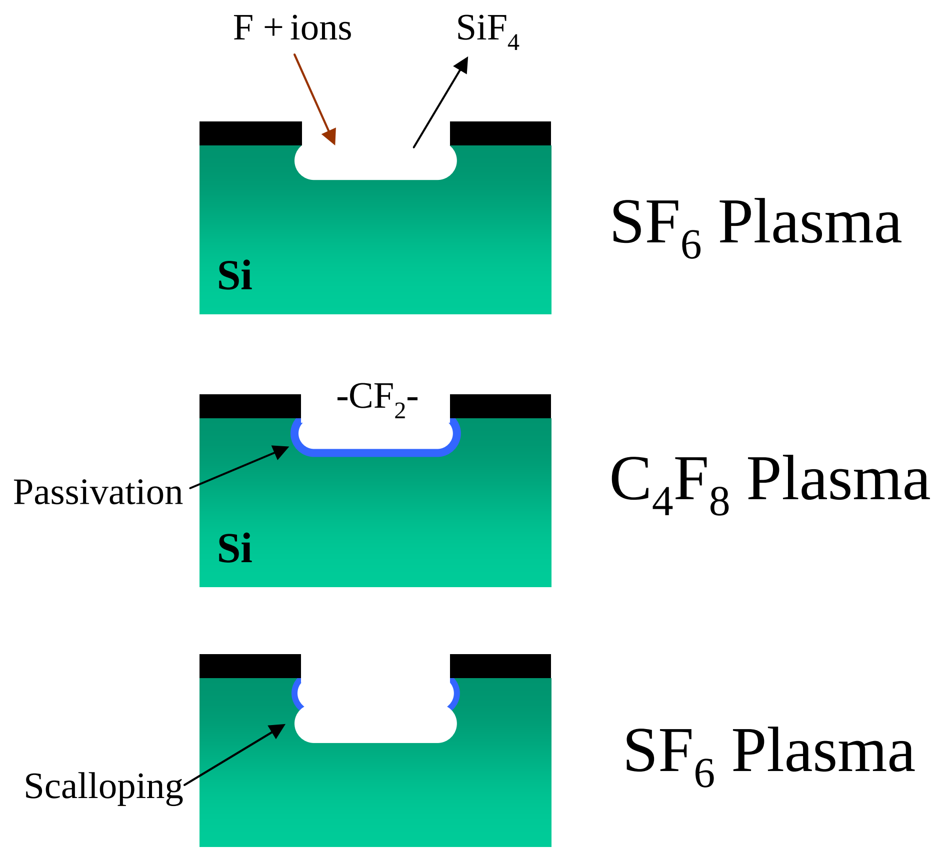


MEMs encompass a wide range of dimensions

The Bosch DRIE Process

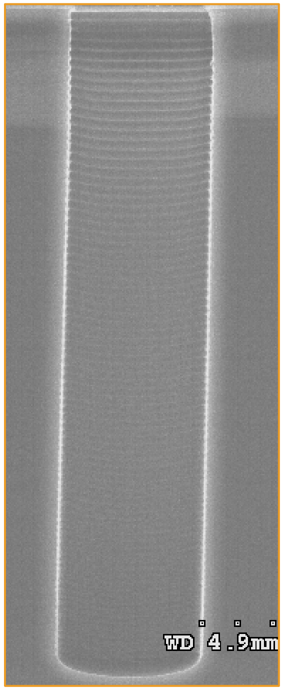


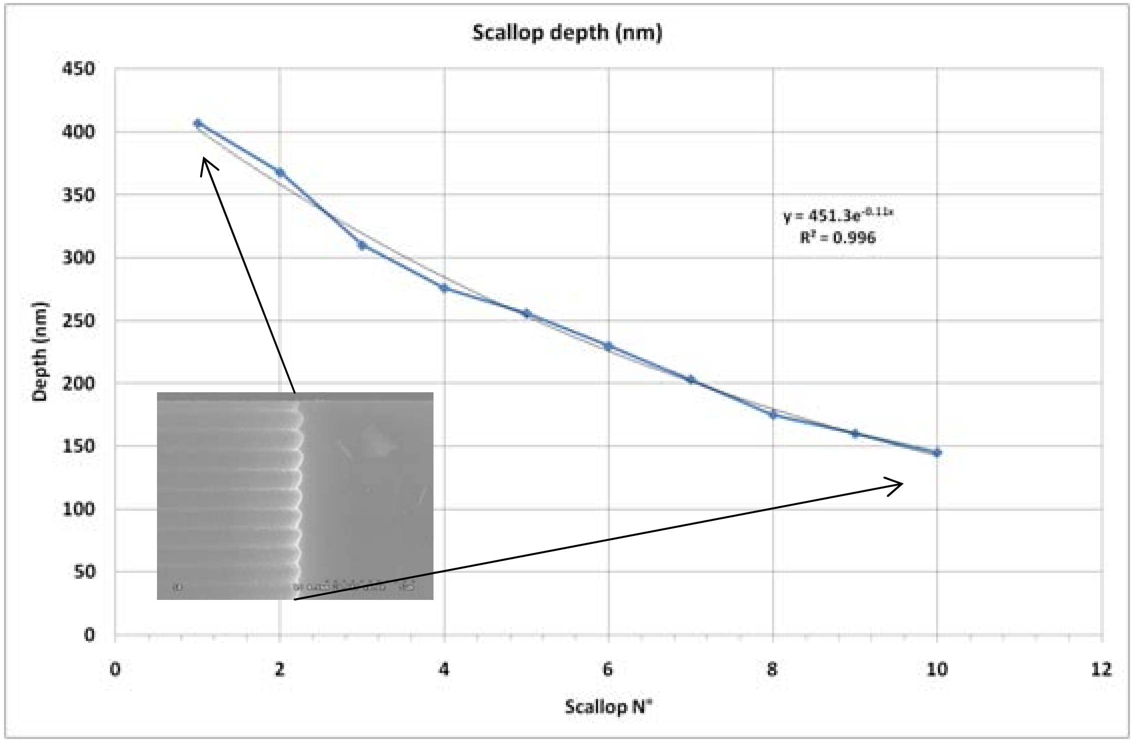




Bosch: A cyclic process alternating between Etch and passivation

Silicon DRIE – Scallops





Scallops get smoother with depth, and can be reduced by increasing C_4F_8 during the etch step.

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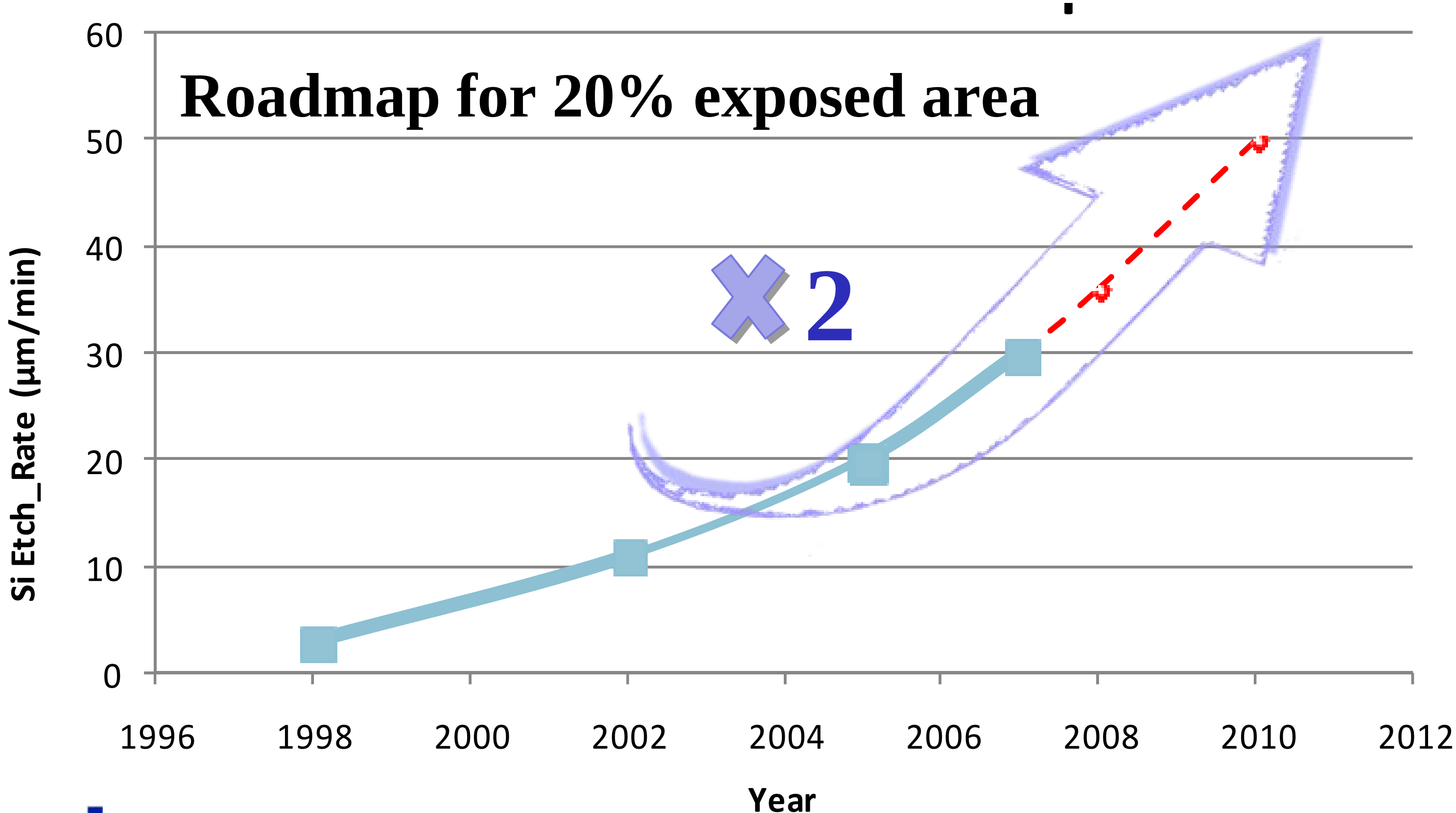
The Race Toward Higher Etch Rate

- Silicon etching is by “F”, a chemical process with loading effects.
- Higher gas flow and pressure, better gas utilization are needed.
- Higher RF Power is needed.



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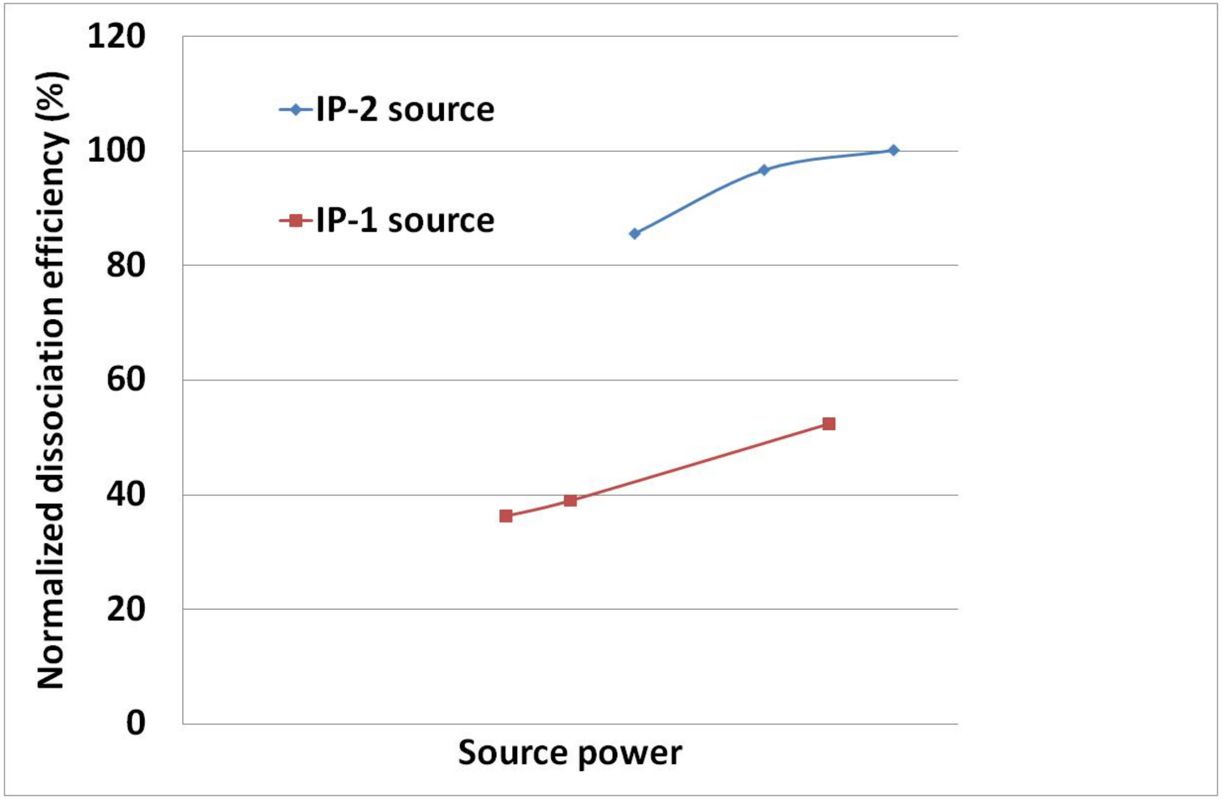
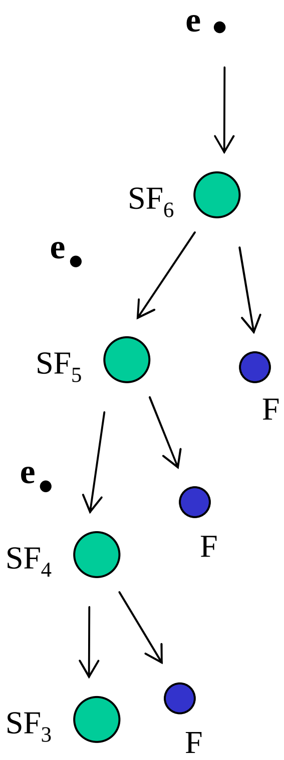
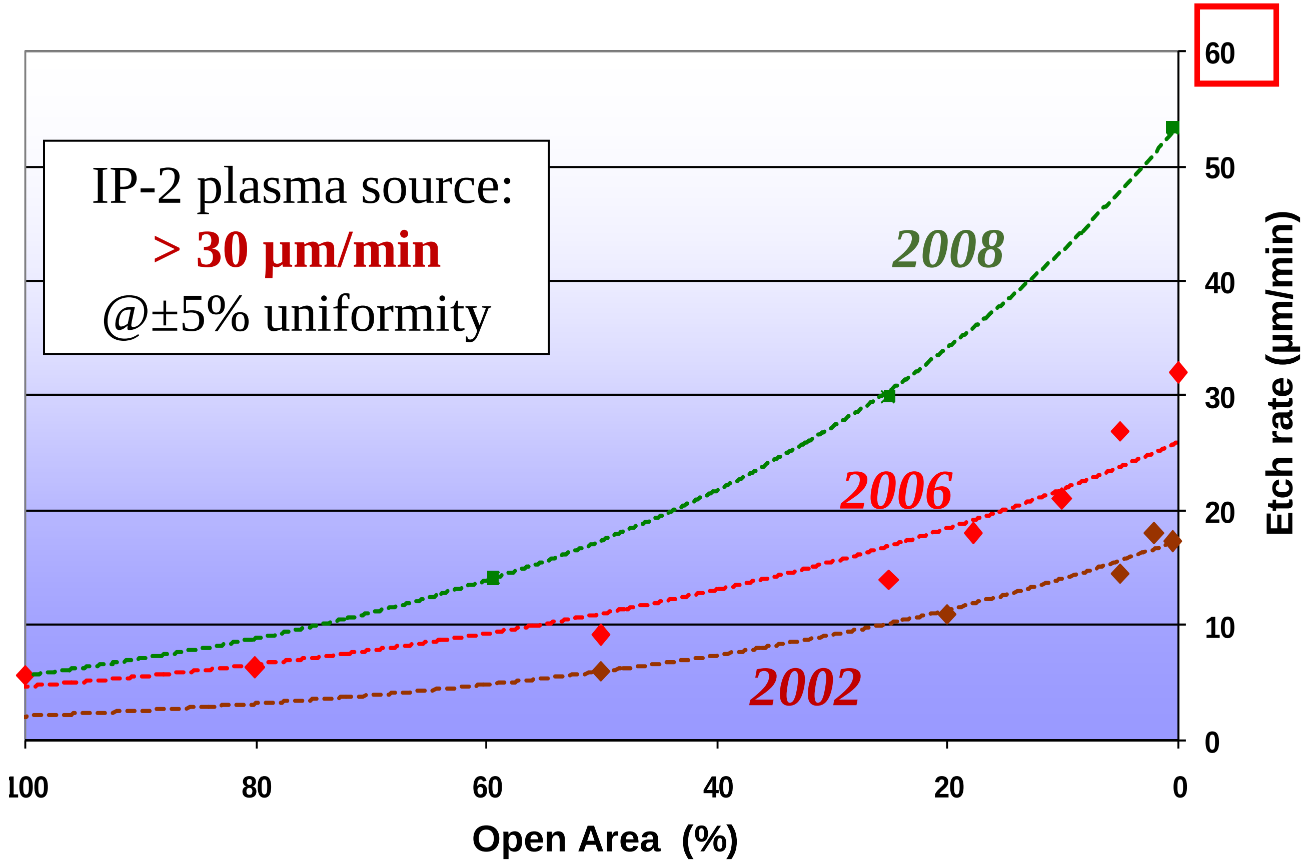
Silicon DRIE – Improved gas utilization





100 % Increase in gas dissociation with IP-2 source

Silicon DRIE – Improved etch rate



Newest Generation plasma source significantly increases silicon etch rate

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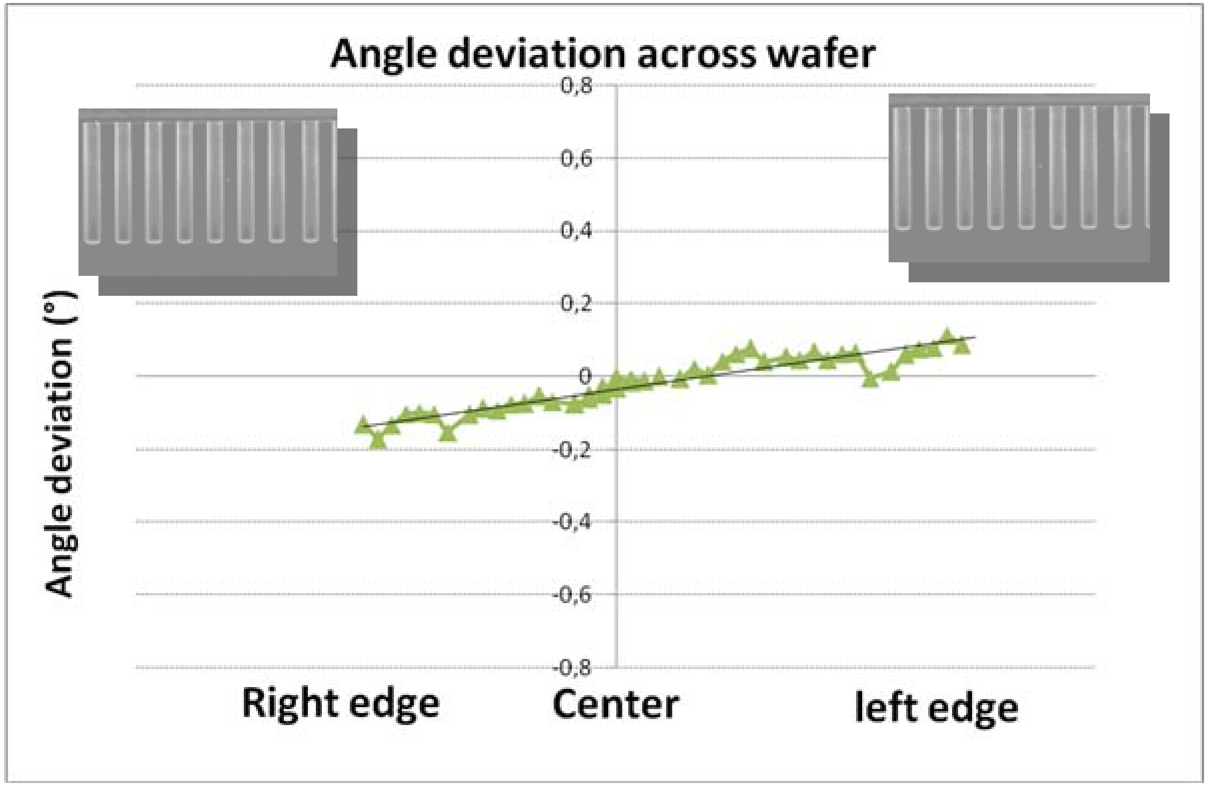
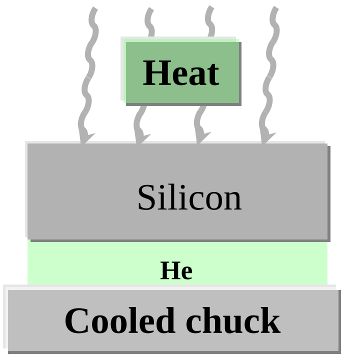
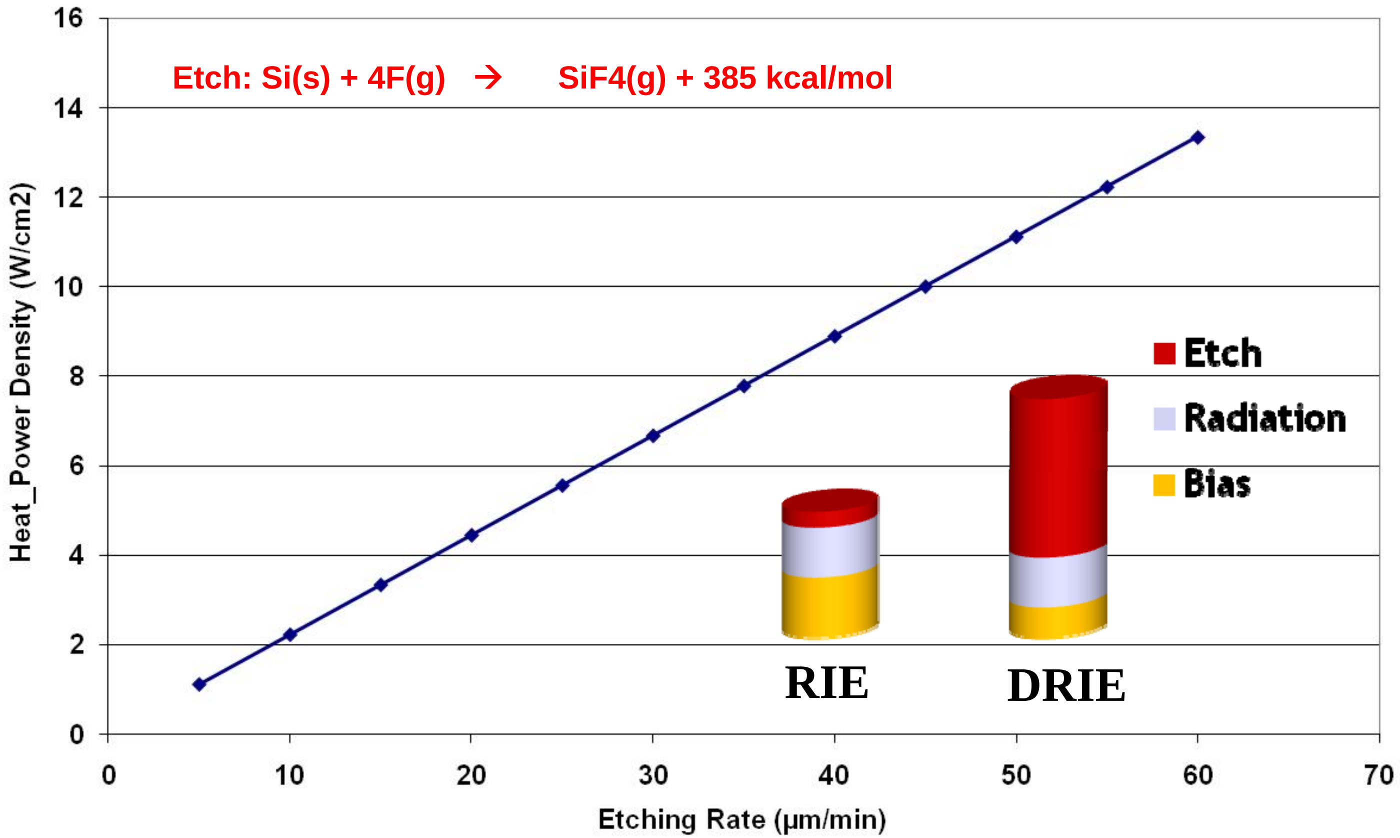
Silicon DRIE - Angle Deviation



Gas and plasma uniformity improvements provide tight profile control across the wafer, < 0.15 °

Thermal Dissipation Issues

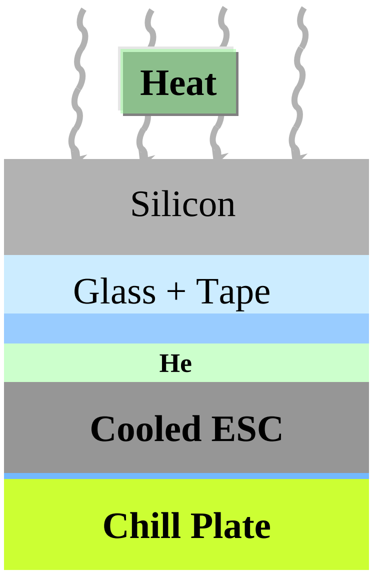




Increasing etch rate inevitably produces more heat to dissipate.

Thermal Dissipation Issues

- Wafer clamping with He backside pressure is the only way to maintain a low temperature substrate surface.

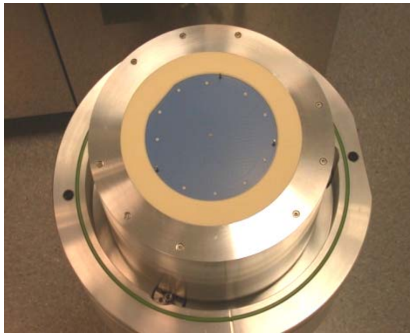


Thermal conductivity of materials (W/M-K)

Glass	Alumina	AlN	Kapton	Silicon	Aluminum	Helium
≈ 1	15-30	180	0.16	156	210	0.15

Thermal resistive substrate materials can be a limiting factor for High etching rate and profile control.

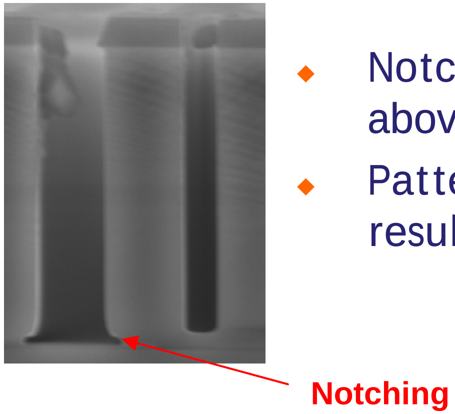
Chill plate interface can impact the ESC cooling effectiveness .



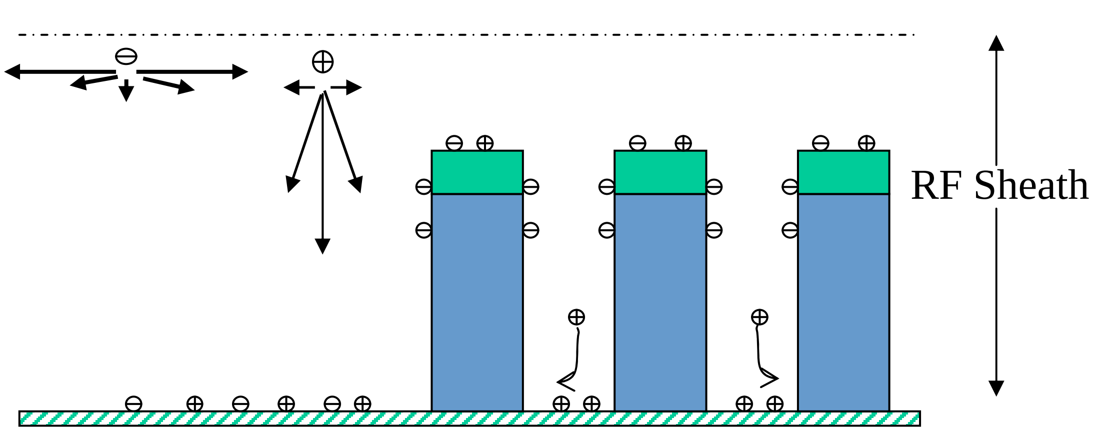
ESC for SOI

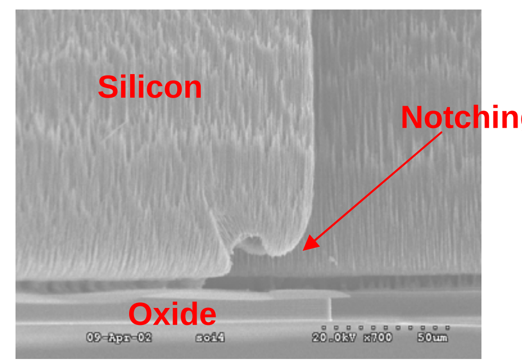
Newest generation ESC design improves wafer cooling efficiency

MEMS & SOI: notching



- Notching is the local side etching of a conductive layer (silicon) above an insulating layer (oxide).
- Pattern bottoms are charged up by an excess of positive ions, resulting in a divergence of ion trajectories close to the oxide layer.

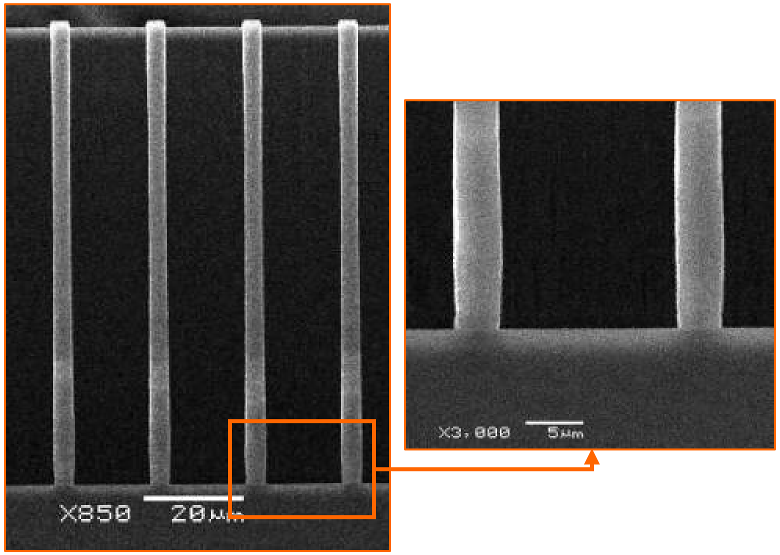




MEMS devices on SOI substrates require careful attention to notch suppression

How to suppress the notching ?

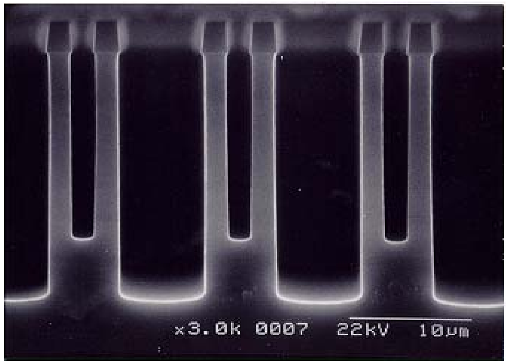
- 1 – Increase the sidewall protection
  - Protection decreases with Aspect Ratio
  - Net Etch rate tends to zero at higher AR!!!
- 2 – Neutralize the charge built-up
  - Reduce the bias frequency and pulse the bias power.
  - During the “Off” period, surface potential decreases.
  - Electrons accelerate toward the surface and neutralize the positive charges at the bottom.
  - Less charge => less trajectory bending
    => smaller notches

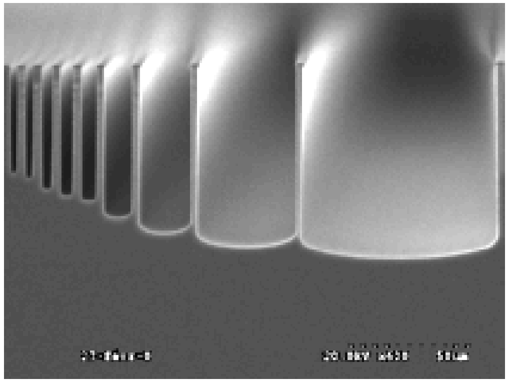


Tegal DRIE process technology can suppress notch formation on SOI substrates

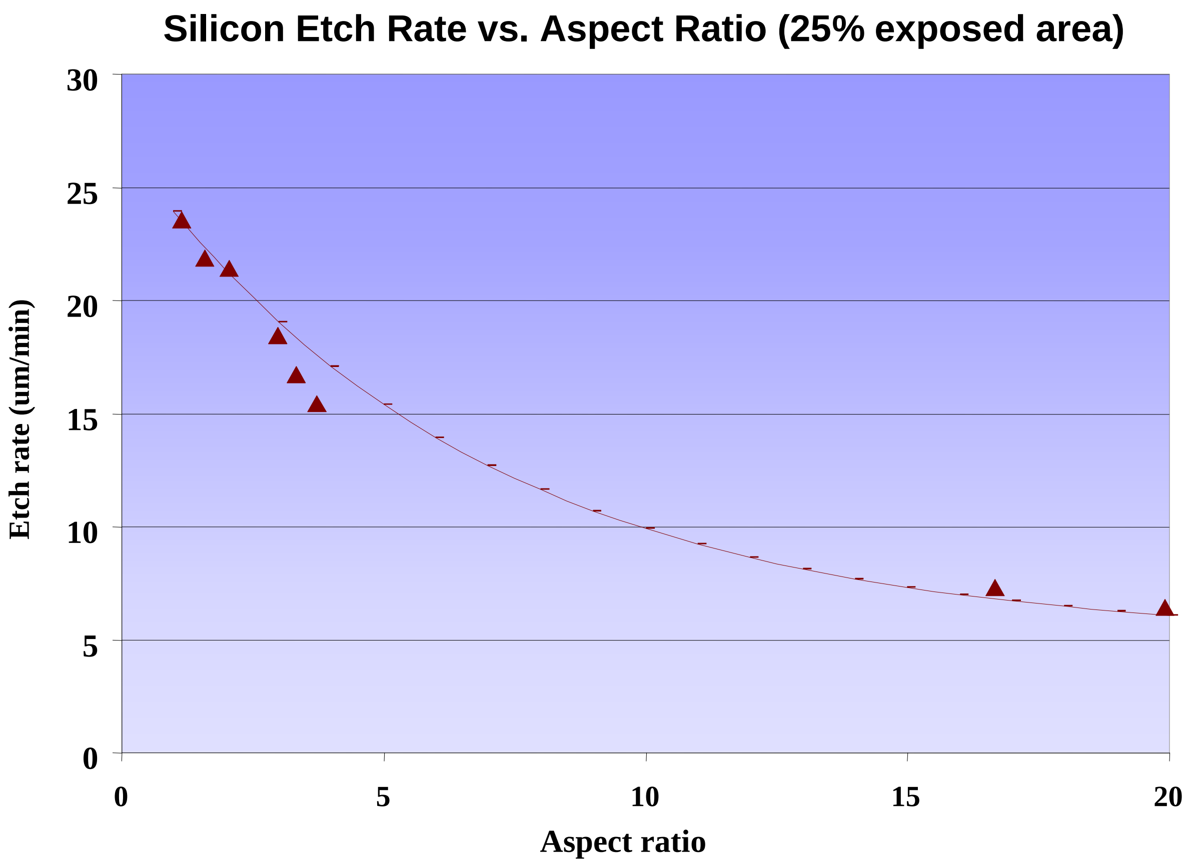
ARDE Control in Si Etching

- Aspect Ratio Dependent Etching (ARDE): etch rate decreases when A.R increases.
- Most MEMS devices include structures with a wide range of feature sizes, which can have different etch rates.
- High over-etching time is required to complete the etching of the narrow features.





Silicon DRIE – ARDE



Aspect **R**atio **D**ependent **E**tch rate: Higher Aspect Ratios result in lower etch rates

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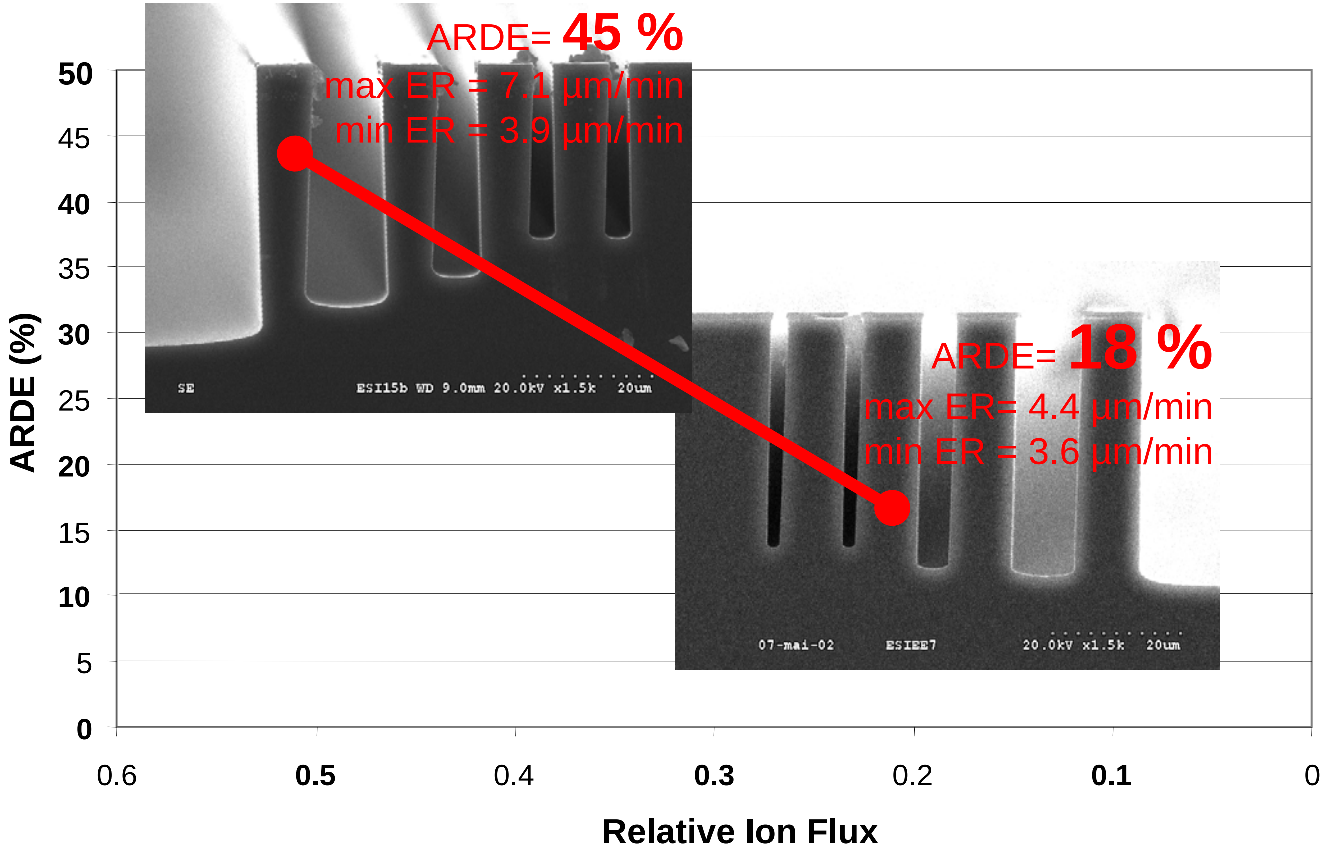
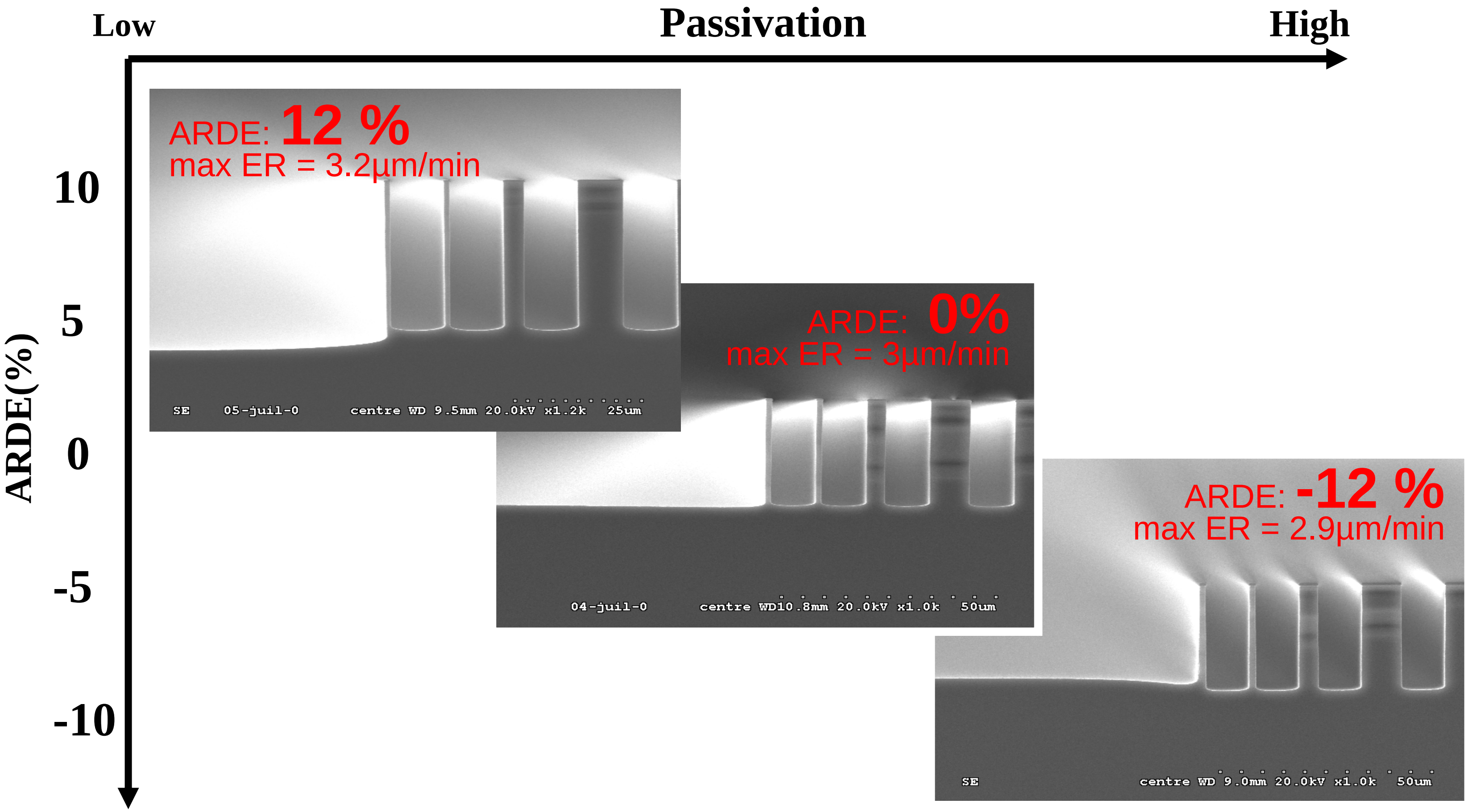
ARDE: Role of Ions



Decreasing the Ion flux reduces the effect of ARDE

ARDE: Role of passivation layer



Further ARDE improvement can be made by modification of the passivation process

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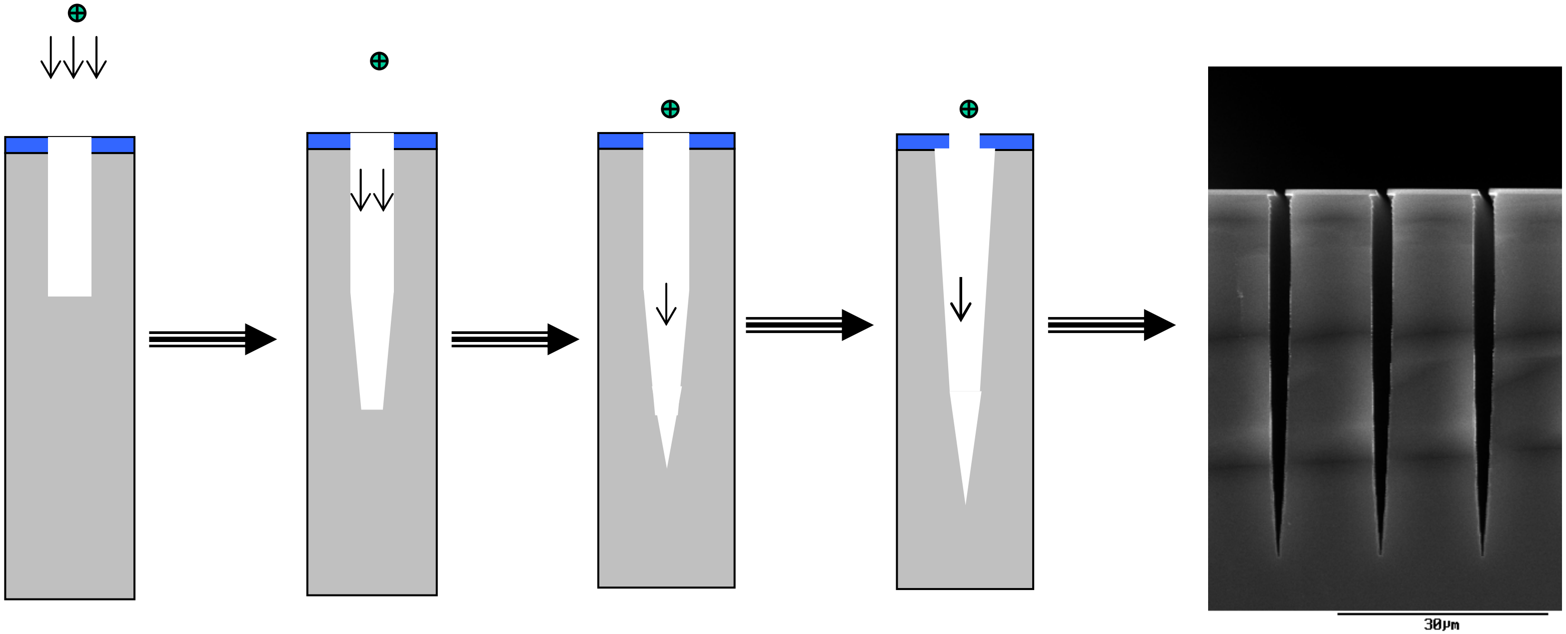
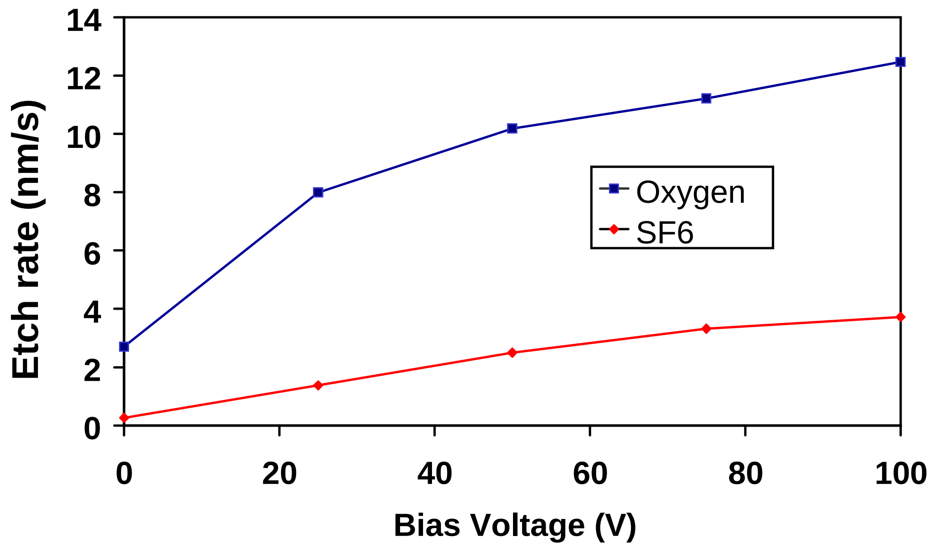
High Aspect Ratio limitation



The standard Bosch process is limited to an aspect ratio of ~20.

The Tegal SHARP Process

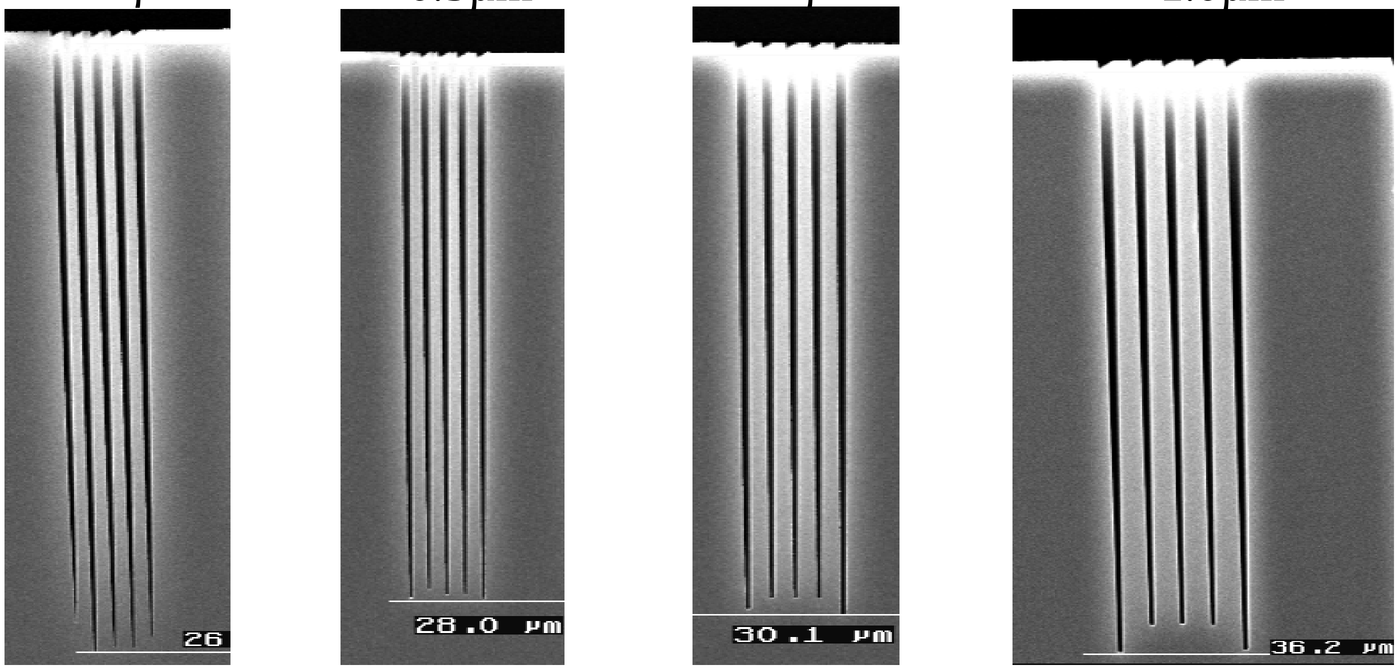
- Standard solutions for increasing the maximum aspect ratio are inefficient. (pressure, bias, ion flux)



An O2 Plasma removes polymer 5 time faster than an SF6 plasma.

SHARP*: Super High Aspect Ratio Process

*Patent pending



0.4µm	0.5µm	0.6µm	1.0µm
AR= 65	AR= 56	AR= 50	AR= 36

Insertion of an O_2 step into a standard Bosch process sequence optimizes polymer removal. Aspect Ratios of 100:1 can be achieved.

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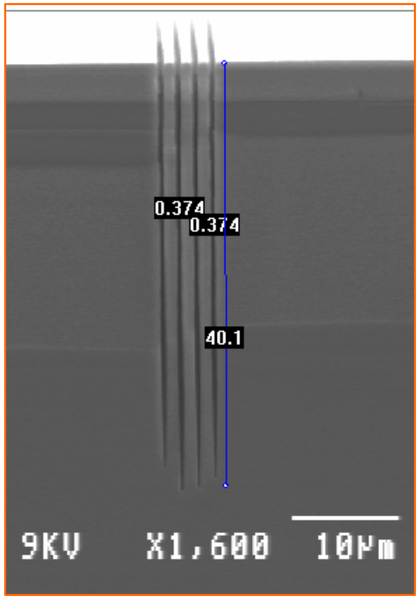
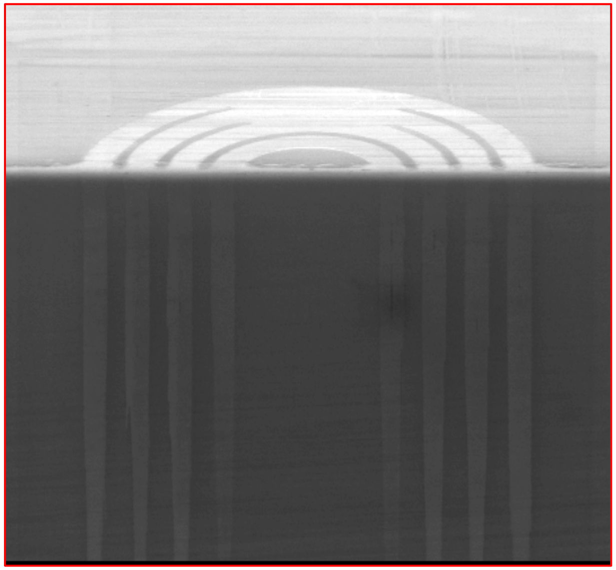
Super High Aspect Ratio Process (SHARP)



Courtesy: ESIEE

AR= 107

SHARP Patented Process
Achieving Aspect Ratio
> 100



Courtesy: CEA .LETI

Selective and faster removal of the polymer layer improves high aspect ratio etching

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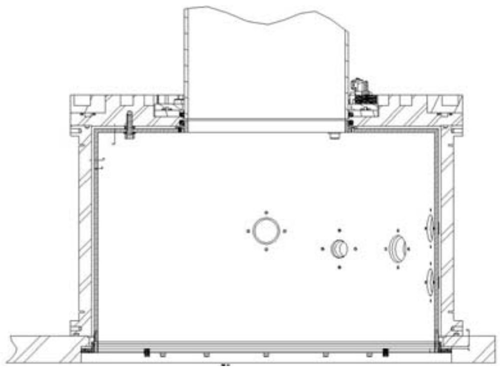
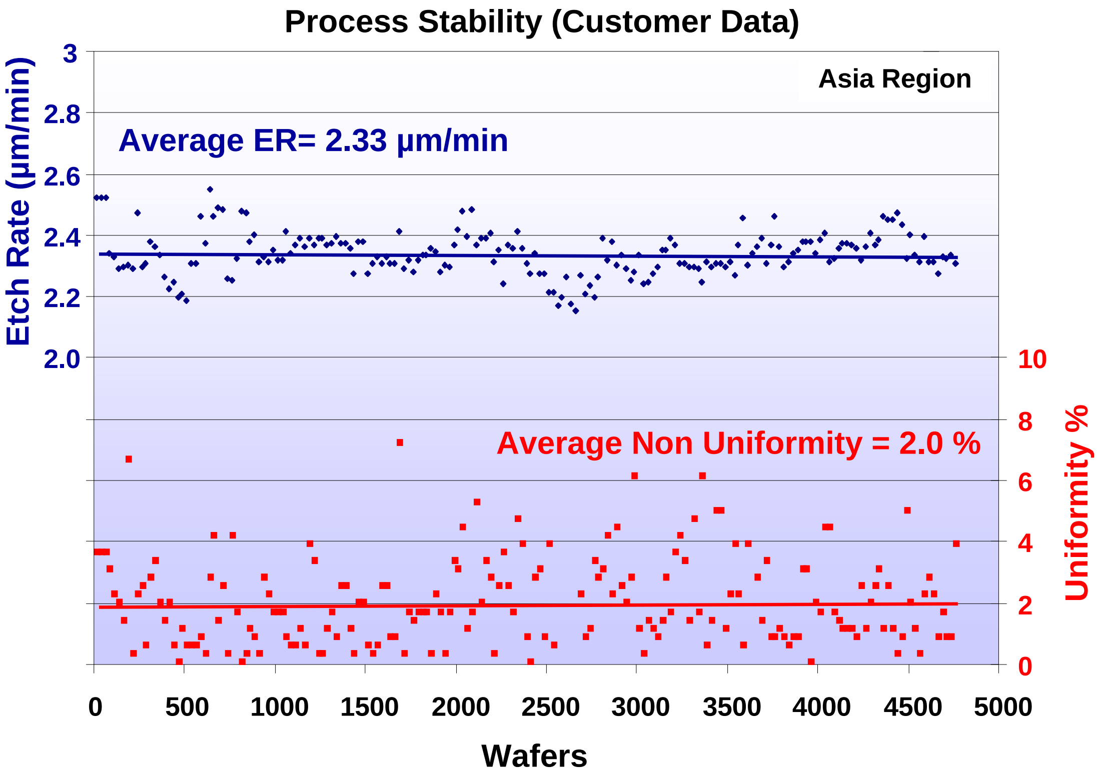
Process Stability

- Passivation polymers deposit on all the cooled reactor surfaces.
- Accumulation of polymers can produce process drift.





- Tegal chamber walls are temperature controlled to reduce polymer layer built up.
- Less frequent "wet" cleans are required.

Reactor design improves process stability and reduces manual cleaning downtime.

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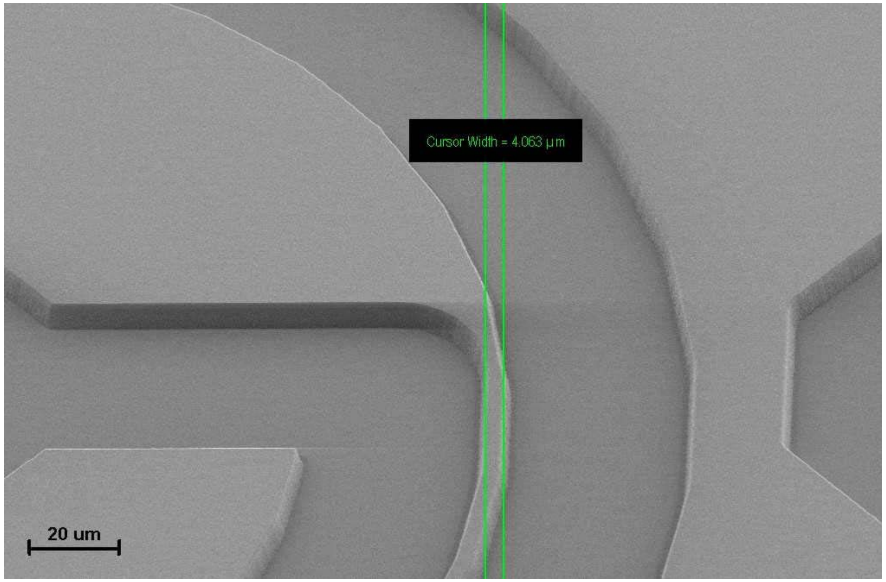
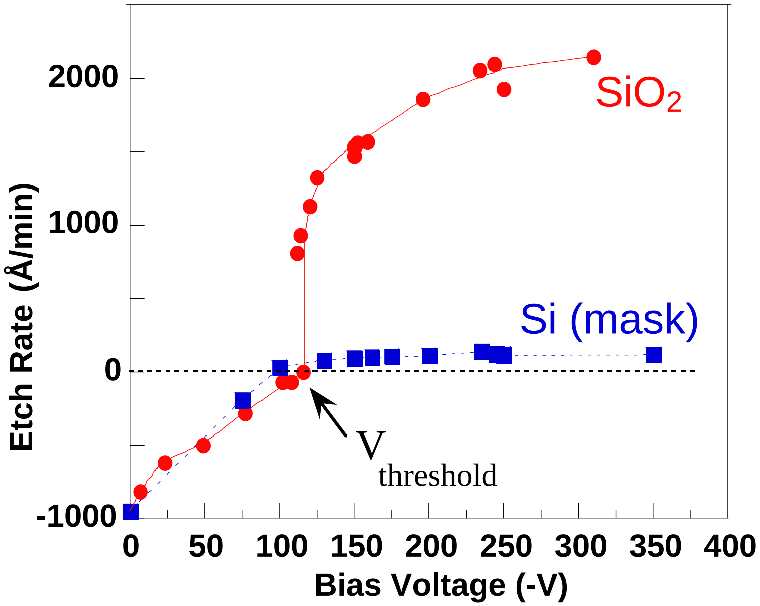
Thick Oxide & Glass Etching

- Deep etching of glass materials
- Bias Voltage optimized
- Etch Rate > 0.4 µm/min
- Selectivity > 18:1





Tegal DRIE can also etch deep oxide features.

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Conclusion

- DRIE of silicon is a key enabling technology for MEMS.
- Significant DRIE improvements have been discussed:
  - Improved gas utilization and etch rate (Hardware)
  - Angle deviation (Process & Hardware)
  - Improved thermal dissipation (Hardware)
  - Notching control (Process & Hardware)
  - Improved ARDE (Process)
  - SHARP (Process)
  - Improved Process Stability (Hardware)

Questions?