MEMS Development at Maxim Using STS VPX

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Outline

- STS VPX Introduction
- MEMS Development Examples
- Summary

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STS VPX Platform

- Released January 2006, up to three process chambers to share a common automated wafer transport platform
- Provide advanced high rate for silicon and compound semiconductor DRIE
- Well-suited for pilot production markets to transfer new device technology from R&D

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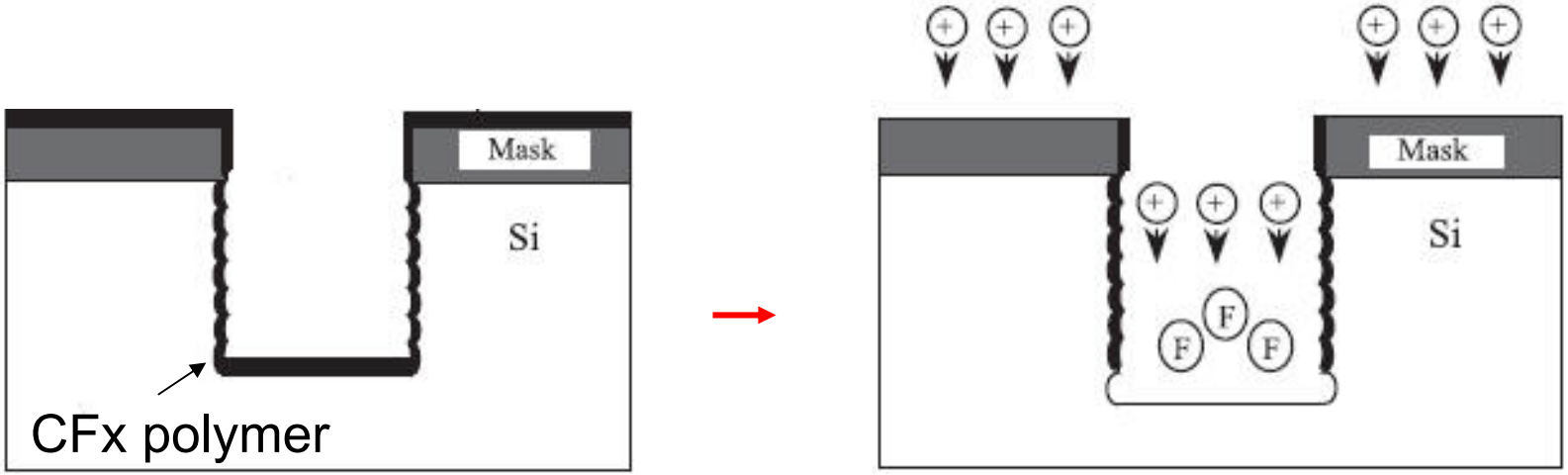
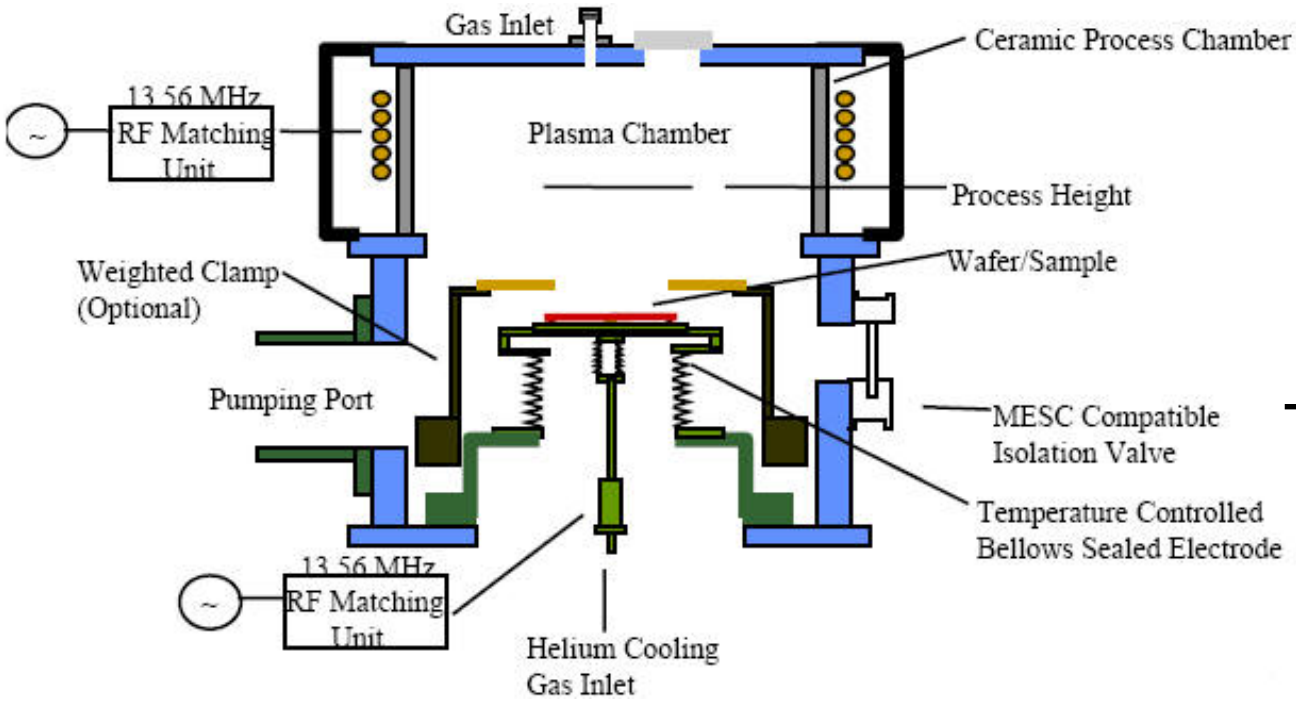
General Principle – ASE™ Bosch Process





ASE Anisotropic Etching schematic (Top)

Typical STS ICP system schematic (Bottom)

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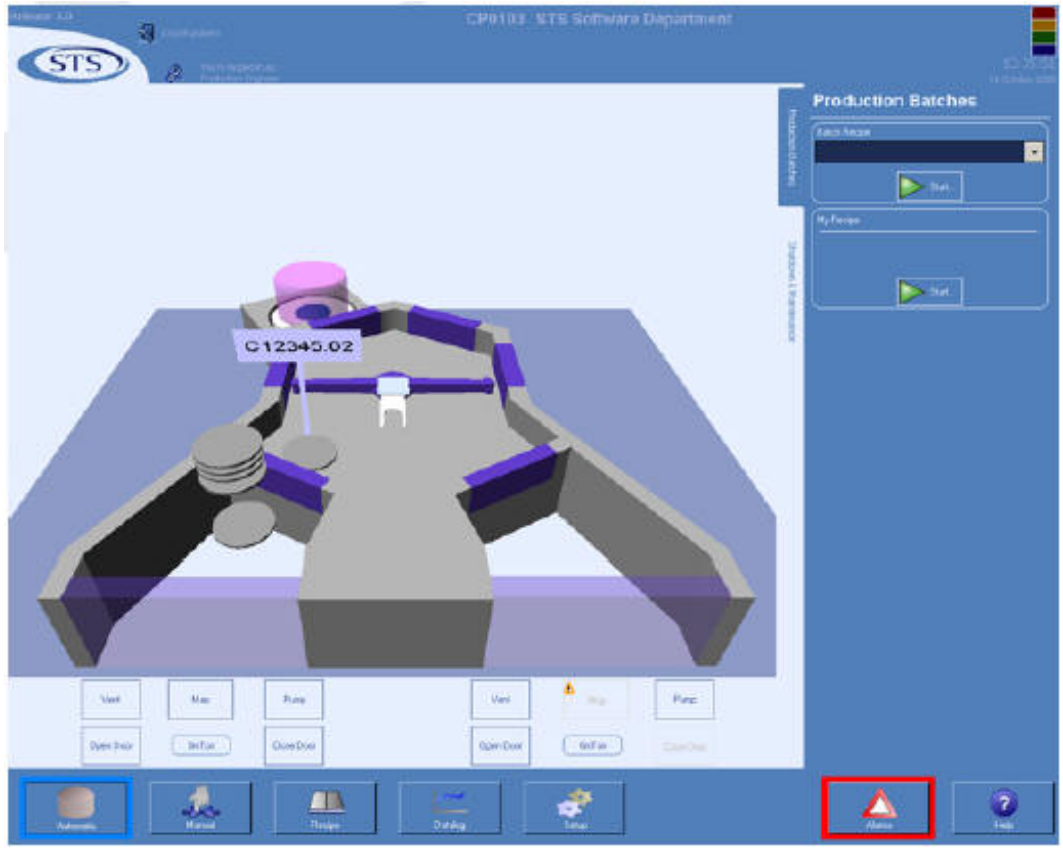
Maxim STS VPX System



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Process Development 1

Etch Characteristics	Specification	STS UK Results	Dallas Results
Depth (µm)	200	227.3	188
Etch Rate (µm/min)	10	10.3	11.8
Uniformity (±%)	3	1.9	1.3
Repeatability (%)	3	0.3	2.2
Selectivity to PR	80:1	90:1	>90:1
Profile (º)	90±1	90.7	91
Initial Mask Undercut (µm/edge)	<1	0.52	0.3
Scalloping (nm)	<500	352.4	438.8

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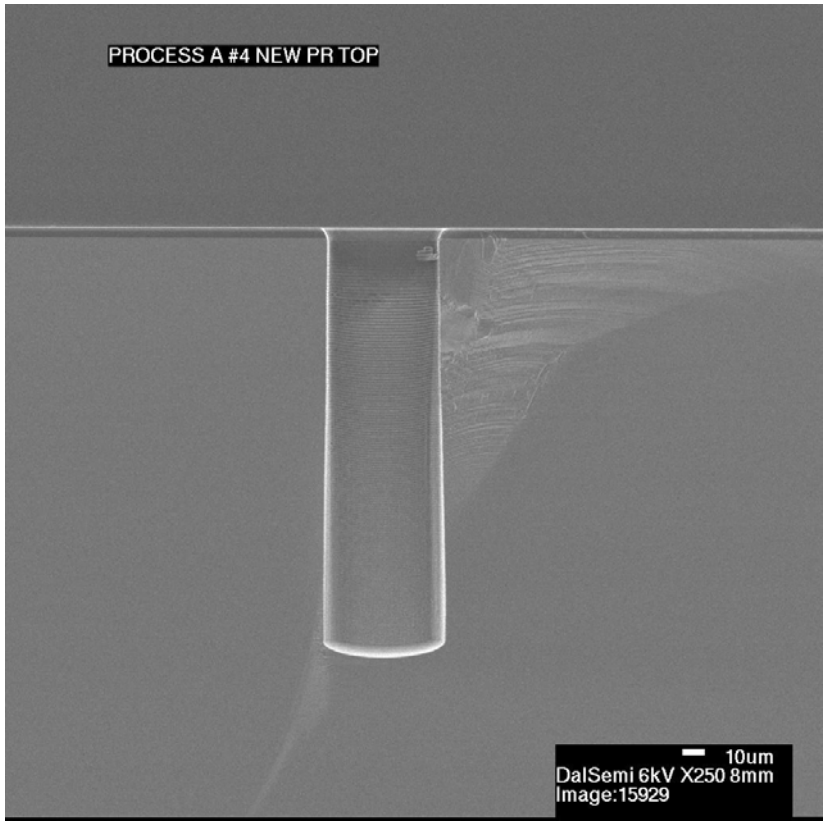
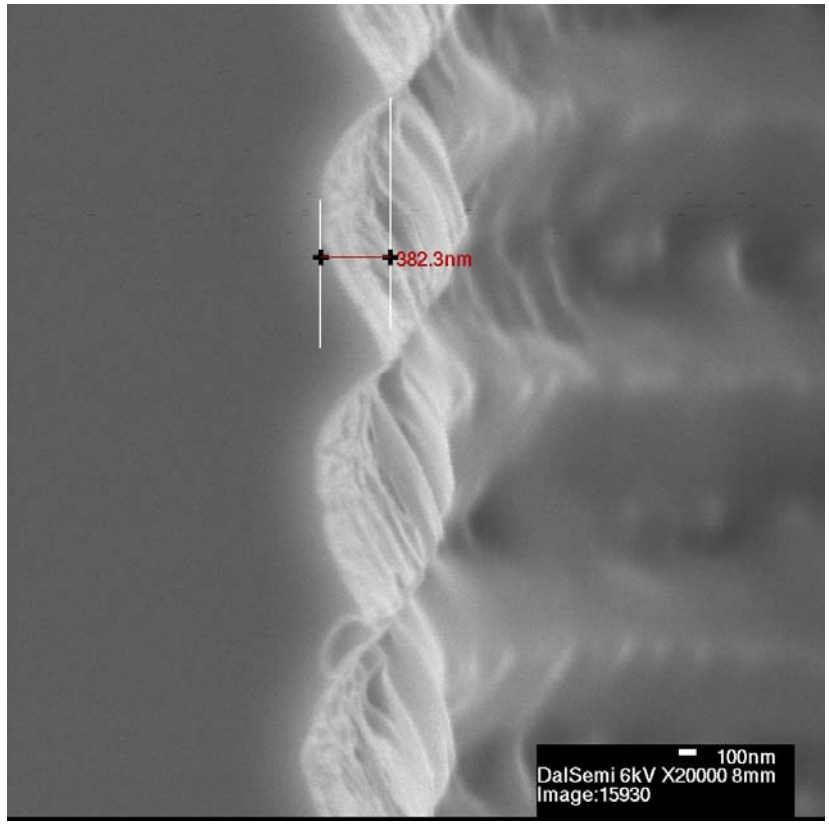
SEM Micrographs



(a)



(b)

SEM micrograph for a 200-μm-deep trench with 382 nm scalloping

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Process Development 2

Etch Characteristics	Specification	STS UK Results	Dallas Results
Depth (µm)	200	200	203
Etch Rate (µm/min)	>7	9.1	9.3
Uniformity (±%)	3	1.3	1
Repeatability (%)	3	1.3	1.1
Selectivity to PR	60	72	>61:1
Profile (º)	90±1	90.6	90.6
Initial Mask Undercut (µm/edge)	<1	0.33	0.26
Scalloping (nm)	<300	290.8	236.4

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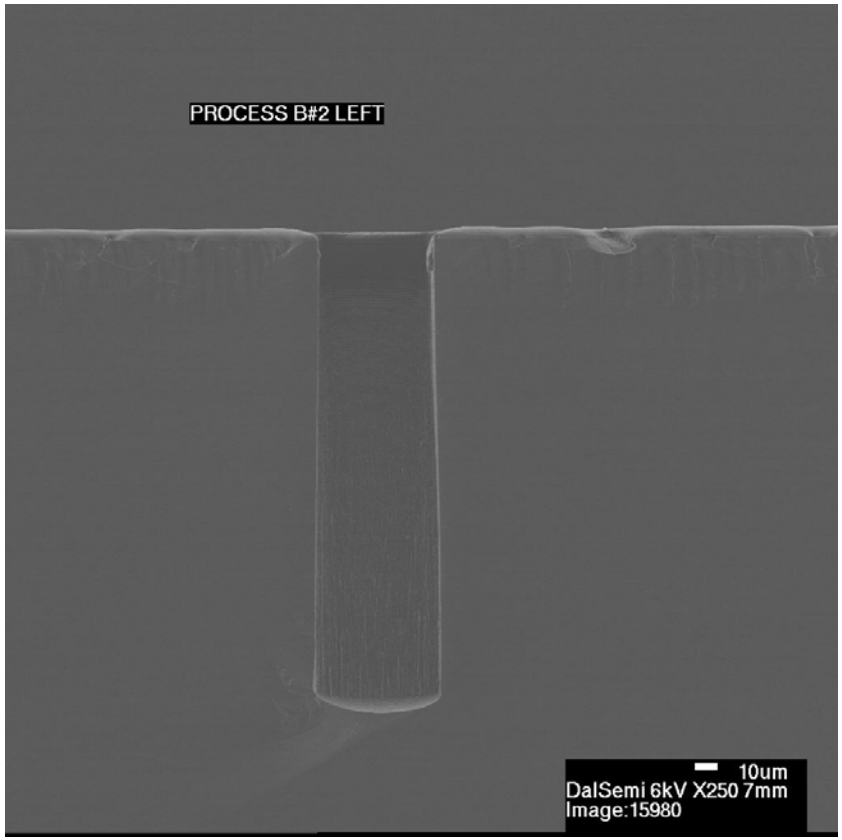
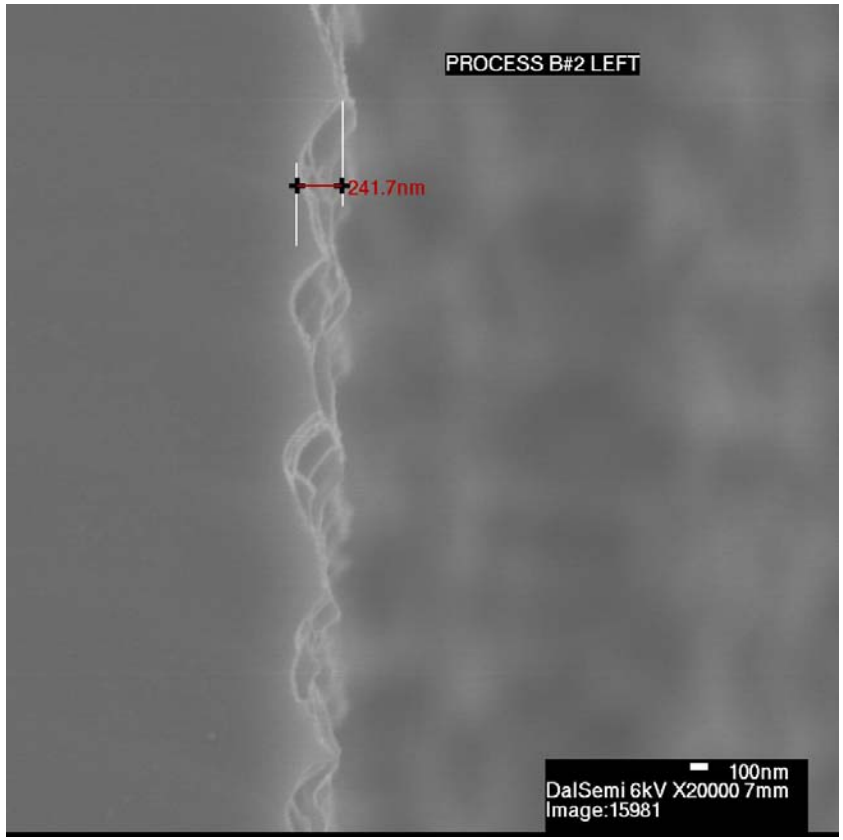
SEM Micrographs



(a)



(b)

SEM micrograph for a 200-μm-deep trench with 242 nm scalloping

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Process Development 3

Etch Characteristics	Specification	Dallas Results
Depth (μm)	100	101
Etch Rate (μm/min)	>10	12
Uniformity (±%)	3	1.23
Selectivity to PR	70:1	>78:1
Profile (º)	slightly positive	89.6
Initial Mask Undercut (μm/edge)	<1.2	0.83
Scalloping (nm)	<1000	800

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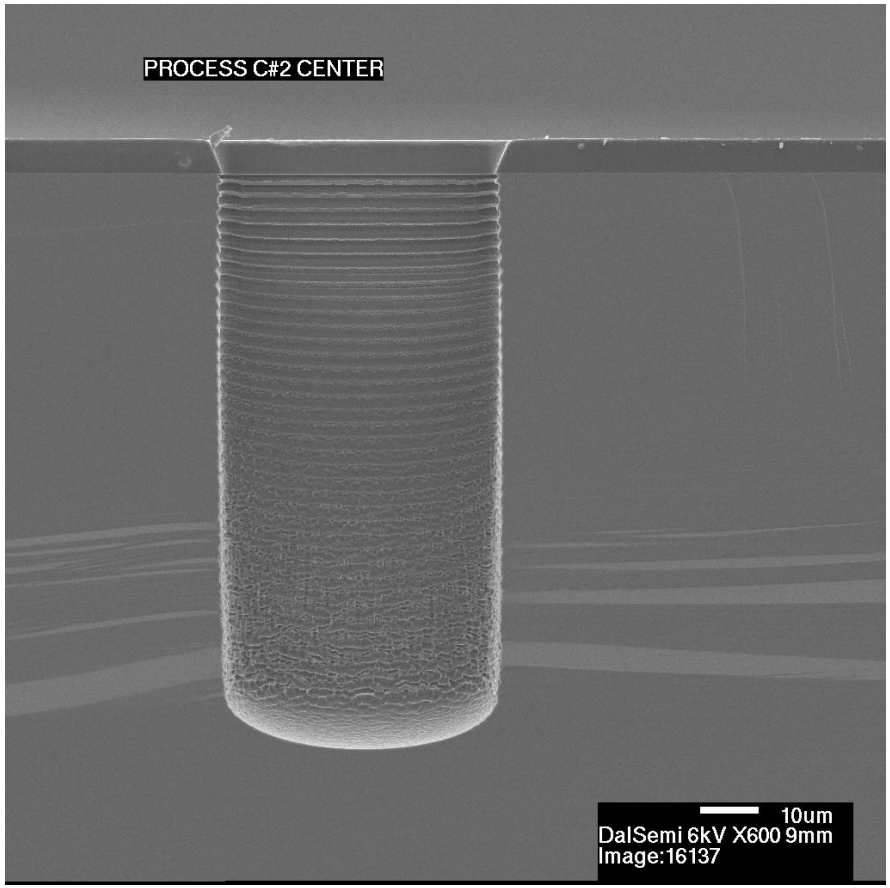
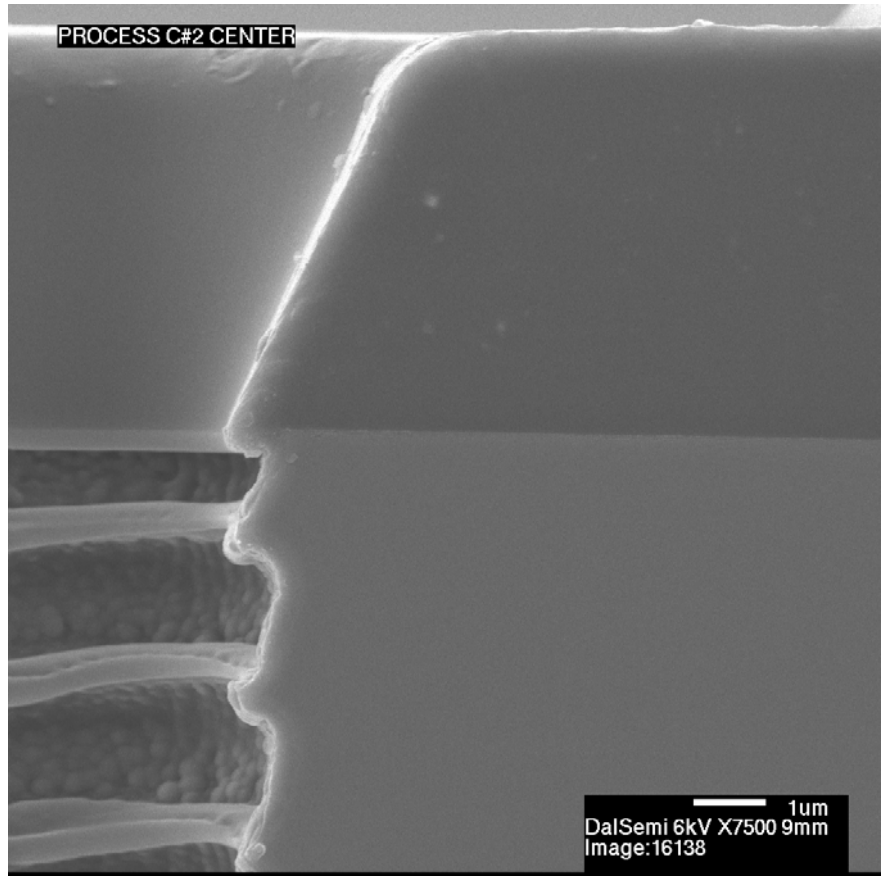
SEM Micrographs



(a)



(b)

SEM micrograph for a 100-μm-deep trench with 600 nm scalloping

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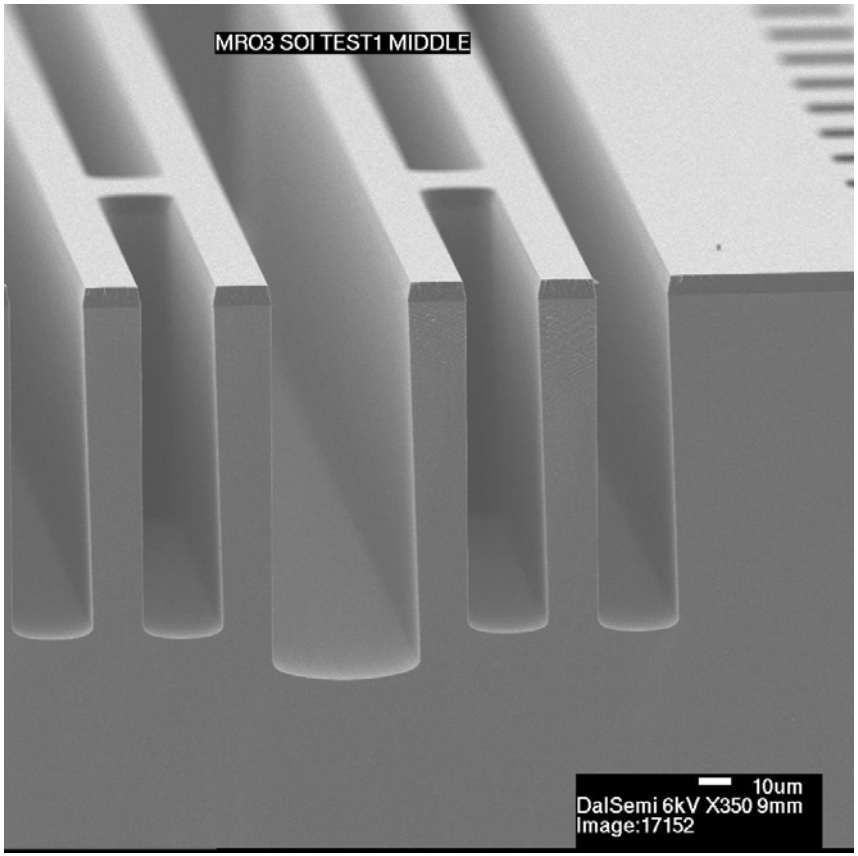
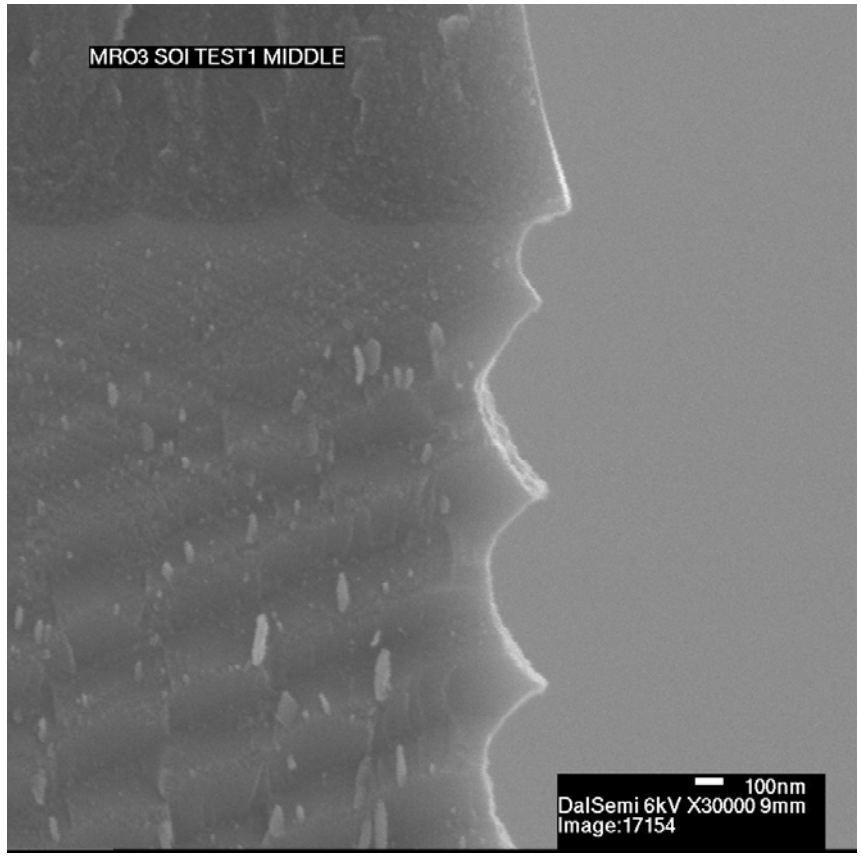
Process Development 4

- 80-100 μm silicon DRIE on SOI substrate without micro-grassing, good selectivity over oxide layer
- No notching issue at the interface of device silicon layer and buried oxide layer
- ARDE ratio should be less than 2:1

SEM Micrographs



(a)



(b)

SOI 100-μm-deep release with 210 nm scalloping

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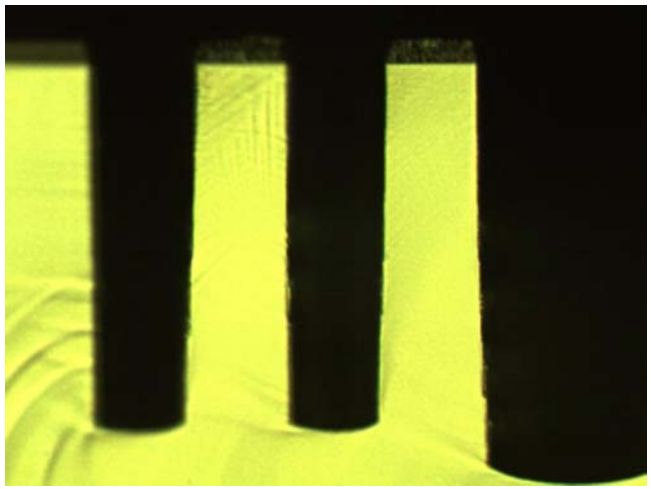
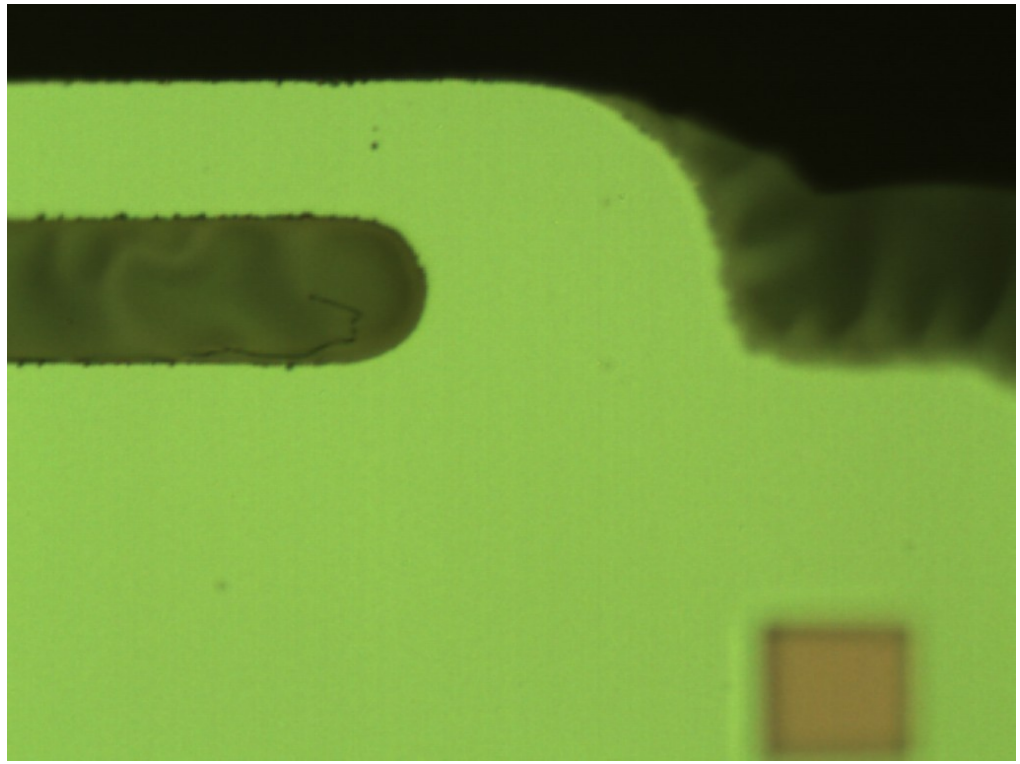
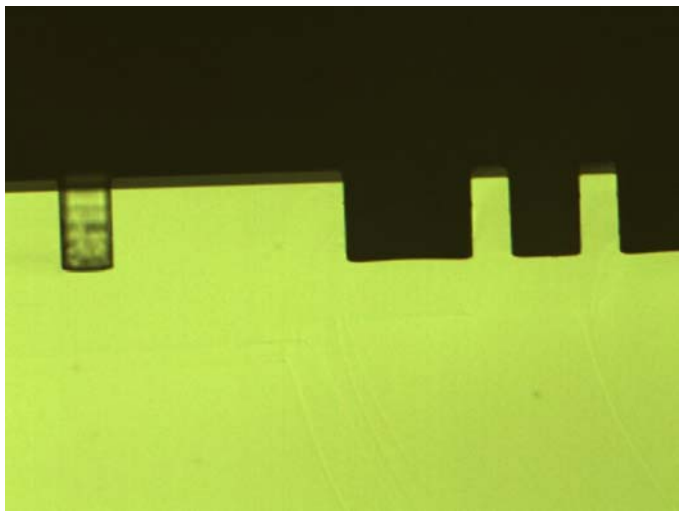
Other Development for Process 4



Positive slope





No notching at the silicon and oxide interface with ER 8 μm/min and selectivity to oxide over 200:1

No ARDE effect for 50 μm etch

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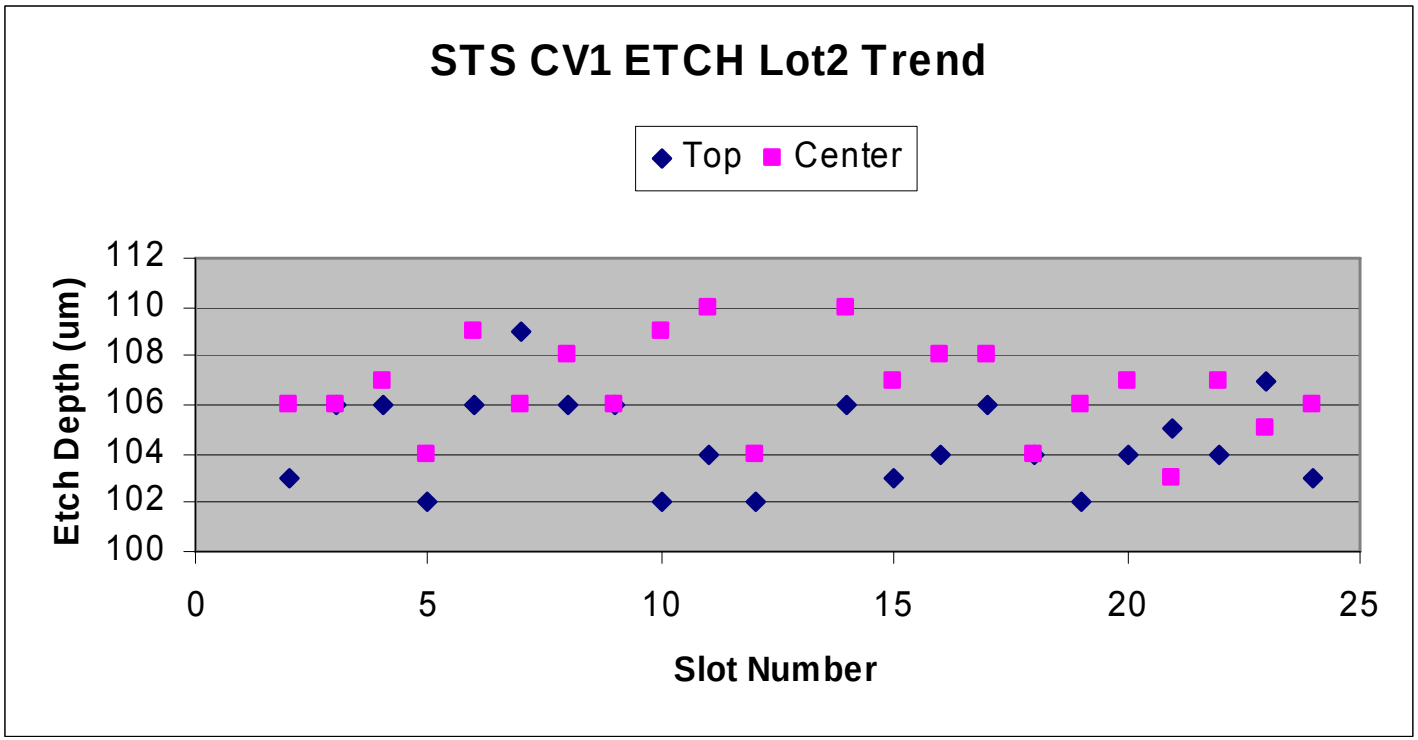
Production Implement Example

- High throughput for Process 3 (100 μm trench): 5 wafer/hr, including loading, wafer transfer, and unloading.
- Lot manufacturing is stable and meets IOS target



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Current Issue for the VPX Platform

- Wafer handling repeatability is not 100% guaranteed.

During a 1000-wafer handling test, the scheduler log showed an error for wafer transfer in either robot or aligner stage for the No. 764 wafer.

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Summary

- High Etch Rate
- High selectivity over oxide and photoresist
- Good uniformity
- Versatile tunable parameters provide the flexibility for varied MEMS device structures realization
- Wafer handling repeatability is not so stable yet due to glitches in the operation software and Brooks Robot control

→ **Powerful and convenient platform for MEMS production**

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