Etch Processes for Nano-scale Vertical MOS Devices

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Outline

1. Introduction of Vertical MOS Structures

2. Development a Spacer Process

- Stable Process : widths down to 5nm (Demonstrated)
- Start with Improvement of photo resist profile

→ Poly-Si block etch profile

→ spacer mask profile

→ Si etch profile

3. Improvement in Bulk Si-Fin or pillar etch profile

*This talk is based on :
H. Cho, P. Kapur, P. Kalavade and K. C. Saraswat, "A novel spacer process for sub 25nm thick vertical MOS and its integration with planar MOS device," *Silicon Nanoelectronics Workshop*, No. 5-16, 2005

Introduction of Vertical MOS Structures

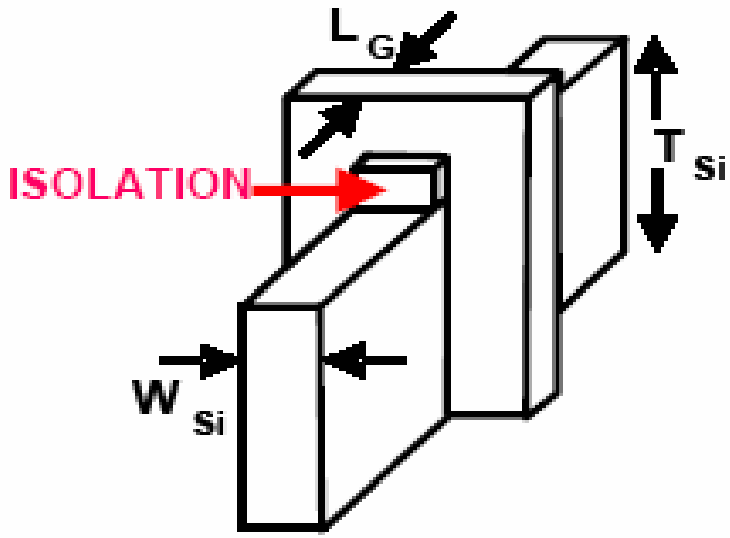
Motivation

- Scalability
- Density
- Easy to achieve Double gate or Tri-gate MOSFET

Types of vertical structures

- The pillar structure
- FINFET
- Vertical S/D Transistor

→Need Spacer process to build a nano-scale Si Fin or Pillar



Double Gate (e.g. FINFET)

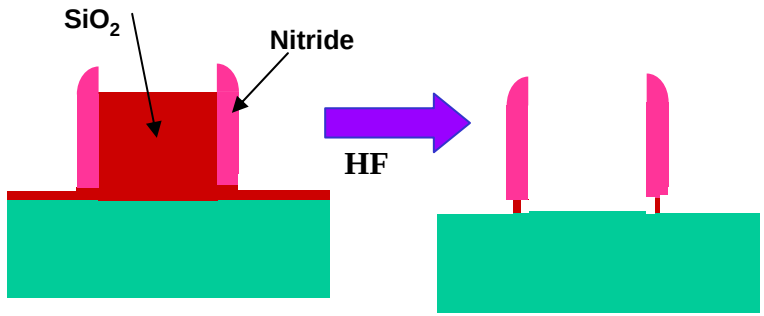
Robert Chau, ICSICT, 2004

New Spacer Process

	Spacer	Block	Pros/Cons
1	**SiN**	**SiO2**	Once tested Nitride uniformity Oxide Undercut (lift-off)
2.	**SiN**	**Poly-Si**	Poly roughness Nitride uniformity
3.	SiN	Si/Ge	Etch selectivity to nitride/oxide
4.	SiO2	SiN	Stress issues
5.	SiO2	Poly-Si	#2 is a better option (nitride uniformity)
6.	Poly-Si	SiO2	A. High aspect ratio, B.Mask erosion
7.	Poly-Si	SiN	

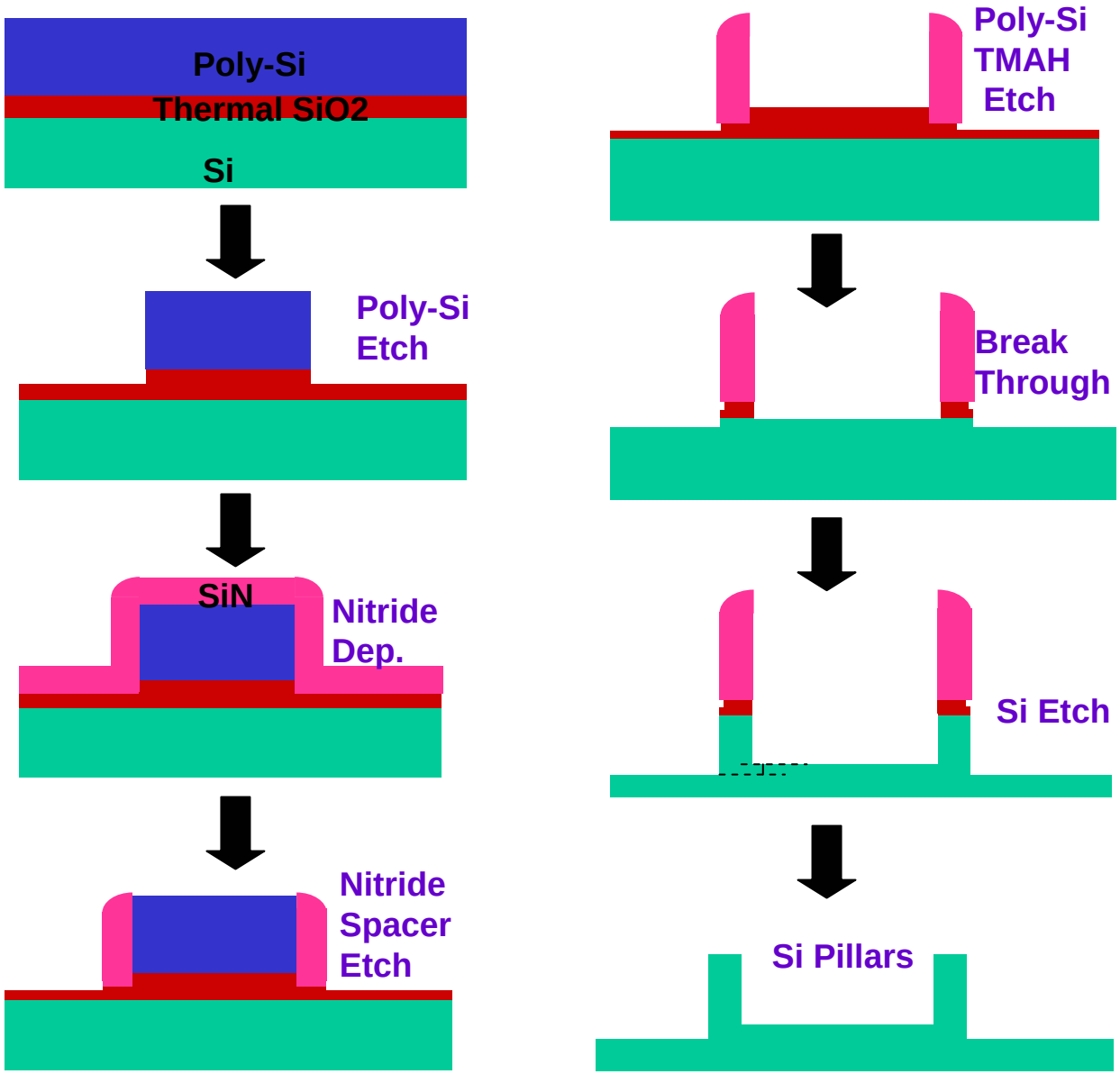
→ **Pursued !!**

Example) Spacer with oxide block



- hard to make very thin spacer due to lift off !!

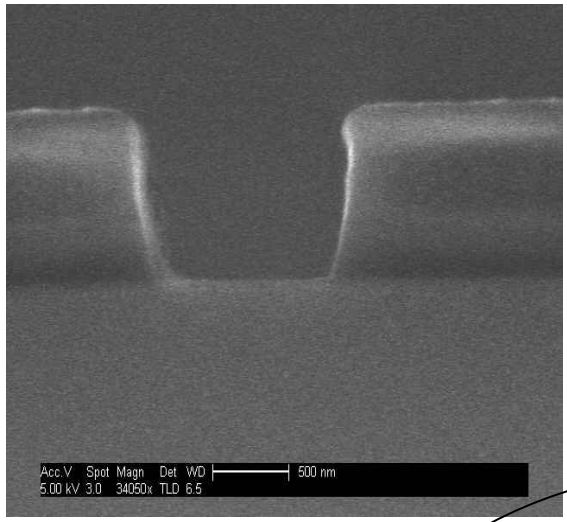
New Spacer Process Flow



Photoresist sidewall Optimization with Nikon

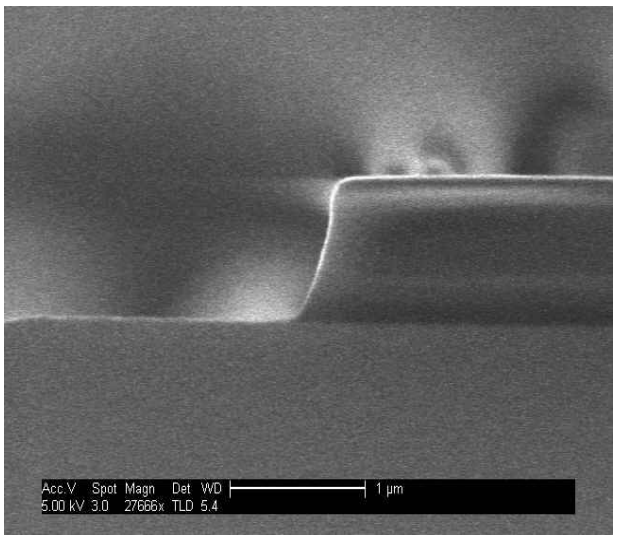
Critical as it dictates the Si-Fin's reverse tapering

-1um positive photo resist
-With a post expose baking:
1min, 110^{o}C



Expose time= 240msec ,
focus offset=0

Choose this



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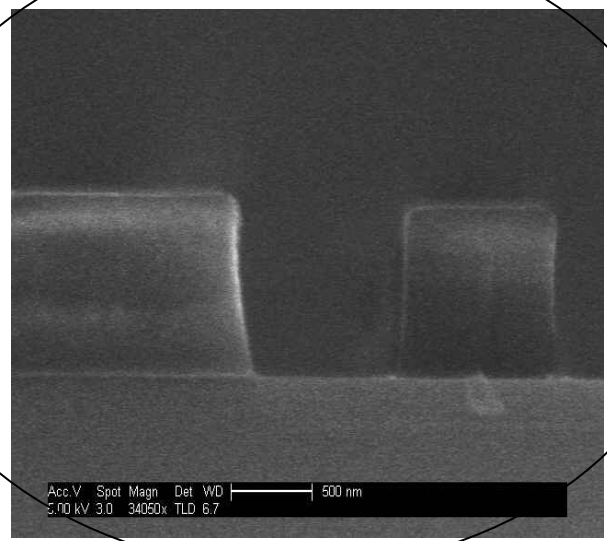


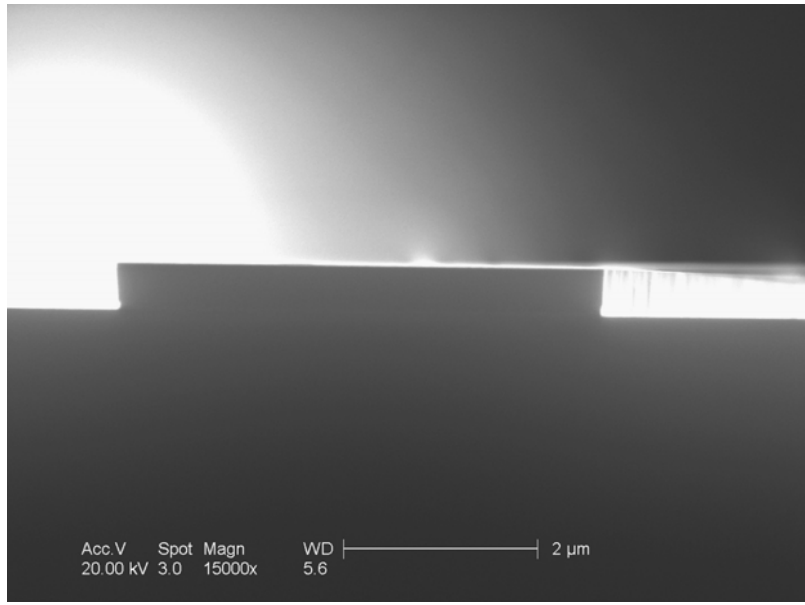
Expose time= 200msec ,
focus offset=1

Thickness Choices

- **Thermal oxide thickness: 15nm (Tradeoffs)**
  - Thin: can be etched
  - Thick: more undercutting during BT (relatively isotropic), higher AR
- **Poly Block: 3:1 (Tradeoffs)**
  - Thick: Mechanical stability and AR
  - Thin: Rounding (dynamic mask profile), Selectivity to Si
- **Starting with Various Spacer thicknesses**
  - 30, 50, 100 and 200nm
  - For each had a 3:1 block
  - For 50nm (target) had two additional blocks: 6:1(300nm) and 12:1(600nm)

Poly-Si Etch-I: Lam 9400

Recipe	Break Through (BT)	Main Etch (ME)	Over Etch (OE) 20%
Etch time (sec)	10	End-Point	20
C2F6 (sccm)	100	0	0
HBr (sccm)	0	150	50
Cl2 (sccm)	0	0	0
O2 (sccm)	0	5	5
RF Power (W)	250	250	250
Pressure (mT)	13	10	15
M-Field (G)	0	0	0



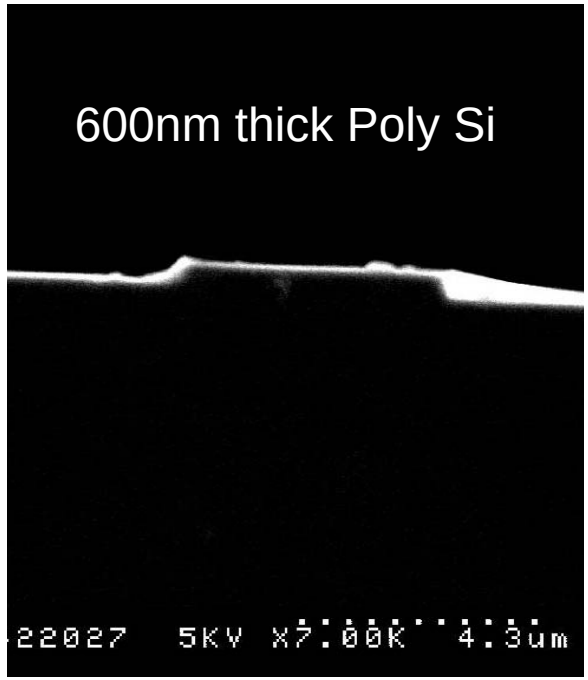
Etch Rate	ME	OE
Poly Etch Rate (A/min)	1610	3530
Oxide Etch Rate (A/min)	130	35
Selectivity (Poly : Oxide)	~12 : 1	100 : 1

Problems: Reentrant

Sources of problems: Less deposition and/or charging

Poly-Si Etch-III: AMAT P5000

Recipe	BT	ME	OE
Etch time (sec)	10	EndPoint	
CF4 (sccm)	35	0	0
HBr (sccm)	0	**20**	30
Cl2 (sccm)	0	**20**	15
HE-O2 (sccm)	0	0	17
RF Power (W)	250	200	90
Pressure (mT)	100	100	100
M-Field (G)	0	40	50



Etch Rate	BT	ME	OE
Poly Etch Rate (A/min)	1300	2800	1400
Oxide Etch Rate (A/min)	1000	250	<10
Selectivity (Poly : Oxide)	1.3 : 1	11 : 1	140 : 1

➢ Problems

- tapering

-High HBR causes more angle

➢ Solutions

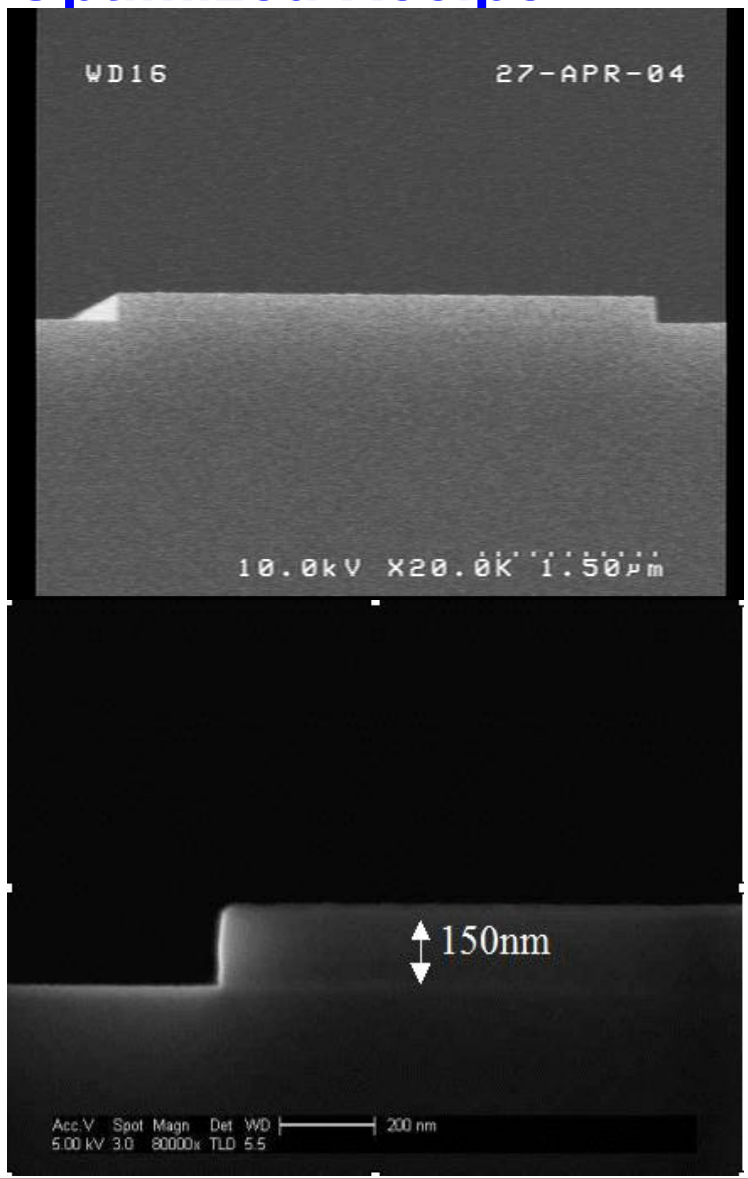
- Increase CL2 (22) & decrease HBR (18)
- Decreases deposition & reduces taper

Poly-Si Etch-IV: Increase Cl2 to HBr Ratio

Recipe	BT	ME	OE
Etch time (sec)	10	EndPoint	25-35
CF4 (sccm)	35	0	0
HBr (sccm)	0	**18**	30
Cl2 (sccm)	0	**22**	15
HE-O2 (sccm)	0	0	17
RF Power (W)	250	200	90
Pressure (mT)	100	100	100
M-Field (G)	0	40	50

Etch Rate	BT	ME	OE
Poly Etch Rate (A/min)	1300	2900	1400
Oxide Etch Rate (A/min)	1000	240	<10
Selectivity (Poly : Oxide)	1.3 : 1	12 : 1	140 : 1

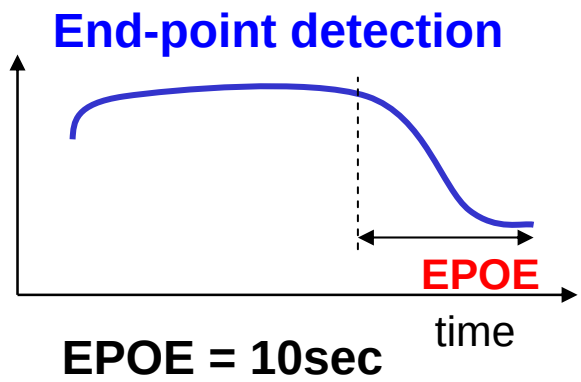
Optimized Recipe



Nitride Spacer Etch: AMAT P5000

Recipe	ME
Etch time (sec)	Manually stop by EndPoint
CF4 (sccm)	10
CHF3 (sccm)	15
Ar (sccm)	60
O2 (sccm)	8
RF Power (W)	50
Pressure (mT)	30
M-Field (G)	0

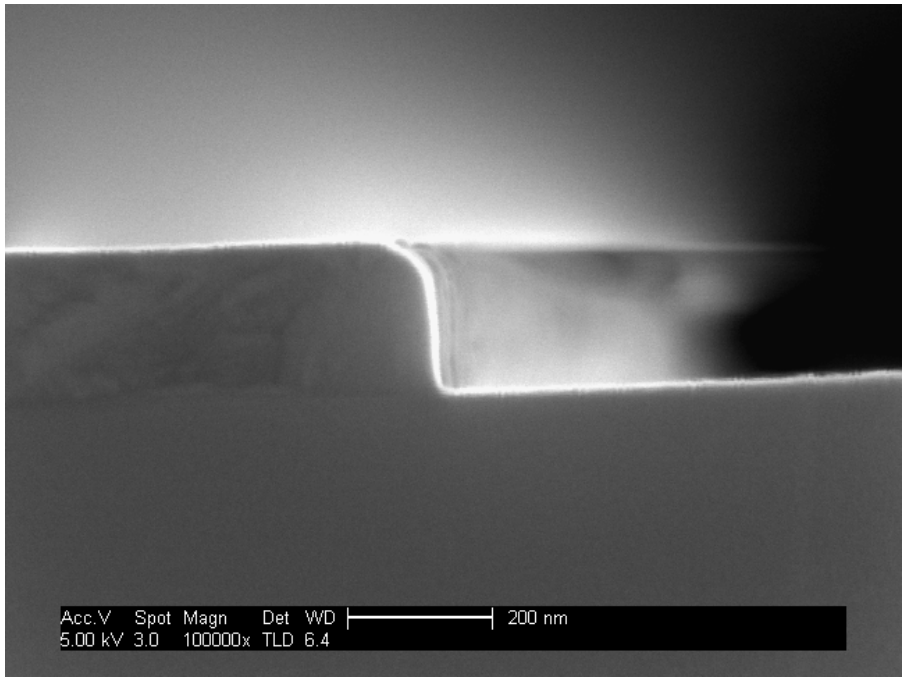
Etch Rate	ME
Nitride Etch Rate (A/min)	300
Oxide Etch Rate (A/min)	130
Selectivity (Nitride : Oxide)	2.3 : 1



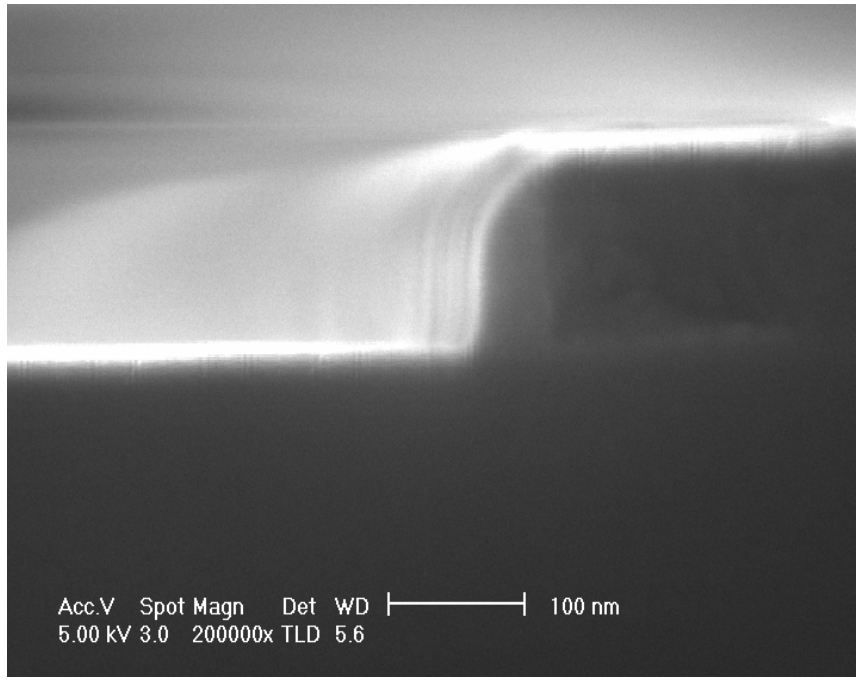
EPOE = 10sec

Only 10sec over etch(EPOE) to protect the oxide layer
- It was OK due to the very uniform nitride film

Nitride Spacer Etch

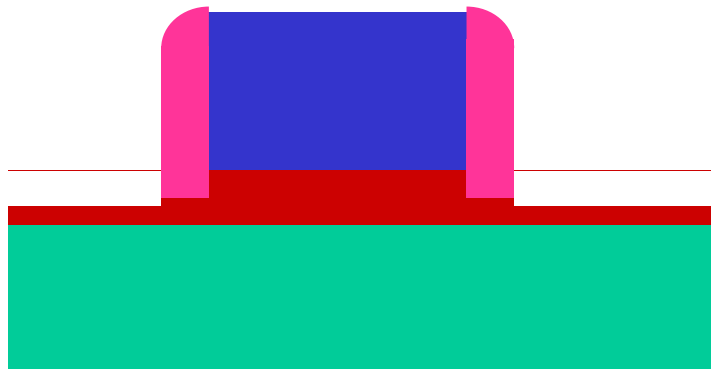


300nm Poly, 60nm Nitride: 6:1



150nm Poly, 60nm Nitride: 3:1

- ✓ Spacer Anisotropically etched
- ✓ Next step--- TMAH etch to remove poly-Si block



TMAH Etch-I

Characterized on Dummy and settled on the following conditions

- Temperature : 90 degree (Highly sensitive to temperature)
- Ratio with water : 25% TMAH

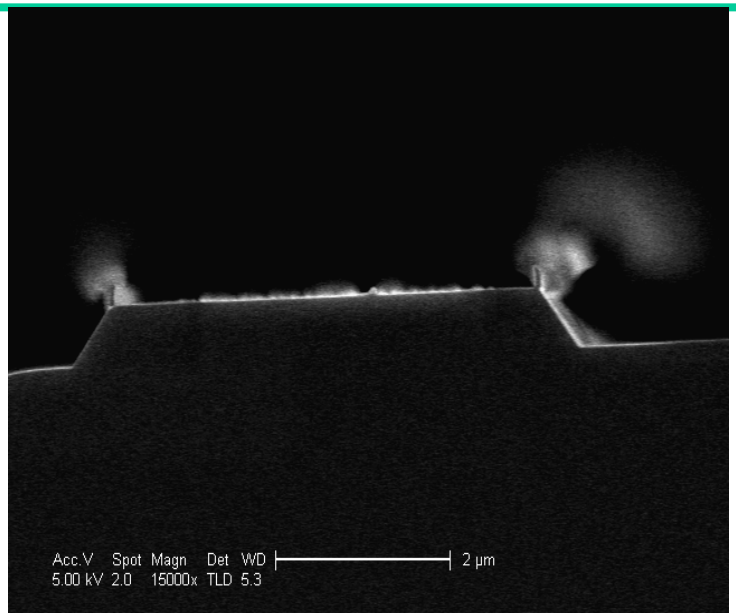
Etch Rate	ME
Poly Etch Rate (A/min)	~8000
Nitride Etch Rate (A/min)	<2
Oxide Etch Rate (A/min)	<2
Selectivity (Poly : Oxide or Nitride)	Almost infinity

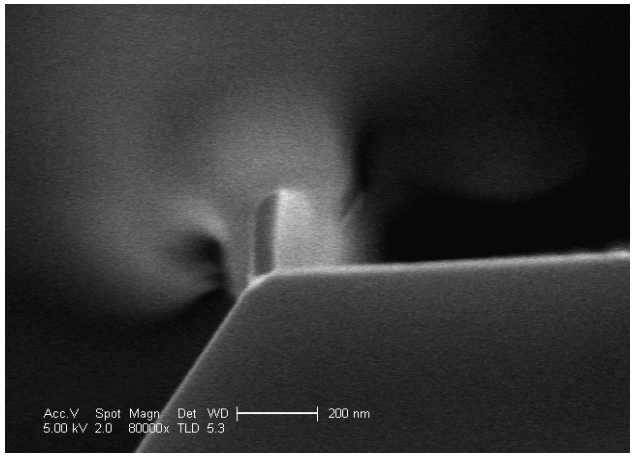
Question: Pre-TMAH HF dip and how long (Trade-off)?

- Need to remove native oxide
- Will take out already tenuous oxide film

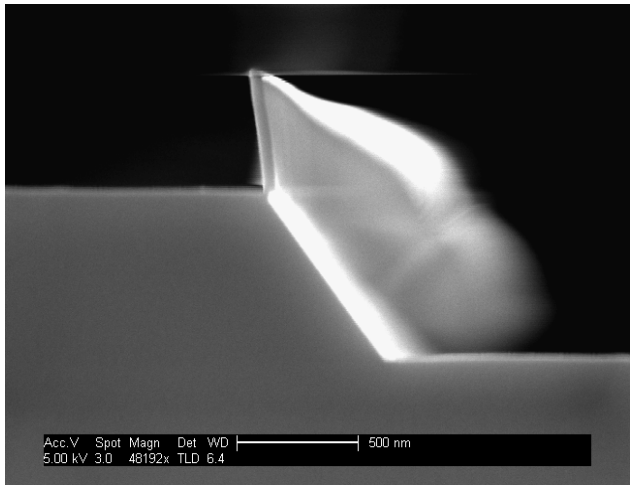
→7sec 50:1 HF dip

SEMs after TMAH Etch-II

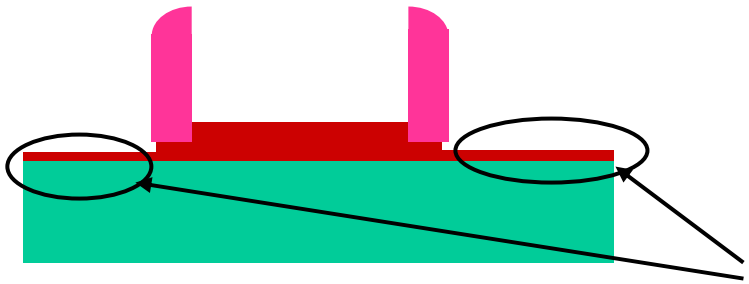




5:1 aspect ratio spacer
-Width: 52nm



10:1 aspect ratio spacer
-Width: 47nm



No oxide during TMAH etch

Problem

- There is **no oxide remaining**, hence etches single crystal Si at a facet
- Except for that good spacers

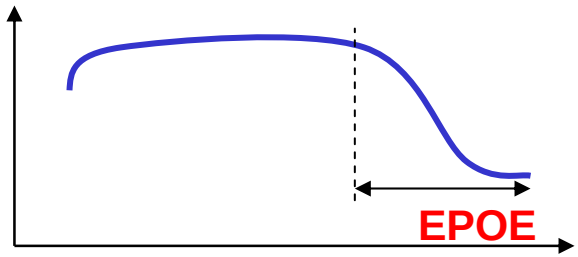
Resolve the No-Oxide Problem

➢Steps which remove oxide (initial 150A)

- Poly-Si overetch ->15s EPOE and ~30s OE → ~**70A**
- Post Poly-Si cleaning ->10s 50:1 HF→ **9A**
- Nitride overetch-> 15s EPOE→**32A**
- HF dip to remove native oxide before TMAH-7s 50:1→ **7A**

➢Poly-Si over-etch(EPOE) biggest culprit

End-point detection During Main Etch



EPOE = 15sec

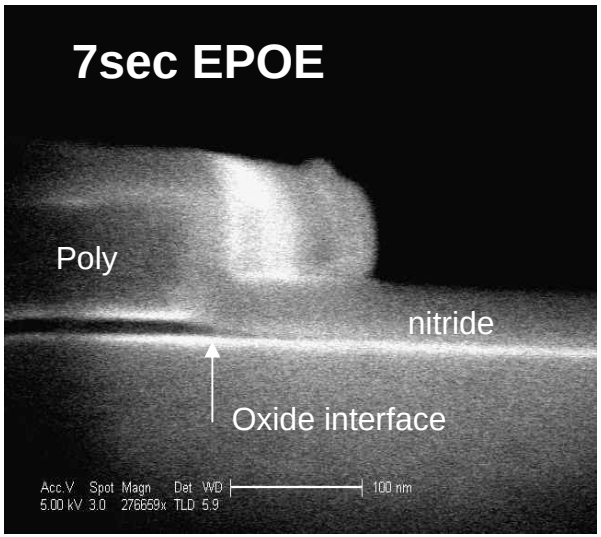
➢Solution

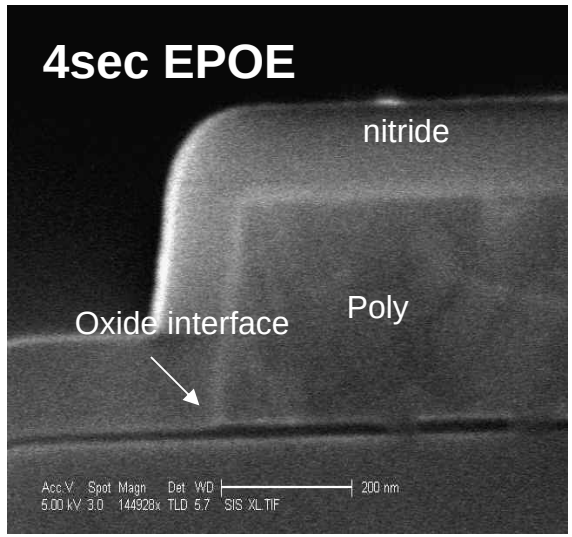
- Increase initial oxide thickness to 200A
- Reduce EPOE in poly-Si etch for since have an overetch step

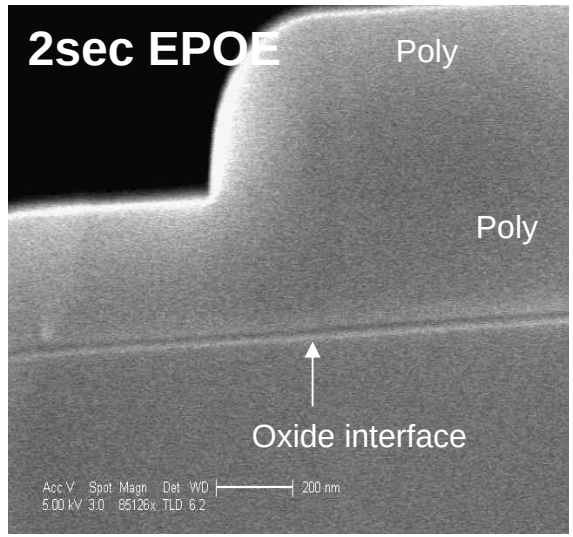
Inspection of the No-Oxide Problem

But Still had same problem: There is no oxide remaining

→Need to check oxide thickness by SEM
after the Poly-Si etch step







Most oxide was gone during the Poly-Si main etch, >7 times faster oxide etch!!

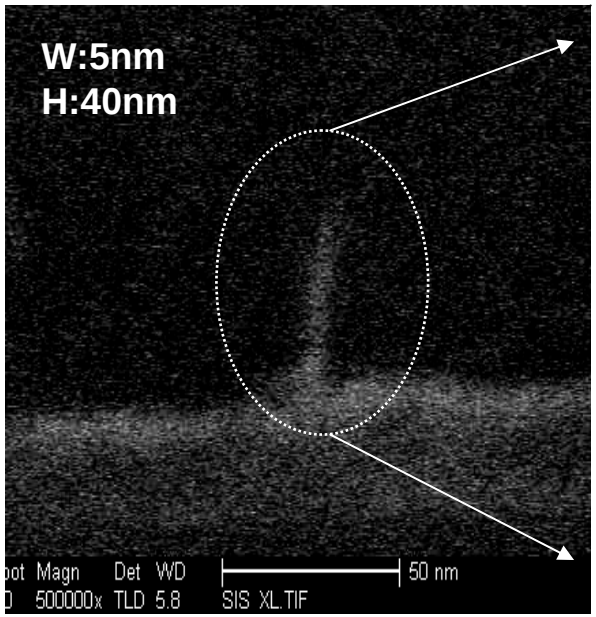
Possible reasons: Interface stress on oxide
→ weaker than thick oxide

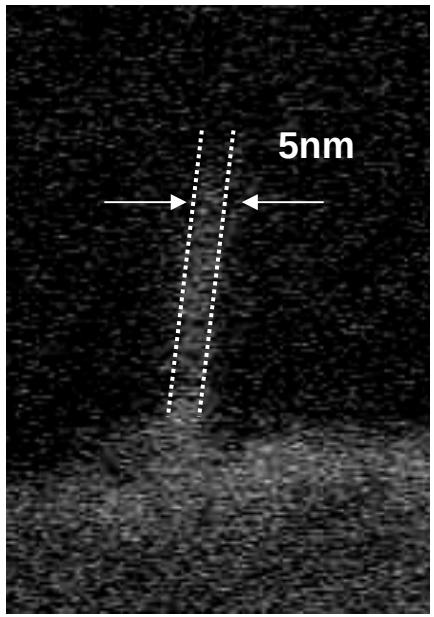
Solution : Reducing EPOE time below 2 sec !!

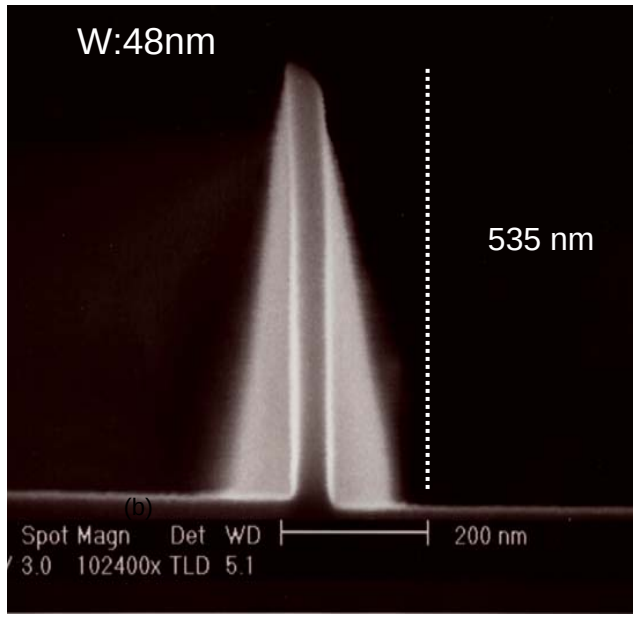
Run 3

- Poly etch by 2sec EPOE, 25sec OE
- TMAH with 200% OE (no HF-dip before TMAH)

Very uniform and robust spacers
→can make below 5nm width spacer with very high aspect ratio







Various Approaches For Si Fin Etch

- **Approach I: HBr/Cl2 with normal BT with CHF3**
- **Approach II: NF3 with normal BT with CHF3**
- **Approach III: Added O2 in the HBr/Cl2 approach**

  1)with normal BT with CHF3

  2)with new BT

*All Si Fin etches are done by AMAT P5000

Si Fin Etch – Ist Approach

- **Two types of wafers**
  - Calibration wafers : 2100A thick nitride hard mask and 200A thick oxide
  - Spacer mask wafers
- **Start with poly etch recipe and play with HBr, Cl2 and power**

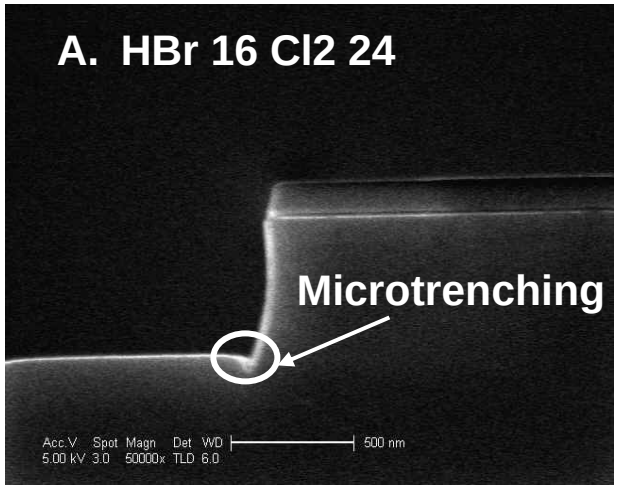
Recipe-1	BT	ME
Etch time (sec)	10	60
CF4 (sccm)	35	0
HBr (sccm)	0	**12 ~ 28**
Cl2 (sccm)	0	**28 ~12**
HE-O2 (sccm)	0	0
RF Power (W)	250	***170 ~ 225**
Pressure (mT)	100	100
M-Field (G)	0	40

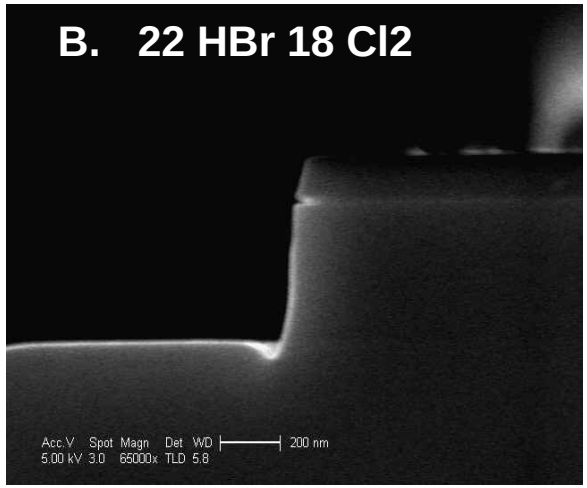
Etch Rate	BT	ME
SI Etch Rate (A/min)	1300	3000 ~ 5000**
Nitride Etch Rate (A/Min)	1500	800 ~ 1000
Oxide Etch Rate (A/min)	1000	240

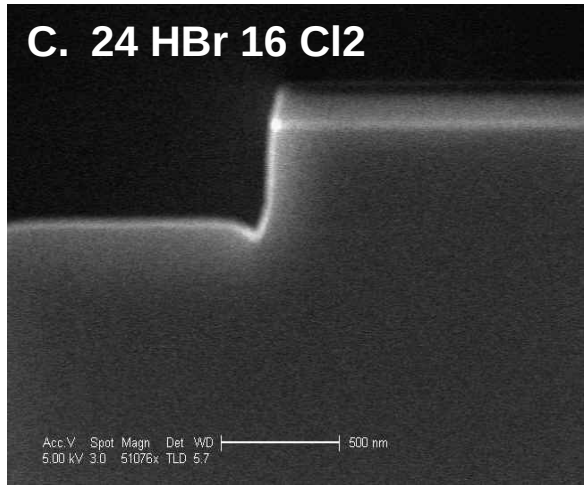
**** Higher Cl2 made higher etch rate**

*** Changing power didn't make a big difference**

Si Fin Etch – with Calibration wafers







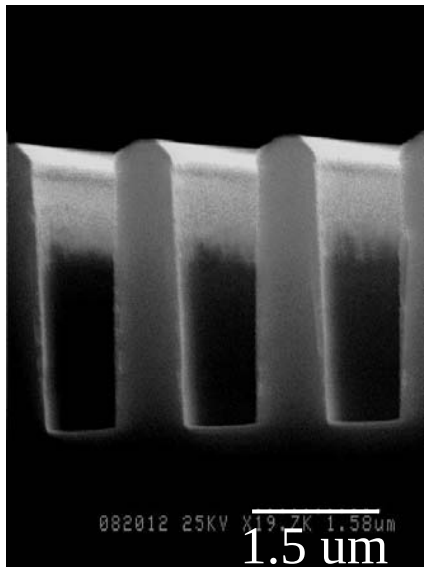
- **Started with similar recepie as poly-Si etch**
- **Observed Microtrenching**
  - Ion Reflection (Profile bowing)
  - Some ion reflection is desirable: gives square corners

- **Solution**
  - Higher HBr to Cl2 (Bromine ions broader angular distr. than Cl2 ions)
  - Optimize with power: to change angular distr.
  - Mask profile

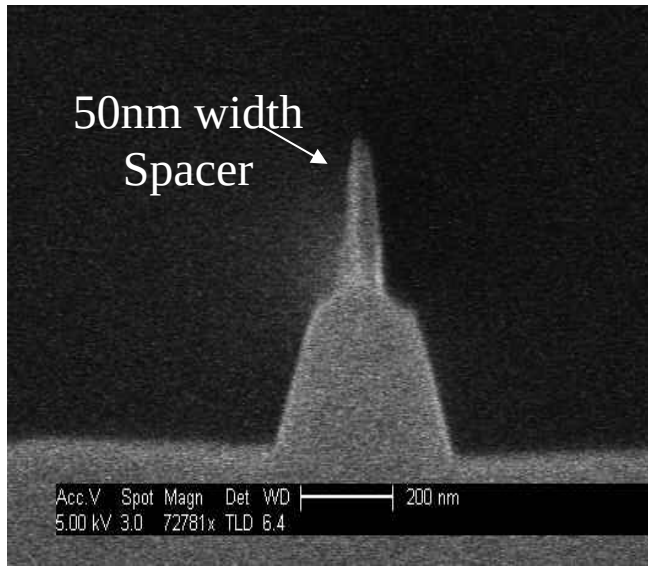
Si Etch – NF3 (2nd Approach)

- NF3 for ME for better Si etch profile
- Rationale: very good in the past

Recipe	ME
Etch time (sec)	30
CHF3 (sccm)	0
CF4 (sccm)	0
HBr (sccm)	45
NF3 (sccm)	13
Ar (sccm)	0
HE-O2 (sccm)	11
RF Power (W)	300
Pressure (mT)	100
M-Field (G)	65



Previous Work

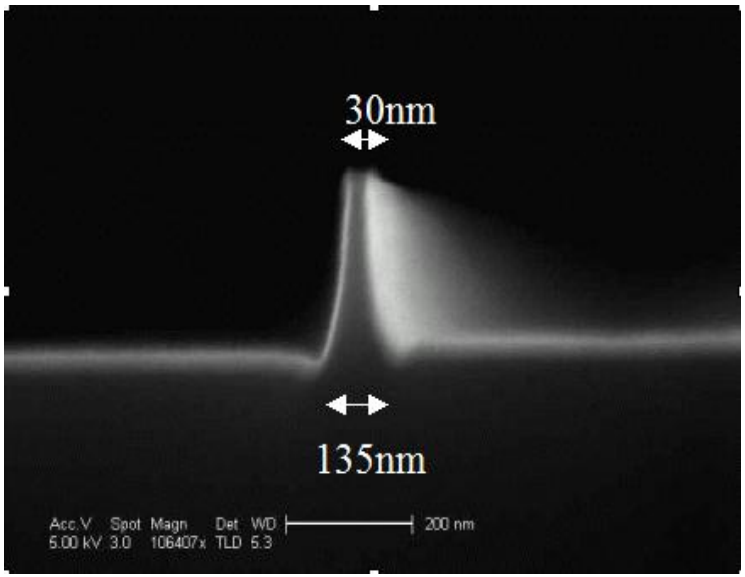


Etch with the spacer mask for 30sec ME

Using NF3 is not good for nano-scale
Discarded!!

Vertical Structure: Si Fin-Etch

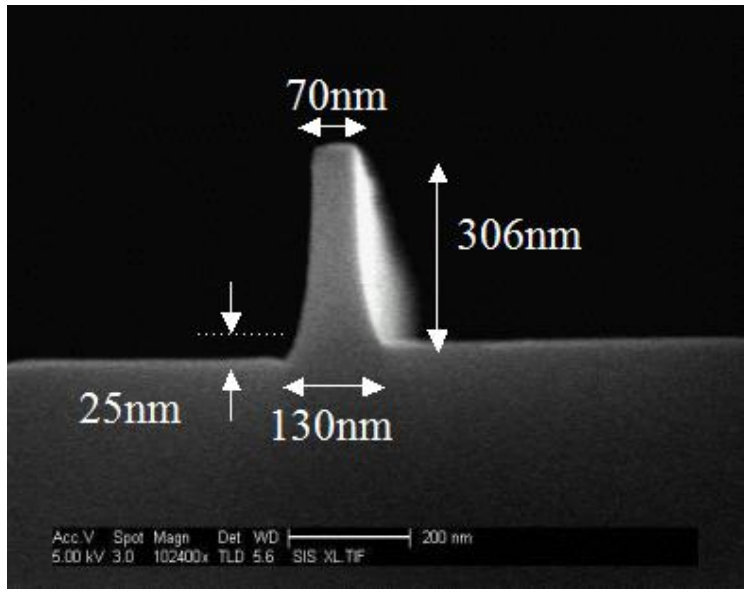
- HBr 24sccm, Cl2 16sccm



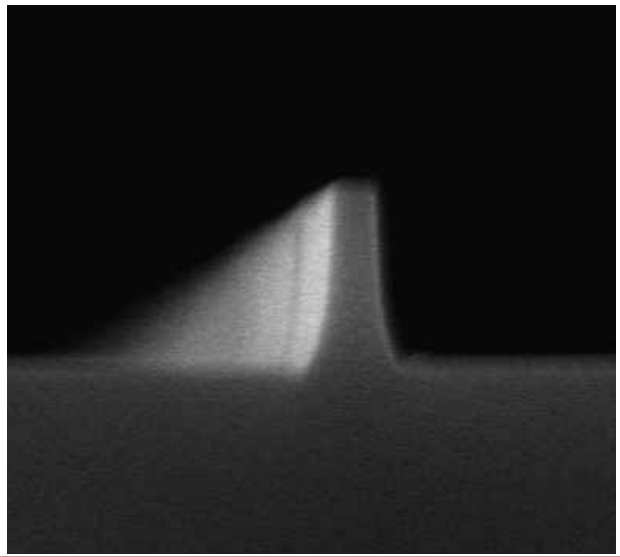
Reduce the micro trench with adding O2

More deposition during the etch

- HBr 24, Cl2 16, O2 8sccm



A new breakthrough Step (high selective oxide etch) before Si etch

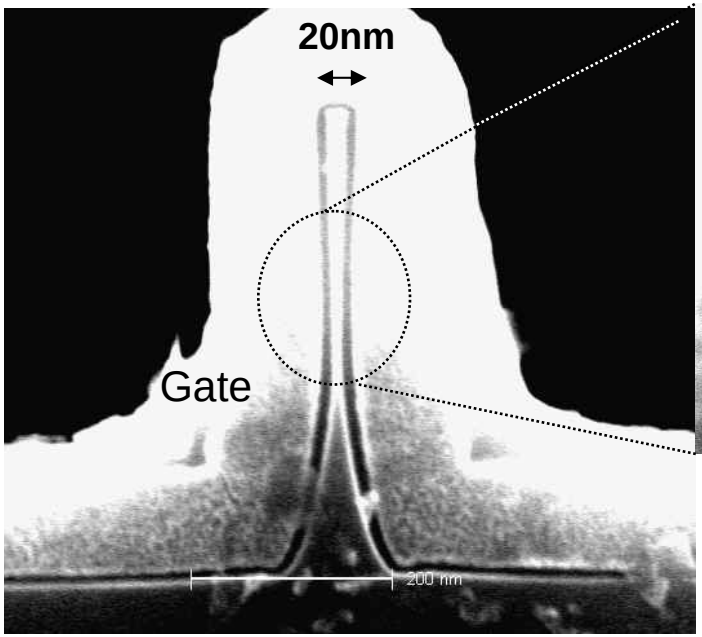


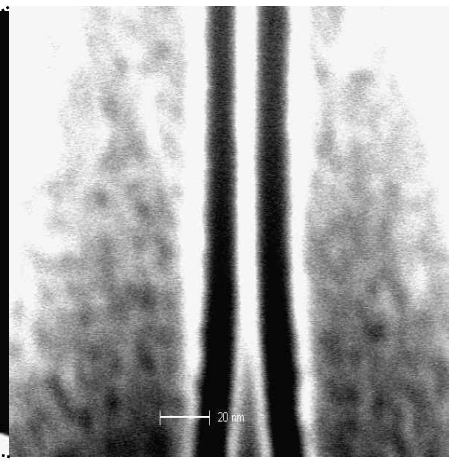
New BT reduces the difference in fin height

Conclusion & Acknowledgement

Vertical MOS Device done with thinner spacer mask(~25nm)

- Side oxide thickness=10nm
- Bottom corner oxide thickness=8nm
- Transistor suitability(Source region_bottom)





~7nm width Si body

Acknowledgement

Jim McVittie, Cesar Baxter, Elmer Enriquez and other SNF staffs