Dual Frequency Dry Etching for Advanced Memory Applications

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Abstract

Abstract – A wide variety of new materials have been, and continue to be investigated to enhance the performance of current IC device structures and to introduce new features. In advanced memory applications, for example, such as MRAM, FeRAM, PRAM, and RRAM, numerous metal and dielectric layers are under investigation that require advanced patterning techniques to overcome the issue of reduced etch volatility in comparison to more conventional materials. In this presentation, dry etching results that have been obtained from a number of dual frequency reactor configurations for a variety of films used in advanced memory structures are presented. In these dual frequency reactors, plasma generation is accomplished using 13.56MHz and wafer bias is accomplished with 450kHz. The benefits of the use of the high 13.56MHz frequencies for efficient plasma generation and the use of low 450kHz bias frequency at the extreme ranges of producing high bias voltages for efficient removal of low volatility etch byproducts and low bias voltages for producing high selectivity to underlying layers are also discussed.

Outline

- Motivation
- Dual Frequency configurations using 13.56MHz/450kHz
- Frequency effects
- MRAM top electrode/stop-on-alumina process results (low bias regime)
- FeRAM stack etch process results (high bias regime)
- Conclusions

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Motivation

- Advanced Non-volatile Memory applications, Integrated Passive Devices, Compound Semiconductor Devices, and many MEMs devices use materials that are difficult to etch relative to conventional Si IC based films
- Etch tool requirements for these new materials can vary across a wide spectrum of bias power and process temperature
- Dual frequency plasma sources using high (13.56MHz) and low (450kHz) frequencies are suited to the requirements for advanced materials over a wide range of process requirements

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Some "New" Materials used in Advanced Memory Devices

MRAM

Metals – NiFe, CoFe, CoFeB, PtMn, IrMn, Ru
dielectric materials -- AlOx, MgO

FeRAM

Metals -- Pt, Ir, IrOx, Ru
Ferroelectrics -- PZT, BST, SBT

RRAM/ReRAM/CBRAM/PRAM

Metals -- Au, Ag, Cu, Se, Pt, Ir, IrOx, Ru, Ni
Dielectric materials -- manganites, …, NiO

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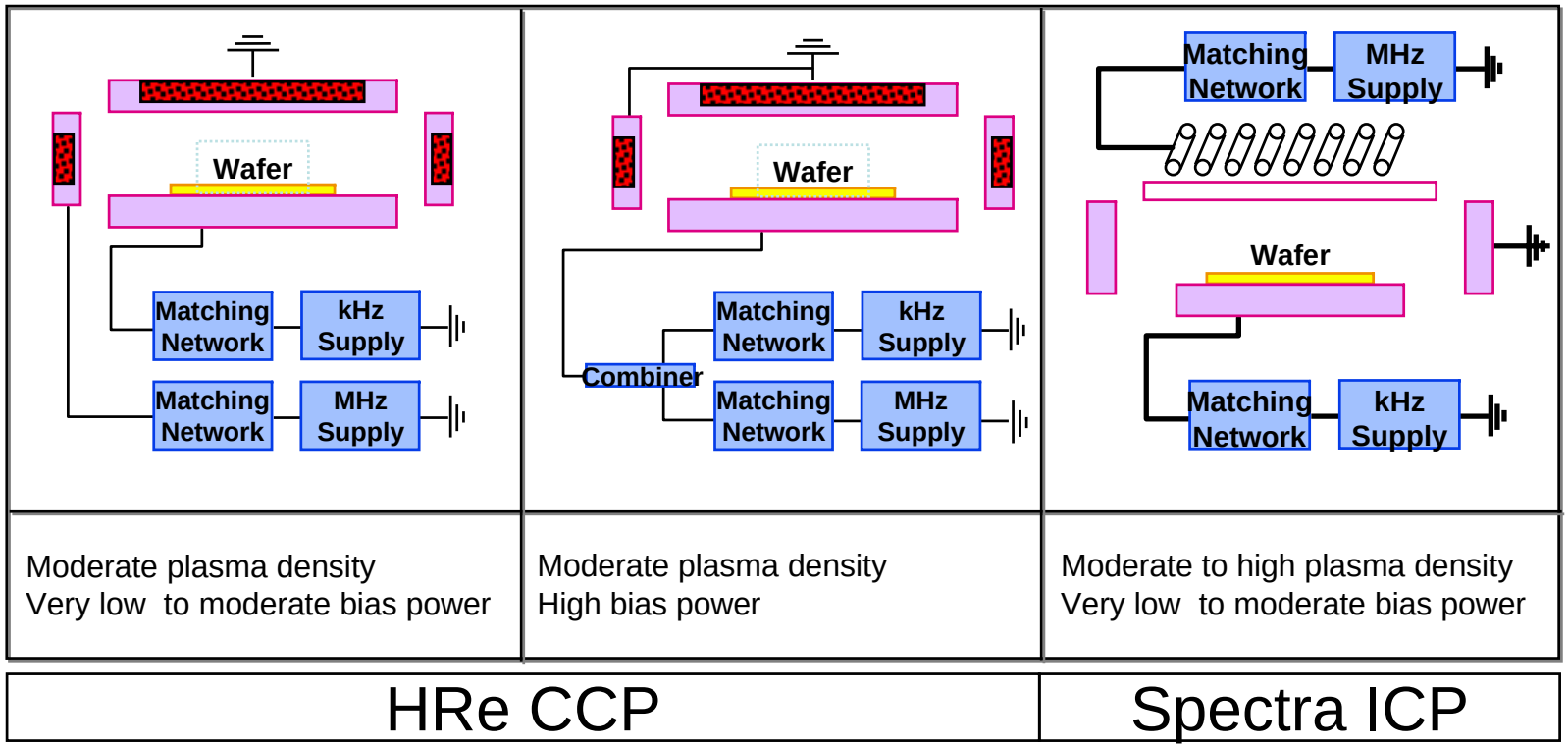
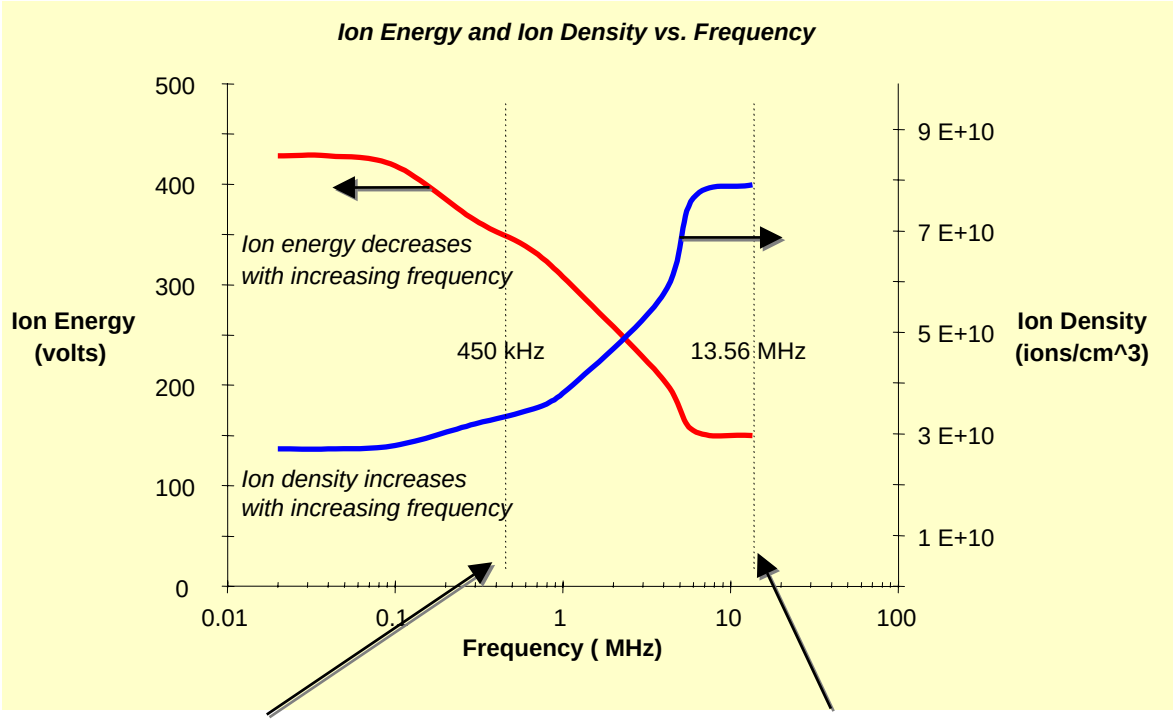
Tegal Dual Frequency Plasma Technology



Moderate plasma density Very low to moderate bias power	Moderate plasma density High bias power	Moderate to high plasma density Very low to moderate bias power
HRe CCP		Spectra ICP

Frequency effects
parallel plate reactor

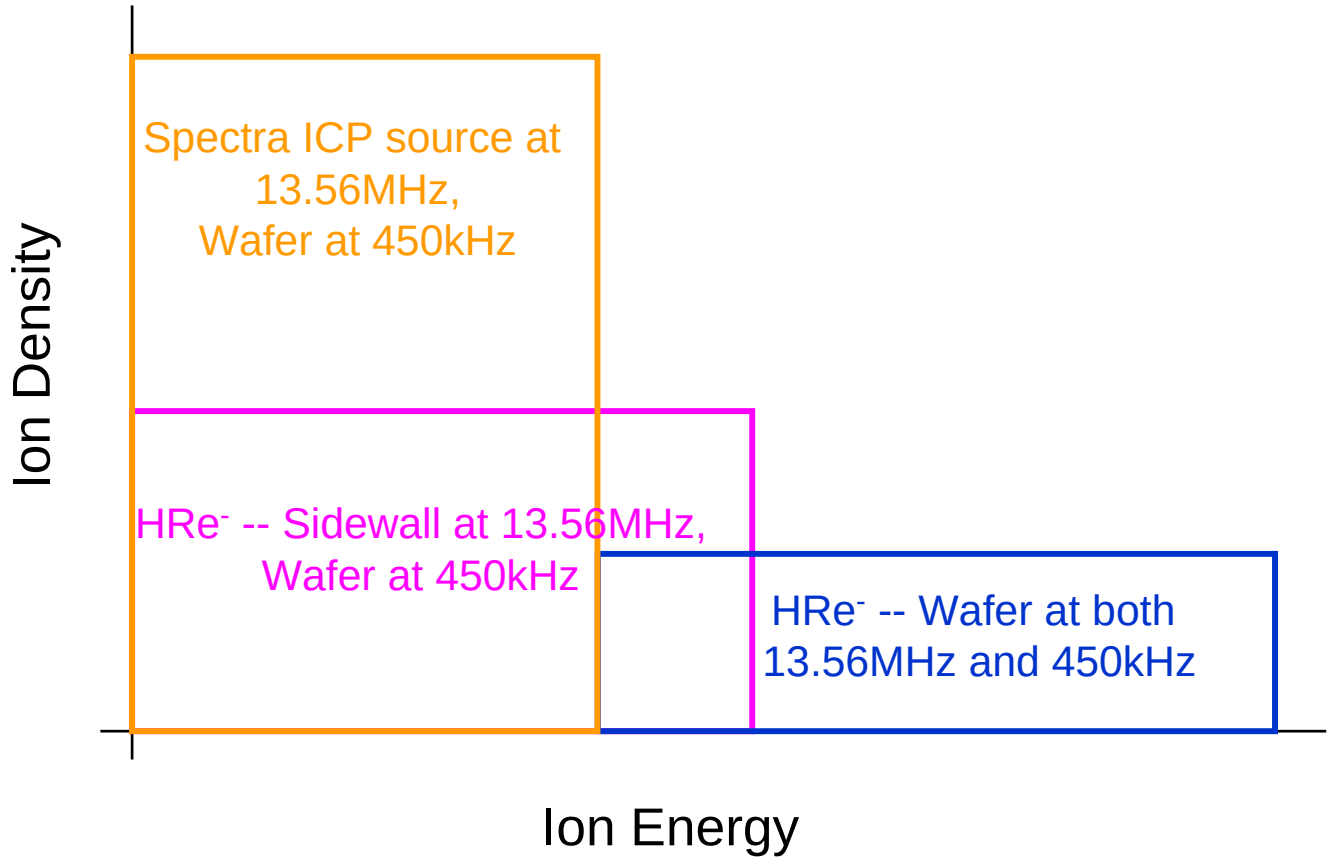


450kHz -- Efficient ion bombardment frequency without secondary ion generation

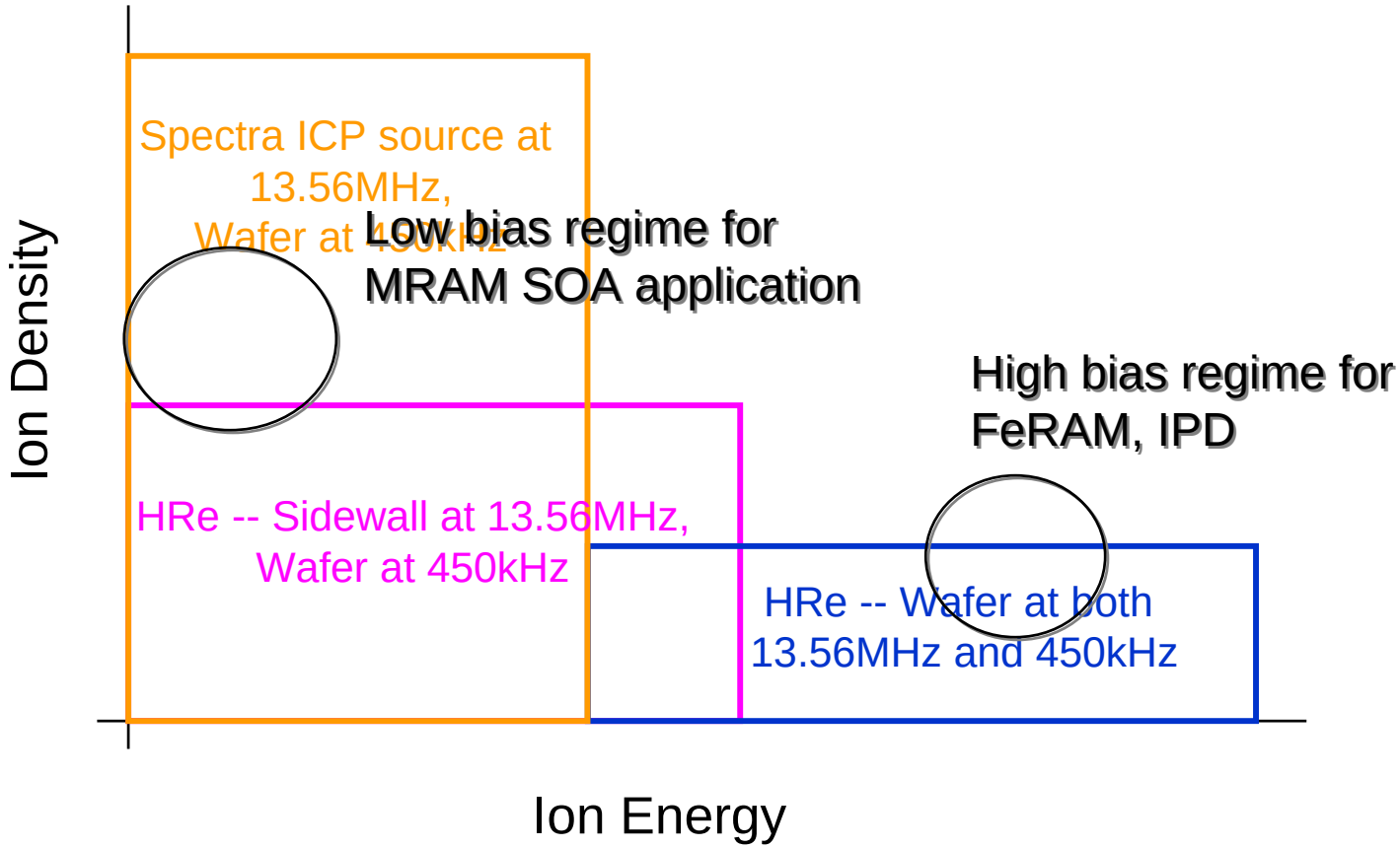
13.56MHz -- Efficient plasma generation frequency

Flamm et.al.

Relative Ion density/Ion Energy Levels for Various Dual Frequency Configurations



Relative Ion density/Ion Energy Levels for Various Dual Frequency Configurations



MRAM

Top Electrode/Stop-on-Alumina Process

Low Bias Spectra™ ICP processing regime utilizing dual frequencies – 13.56MHz/450kHz

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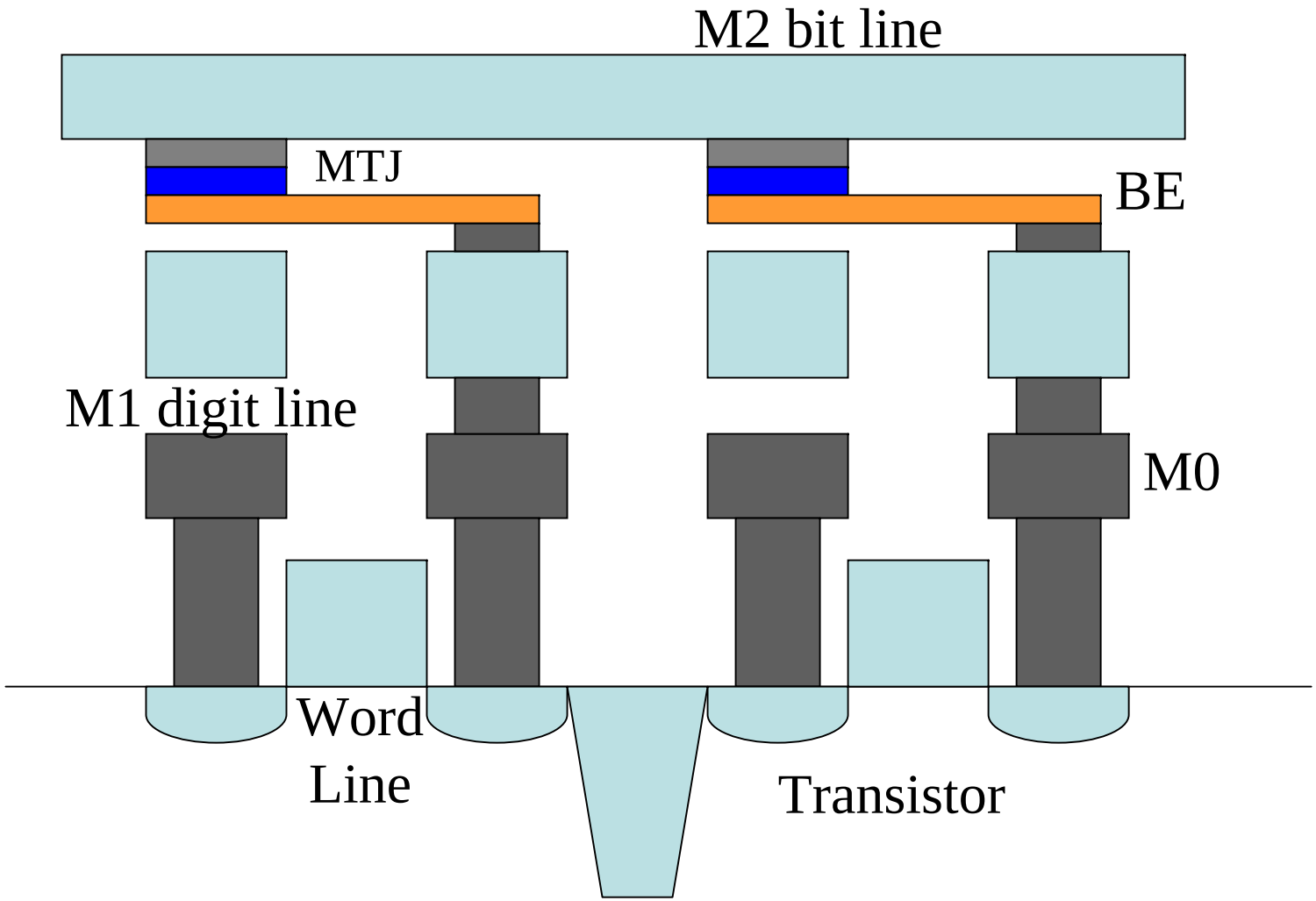
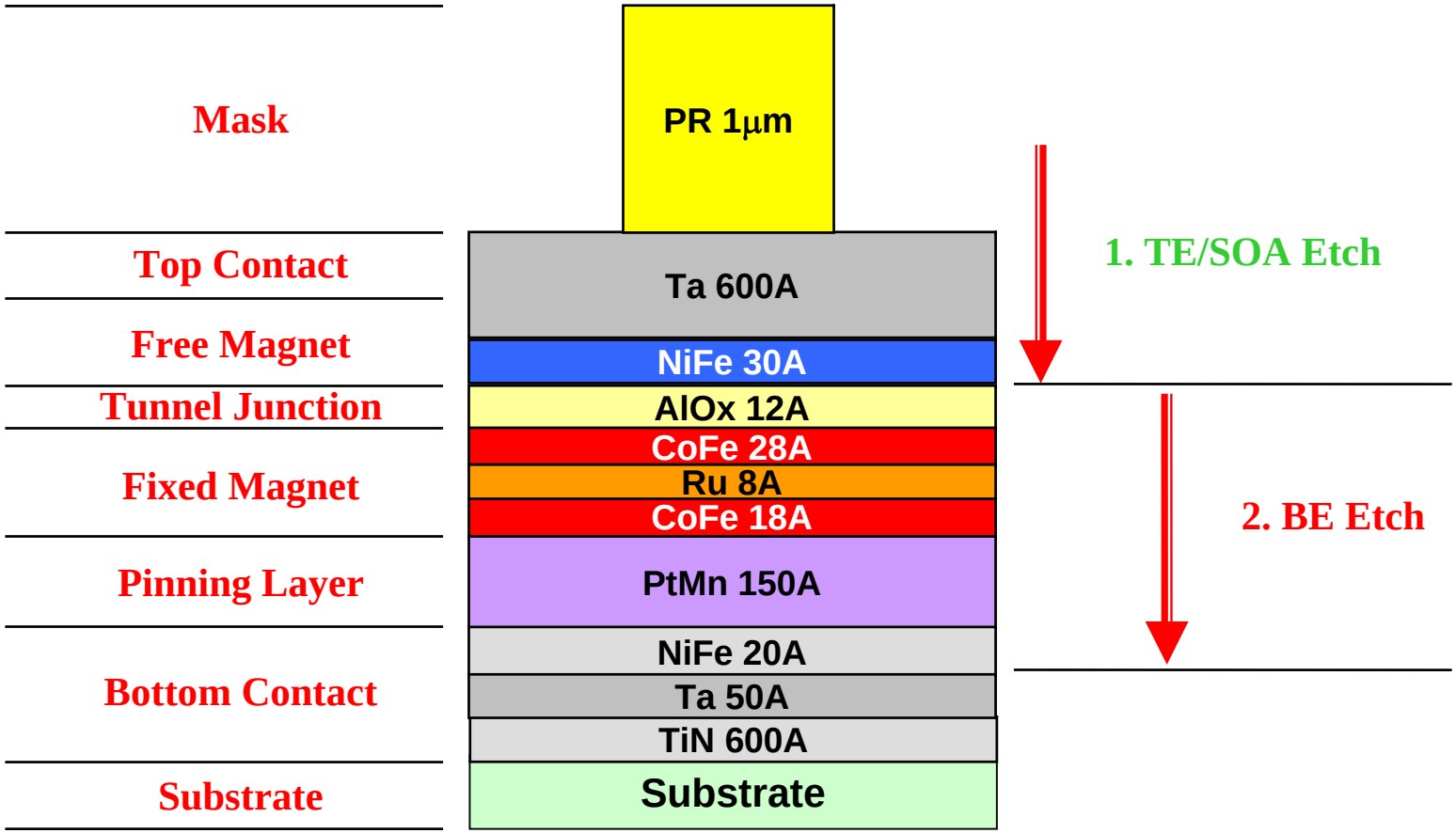
Off-Axis MRAM Cell Architecture

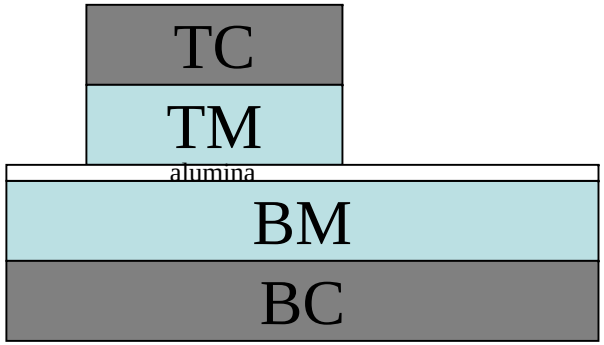


Typical MRAM Stack Structure

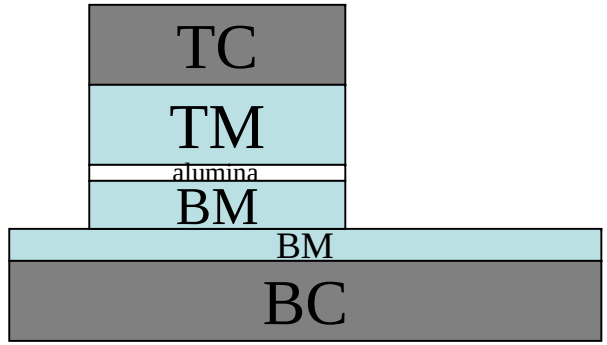


Two Step Process

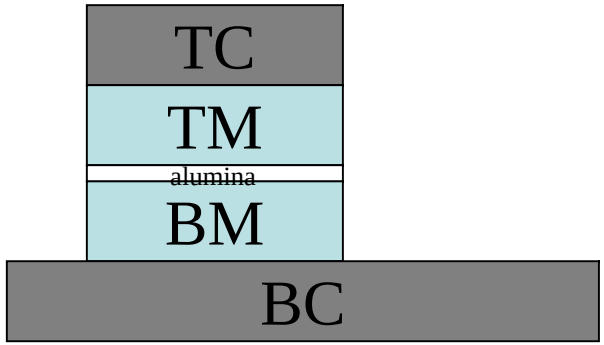
Two-mask Etch Schemes for Patterning MRAM stacks



Stop on Alumina

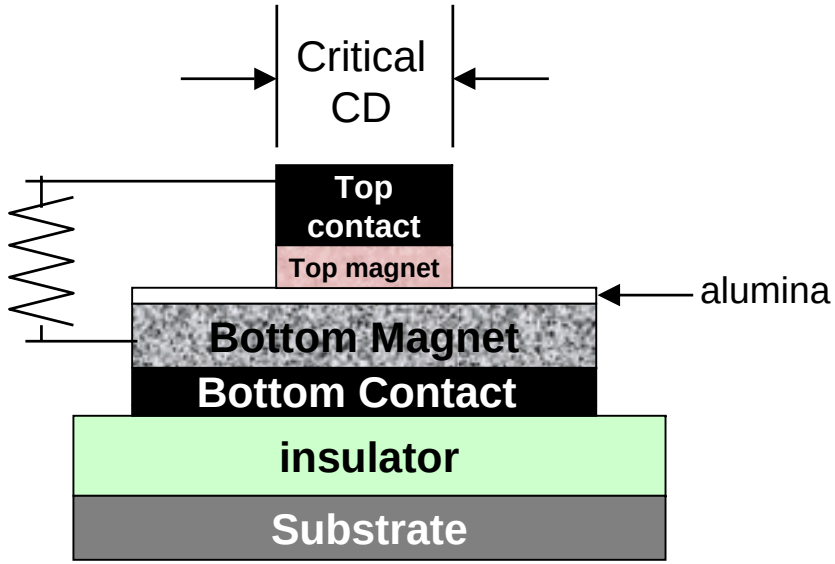


Stop within BM



Stop on BC

Benefits of SOA approach



- **Isolation between TM and BM**
- **CD Control dictated by patterning of TC/TM etch rather than full stack etch**

Top Electrode/Stop-on-Alumina Etch Requirements

- **Control of Ion energy at low levels (ER<50A/min)**
- **Uniform Etch Capability**
- **Temperature <300ºC during processing**
- **Good endpoint sensitivity and accuracy**
  - **to identify etch-stop layers**
- **No corrosion or residues**
- **Magnetic bit performance**
- **Throughput, MWBC (high)**

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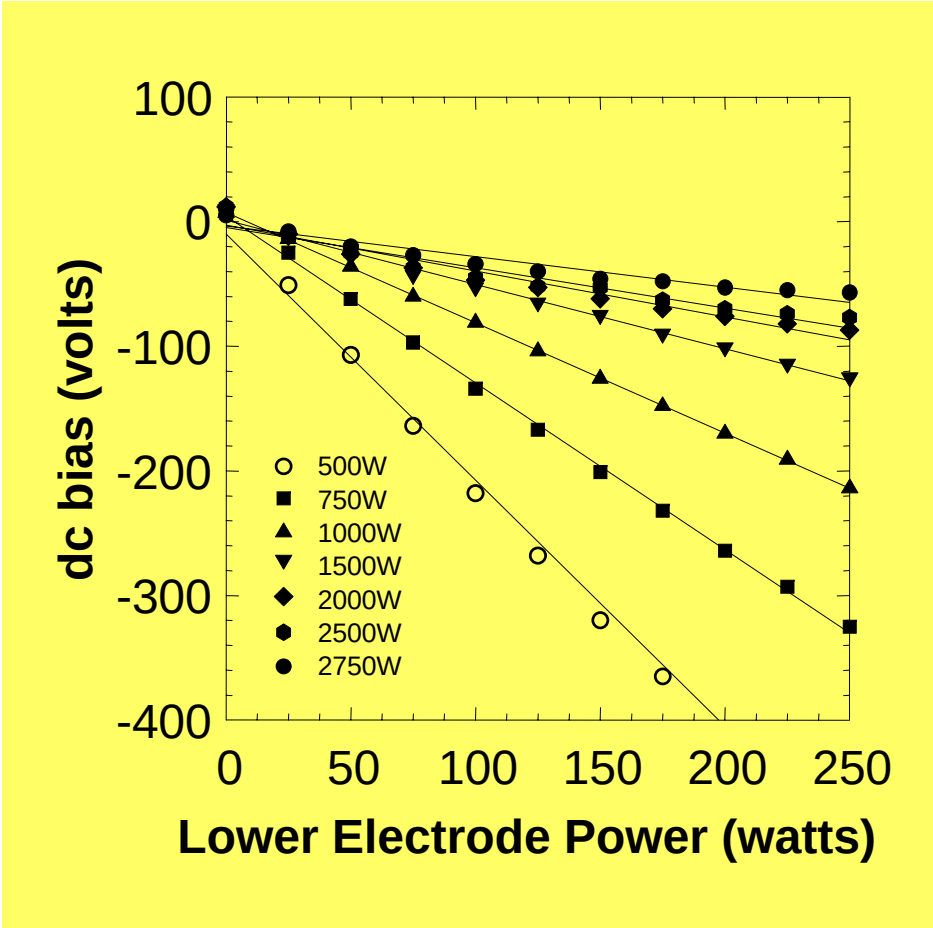
Control of ion energy

Spectra Process Module

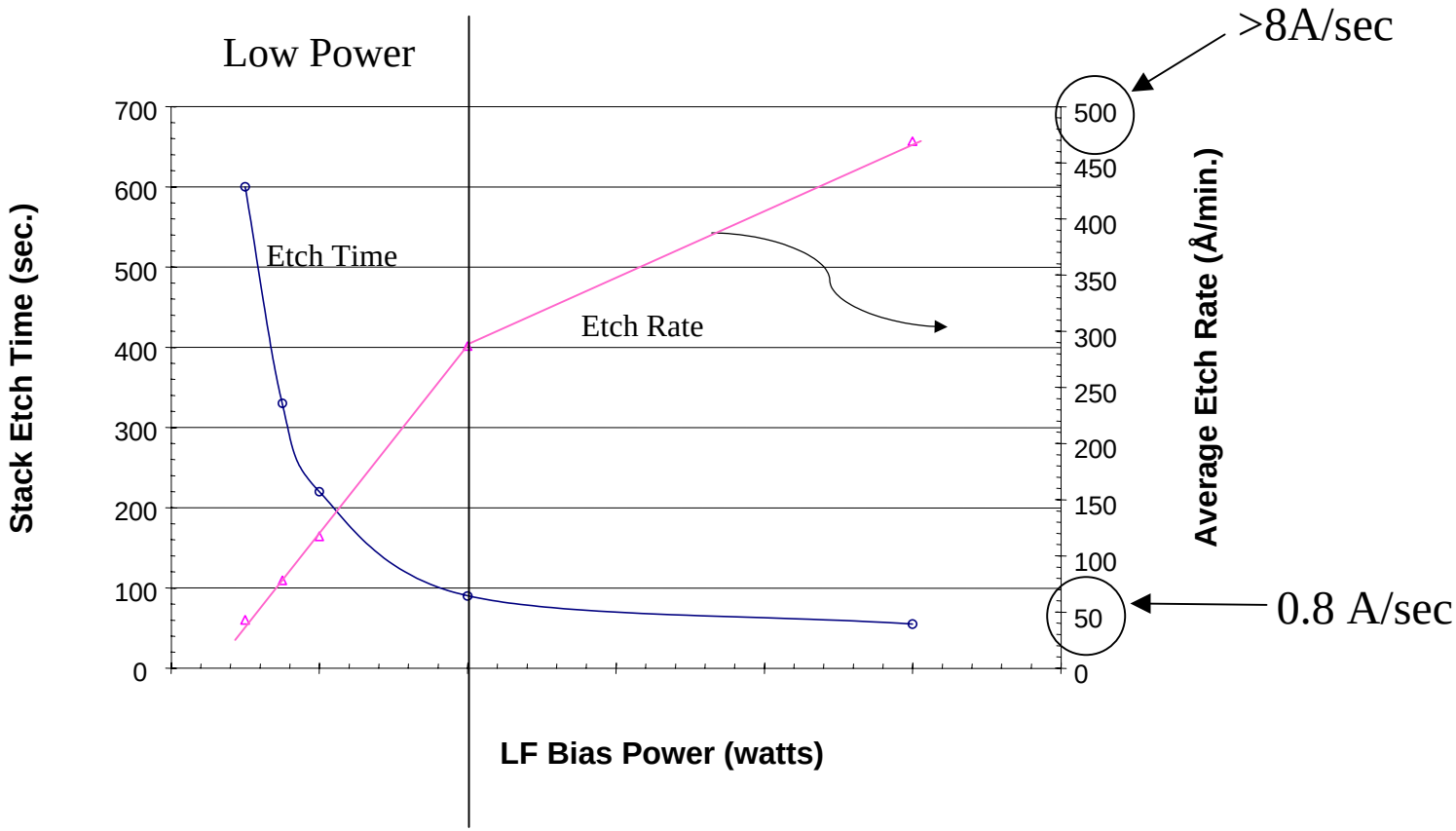
Linear DC Bias Dependence in Chlorine Plasma

Pressure = 2mTorr



Control of Ion Energy

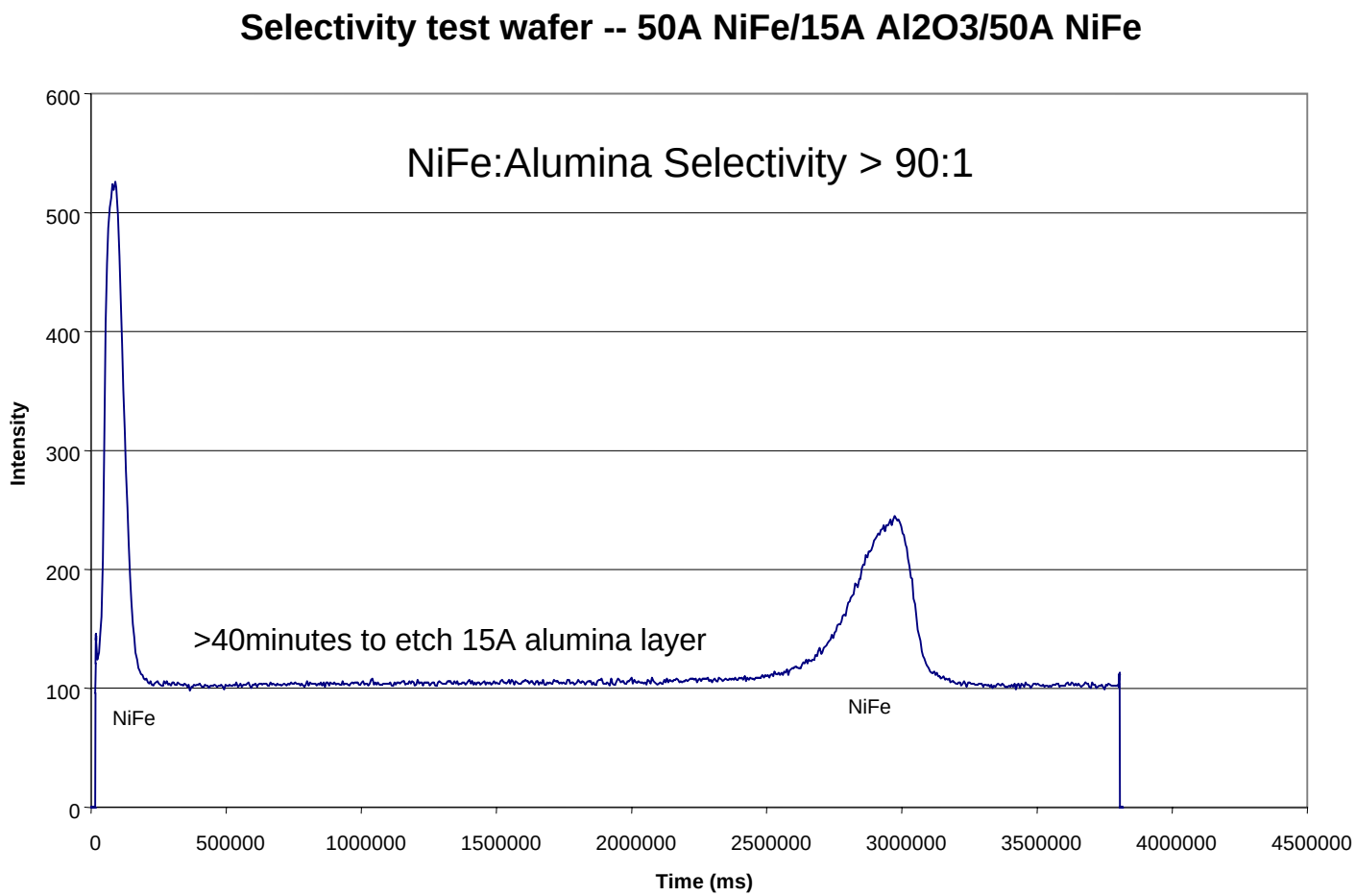
Magnetic Stack Etch Rate vs. Bias Power



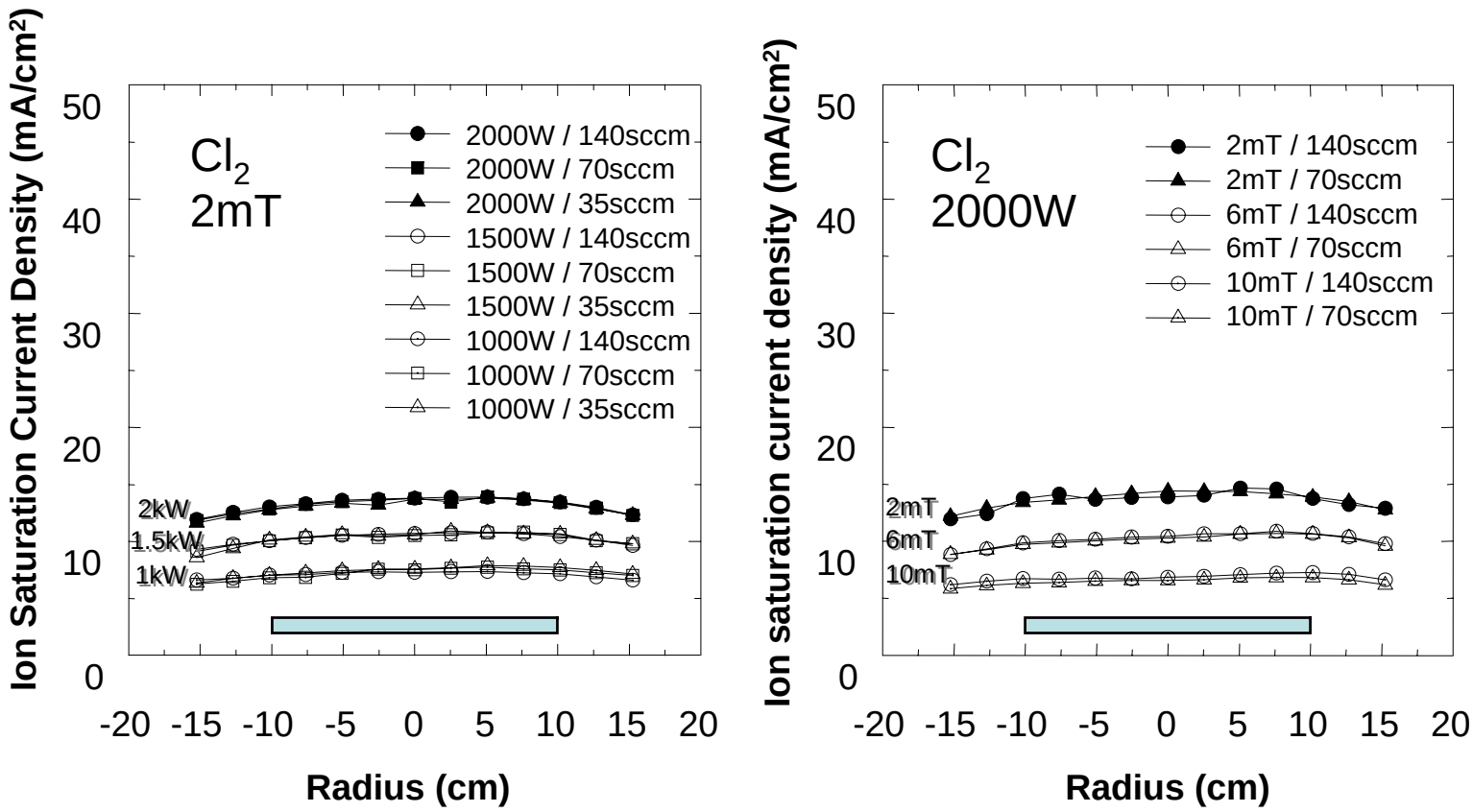
Switching magnet layer thickness is typically <50A thick

NiFe/Alumina Selectivity >90:1

proprietary etch chemistry



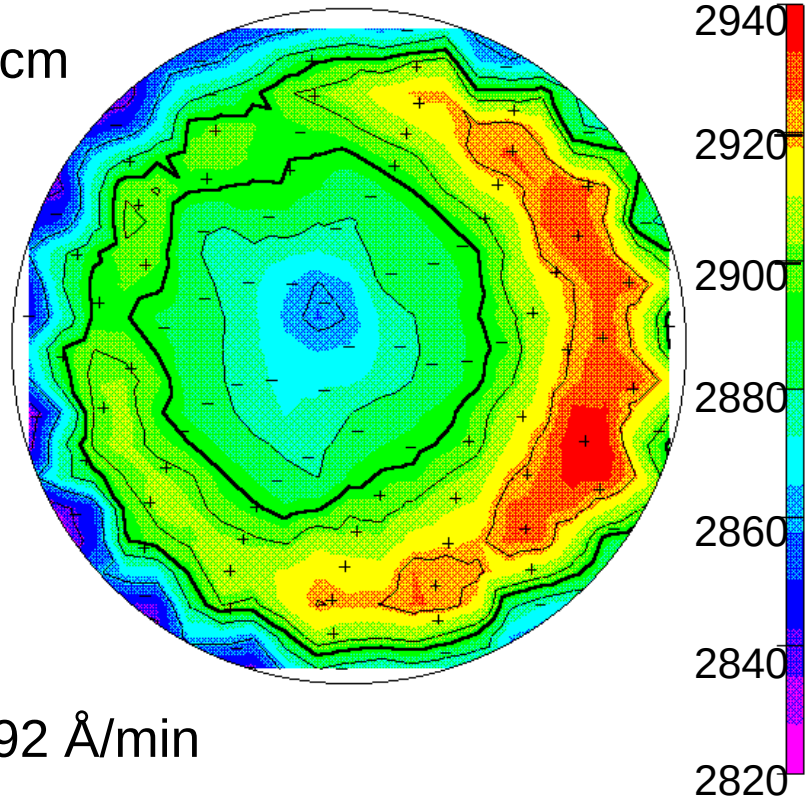
Control of Uniformity
(at the wafer)



Plasma Non-uniformity of ~5% max-min across 8" wafer diameter

200mm Polysilicon Wafer Etch Map

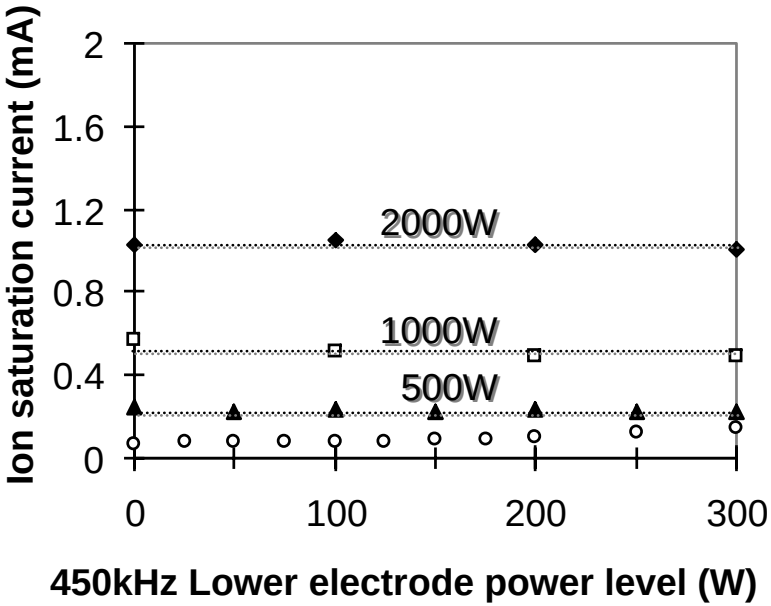
Cl_2 140sccm
2mtorr

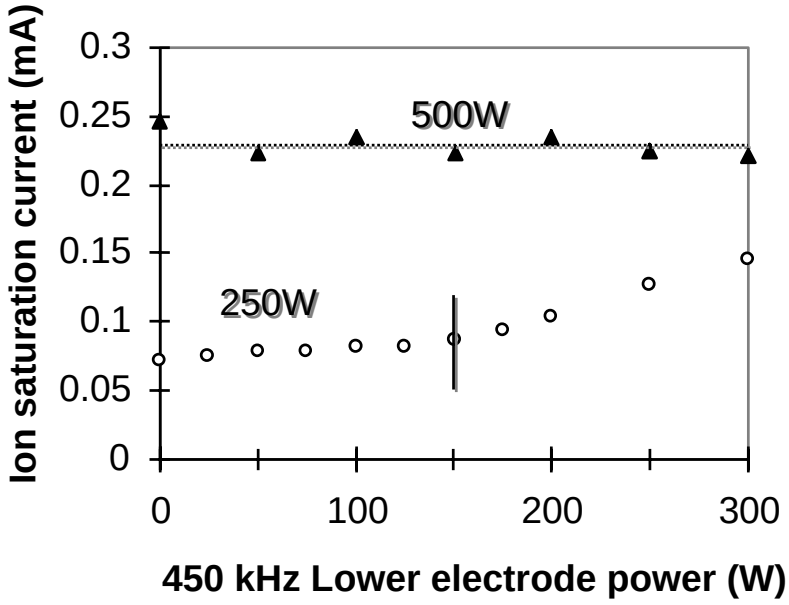


1s = 1%
ER = 2892 Å/min

Control of Uniformity

Contribution of 450kHz bias power to plasma density





Selection of frequencies can minimize contribution of lower electrode power on plasma density to provide independent control of ion density and ion energy

Summary of benefits of dual frequency configuration

- High frequency (13.56MHz) efficient for plasma generation
- Low frequency (450kHz) efficient for biasing wafer – very low applied power levels for free magnet layer etch
- Dual frequency (13.56MHz + 450kHz) allows for independent control of ion density and ion energy -- low frequency of 450kHz on the wafer minimizes secondary plasma generation over the wafer
- Plasma uniformity is dictated by chamber design, not by secondary plasma generation over the wafer

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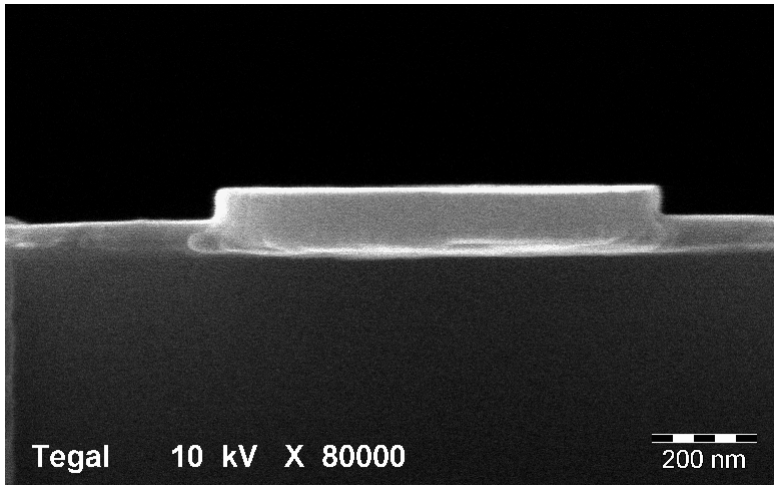
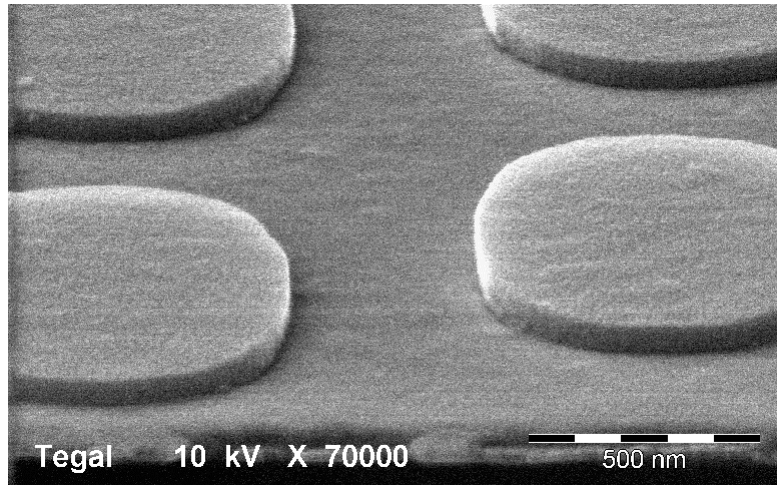
Typical SOA Etch Performance

Photoresist Mask TE process





750A Composite Top electrode thickness

Corrosion-free, residue-free surfaces
vertical profiles

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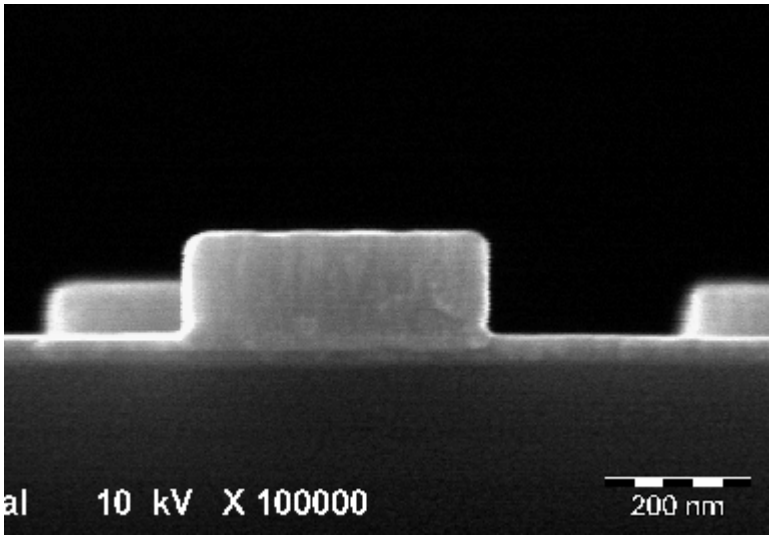
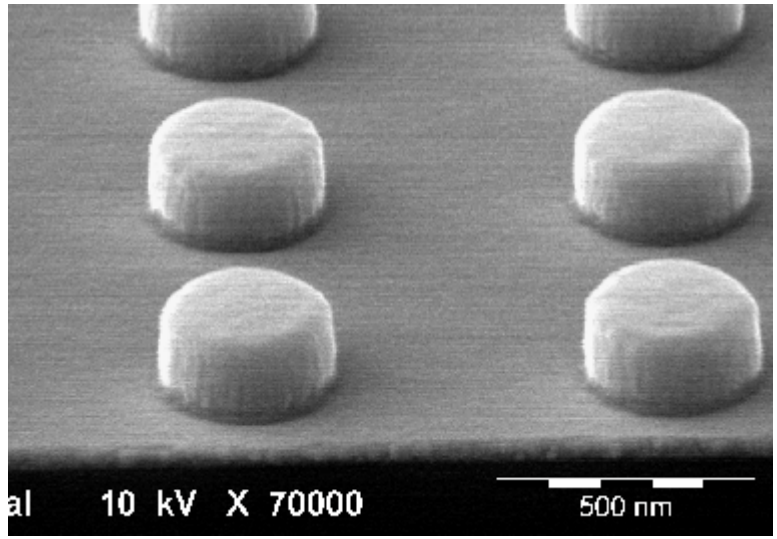
Typical SOA Etch Performance

Photoresist Mask TE process





1650A Composite Top electrode thickness

Corrosion-free, residue-free surfaces
vertical profiles

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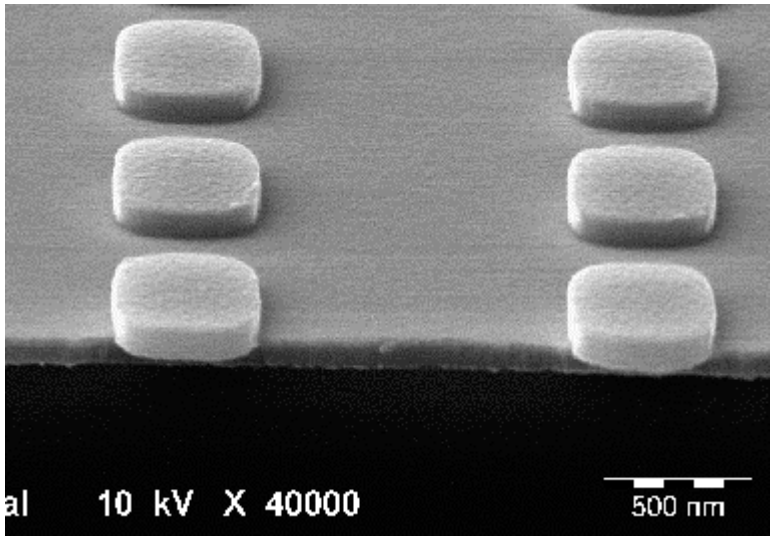
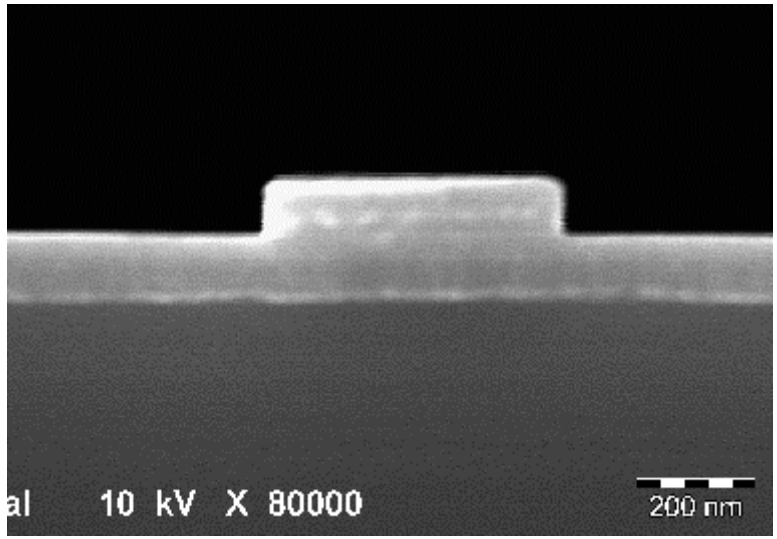
Typical SOA Etch Performance

Photoresist Mask TE process





1135Å Composite Top Electrode Stack Thickness of
0.5µm x 0.7µm

Corrosion-free, residue-free surfaces
vertical profiles

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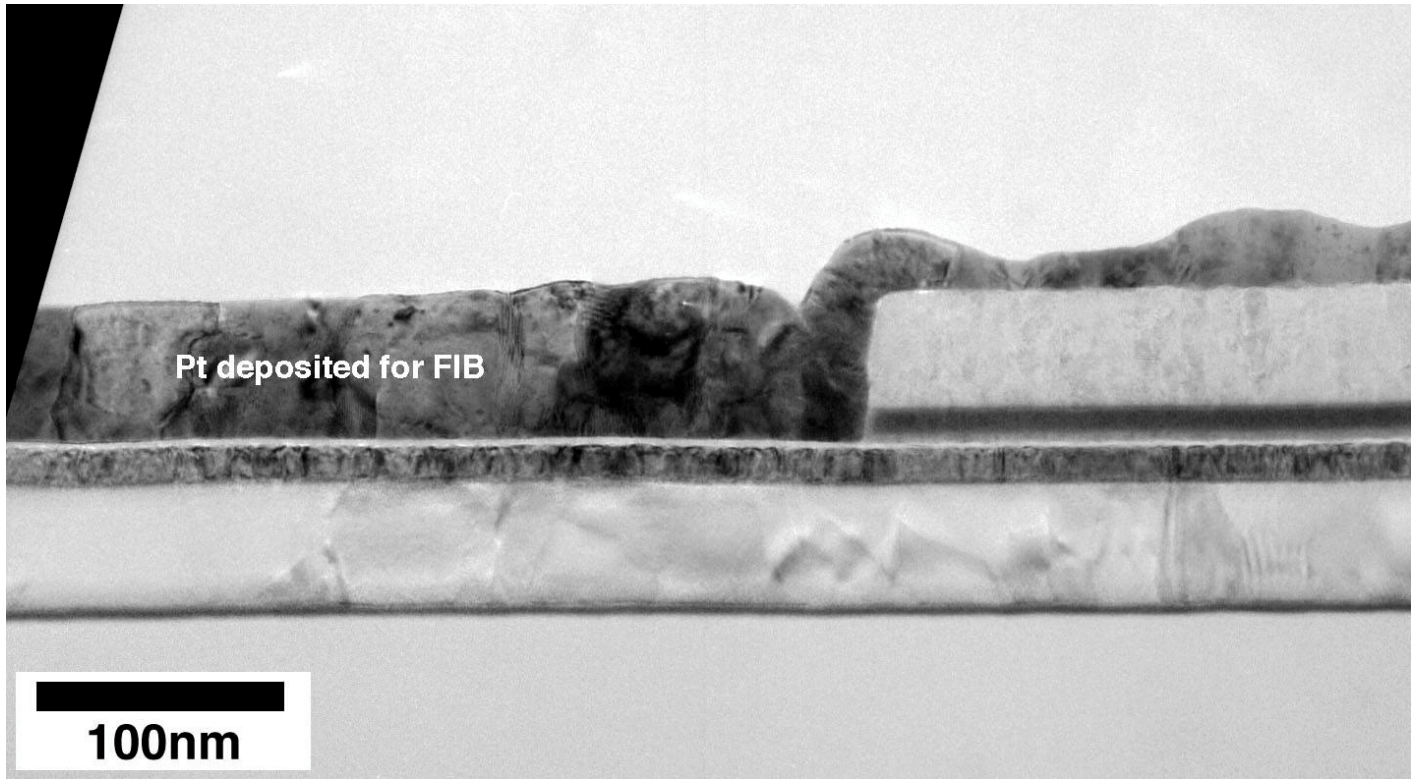
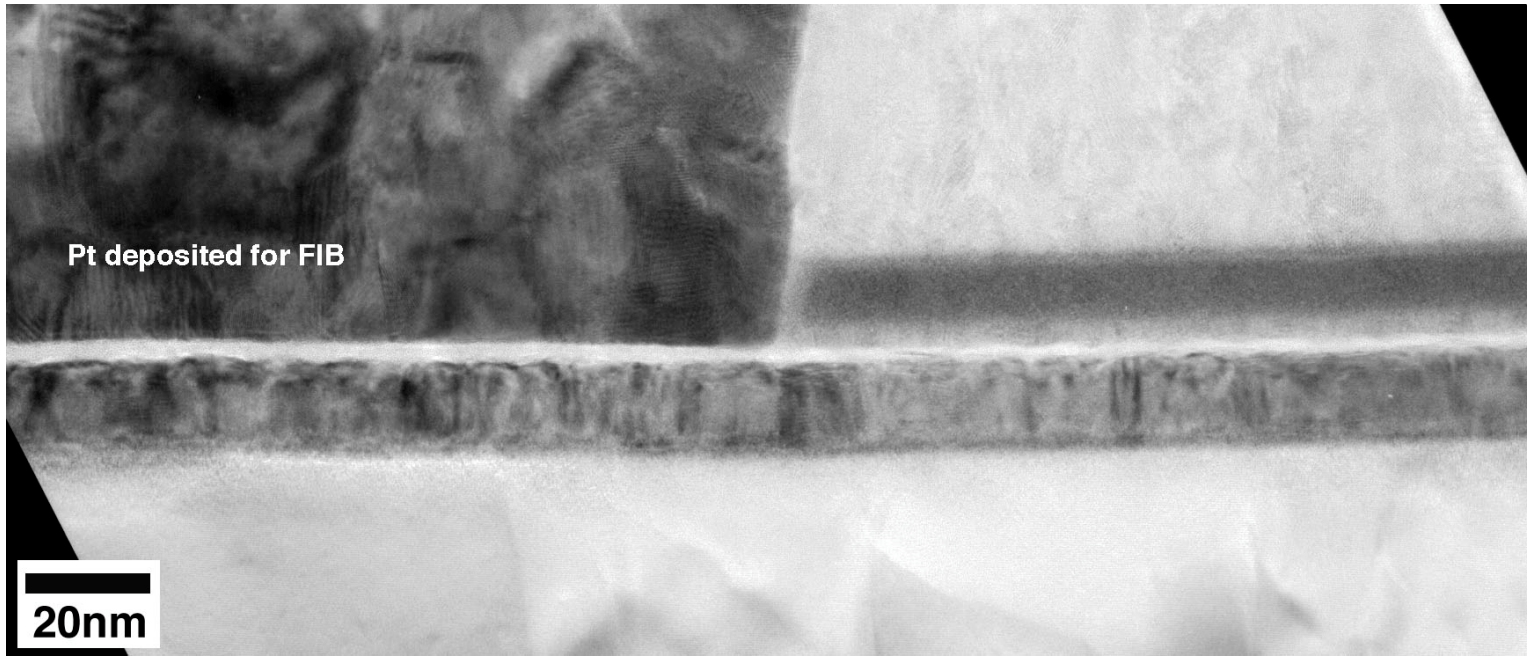
TEM of MRAM Stack after Stop-on-Al_2O_3 Process



0.6µm feature

Etch stopped on 15Å alumina layer

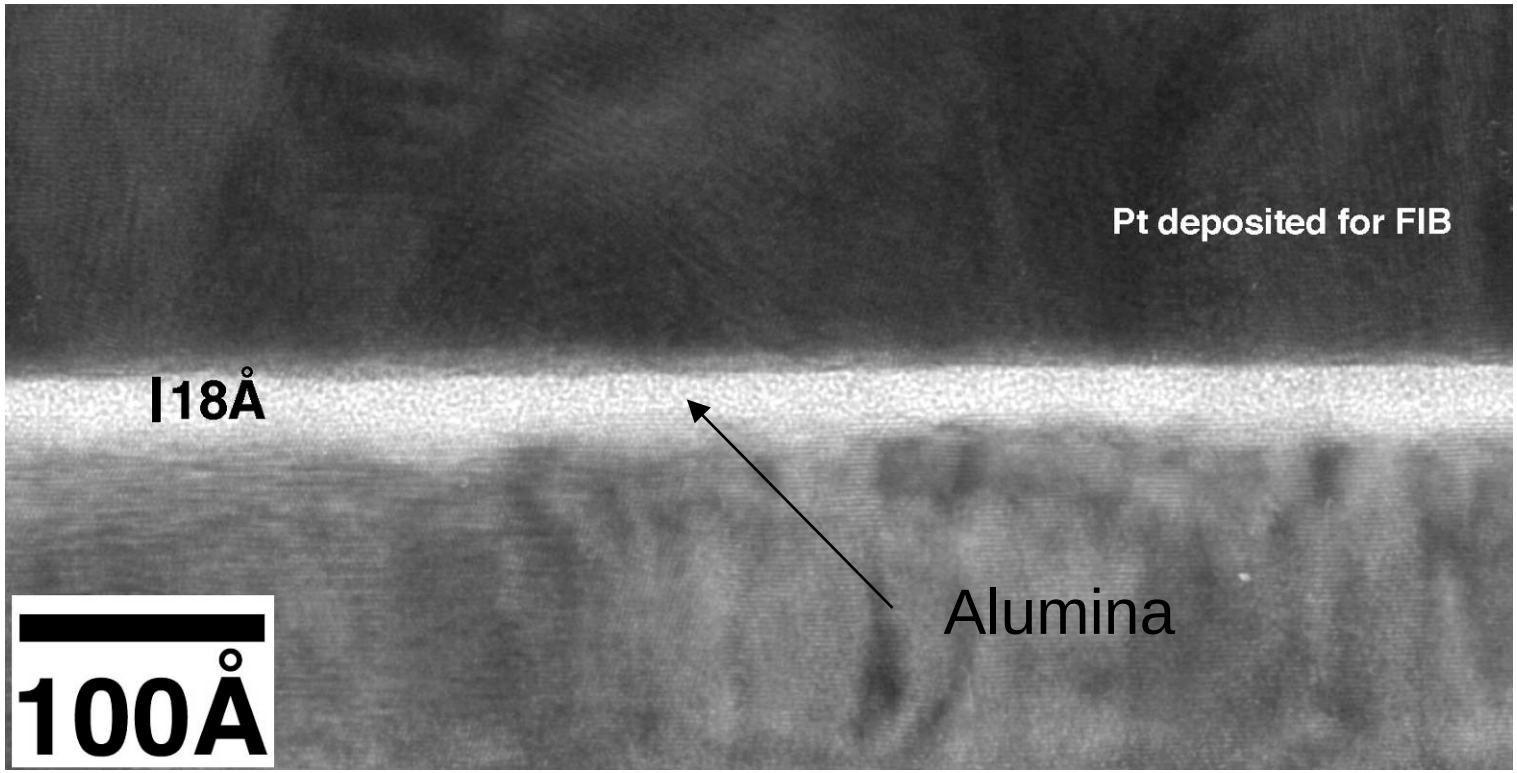
TEM of MRAM Stack after Stop-on-Al_2O_3 Process



0.6µm feature

Etch stopped on 15Å alumina layer

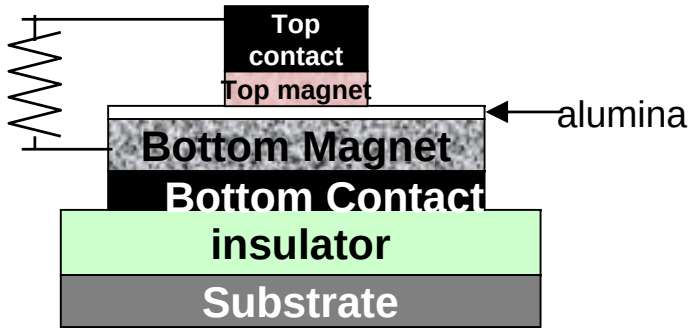
High Mag TEM of MRAM Stack after Stop-on-Al_2O_3 Process



SOA process leaves alumina layer intact

SOA Verification

- **Proprietary technique developed and used to determine if alumina was breached during processing**
- **TEM used to confirm continuity of alumina**
- **Kerr Optical Magnetometry measurements confirming that the alumina layer and fixed magnet layer below the alumina are intact**
- **Electrical resistance measurements have confirmed no electrical shorting across junction**
- **Magnetic Ratio measurements confirmed working devices**



FeRAM
Stack Etch Process

HRe- CCP High Bias processing regime utilizing dual frequencies – 13.56MHz/450kHz

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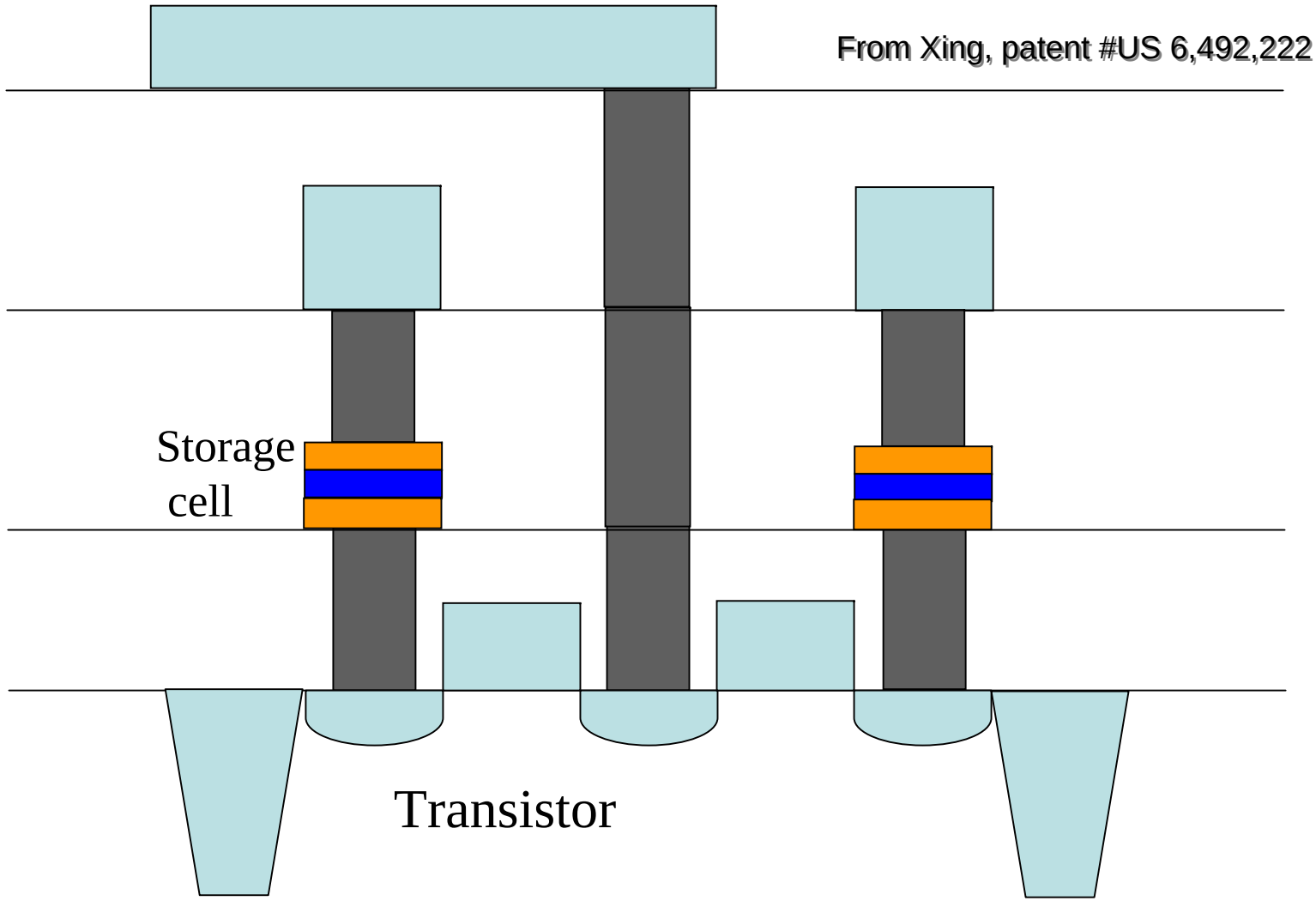
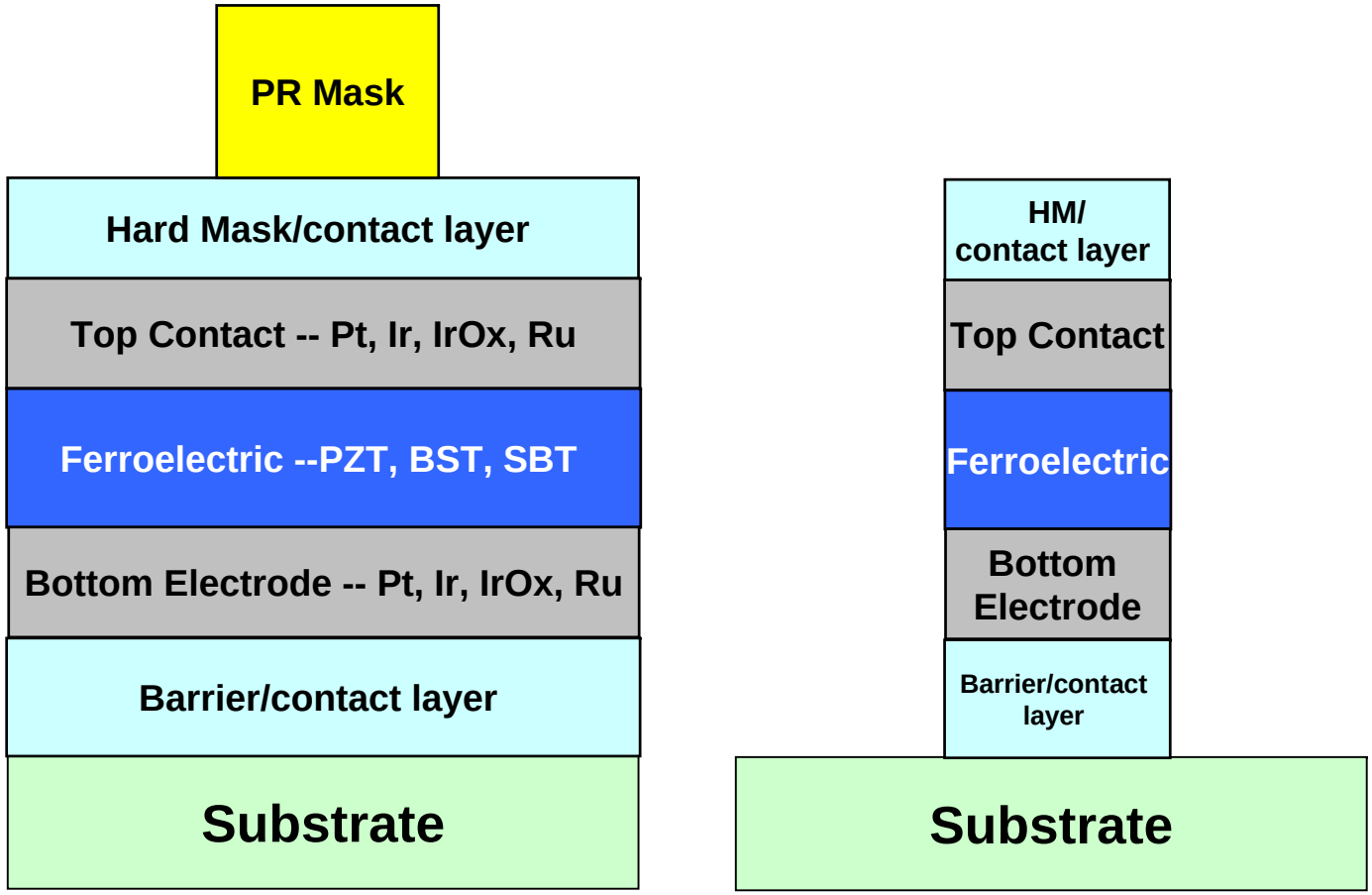
FeRAM Cell Architecture



Typical FeRAM Stack Structure



Note: similar materials used in Integrated Capacitor Devices and MEMs

FeRAM Etch Requirements

- High Ion energy
- Process Stability over time
- Uniform Etch Capability
- Temperature <500ºC during processing
- High Throughput and MWBC
- Memory cell bit performance

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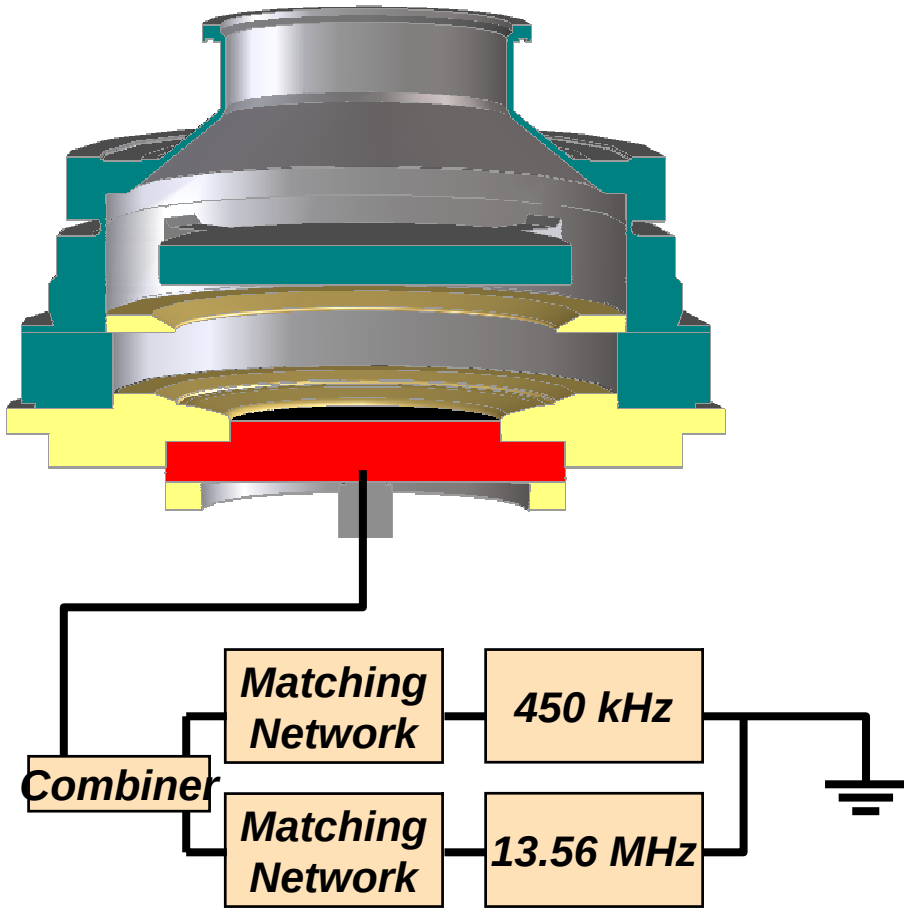
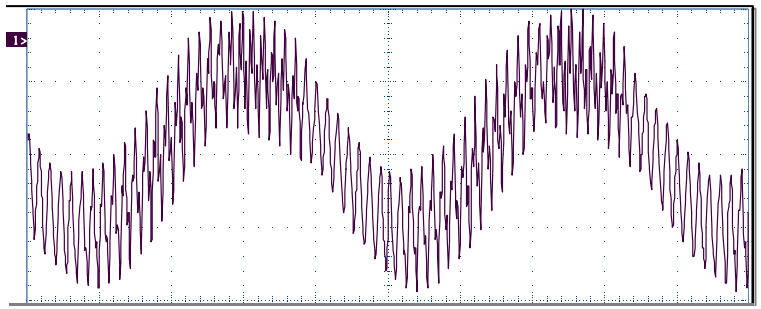
Dual Frequency HRe- Process Module for FeRAM applications

- Dual Frequency through wafer
- High ion energy
  - –increased volatility of hard to etch materials
- Plasma stability
  - –No sputtering of deposited material from internal surfaces



Power delivered only through the wafer

Independent control of Ion Density and Bias Voltage using Dual Frequencies through the wafer

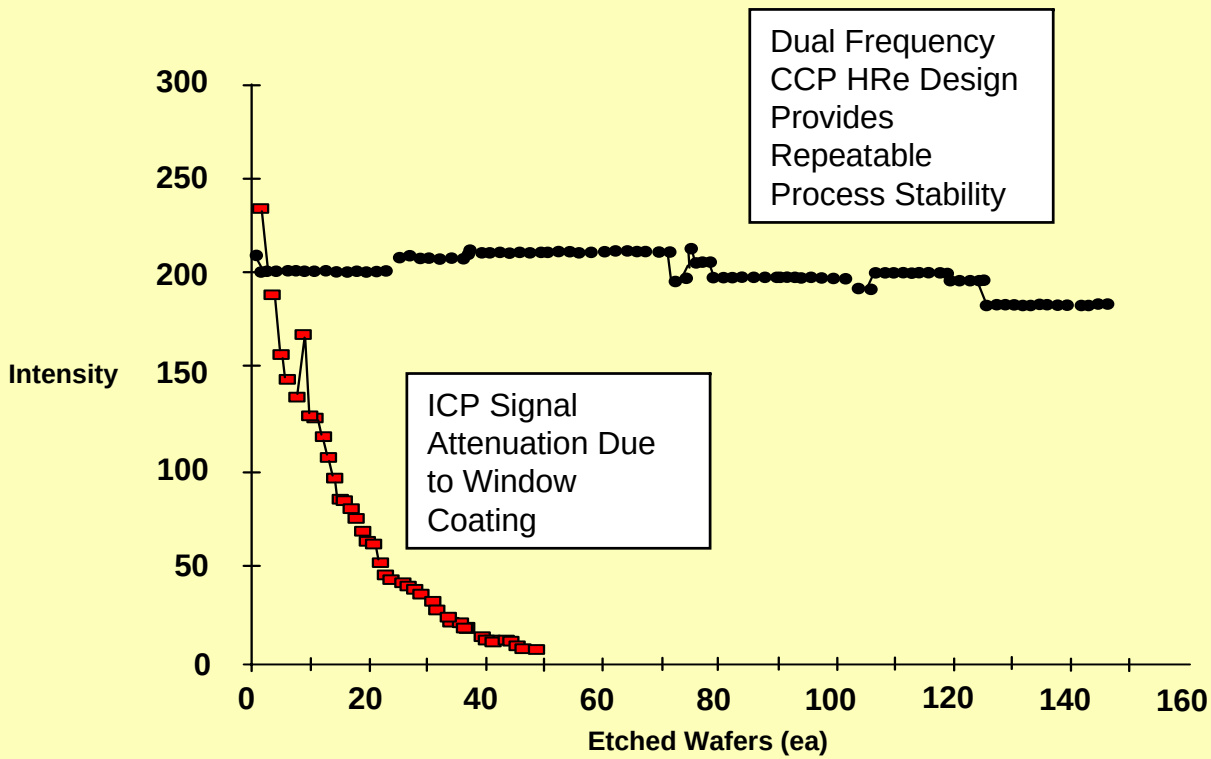


13.56MHz + 450kHz

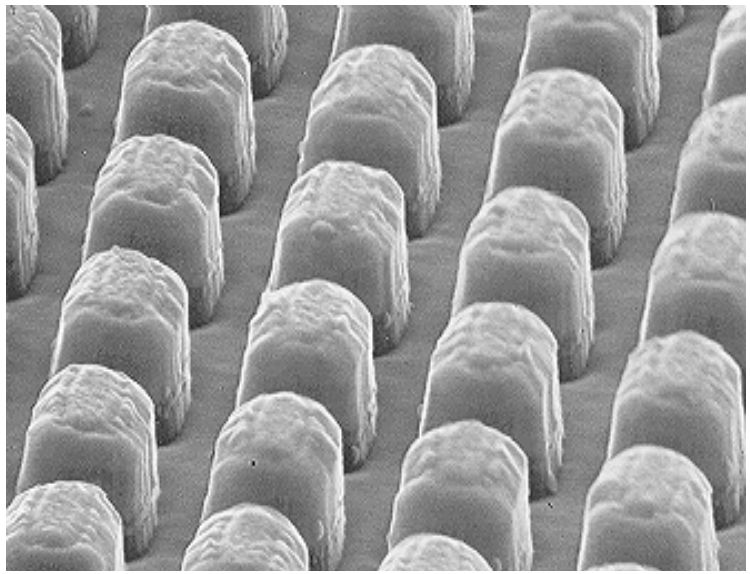
HF/LF Power (Watts)	DC Bias (Volts)
500/0	*640*
300/200	*1400*
700/0	*760*
500/200	*1400*

Control of Process Stability

no attenuation of plasma over time in CCP HRe

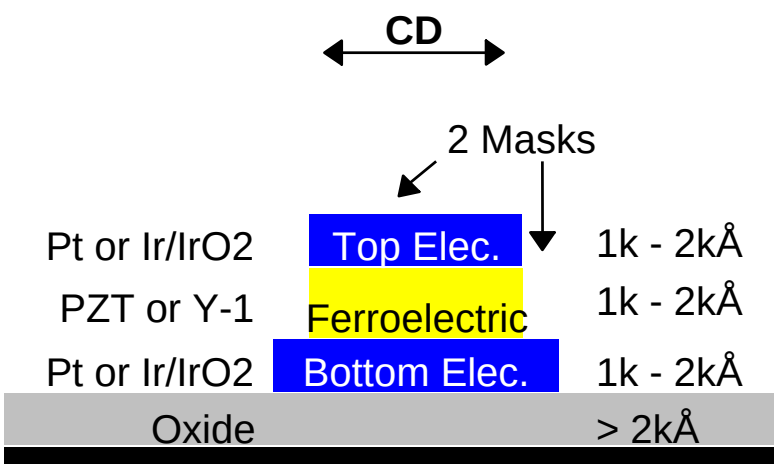


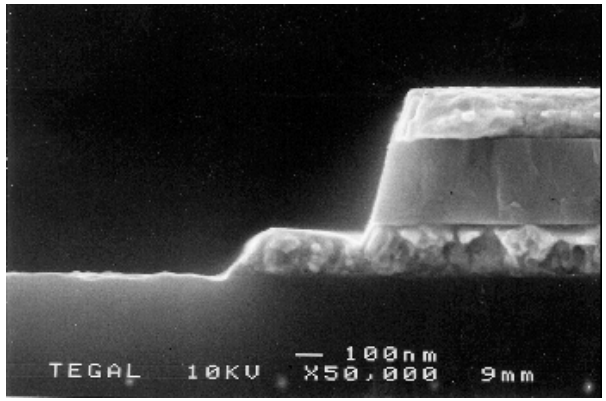
Pt post



Process temperature <100C
ER>1000 Å /min
Profile <80°

FeRAM Planar Stack Etch Results





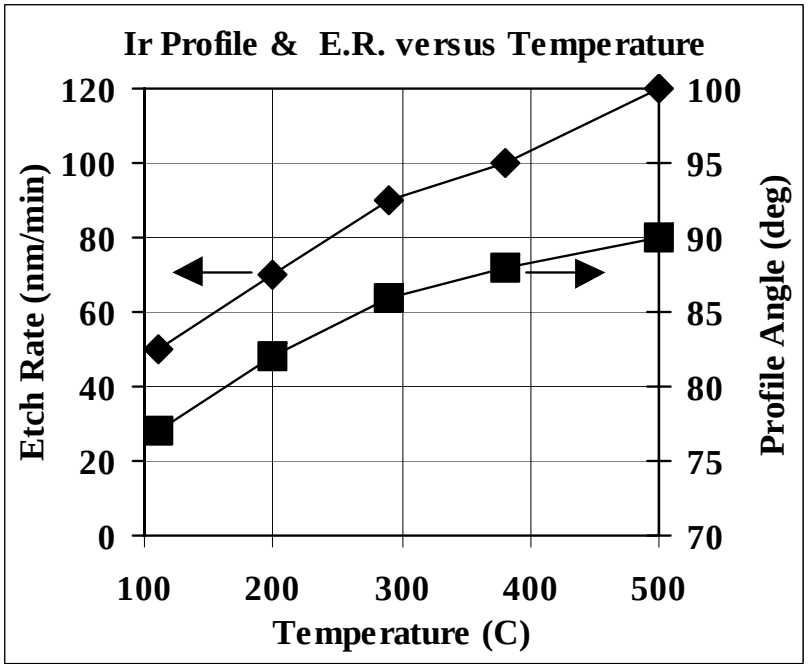
Pt/PZT/Pt

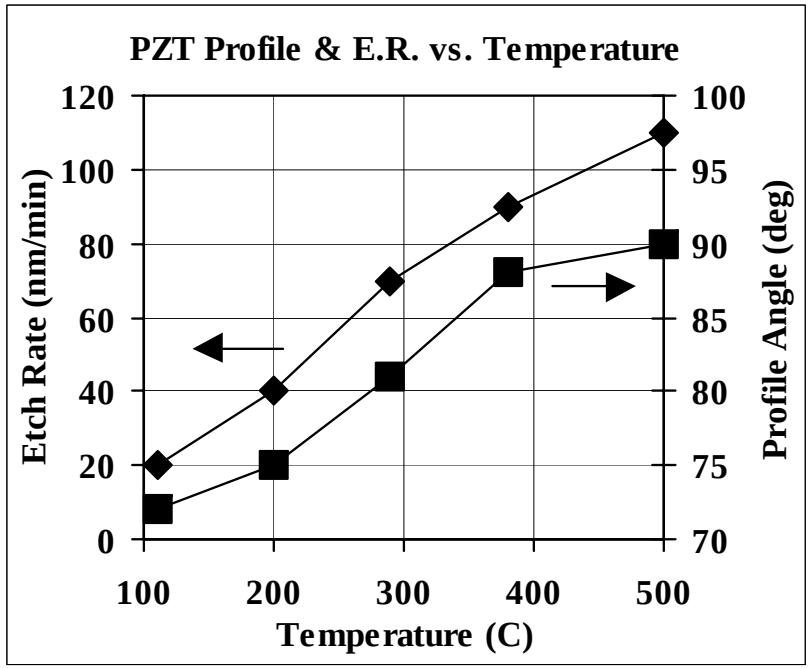
Capacitor stack etch (two masking steps)

Key etch results are profile, residue, selectivities, rate

Process temperature <100C
ER>1000A/min

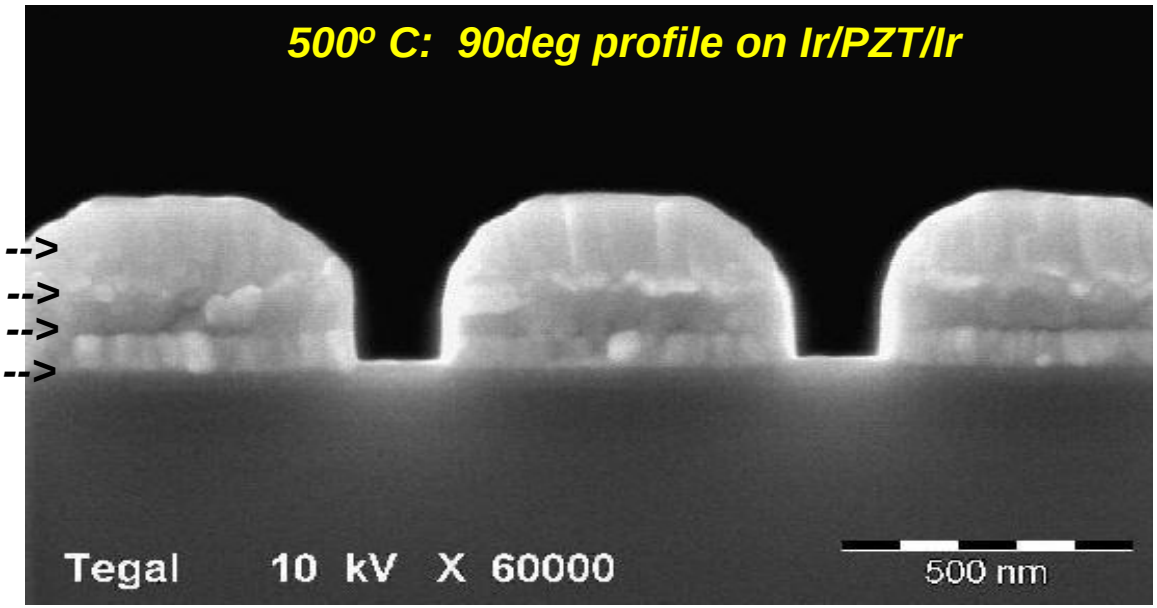
High Temperature Ir and PZT Etching in CCP HRe-





Incorporation of high temperature capability provides improved process performance

High Temperature Etch Performance for Ir/PZT/Ir Stack in Dual Frequency HRe CCP Process Module



90 degree Stack Profile

0.13 micron spaces

Conclusions

- Dual frequency plasma tools utilizing 13.56MHz for efficient plasma generation and 450kHz for efficient biasing can be used to produce a wide range of process conditions suitable for advanced memory cell fabrication
- A unique stop-on-alumina process has been demonstrated for MRAM device fabrication using the Spectra™ dual frequency ICP process module
- The stop-on-alumina process was achieved specifically using the features of control of ion energy to very low levels and control of plasma uniformity

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Conclusions

- Dry etching of FeRAM device structures has been demonstrated using the features of control of ion energy to very high levels and delivery of all power through the wafer
- High etch rates (1000-3000 Å/min) can be obtained in the HRe$^-$ CCP at Temperatures <100C with no loss in plasma stability
- High temperature processing (500°C) in combination with dual frequencies applied to the wafer has been shown to produce high etch rates and vertical profiles in advances FeRAM stack structures

Acknowledgements

Steven Marks for providing the FeRAM results

END