# Consumables Erosion and Temperature Effects on Dielectric Etch Rates

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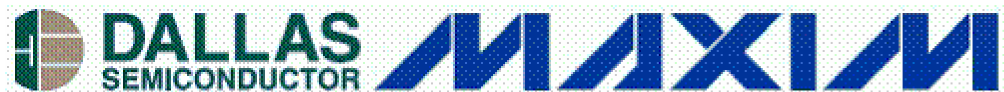
September 08, 2005



# Topics

- Lam Exelan (200mm)
  - Erosion of Upper Si Electrode
- Amat Centura 5200 MXP+ (200mm)
  - Temperature effects on Spin on Glass Etch Rates
- Lam 9500 (150mm)
  - Erosion of conductive SiC RF "Sense" pins

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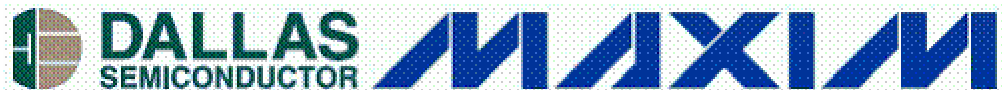
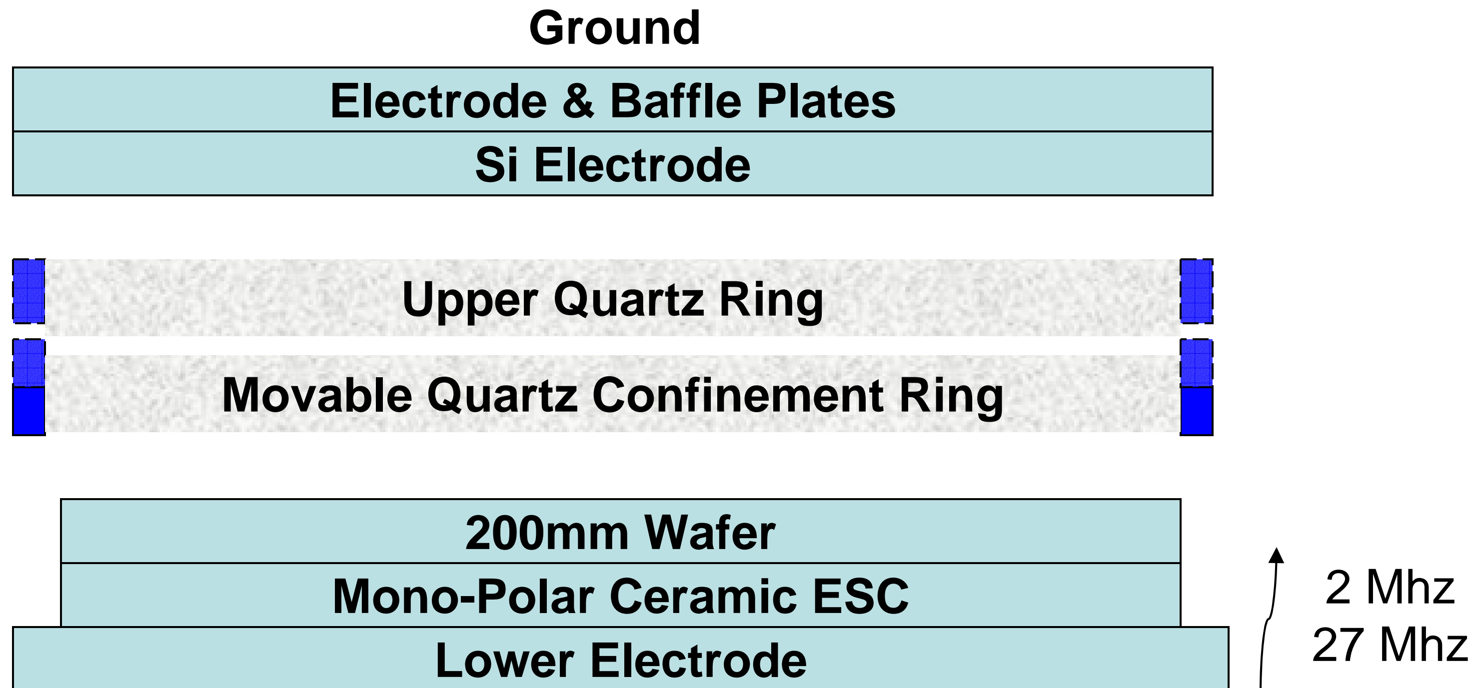
# Lam Exelan

# Erosion of the Upper Si Electrode



# Lam Exelan - Chamber Configuration




- 2 & 27 Mhz Power is applied to the Lower Electrode.
- Upper Electrode is grounded.
- Pressure Control is modulated by Total Gas Flow and Movable Quartz Confinement Ring.
- Si Electrode is part of the Gas Distribution system and the grounded Electrode

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# Lam Exelan Si Electrode RF Hours vs Etch Rate / %STDev

Unpatterned Thermal Oxide Avg. Etch Rate (Ang / Min)

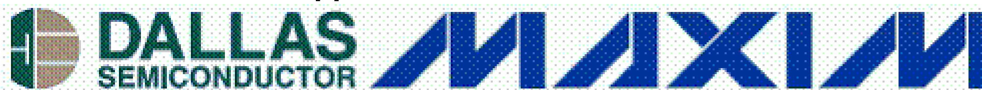
% STDev

Avg. ER
%STDev

Etch Rate Declining
Uniformity Increasing

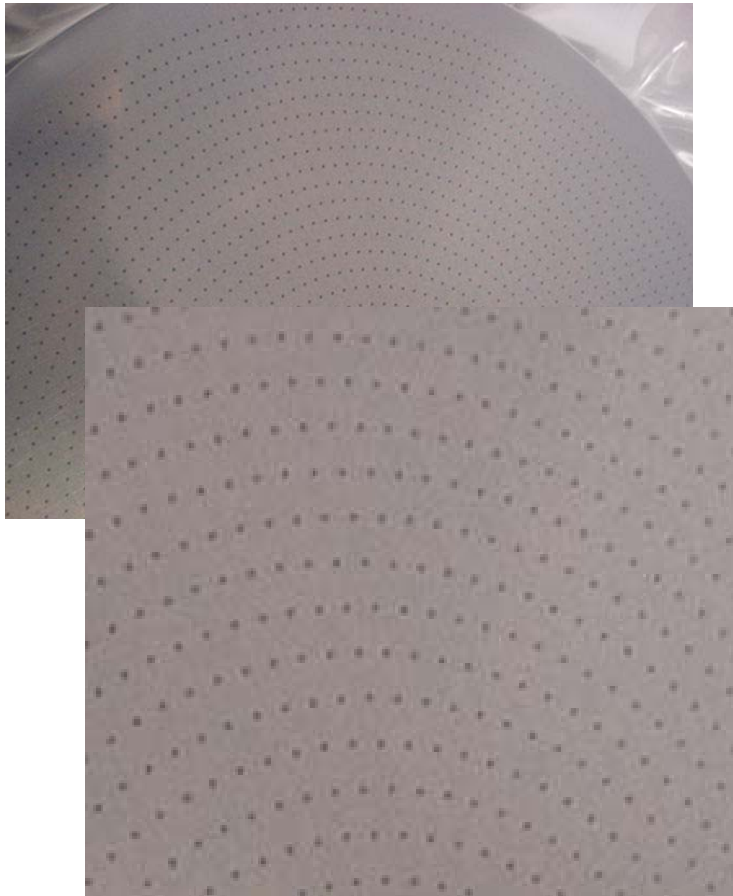
|  |  | PM2 | PM3 | PM4 |
|---|---|---|---|---|
|  | Type | Company A | Company A | Company B |
| Etch Rate (A / Min) | Start | 1980 | 2030 | 1880 |
|  | Finish | 1780 | 1800 | 1730 |
|  | Delta | 200 | 230 | 150 |
|  | Delta, % | 10.10% | 11.30% | 7.90% |
| % STDev | Start | 1.7 | 2 | 3.5 |
|  | Finish | 4.6 | 4.8 | 6.5 |
|  | Delta | 2.9 | 2.8 | 3 |

Upper Si Electrode RF Hours

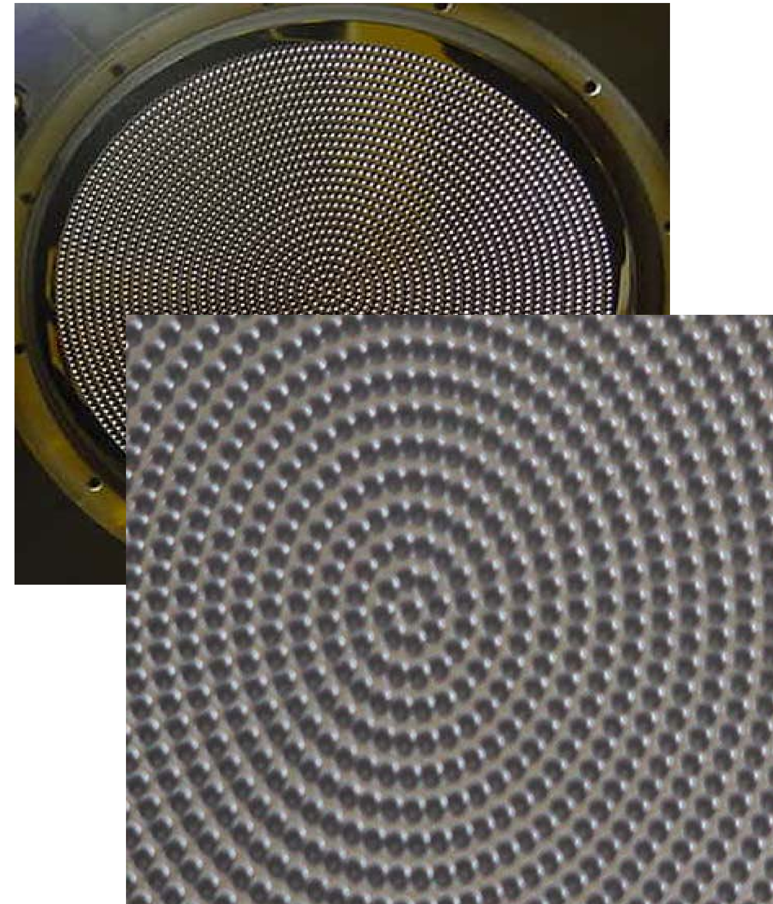


# New/Used Upper Si Electrode

**New Electrode**



**Used Electrode**



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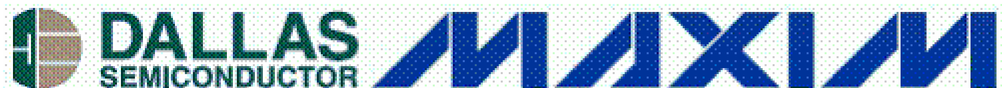
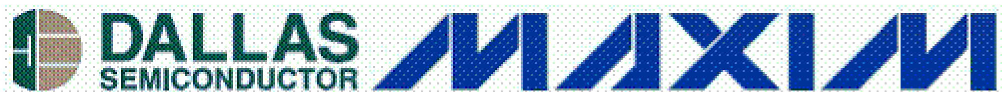
# Summary

- Observations:
  - Unpatterned Oxide Etch Rate decreases with RF Hours on Upper Si Electrode
  - Non-uniformity increases with RF Hours on Upper Si Electrode
  - Si Electrode "Hole" profile becomes "fluted"
  - From subsequent Electrode changes, the Electrode appears to influence Uniformity more than Etch Rate.
  - Etch Rate seems to be more influenced by other chamber hardware
  - Using this data Wet Clean schedule has been optimized for desired Etch Rate / Uniformity range
- Theories:
  - Gas distribution changes due to the increase in Si Electrode "Hole" size
  - Gap between Si Electrode and wafer increases, decreasing Etch Rate

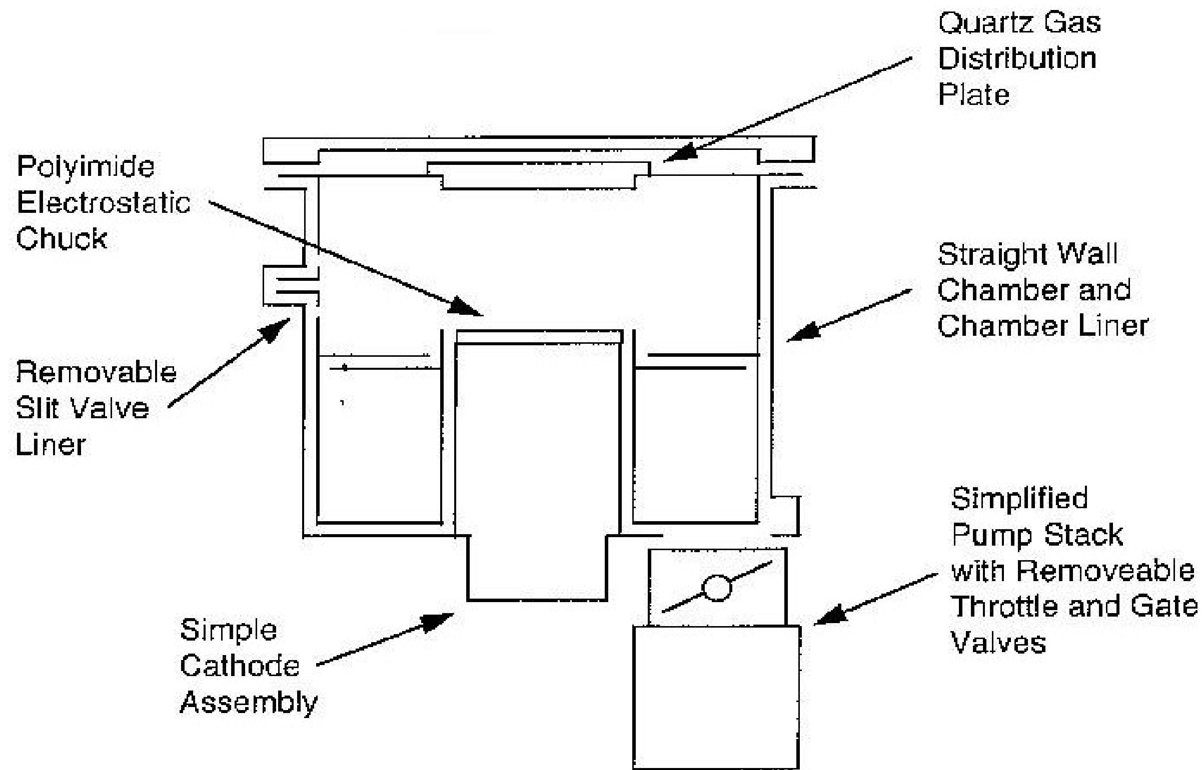


# Amat MXP+ (200mm)

# Effect of Temperature on Spin on Glass Film Etch Rate



# Amat MXP+ - Chamber Configuration




- MERIE Chamber
- Power is applied to the Lower Electrode (13.56 Mhz)
- Anodized Al Chamber Liner acts as the Grounded Electrode

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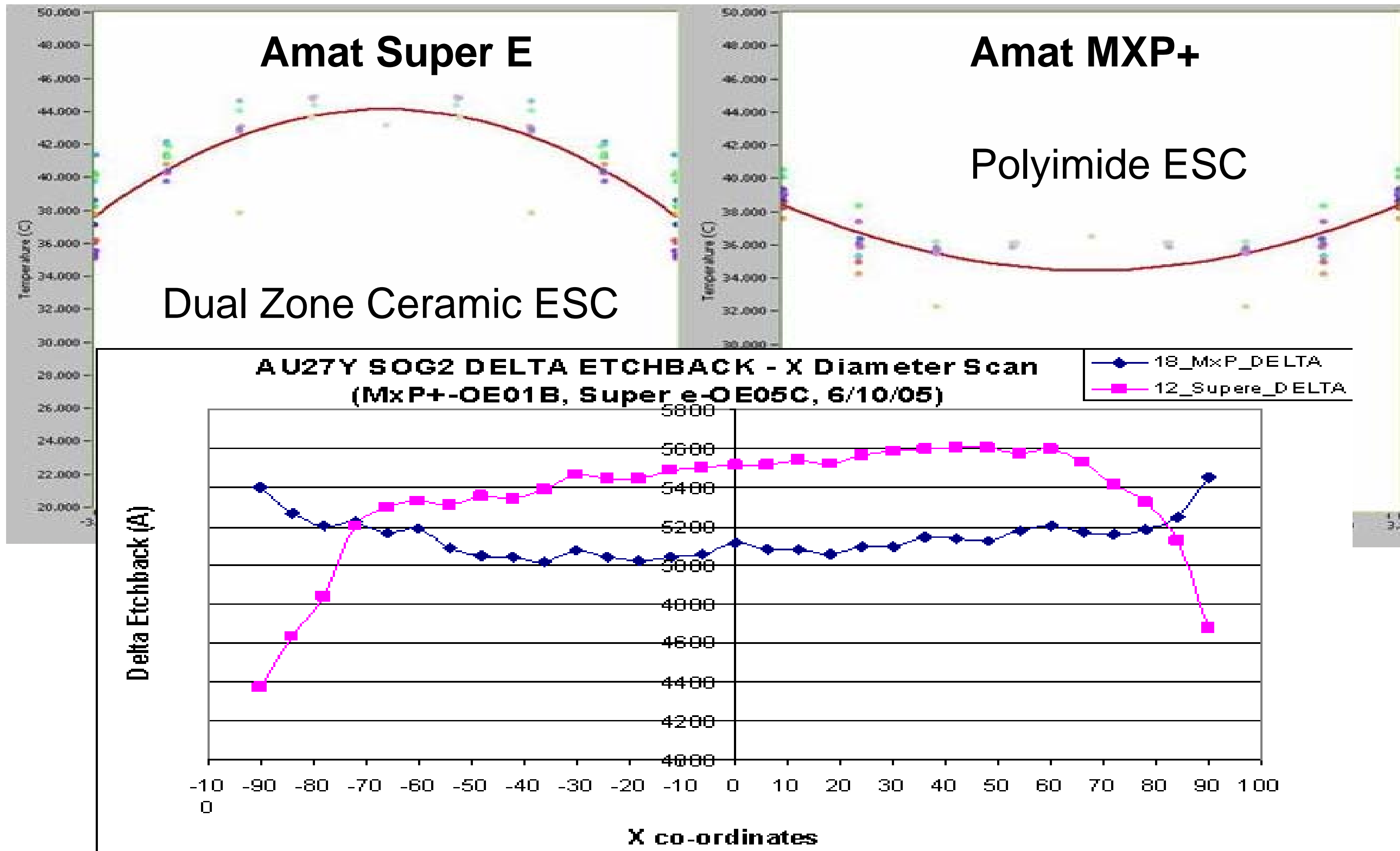
# Temperature / Etch Delta Profile




Increase in Temperature correlates with higher Etch Delta

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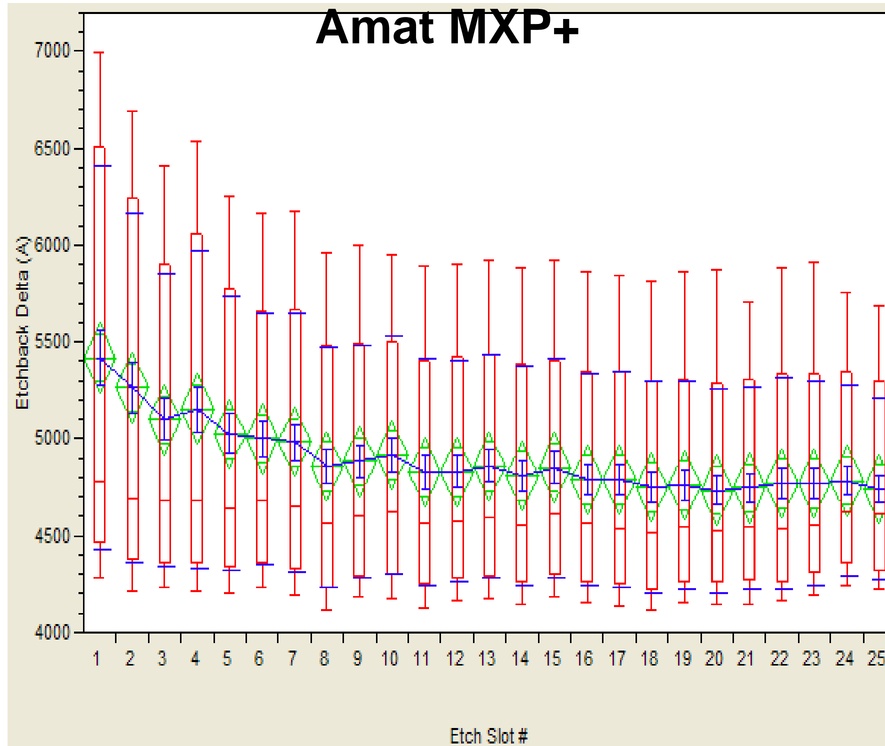
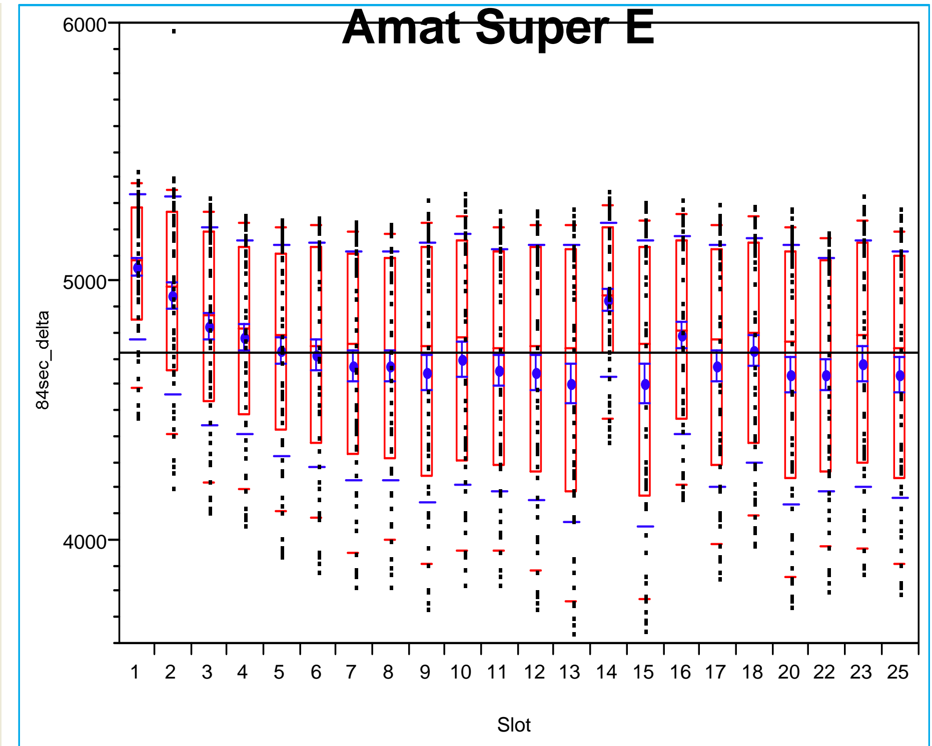
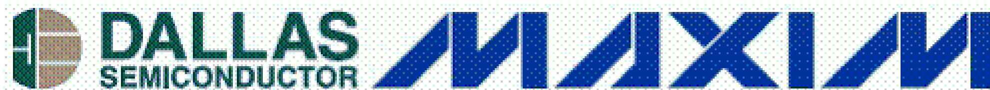
# Across Run Etch Delta Profile



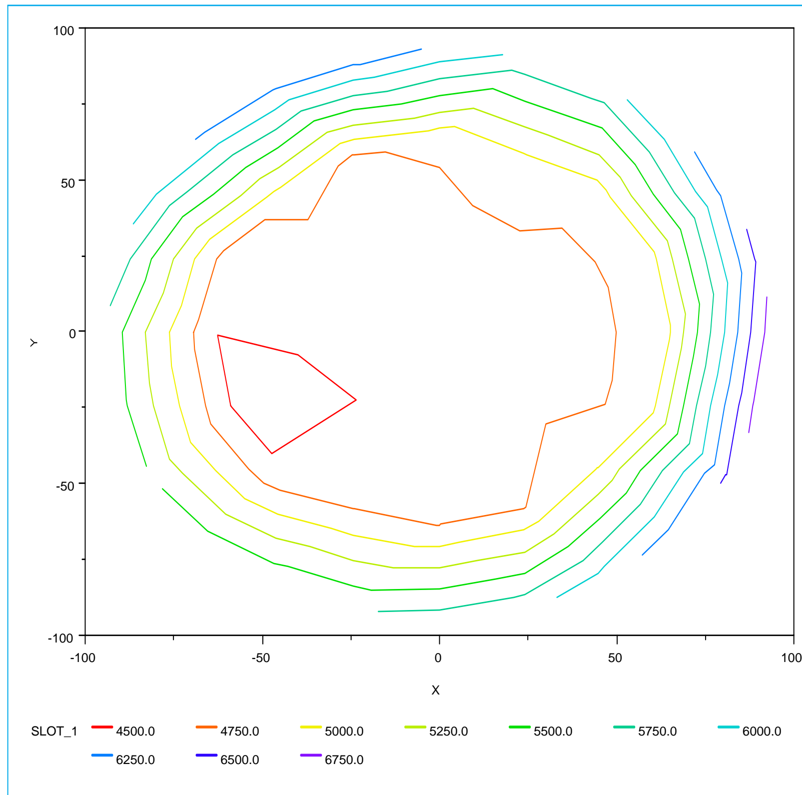




**MXP+** - Within wafer uniformity **decreases** across a 25 wafer run.
**Super E** - Within wafer uniformity **increases** across a 25 wafer run

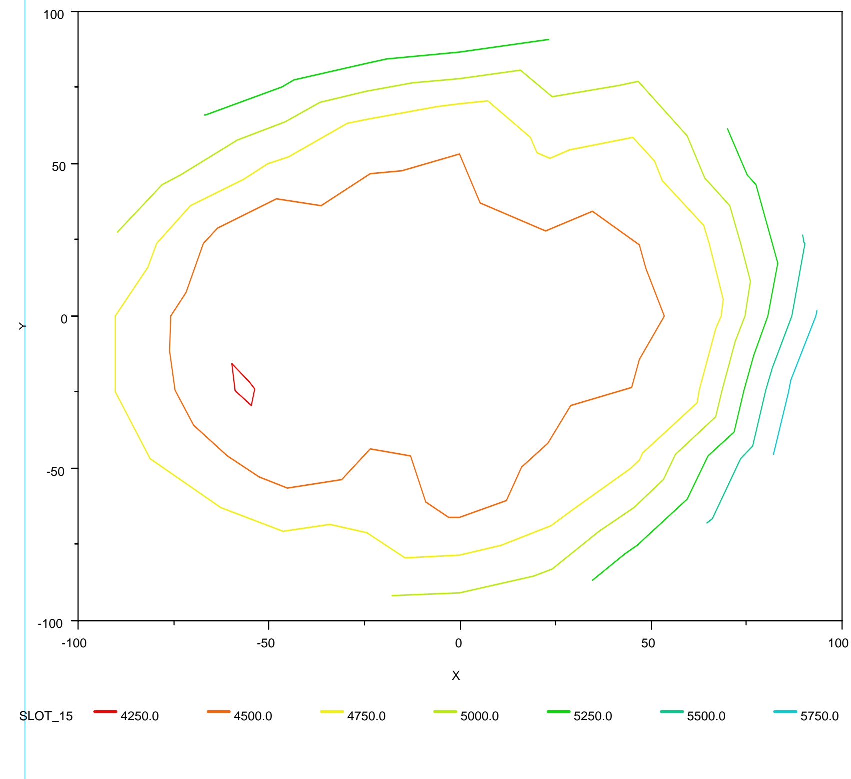


# MXP+ Etch Delta Contour Plots

## MXP+ - Slot 1




## MXP+ - Slot 8




Slot #8 shows less within wafer Etch Delta variation.
Center Etch Delta remains the same. Edge Etch delta decreases
Non-uniformity occurs at edge of wafer.

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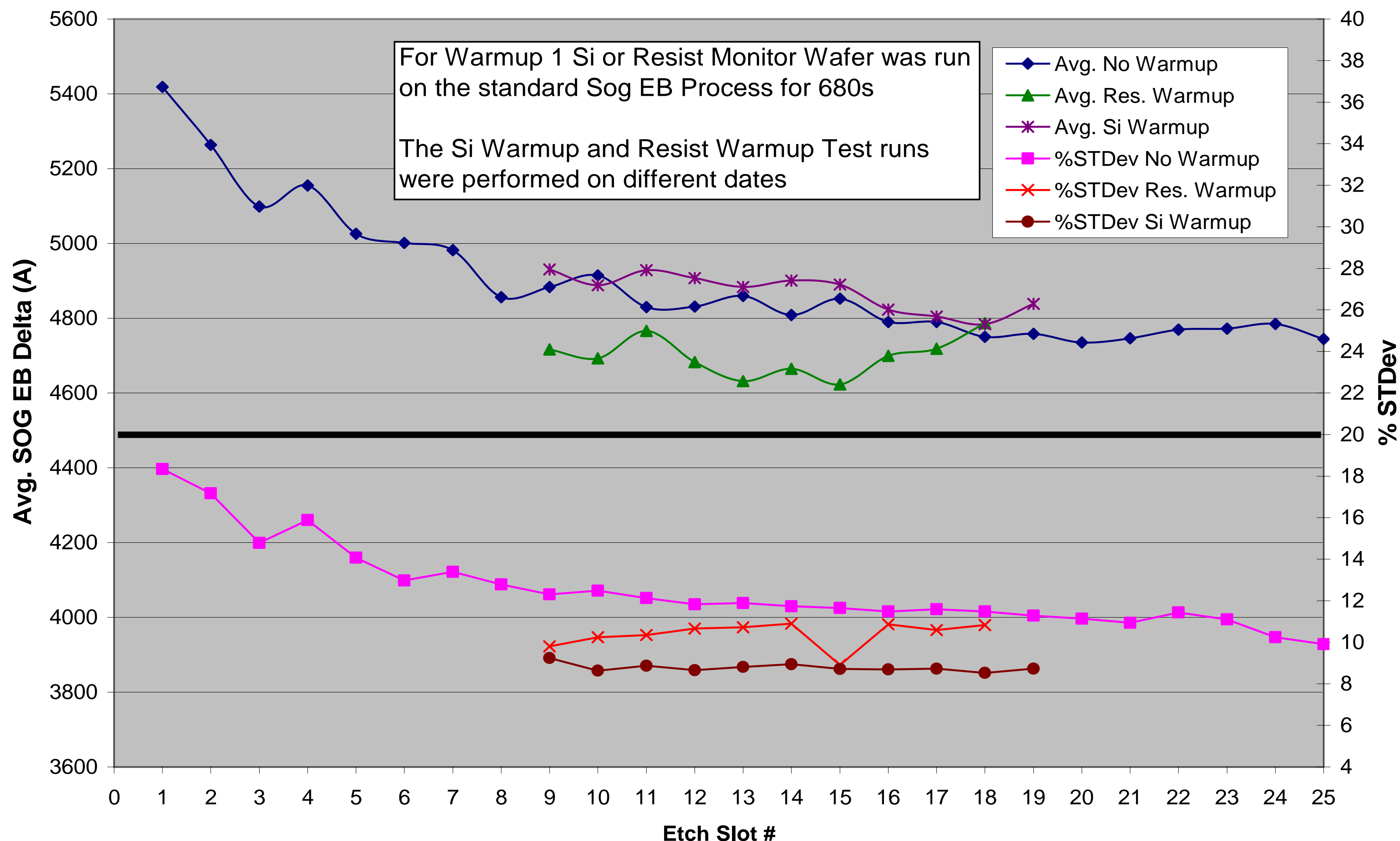
# MXP+ Warm-up Procedure

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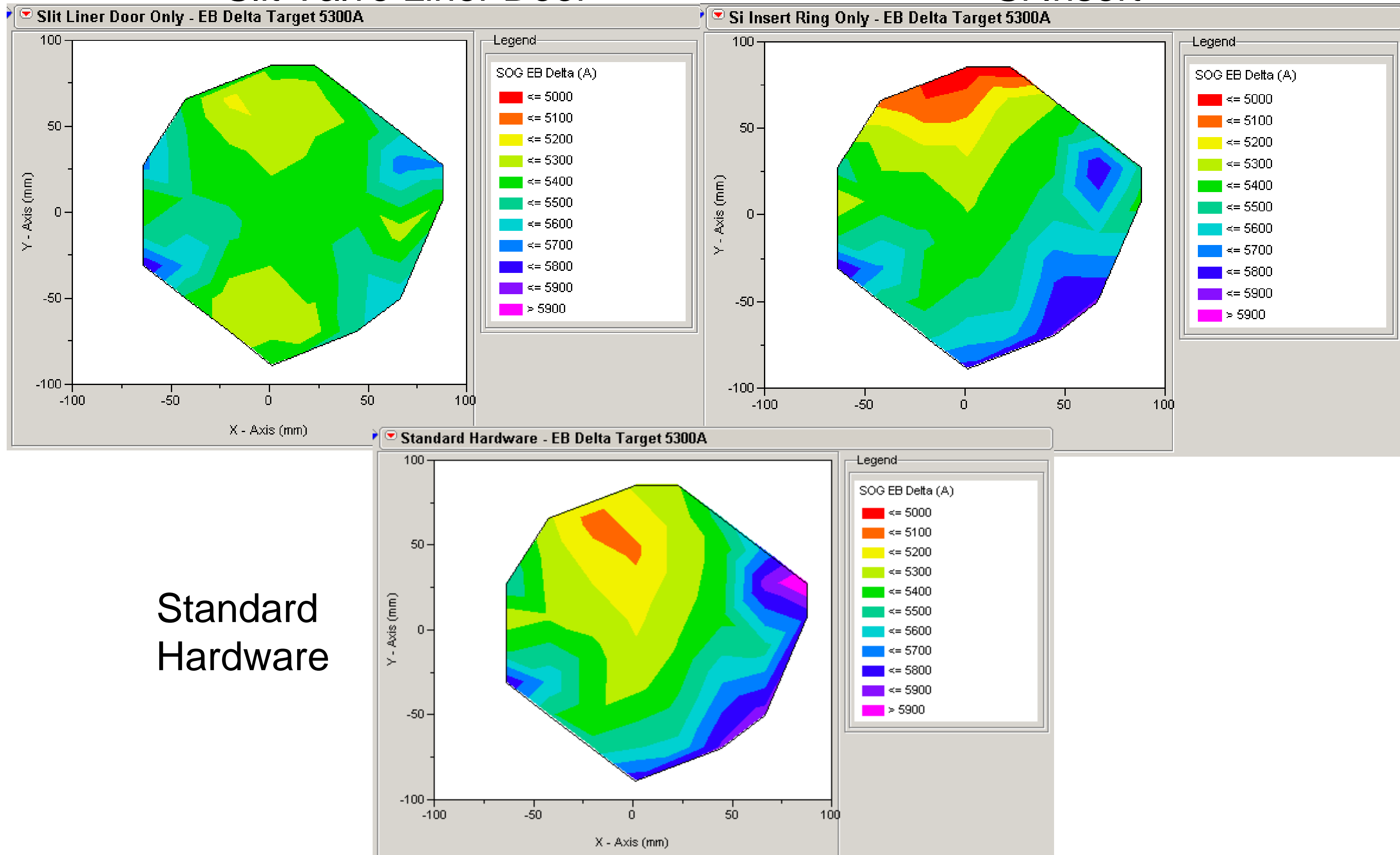
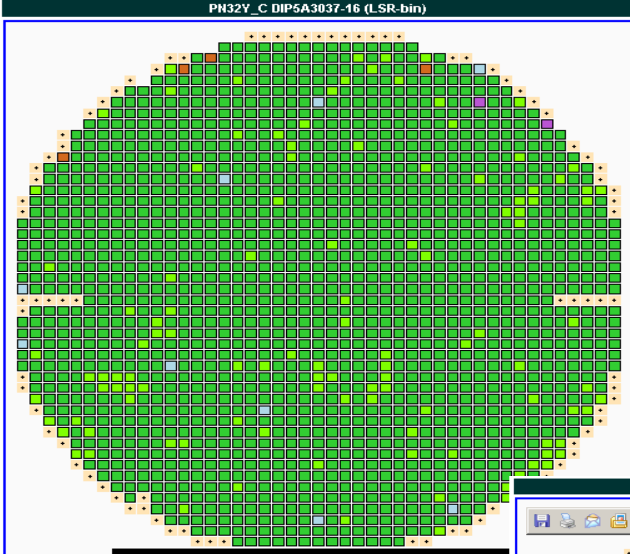
# Product Delta Contour Plots – Etchback Delta 5300A

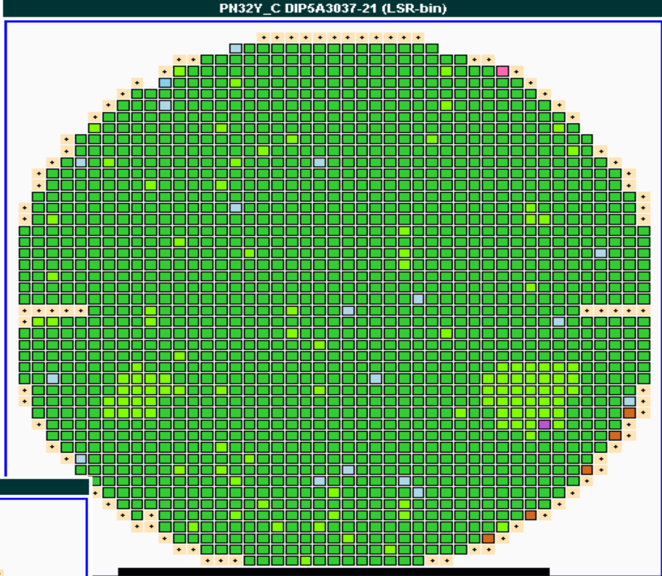


# Yield Map Contour Plot Comparison – EB Target 5300A

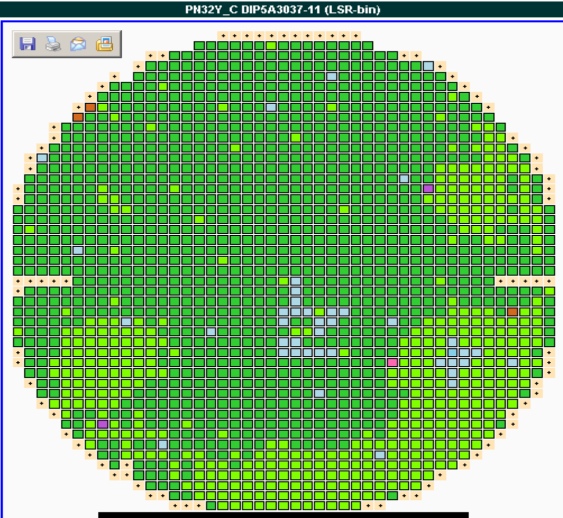
Slit Liner Door




Si Insert




Standard Hardware

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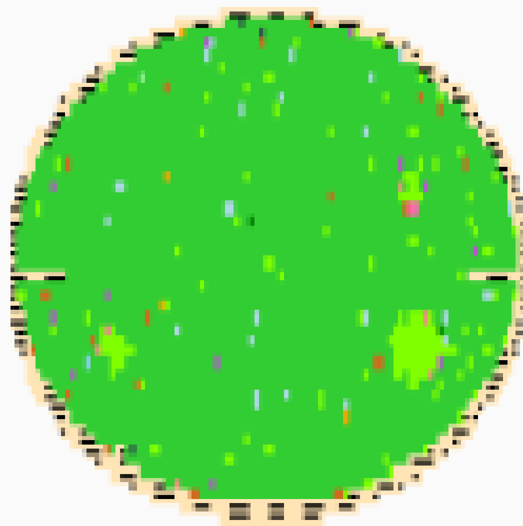
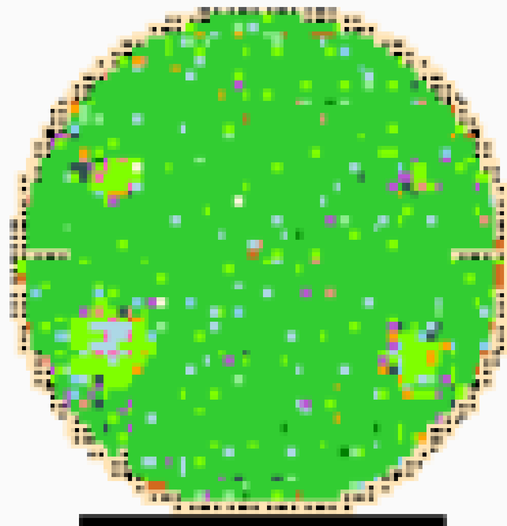
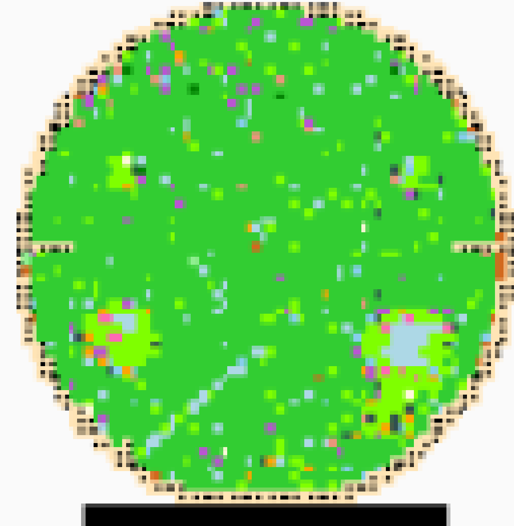
# Lift Pin Yield Pattern

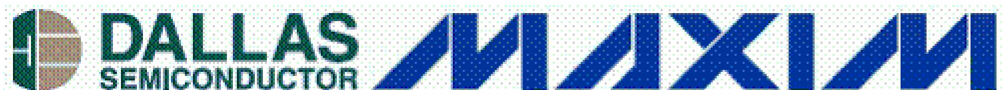






# Summary

- Observations:
  - At Time = 0; Super E ESC is colder at the Edge, MXP+ is hotter at the edge
  - Increase in temperature correlates with a higher etch delta on Amat Super E (Center Fast) and MXP+ systems (Edge Fast)
  - MXP+ system within wafer non-uniformity occurs primarily at the edge of the wafer (Higher Etch Delta)
  - MXP+ system within wafer non-uniformity improves across a 25 wafer run. (Edge Etch Delta decreases, Center Etch Delta remains the same)
- Theories
  - Fluorine quenching – As the Outer Quartz Shadow ring heats up Fluorine reacts; therefore reducing the availability of free F* at the wafer edge decreasing the Edge Etch Delta
  - The Outer Quartz Shadow ring heats up, relative Temperature delta between ESC edge and Shadow ring is reduced: less polymer deposition occurs on the Quartz Ring / more polymer deposition occurs on the Edge of the wafer decreasing the Edge Etch Delta.
- What Next?
  - Additional across run tests using OnWafer/Sensarray Insitu Temperature monitors.
  - Repeat tests with Si Insert Ring kit.



# Lam 9500 (150mm)

# Erosion of Conductive SiC RF "Sense" pins

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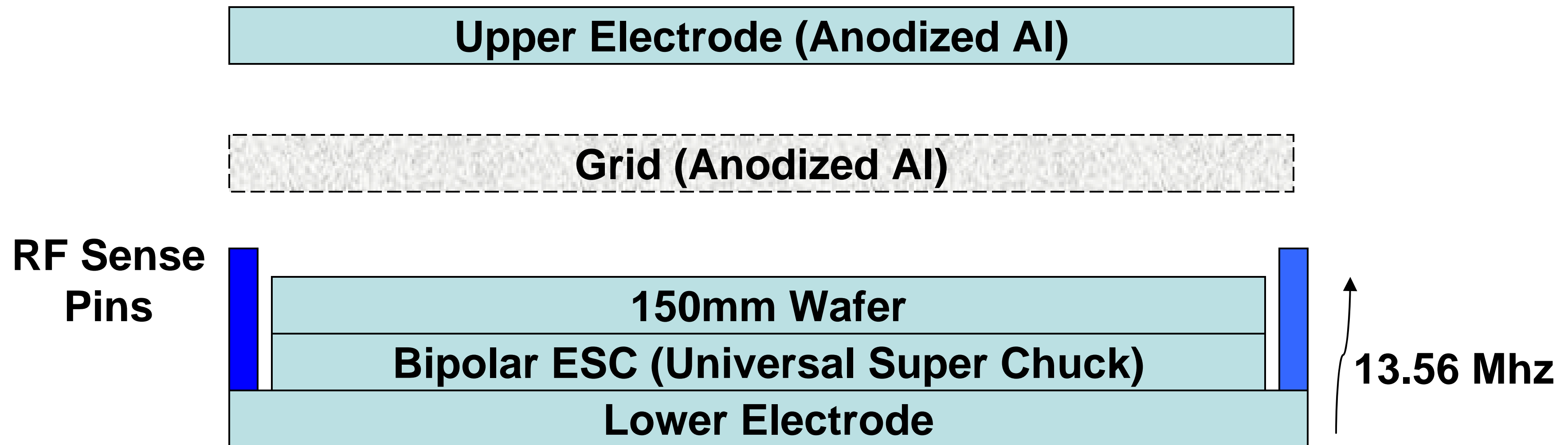
# Lam 9500 – Triode Chamber Configuration




- Power is applied to the Lower Electrode.
- Grid and Upper Electrode is grounded.
- The Anodized Al Grid helps densify the Plasma (Hollow Anode Effect)
- Bipolar ESC (Universal Super Chuck)
- RF “Sense” Pins determines the amount of voltage needed to keep the wafer clamped

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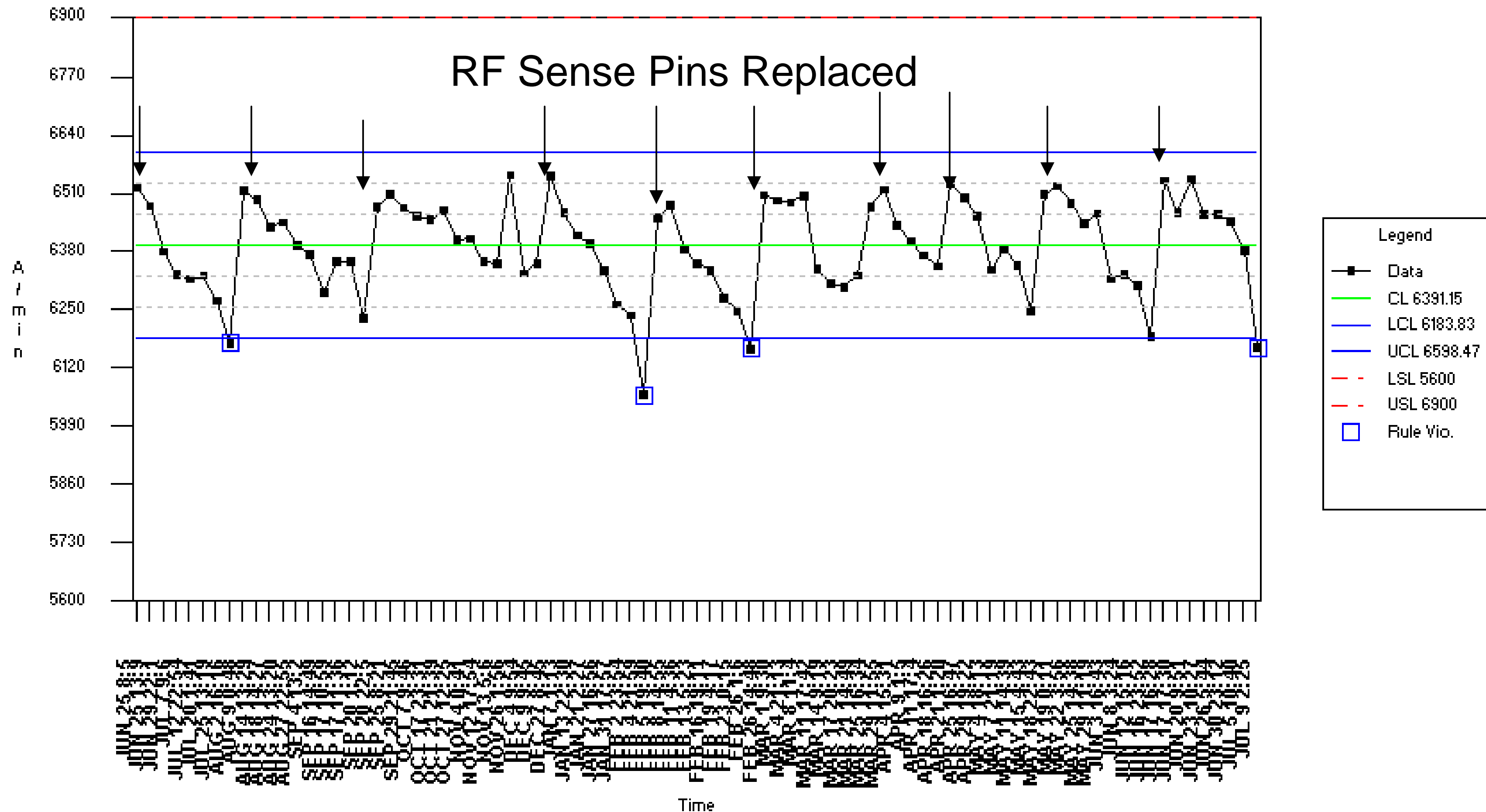
# High Power Recipe - Etch Rate vs. RF Hours



# Etch Rate vs. RF Hours – Low Power

Contact Soft Etch-Etch Rate

Control - Individuals

Machine: LAM_10 CH2

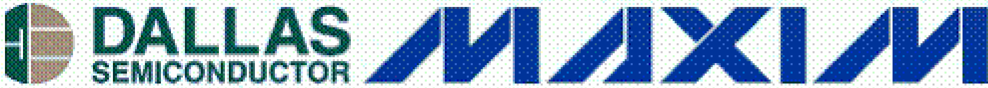
A/min

570
555
540
525
510
495
480
465
450
435
420

Legend
Data
CL 501
LCL 432
UCL 570
LSL 420
USL 570

SEP 20 22:5
SEP 25 8:21
SEP 29 21:45
OCT 7 9:46
OCT 17 23:31
OCT 21 21:39
OCT 27 12:25
NOV 4 0:38
NOV 12 18:0
NOV 13 5:6
NOV 26 1:56
DEC 4 9:49
DEC 9 9:47
DEC 27 8:45
JAN 7 1:13
JAN 13 22:30
JAN 21 2:27
JAN 27 16:45
JAN 31 17:57
FEB 2 23:54
FEB 4 21:59
FEB 5 19:40
FEB 8 14:55
FEB 11 4:36
FEB 13 5:23
FEB 16 19:11
FEB 19 4:17
FEB 23 0:15
FEB 26 1:6
FEB 26 14:48
MAR 1 9:30
MAR 4 21:56
MAR 8 11:4
MAR 11 17:34
MAR 14 9:19
MAR 17 20:23
MAR 22 10:57
MAR 25 16:34
MAR 29 11:55
APR 4 15:31
APR 9 1:4
APR 11 17:4
APR 18 16:26
APR 21 1:20
APR 25 16:46
APR 29 19:22
MAY 4 18:12
MAY 7 21:19
MAY 11 15:53
MAY 15 4:43
MAY 18 22:43
MAY 22 3:56
MAY 25 14:38
MAY 29 11:19
JUN 3 16:38
JUN 8 3:24
JUN 12 15:14
JUN 16 23:52
JUN 17 16:28
JUN 20 9:51
JUN 23 10:27

Time



# Summary

- Observations:
  - High RF Power Unpatterned Oxide Etch Rate decreases with RF Hours on RF Sense Pins
  - Low RF Power (Chemical Etch) is less sensitive to RF Hours on RF Sense Pins
  - After Wet Clean Etch Rate remains low if RF Sense Pins are not replaced
- Theory:
  - As the RF Sense Pins wear, it changes the ability of system to keep a constant clamping voltage.

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