A 300mm test wafer to evaluate charging damage

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Philtech Inc. Introduction

Established on May 21, 2001
Funded by Yuji Furumura
Capital JP Yen 205,300,000

Philtech, Inc. produces test wafers which enable to create advanced market for semiconductor development.

Products: 200mm, 300mm Blanket, Patterned wafers
*Philtech-unique products:
  - Charge-up monitor TEG 300mm
  - 100nm-featured electrical TEG
  - Standard fine CMP TEG: phil854
1. **Wafer Diameter:** 200mm and 300mm

2. **TEG Constitution:** Antenna MOS Capacitor

3. **Application:**
   - **200mm Wafer**
     - Gate Antenna: Available
     - Metal Antenna: Available
     - Contact Antenna: Available
   - **300mm Wafer**
     - Available
     - Available on request
     - Available on request

4. **Features:**
   - Practical pattern: Designed by well-experienced Engineer
   - Reliable quality: Fabrication in Super Clean-room
   - Process condition: Process option (Tox etc.) available
TEG-Pattern-1: TEG Top View

<table>
<thead>
<tr>
<th>General_Cap</th>
<th>G_BOX_Cap</th>
<th>M_BOX_Cap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G_Comb_Cap</td>
<td>M_Comb_Cap</td>
<td>CONT_Cap</td>
</tr>
</tbody>
</table>

G_BOX_Cap: Gate BOX-Antenna MOS Capacitor
G_Comb_Cap: Gate Comb-Antenna MOS Capacitor
**TEG-Pattern-2: Gate BOX-Antenna MOS Capacitor**

Antenna Ratio = \( \frac{\text{Antenna Area}}{\text{Active Area}} \)

<table>
<thead>
<tr>
<th>Gate Antenna</th>
<th>Active</th>
<th>Gate Pad</th>
<th>Antenna Ratio</th>
<th>Antenna Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.02mm²</td>
<td>10</td>
<td>0.10mm²</td>
<td>100</td>
</tr>
<tr>
<td>100</td>
<td>1mm²</td>
<td>500</td>
<td>5mm²</td>
<td>1K</td>
</tr>
<tr>
<td>1K</td>
<td>10mm²</td>
<td>2K</td>
<td>20mm²</td>
<td>2.5K</td>
</tr>
<tr>
<td>2.5K</td>
<td>0.01mm²</td>
<td>10K</td>
<td>0.04mm²</td>
<td>100K</td>
</tr>
<tr>
<td>100K</td>
<td>0.4mm²</td>
<td>1M</td>
<td>4mm²</td>
<td></td>
</tr>
<tr>
<td>1M</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Gate Edge on Field**

![Top View Diagram]

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**TEG-Pattern-2: Gate Comb-Antenna MOS Capacitor**

![Diagram of Gate Comb-Antenna MOS Capacitor]

**Antenna Ratio** = (Thickness) / (Peripheral Length) / (Active Area)

<table>
<thead>
<tr>
<th>Electrode Film Thickness</th>
<th>Antenna Ratio (mm)</th>
<th>Perimeter Length (mm)</th>
<th>Active Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000</td>
<td>0.02</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>0.2</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>100</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>1000</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>10000</td>
<td>5000</td>
</tr>
<tr>
<td></td>
<td>1.2K</td>
<td>60000</td>
<td>50000</td>
</tr>
</tbody>
</table>

**Antenna Ratio**

- 0.02 mm (5 mm to 1 line)
- 0.2 mm (5 mm to 1 line)
- 2 mm (5 mm to 10 lines)
- 20 mm (5 mm to 100 lines)
- 200 mm (5 mm to 1000 lines)
- 1.2 km (5 mm to 6000 lines)

**Top View**

**Gate Edge on Field**

**Antenna**

**COMB**

**Pad**

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300mm-Wafer Shot Layout

Number of Chips

168

Chip Size

X:19.6mm
Y:19.4mm
Philtech Charge-up Monitor  TEG-2

Providing TEG Structure

- TEG for: Gate etching, Ashing
- CVD, PVD, Ion-Impla, Cleaning
- Contact etching, Ashing (Available on request)

*Gate Oxide Thickness Option Available (usual 4nm)

Measurement Service

- I-V Characteristics on Antenna Ratio
- Breakdown-Voltage Map Across the Wafer

*Measurement Option (Condition, point etc.), Consulting Available

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300mm Wafer 1st Trial Lot Results-1

**Bulk Wafer, Poly Etcher A**

**Gate Oxide 3nm**

**Gate Oxide 4nm**

**Antenna Ratio:** 10K 100K 1M
300mm Wafer 1st Trial Lot Results-2

Gate Oxide 4nm I-V Characteristics

Bulk Wafer, Poly Etcher : A

Bulk Wafer, Poly Etcher : B

Antenna Ratio : 10K 100K 1M
300mm Wafer 1st Trial Lot Results-2

Gate Oxide 4nm Breakdown-Voltage Map (1E-6A)

Bulk Wafer, Poly Etcher: A

Bulk Wafer, Poly Etcher: B

Antenna Ratio: 10K 100K 1M
300mm Wafer 2nd-Trial Lot Results

Gate Oxide 4nm I-V Characteristics

Bulk Wafer, Poly Etcher: A

Epi Wafer, Poly Etcher: B

Antenna Ratio: 10K 100K 1M
300mm Wafer 2nd-Trial Lot Results

Gate Oxide 4nm Breakdown-Voltage Map (1E-6A)

Bulk Wafer, Poly Etcher : A

Epi Wafer, Poly Etcher : B

Antenna Ratio : 10K 100K 1M
300mm Wafer 3rd-Trial Lot Results

Gate Oxide 4nm  I-V Characteristics

Epi Wafer, Poly Etcher C

Breakdown-Voltage Map (1E-6A)

Antenna Ratio: 10K 100K 1M
300mm Application Example-1: PE-CVD

Gate Oxide 4nm  I-V Characteristics

Epi Wafer, Poly Etcher B

Breakdown-Voltage Map (1E-6A)

Antenna Ratio: 10K  100K  1M
300mm Application Example-2: Ion-Implant

Gate Oxide 4nm I-V Characteristics

Epi Wafer, Poly Etcher C

Breakdown-Voltage Map(1E-6A)

Antenna Ratio: 10K 100K 1M
Philtech charge-up monitor TEG Service

Providing Test Wafers

- Wafer structures available on processes
- Delivery: ~3 weeks

Measurement Service

- I-V Characteristics on Antenna Ratio
- Breakdown-Voltage Map Across the Wafer
  * Measurement option Available (Condition, point etc.)
- Delivery: ~1 week (after wafer returned)

Cost (Included measurement service)

- Cost depends on wafer structures.
  Please contact to Philtech
Philtech has developed 300mm Charge-up Monitor TEG.

1st, and 2nd Trial Lot results indicate the split I-V Characteristics within wafer. These come from Bulk-Wafer crystal defect, or no-fitting Etching Process.

3rd Trial Lot results indicate the no-split (improved) I-V Characteristics by optimizing Etching process. (Etcher-C)

Philtech test wafers are provided to evaluate some processes Etching, PE-CVD, Ion-Implant, Etc., Those data prove Philtech wafers are effective on damage evaluation.

Philtech test wafers are very helpful to develop equipments and processes for 300mm wafers.