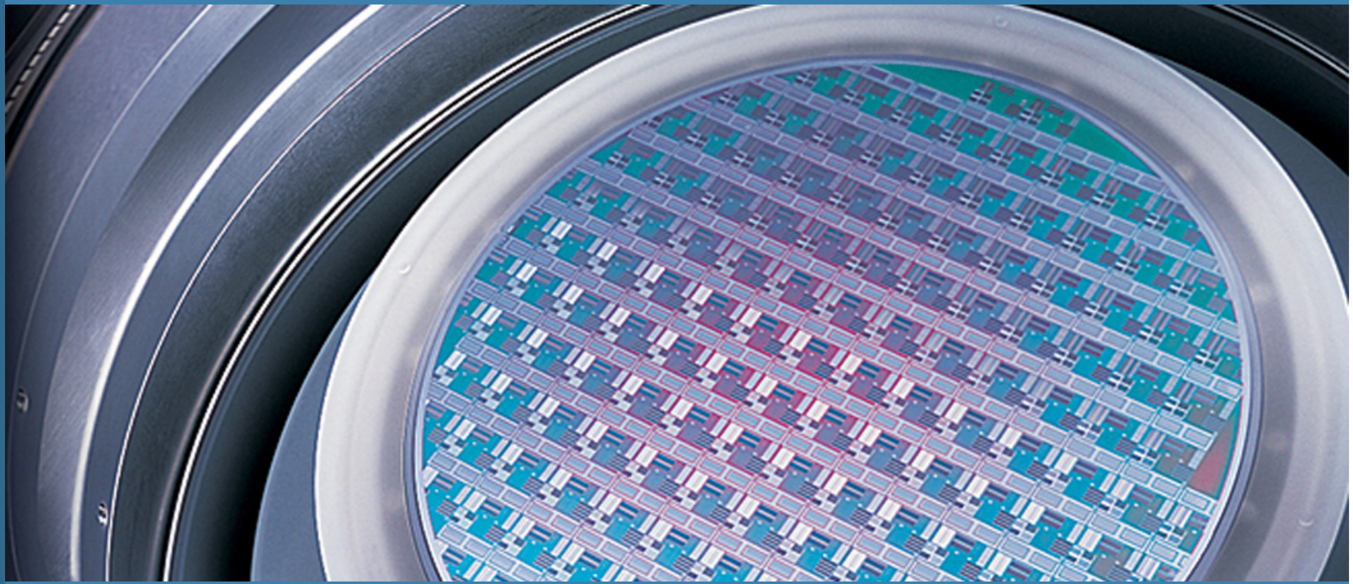
Etch Product Business Group



Minimizing Plasma-Induced Charging Damage during Multi-Step Etching of Dual-Damascene Trench and Via Structures with Process Optimization

M. Kutney, S. Ma, D. Buchberger, A. Zhao, G. Delgadino, D. Hoffman, and K. Horioka*

Etch Product Business Group, Dielectric Etch Div.

***Applied Materials, Inc., Japan**

External Use

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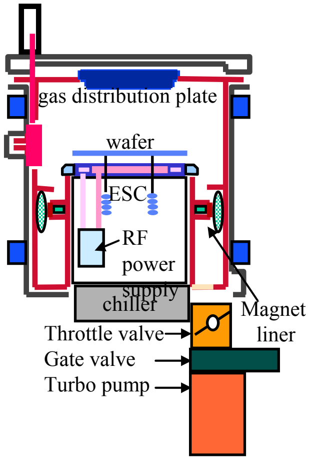
Introduction and Objectives

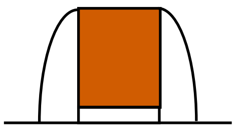
- Plasma-induced charging effects are
  - Influenced by plasma stability and uniformity
  - Strong functions of chamber design and process conditions
- The role of plasma stability can be examined using multiple charging-sensitive electrical test structures
  - EEPROM-based sensors
  - Metal-gate and poly-gate antenna structures
- Identify the risk factors that contribute to charging effects in a very-high-frequency capacitively coupled (VHF CCP) dielectric etcher
- Factors related to plasma uniformity and stability were studied in the VHF CCP Centura® Enabler® dielectric-etch chamber
  - Designed for all-in-one processing of sub-65 nm dual-damascene structures

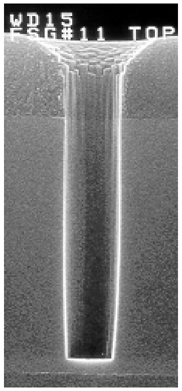
Plasma Charging Damage – Responsible Groups



Hardware
- chamber
- power source
- cathode
- process kit

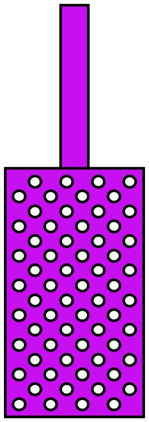
Device
- scaling
- integration
- reliability
- testing method





Process
- profile
- uniformity
- selectivity
- sequence

Layout
- design rule
- die stepping
- alignment mark
- edge exclusion

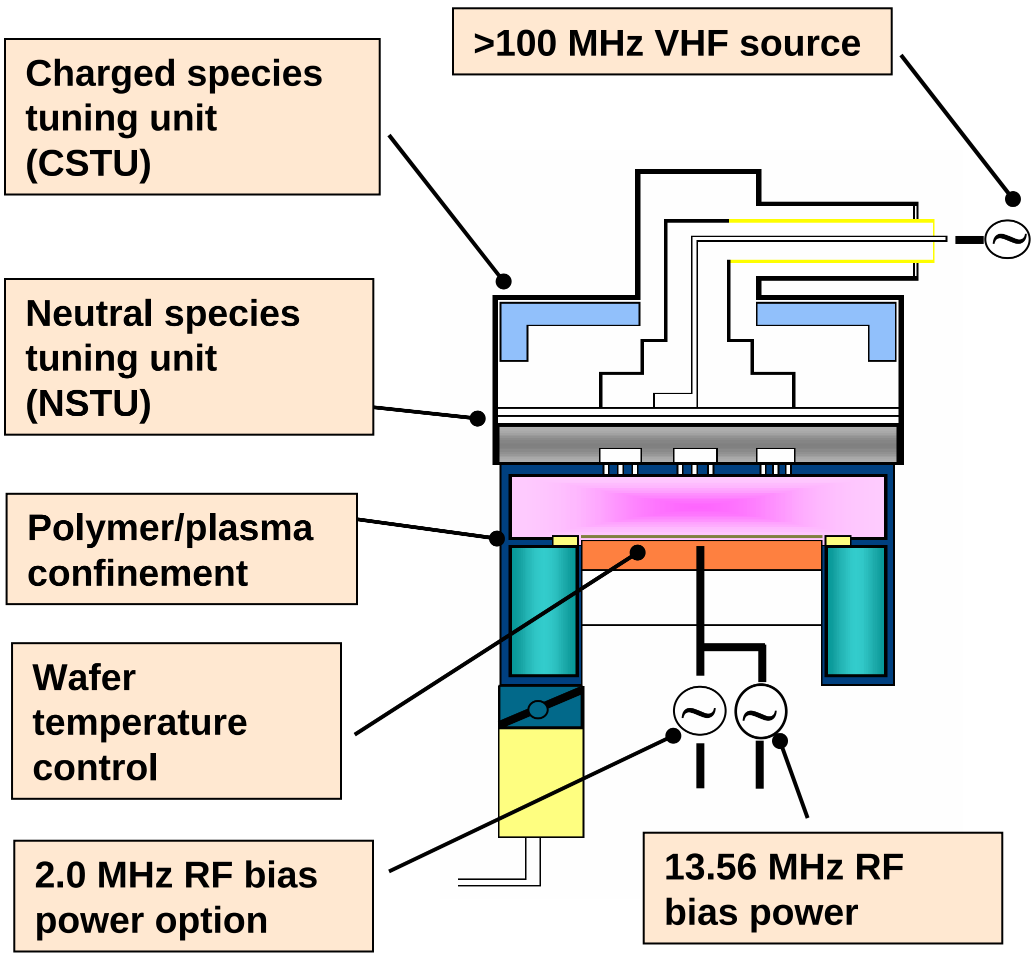


- Four different groups influence the plasma-charging-damage risk
- Understanding all of the group details is challenging

Available Plasma-Damage Characterization Tools

- Device Characterization
  - 200 mm CHARM®-2 wafers: reprogrammable EEPROM wafer
    - Measures threshold-voltage shifts following plasma exposure on various antenna EEPROM structures
    - Local peak voltages and currents are then determined
  - 200 & 300 mm MOS antenna capacitor & transistor wafers
    - Widely accepted in industry for plasma-damage characterization
    - **Difficult and expensive for equipment vendors to acquire, especially 300 mm!!**
- Surface-Charge Characterization
  - 200 & 300 mm Contact Potential Difference (CPD)
    - Measures residue charge before and after plasma exposure on blanket 1kÅ thermal oxide wafers
    - Incompatible for oxide-etching chemistries
- Chamber Characterization
  - Langmuir probe: measures plasma density
    - Plasma density does not necessarily correlate to real plasma damage
    - Cannot be used for every process condition
  - V_{DC} cathode: special cathode for V_{DC} uniformity measurement
    - Measure Vdc at different location and use ΔV_{DC} to relate to damage

300 mm Enabler® Dielectric Etch Chamber Overview

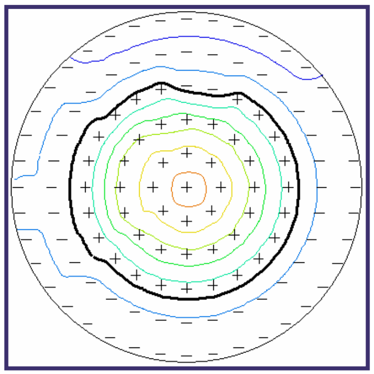


- Very high frequency source (>100MHz) allows very low DC bias etching and ashing capabilities
- Controllable plasma density and neutral dissociation for different etching applications
- Two additional knobs – CSTU (magnetic field) and NSTU (gas distribution) to tune etch rate and CD uniformities
- Very wide, easily tunable and usable operating windows
- Ion Energy Distribution control with dual bias RF

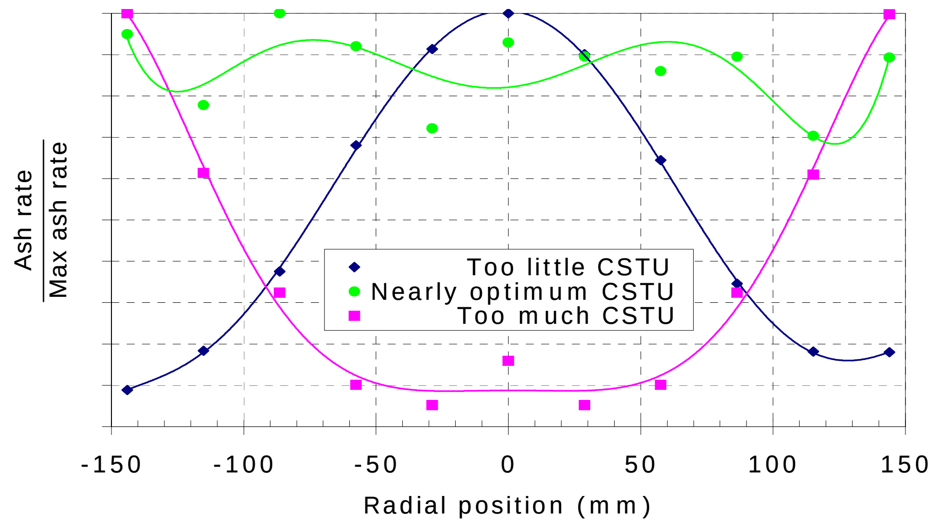
Process Risk #1 – Excessive Magnetic-Field Strength

- As the CSTU value exceeds the optimum setpoint for a process, the plasma and the etch rate become non-uniform

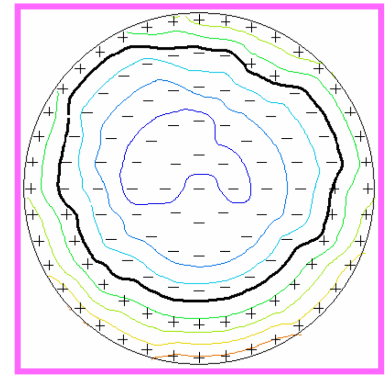
Too little CSTU



Center fast ER

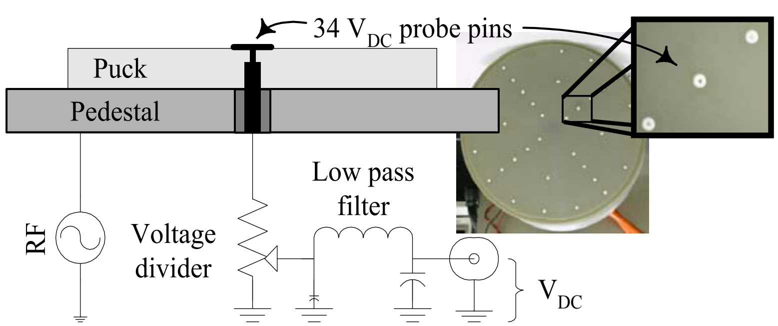


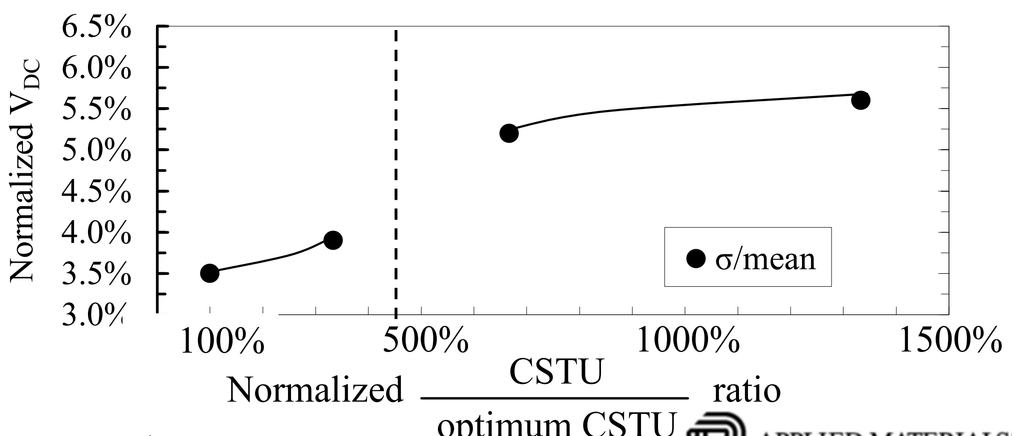
Too much CSTU



Center slow ER

VDC diagnostic cathode



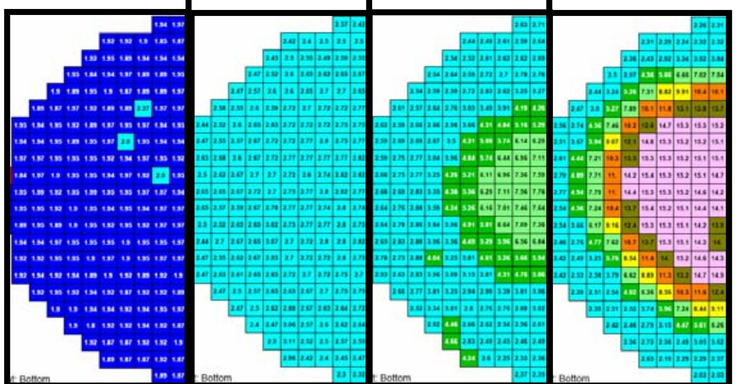


Process Risk #1 – Excessive Magnetic-Field Strength

- As the CSTU value exceeds the optimum setpoint for a process, the risk of plasma-induced charging damage grows

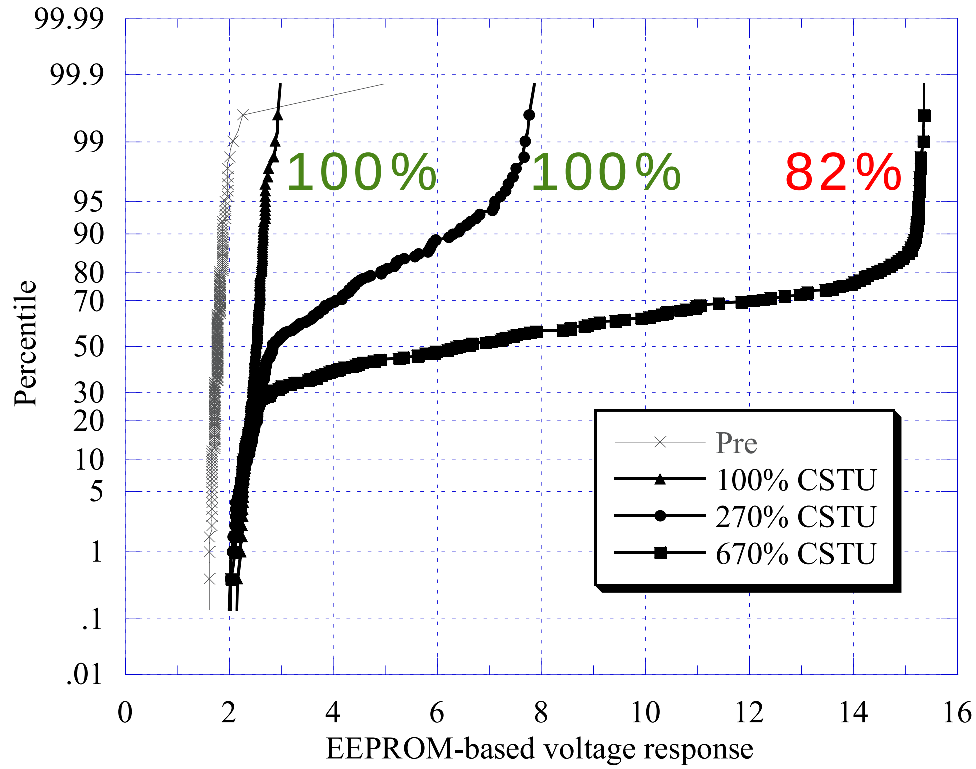
200 mm EEPROM-based voltage
versus normalized CSTU

Pre | 100% | 270% | 670%



100% | 100% | 100% | 82%

Logic customer's poly-gate MOS capacitor voltage-breakdown yield



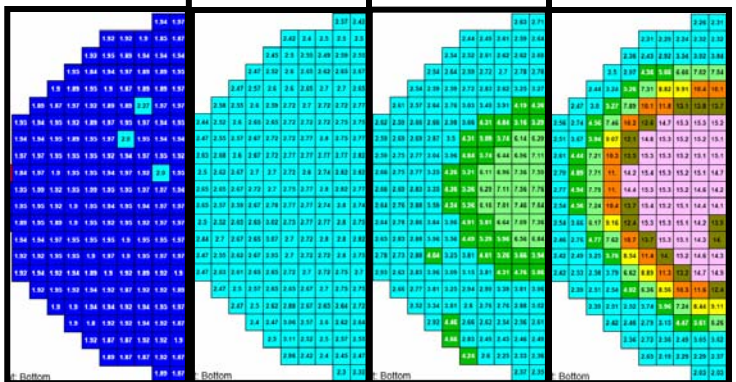
Ref: www.charm-2.com

Process Risk #1 – Excessive Magnetic-Field Strength

- As the CSTU value exceeds the optimum setpoint for a process, the risk of plasma-induced charging damage grows

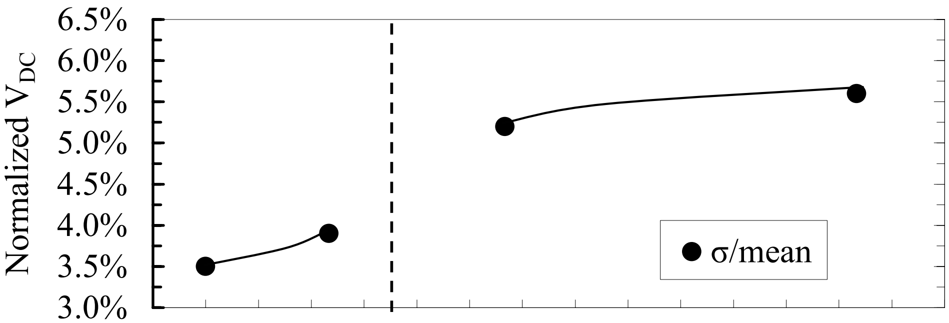
200 mm EEPROM voltage versus normalized CSTU

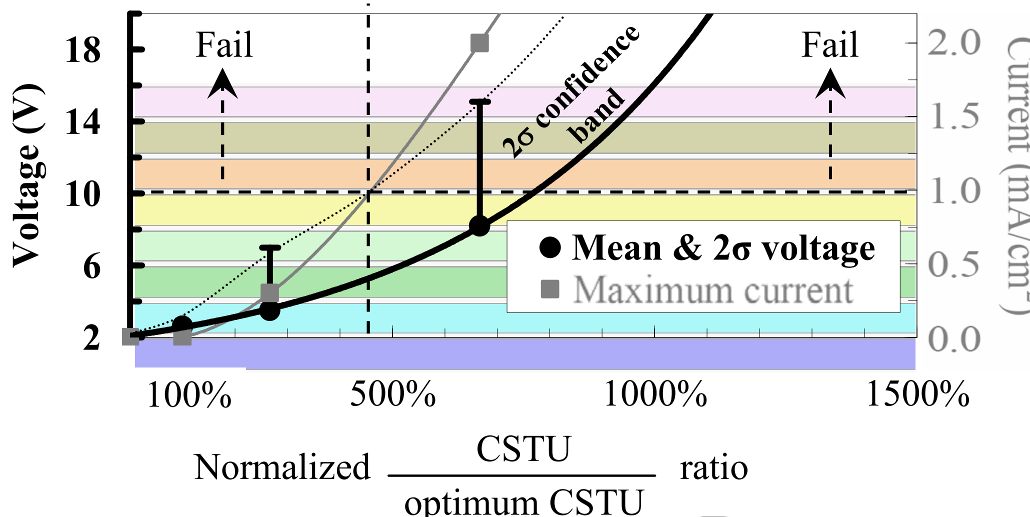
Pre	100%	270%	670%



100%	100%	100%	82%

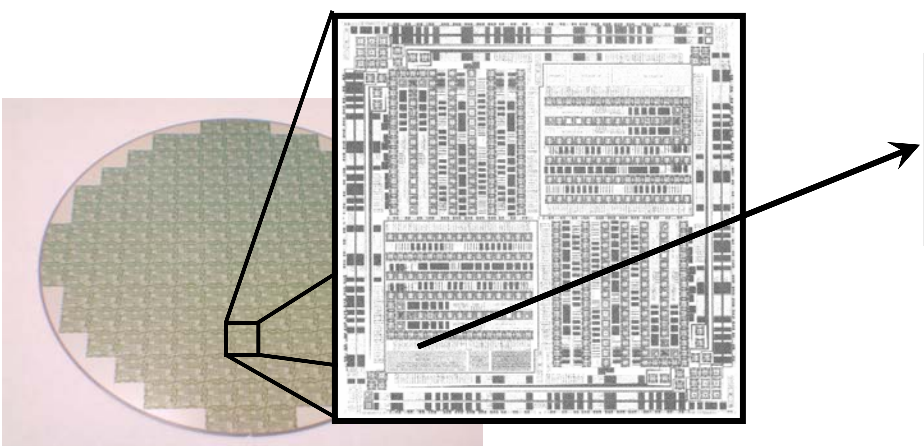
Logic customer's poly-gate MOS capacitor voltage-breakdown yield



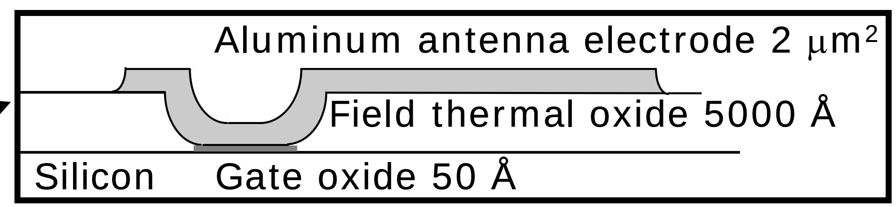


Simplified Antenna MOS Capacitor Structure: SPIDER (SPIDER Systems, Inc)

- Bare metal-gate antenna MOS capacitor structure for plasma-charging-damage evaluation (Ref: IEEE TED, **45(3)**, p.722, 1998)
- Short-flow plasma charging damage test: gate leakage current
  - Two terminals: plasma-exposed Al pad & Si substrate backside
  - Metal gate is directly on top of gate oxide and has various areas
  - Sensitive to plasma charging damage to every part of the process
  - Measure leakage before & immediately after plasma exposure
  - Cannot detect electron-shading effect



SPIDER structure



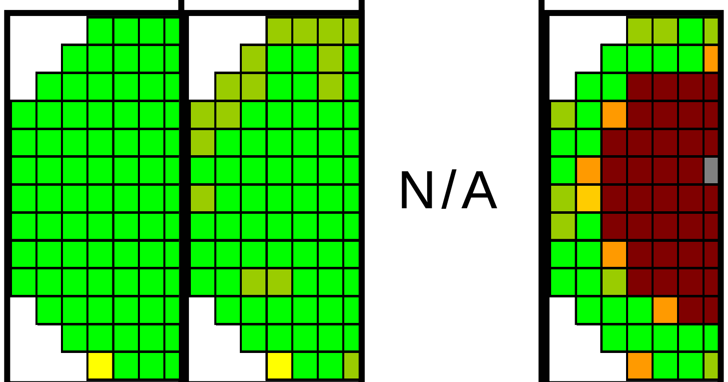
- Pre-leakage should be <0.1 nA
- σ = ±5% accuracy
- Pass criteria = ≥95% at 1 nA

Process Risk #1 – Excessive Magnetic-Field Strength

- As the CSTU value exceeds the optimum setpoint for a process, the risk of plasma-induced charging damage grows

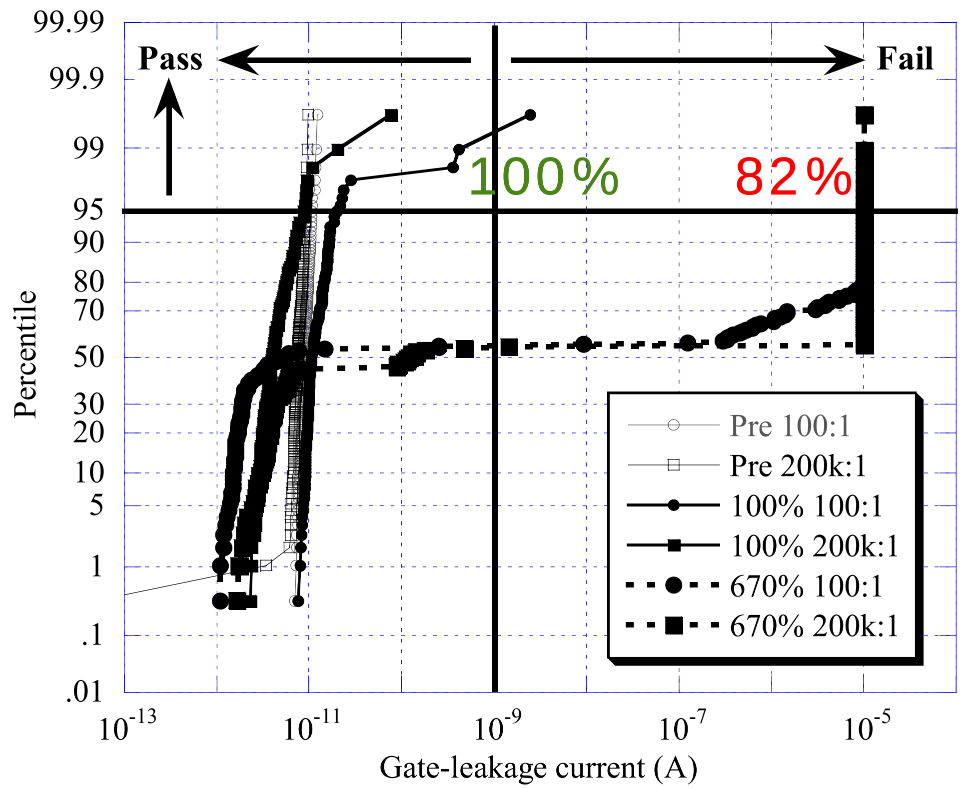
300 mm metal-gate leakage current
versus normalized CSTU

Pre	100%	270%	670%



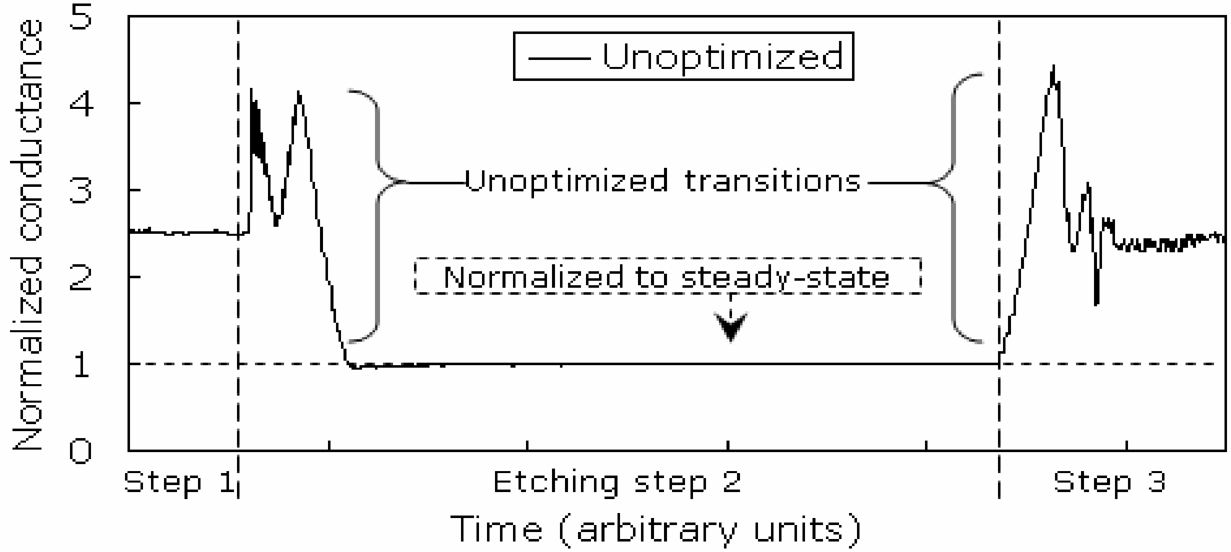
100%	100%	100%	82%

Logic customer's poly-gate MOS capacitor voltage-breakdown yield
(200k:1 antenna ratio)



Process Risk #2 – Unstable Plasma during Transitions

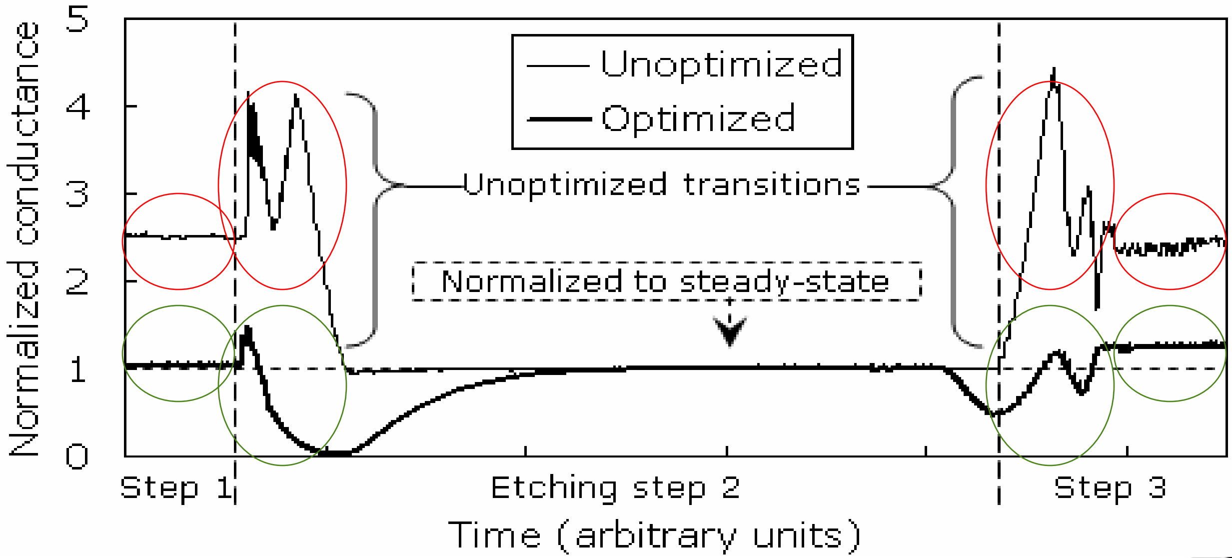
- Often, many process parameters are changed between steps
  - For example, bias & source powers, pressure, CSTU, & chemistry
  - Linearly ramped to new set points or without any control
  - Simultaneously changed at the beginning of each step with varying rates
- Unoptimized transitions increase the plasma-damage risk
  - Plasma is unstable as it undergoes significant distribution, density, and energy changes
- Plasma changes can be represented by plasma conductance
  - Characterizes the energy allowed to flow through the plasma



Process Risk #2 – Unstable Plasma during Transitions

- **Unoptimized transitions have**
  - **Significant plasma conductance changes during transitions to and from the steady-state step-2 etching condition**
  - **Plasma conductance before and after step 2 also deviate**

- **Optimized transitions have**
  - **Significantly less plasma conductance change**
  - **Plasma conductance before and after step 2 deviate less than the steady-state step-2 value**

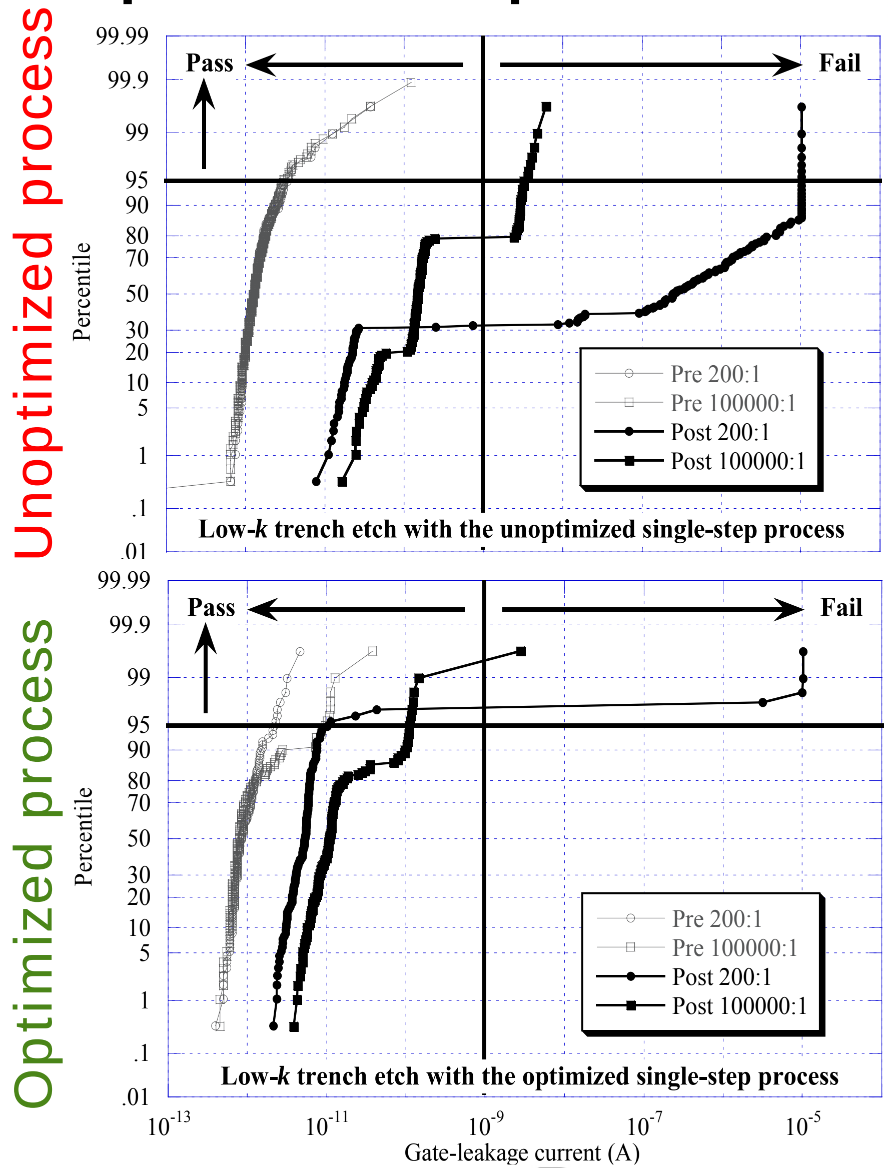


MOS Gate-Leakage Yields for Unoptimized & Optimized Low-κ Single-Step Etching

- 300 mm MOS metal-gate-leakage currents verify risk:
- Unoptimized does not pass
- Optimized does pass

- Logic customer's MOS poly-gate-breakdown-voltage yield also validate:
- Unoptimized: 88% & 37%
- Optimized: 100% & 100%

1k:1 100k:1



Plasma-Induced Charging-Damage Results for Single- and Multi-Step Processes before and after Optimization

Data that meet the threshold specifications and customer criteria are bolded,
while data that do not meet are not

Measurement:	300 mm metal-gate MOS cap. leakage-current yield		200 mm EEPROM-based voltage and current sensors			200 & 300 mm poly-gate MOS cap. voltage-breakdown yield	
	200:1	100k:1	$+V_{mean}$ & $+V_{95\%}$	$-V_{mean}$ & $-V_{95\%}$	$+I_{max}$ & $-I_{min}$	1k:1	100k:1
Passing specification:	≥95% @1 nA (σ±5%)		$\lvert V_{mean}\rvert < 5$ V & $\lvert V_{95\%}\rvert < 10$ V		$\lvert I\rvert <$ 1 mA/cm^2	100%	100%
Pre-measure control	**100%**	**100%**	**~2 & ~2**	**~−2 &−2**	**+0.0 & −0.0**	**100%**	**100%**
Unoptimized single step	79.1%	32.1%	6 & 10	−2 & −6	+2.0 & −0.9	88%	37%
Optimized single step	**97.1%**	**99.5%**	**3 & 5**	**−2 & −4**	**+0.6 & −0.3**	**100%**	**100%**
Unoptimized multiple step	N/A	N/A	10 & 14	−6 & −10	+11.0 & −2.0	N/A	N/A
Optimized multiple step	**N/A**	**N/A**	**4 & 5**	**−2 & −5**	**+0.9 & −0.2**	**100%**	**100%**

- **By optimizing the process, the plasma-damage risk is significantly reduced**

Conclusions

- Two risk factors that contribute to plasma-induced-charging sensitivity in a VHF CCP have been identified
  - Excessive magnetic fields generate a larger charge distribution that is conducive to charging damage
    - Can be easily avoided with simple process ground rules
  - Plasma instability can occur during transitions from one plasma state to another
    - By continuously controlling and stabilizing the plasma during a transition, charging effects can be reduced
- Continuous damage-free etch processes can now be developed
  - Etching and ashing of complex multi-layer stacks
  - For example, all-in-one via and trench etching

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