

MEMS Etching Technology

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Intel Corp.

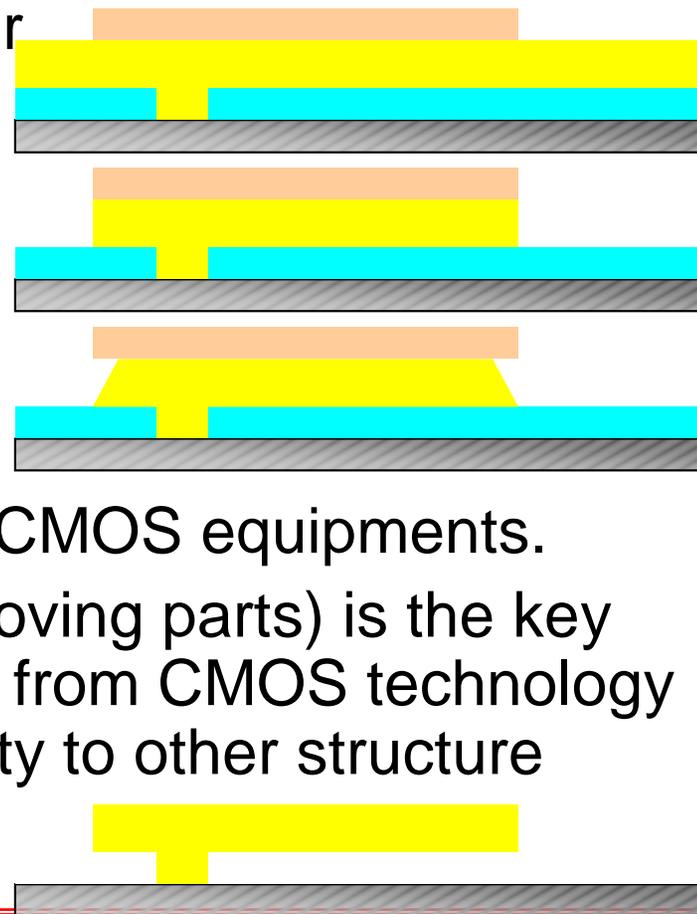
Sep. 9, 2004

Outline

- Overview
- Etching in surface micromachining
- Etching in bulk micromachining
- 3D MEMS etching technology
 - Complex 3D MEMS machinery
 - Through wafer via package
- Summary

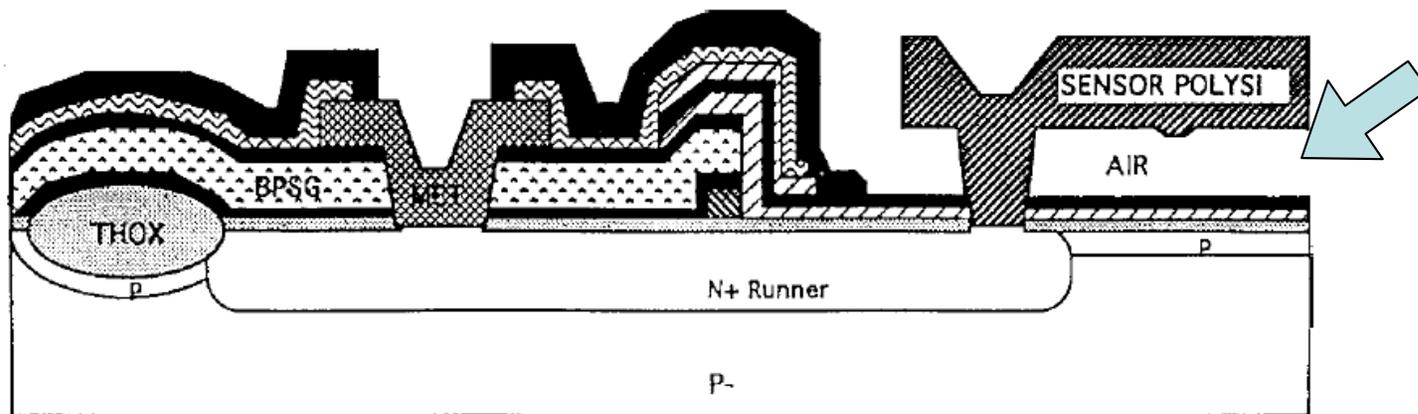
MEMS etching overview

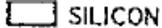
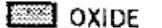
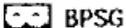
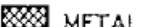
- Then - MEMS etching technology initiated with CMOS etching technology
 - Fundamental pattern transfer
 - Lithography
 - Dry etching
 - Wet etching
 - Can re-use the depreciated CMOS equipments.
 - Final release process (for moving parts) is the key that deviates MEMS etching from CMOS technology (need to have good selectivity to other structure materials)



BiCMOS with surface micromachining

- A standard BiCMOS process follows by a final surface sacrificial layer (e.g., oxide) etching for final structure release



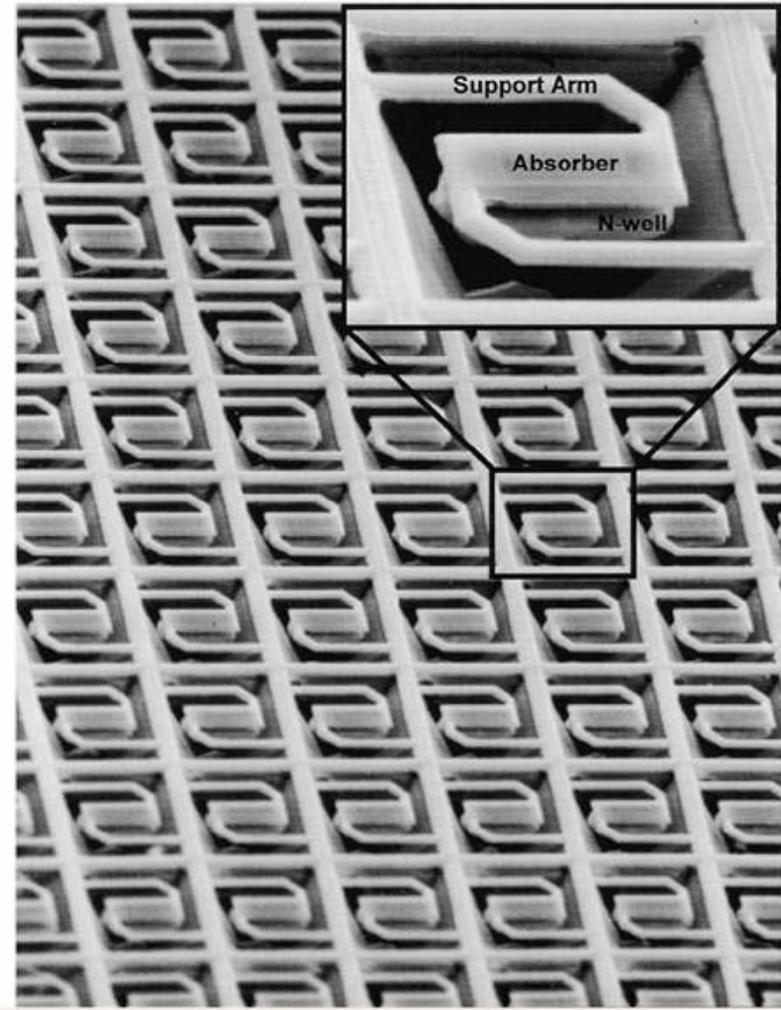
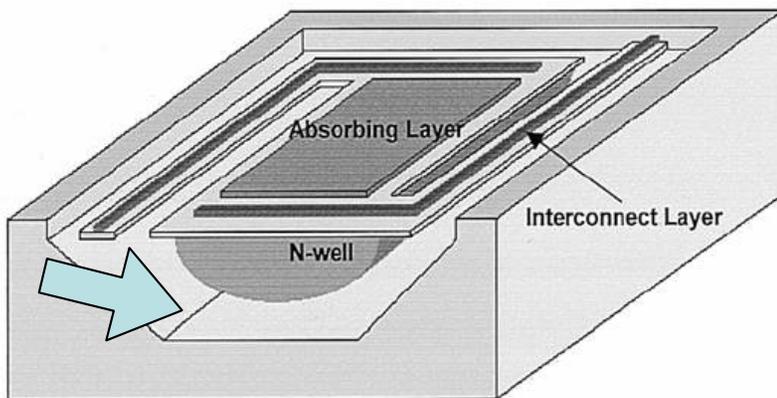
 SILICON	 LPCVD NITRIDE	 SPACER LTO	 PLASMA OXIDE
 OXIDE	 BPSG	 SENSOR POLYSI	 PLASMA NITRIDE
 POLYSI	 LTO	 METAL	

Analog Devices BiMEMS integrated MEMS technology.

Core et al., *Solid State Technol.*, 1993.

CMOS with bulk micromachining

- An infrared detector with standard CMOS process follows by a final bulk silicon etching for final structure release



Tezcan et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, 2003

MEMS etching overview

- Now and future – Complex MEMS structures and etching technology have advanced beyond CMOS
 - MEMS structures are not limited by simple surface or bulk micromachining etch step
 - Deep wafer etching becomes popular
 - Etching technology in MEMS diversifies MEMS into complex 3D structures
 - CMOS related process starts to use MEMS etching technique
 - Final release etching remains the key in MEMS process technology (need to have good selectivity to other structure materials)

Outline

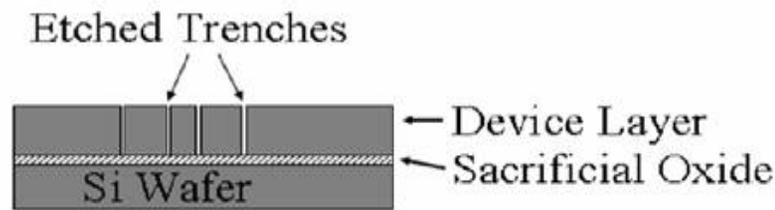
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Etching in Surface Micromachining

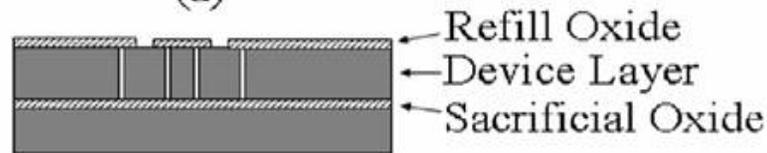
- Etching to produce MEMS pattern as standard CMOS process
- Etching to remove sacrificial material for the MEMS structure release
 - Sacrificial material
 - Oxide – usually used for polysilicon structures (high temp. process).
 - 49% HF (>1um/min)
 - BHF (>0.1um min., depends on deposition of oxide)
 - Vapor HF (very slow ER~350A/min)
 - Metal (low temp. process)
 - Cu with Cu etchant
 - Al with Al etchant
 - Polymer/polyimide/photoresist (low temp. process)
 - Solvent (e.g., Acetone)
 - O₂ plasma
 - Polysilicon (high temp process) - same etching approach as Si bulk etch
 - Si wet etchant
 - SF₆ and XeF₂ dry etchant



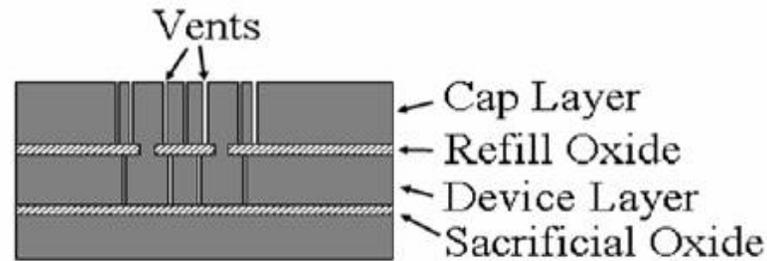
Vapor HF Release



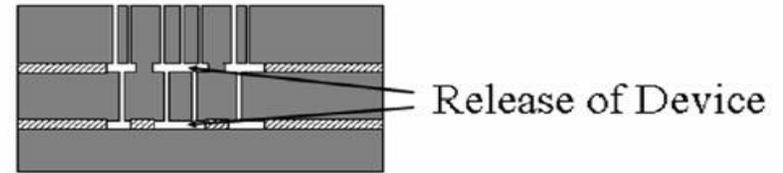
(a)



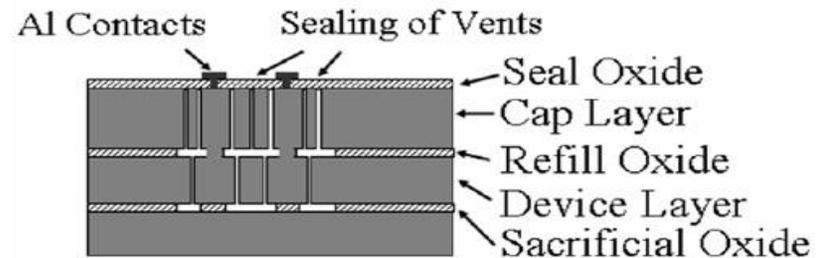
(b)



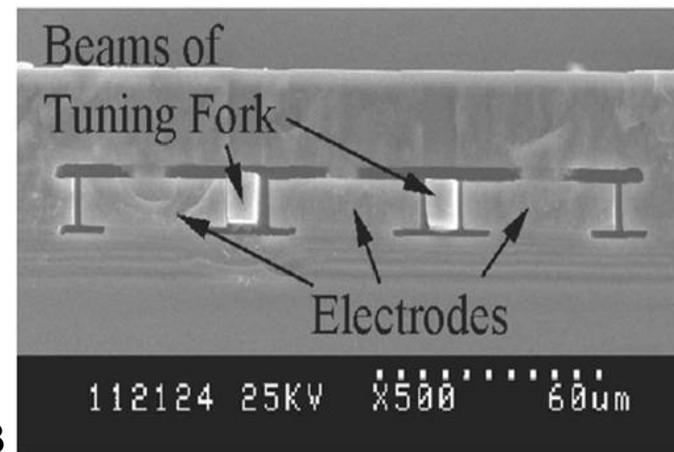
(c)



(d)

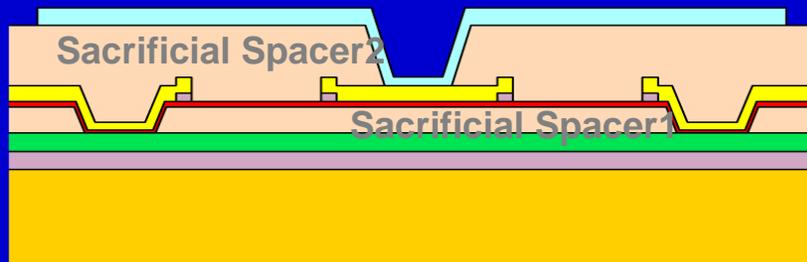


(e)

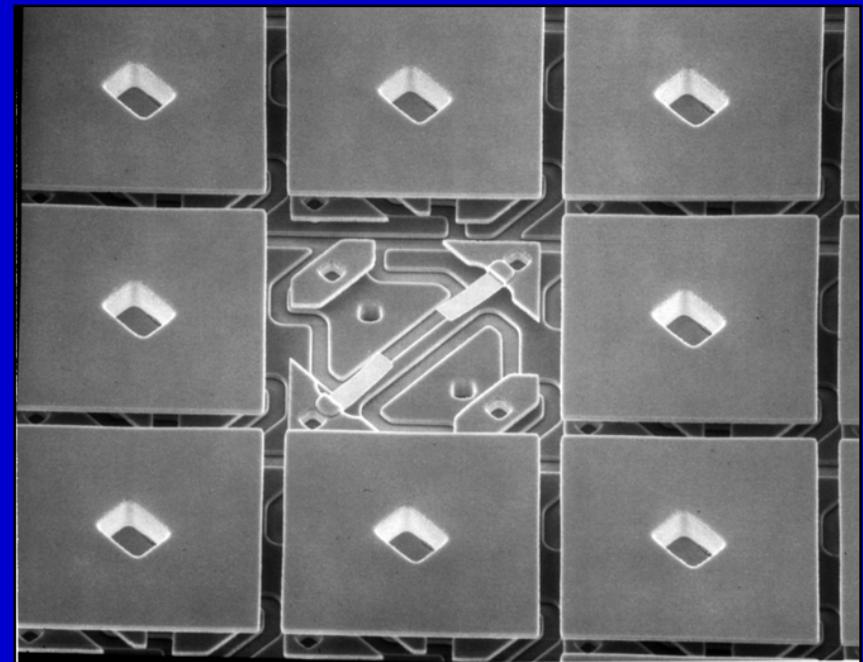
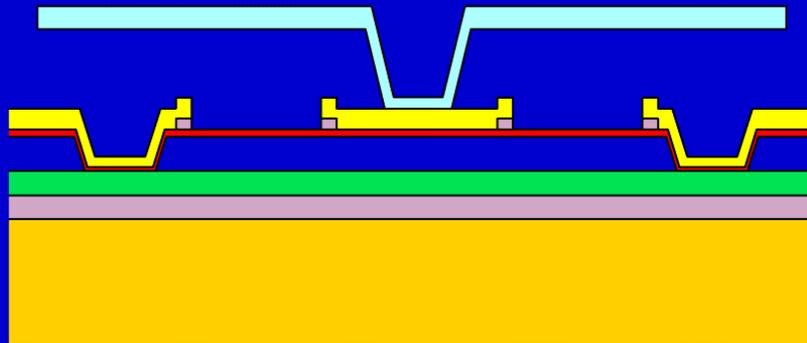


Candler et. al., *IEEE Trans. Advance Packaging*, 2003

Sacrificial polymer etch for surface micromachining



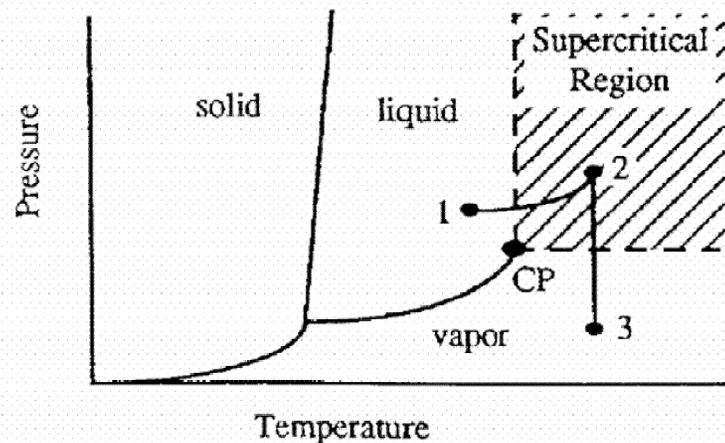
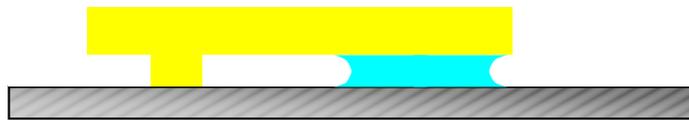
- Plasma release or solvent release with CPD



TI DMD (Digital Micromirror Device)

CPD

- CPD is needed in some MEMS structures due to stiction issue if it is done by wet etch release
- Dry etch release will not need CPD



CP - Critical Point at (P_c, T_c)

G. T. Mulhern et. al., *Transducers'93*

- 1) Exchange methanol with liquid CO₂ (@ ~20C and 1200 psi).
- 1–2) Close off vessel and heat liquid CO₂ to a supercritical fluid. There is no interface formed during this transition.
- 2–3) Vent vessel at a constant temperature above T_c . The CO₂ exists in gaseous form.

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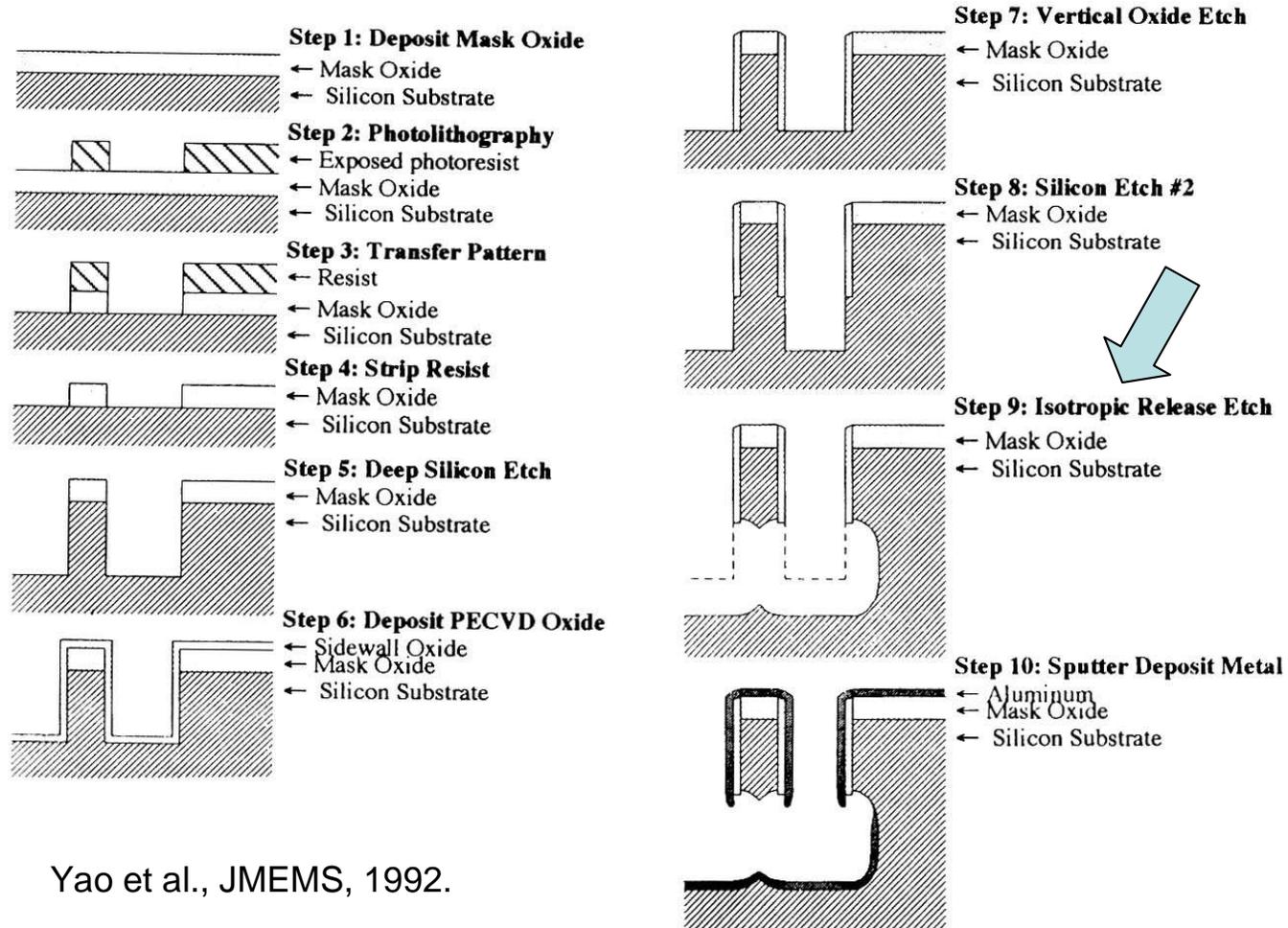
Etching in Bulk microchining

- Si Etch to produce
 - Mold for MEMS structure
 - Si as sacrificial material for structure release
 - Package via
 - Microchannel
- Glass Etch to produce
 - Package cavity, Via
 - Microfluidic channel

Isotropic Si etch

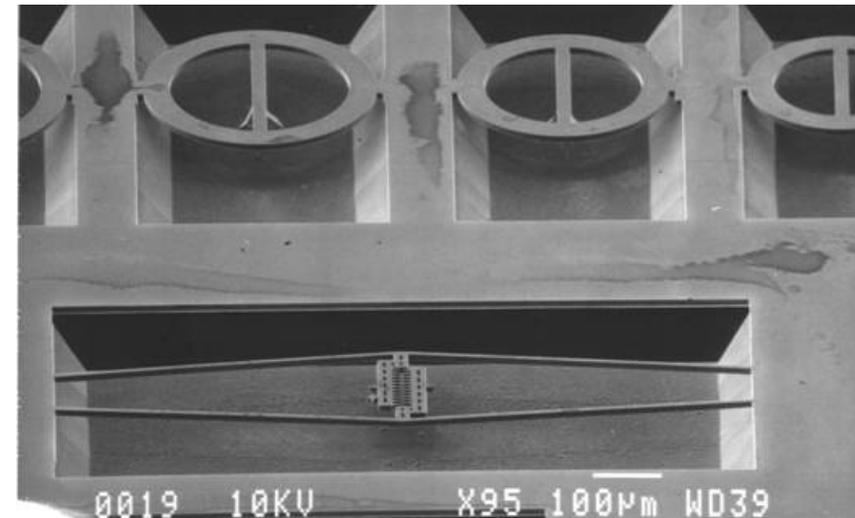
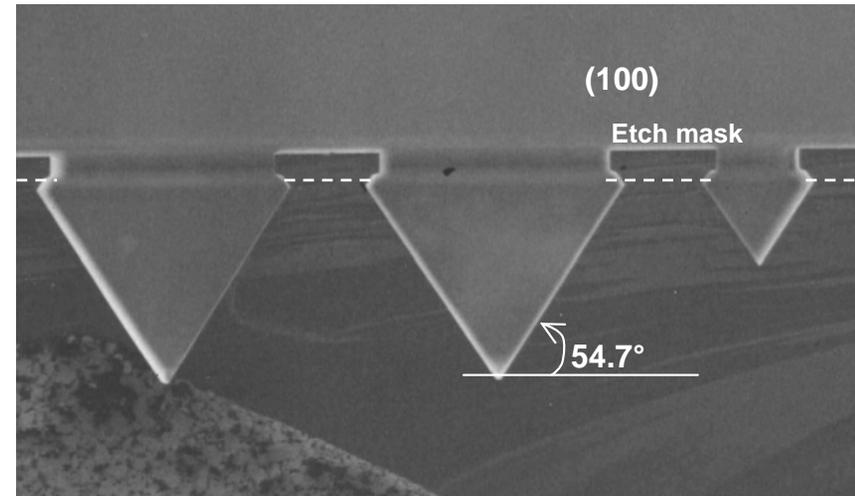
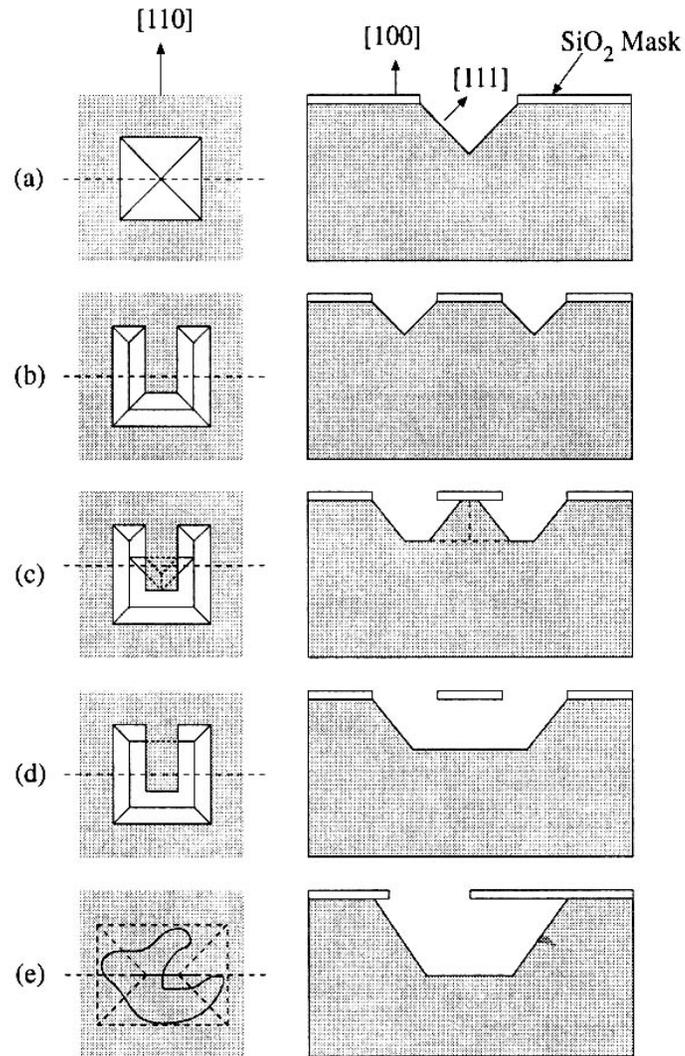
- Wet etch (HNA, hydrofluoric acid, nitric acid, acetic acid)
 - HF+HNO₃+CH₃COOH+H₂O
- Dry etch (usually for final release step)
 - SF₆ RIE
 - Most common dry etch approach for sacrificial Si etch and release
 - XeF₂ – receives attention
 - **$2 \text{XeF}_2 + \text{Si} \rightarrow 2 \text{Xe (g)} + \text{SiF}_4 \text{(g)}$**
 - **Advantages :**
 - Highly selective to silicon with respect to Al, photoresist, and SiO₂.
 - isotropic, large structures can be undercut.
 - Fast (~10μm per hour)
 - Gas phase etching, no stiction between freed structure and substrate

Single Crystal Reactive Etching And Metalization (SCREAM)



Yao et al., JMEMS, 1992.

Si Anisotropic Wet etch



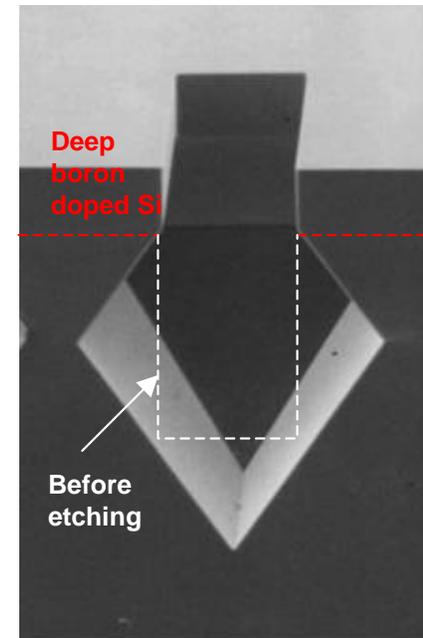
From Micromachined transducers sourcebook by Kovacs

Anisotropic Si etchant

- KOH, EDP, and TMAH are commonly used with SiO₂ as etch mask
- All etchants have good selectivity to heavy boron doped Si
- TMAH is safer and IC compatible with less selectivity to oxide compared to other etchants

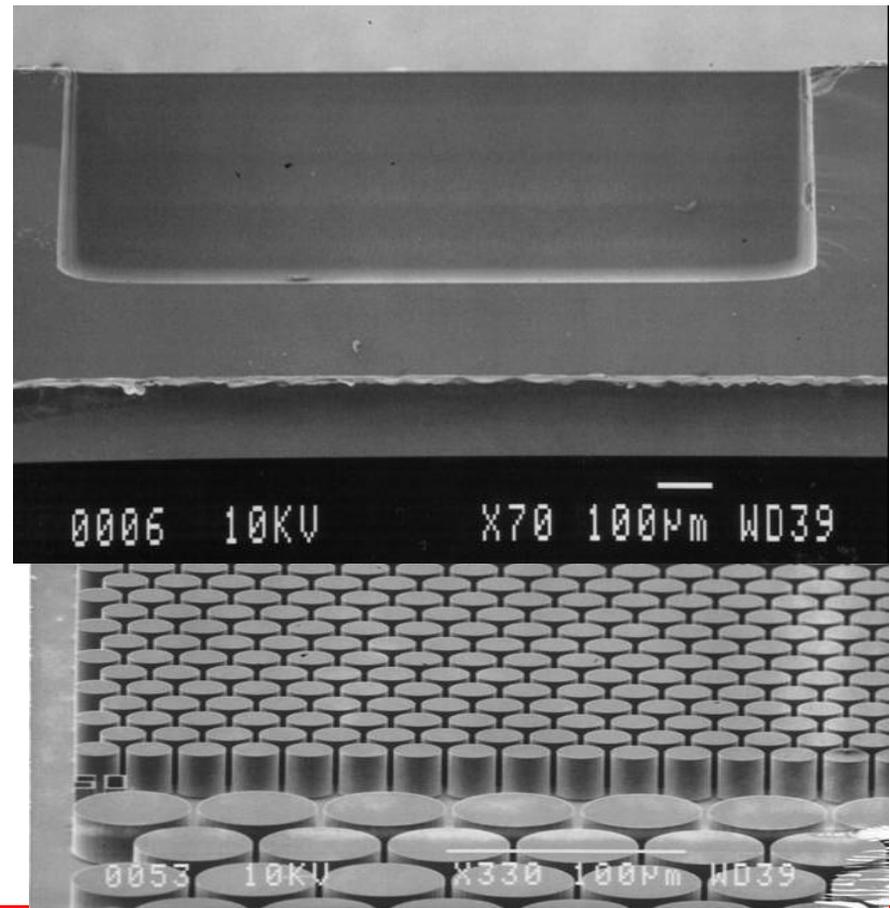
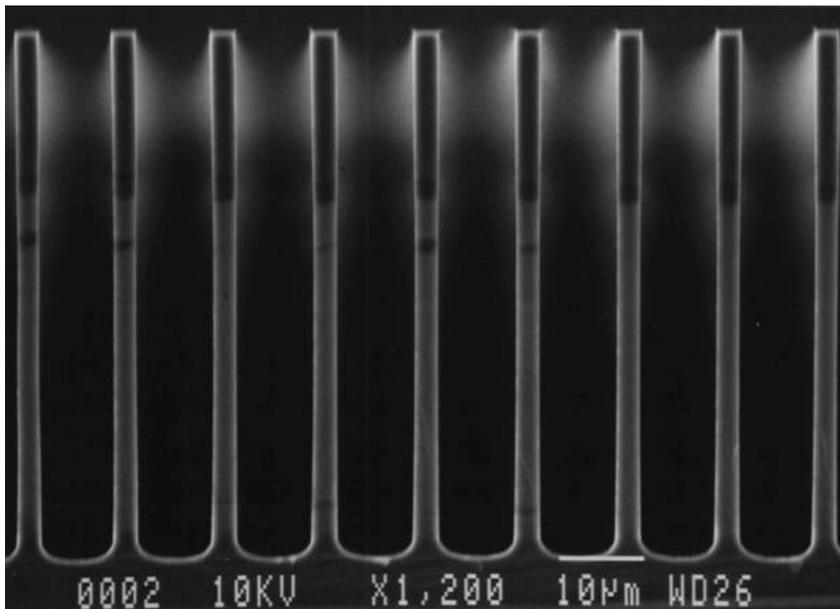
Etchant/Diluent/Additives/ Temperature	Etch Stop	Etch Rate (100) ($\mu\text{m}/\text{min}$)	Etch Rate Ratio (100)/(111)	Remarks	Mask (Etch Rate)
KOH/water, isopropyl alcohol additive, 85°C	$B > 10^{20} \text{ cm}^{-3}$ reduces etch rate by 20	1.4	400 and 600 for (110)/(111)	IC incompatible, avoid eye contact, etches oxide fast, lots of H ₂ bubbles	Photoresist (shallow etch at room temperature); Si ₃ N ₄ (not attacked); SiO ₂ (28 Å/min)
Ethylene diamine pyrocatechol (water), pyrazine additive, 115°C	$\geq 5 \times 10^{19} \text{ cm}^{-3}$ reduces the etch rate by 50	1.25	35	Toxic, ages fast, O ₂ must be excluded, few H ₂ bubbles, silicates may precipitate	SiO ₂ (2-5 Å/min); Si ₃ N ₄ (1 Å/min); Ta, Au, Cr, Ag, Cu
Tetramethyl ammonium hydroxide (TMAH) (water), 90°C	$> 4 \times 10^{20} \text{ cm}^{-3}$ reduces etch rate by 40	1	From 12.5 to 50	IC compatible, easy to handle, smooth surface finish, few studies	SiO ₂ etch rate is 4 orders of magnitude lower than (100) Si LPCVD Si ₃ N ₄
N ₂ H ₄ /(water), isopropyl alcohol, 115°C	$> 1.5 \times 10^{20} \text{ cm}^{-3}$ practically stops the etch	3.0	10	Toxic and explosive, okay at 50% water	SiO ₂ (<2 Å/min) and most metallic films; does not attack Al according to some authors ¹⁰⁴

From Fundamentals of Microfabrication by Madou.

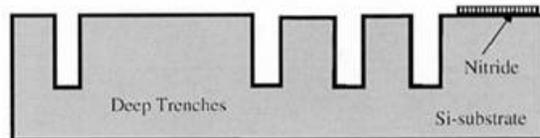


Si DRIE

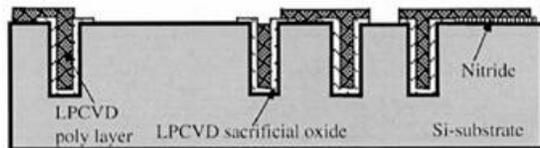
- Bosch passivation/etching process approach
- high aspect ratio Si etching
- Through Si wafer etch with close-to-vertical sidewall
- High etch rate ($>5\mu\text{m}/\text{min.}$) can be achieved but only applies to small exposure area (e.g., $<10\%$)



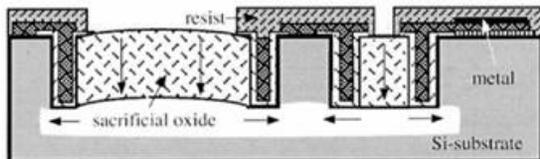
Combination of deep RIE and isotropic Si etch



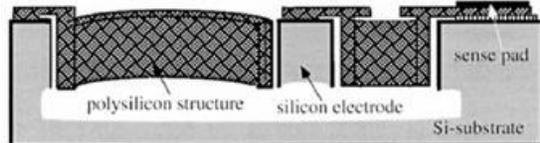
- a) Deposit and pattern the isolating nitride layer;
b) dry etch deep trenches to define the main body structure.



- c) Deposit LPCVD sacrificial oxide and dope surface of the oxide; d) refill trenches with LPCVD polysilicon; e) etch back poly; f) pattern oxide; g) deposit, dope and pattern poly.

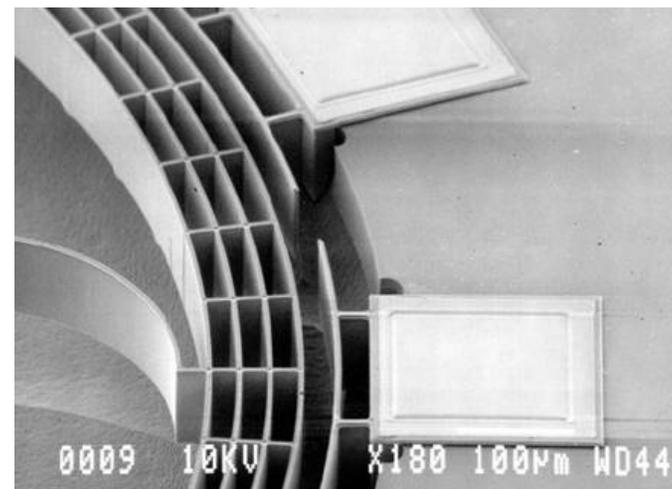
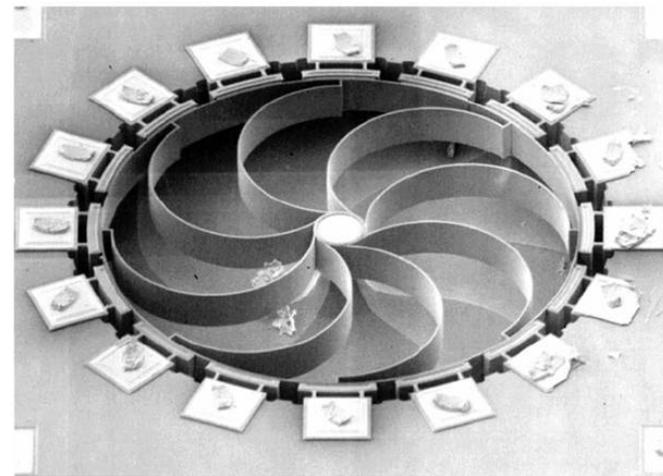


- h) Deposit and pattern Cr/Au; i) SF_6 deep dry directional etch + undercut to release silicon structures/electrodes (thick resist used as a mask);



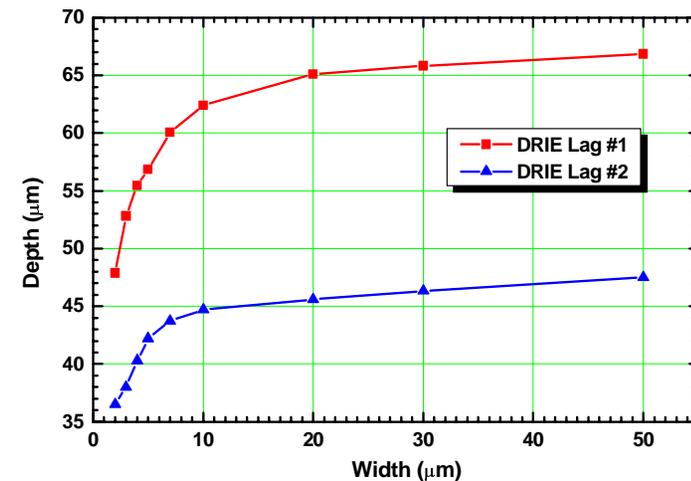
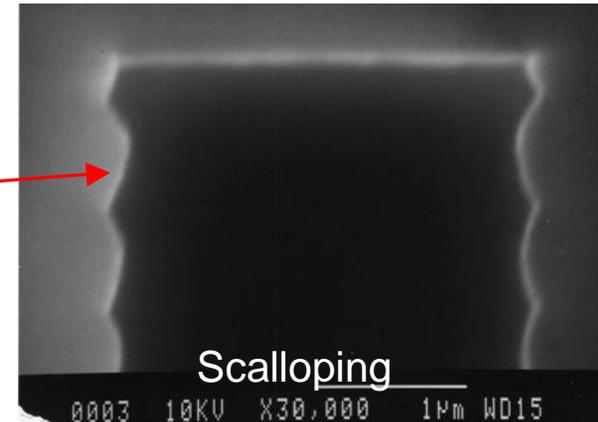
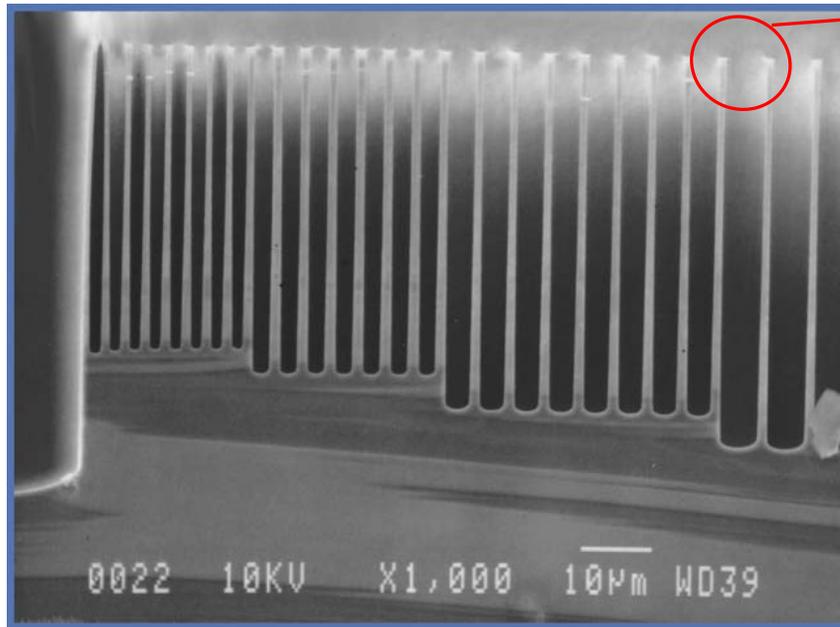
- j) Strip resist; k) etch the sacrificial oxide layer to completely release the structure.

Ayazi et. al., *JMEMS* 2000



DRIE Issue

- Scalloping is common at initial few um of etch
- RIE lag effect arises when aspect ratio $> \sim 2$

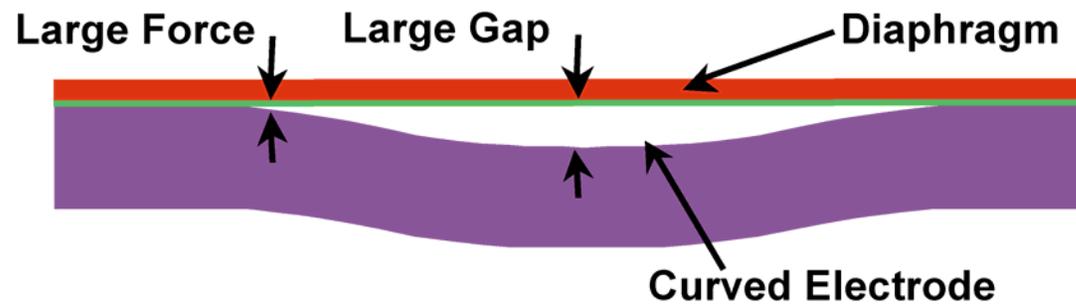
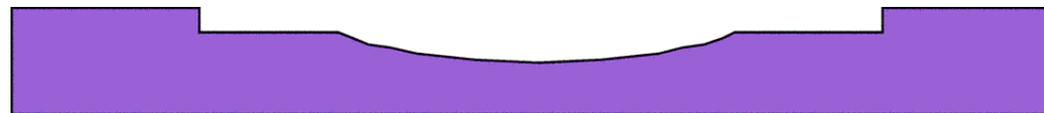


- Loading effect
 - Etching rate reduces drastically with exposure area
 - \rightarrow lower throughput and expensive
- Dielectric charging affect etching direction

RIE for out-of-plane surface

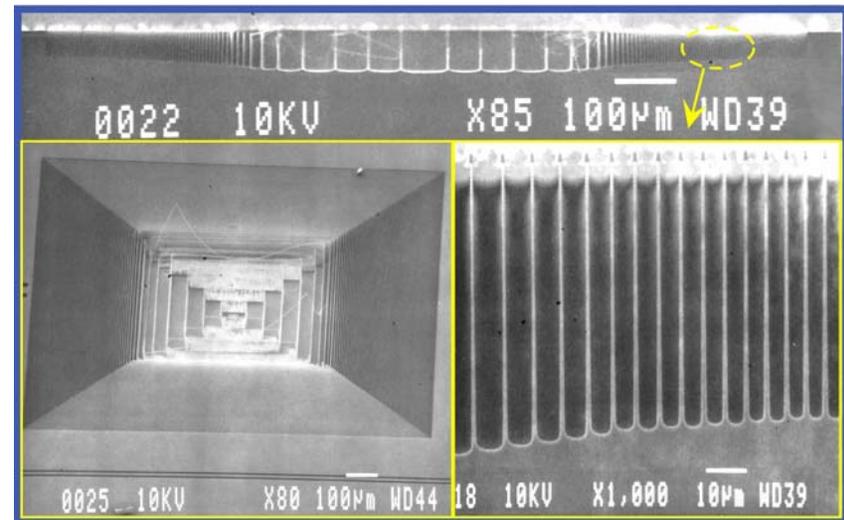
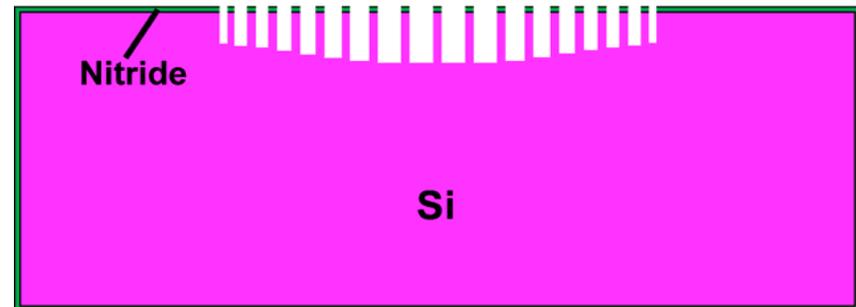
- Turn the con to pro?

Arbitrary curved surface



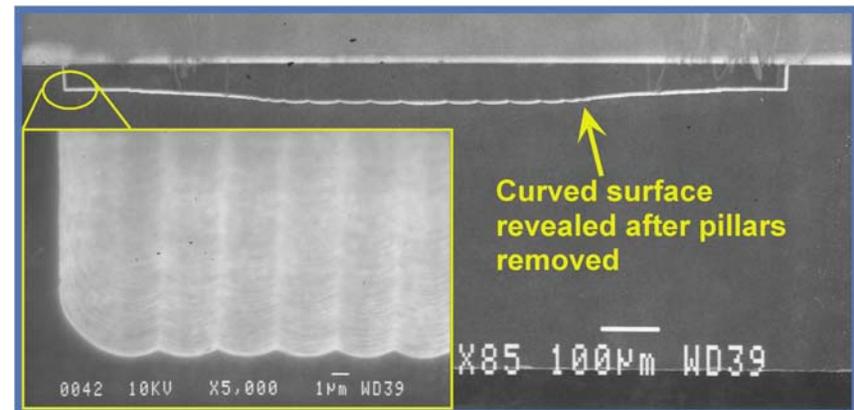
Etching technology for arbitrary out-of-plan surface formation

- (a) Si DRIE etch to create curved bottom profile



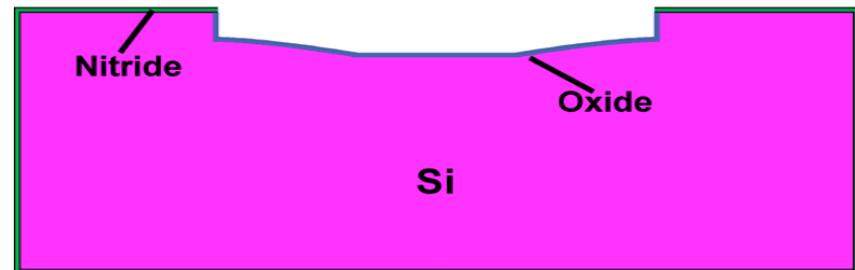
Etching technology for arbitrary out-of-plan surface formation

- (b) Isotropic Si etch to remove pillars



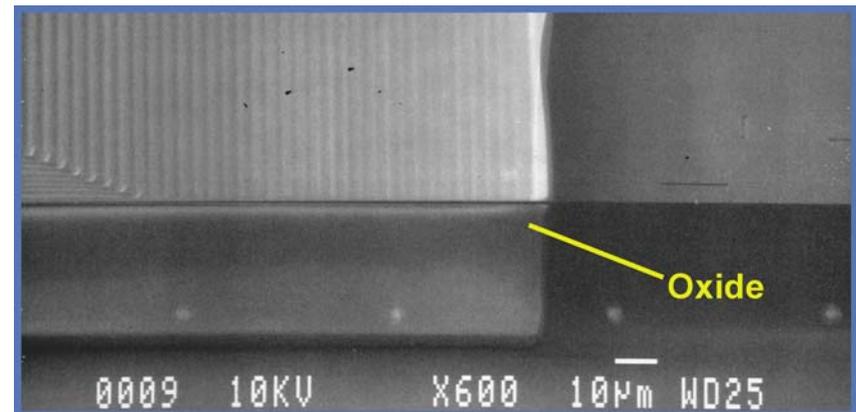
Etching technology for arbitrary out-of-plan surface formation

- (c) Thermal Oxidation to smoothen surface



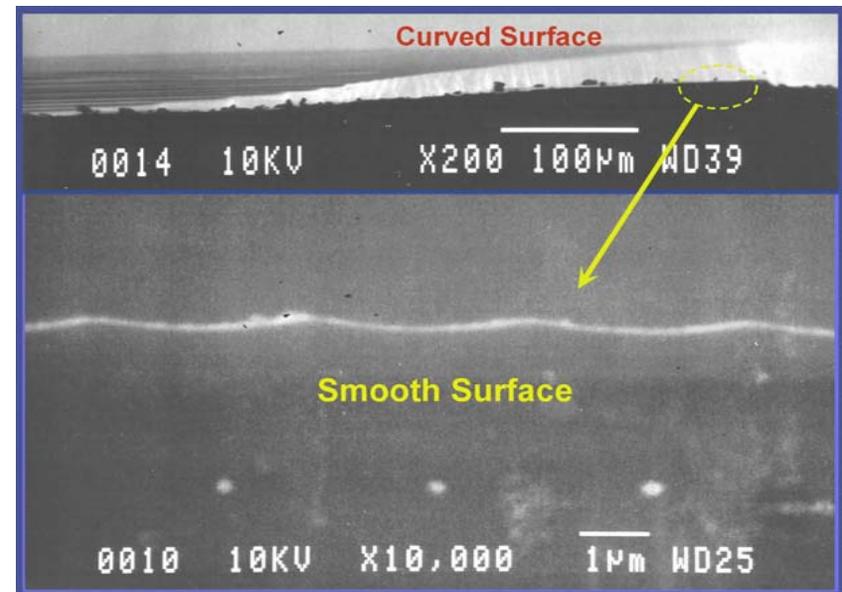
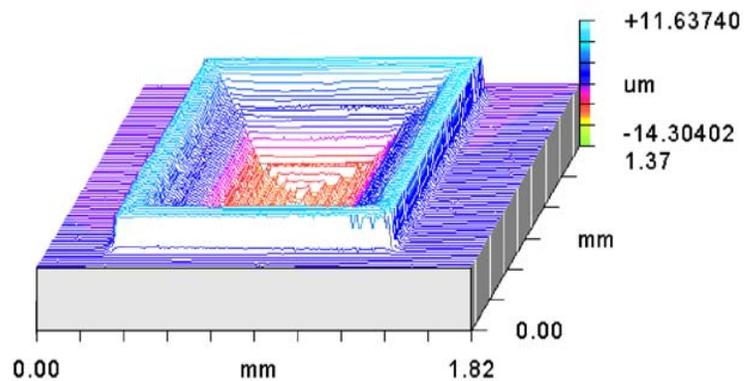
Etching technology for arbitrary out-of-plan surface formation

- (d) Maskless field Si etch

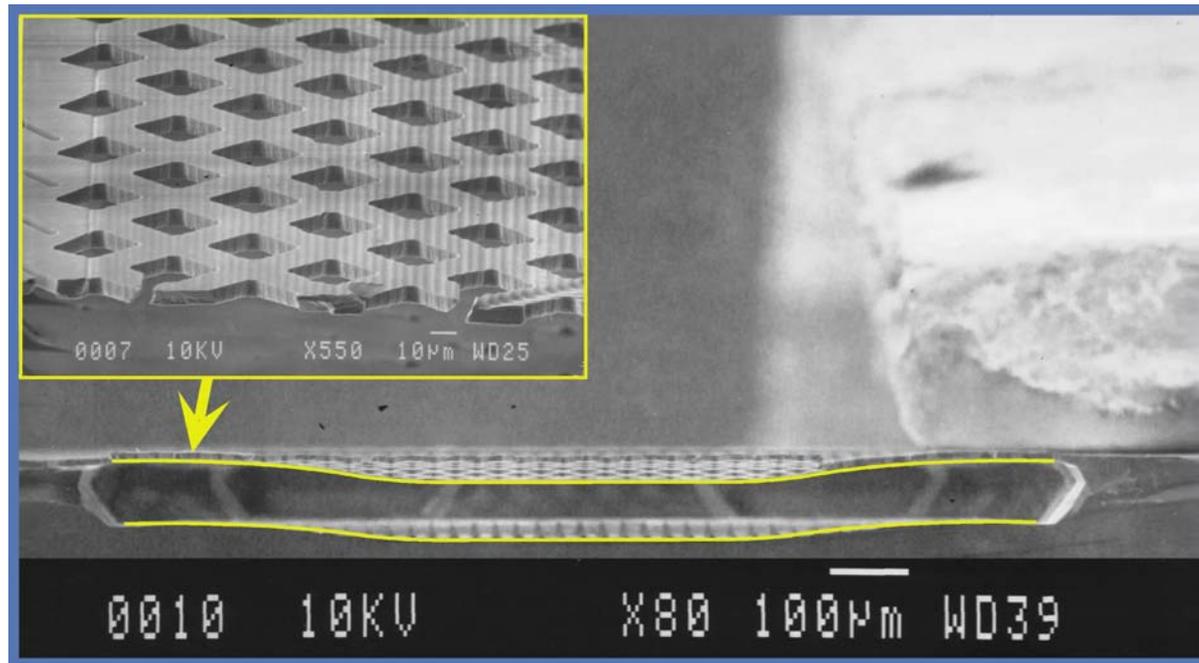
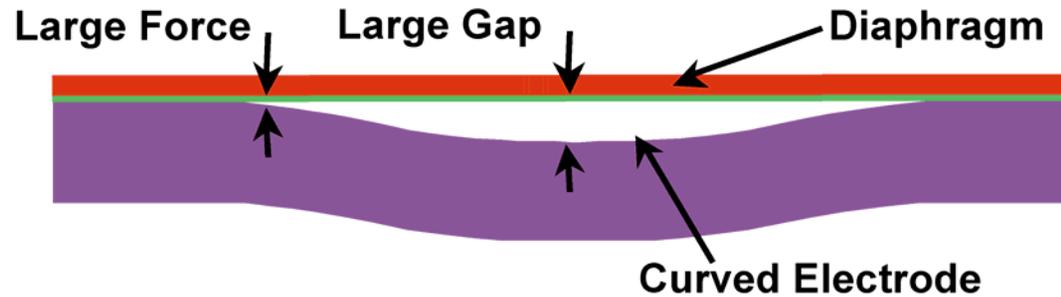


Etching technology for arbitrary out-of-plan surface formation

- (e) Thermal oxide removal

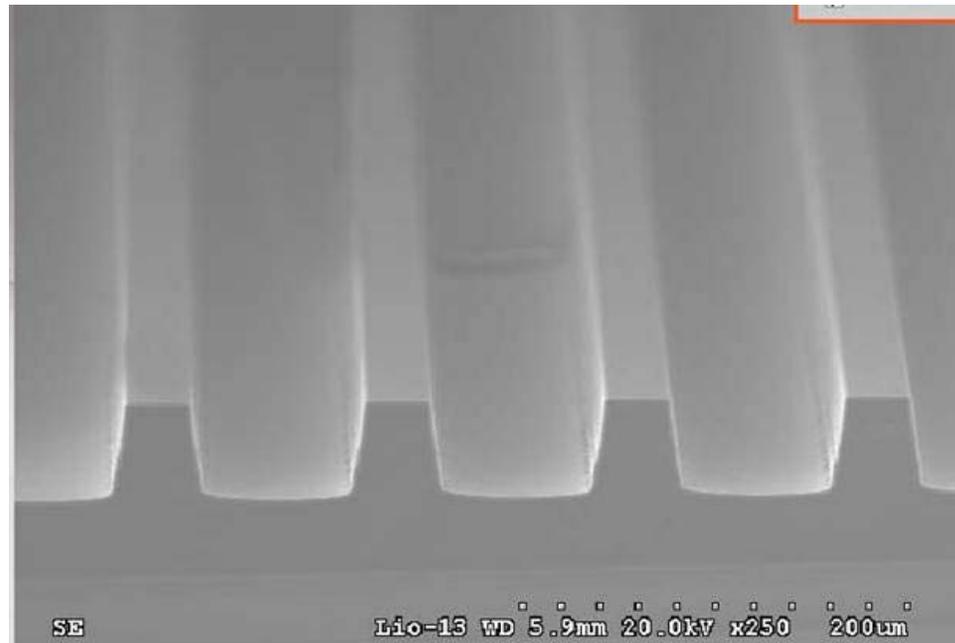


Out-of-plane curved electrode



Glass Micromachining

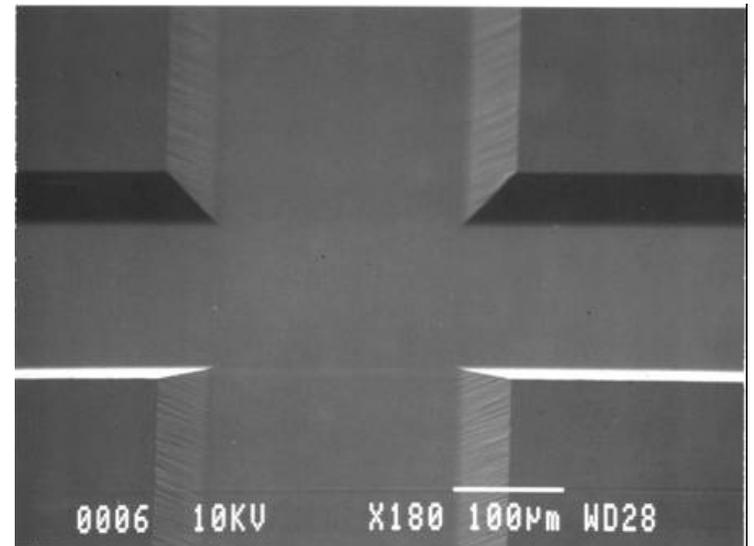
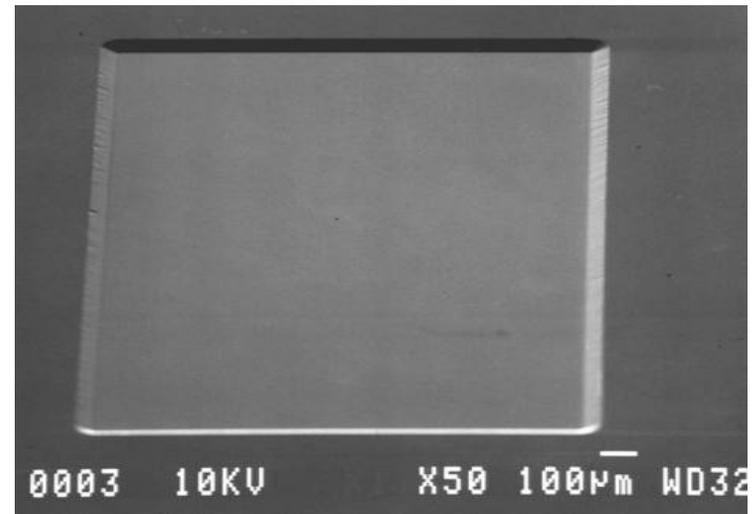
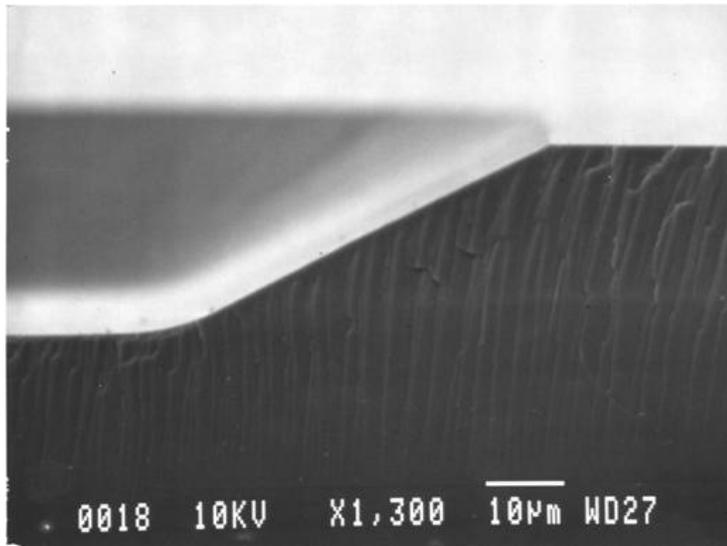
- DRIE
 - Etching of borosilicate glass
 - Up to 50 microns
 - Positive taper
 - Very smooth bottom



DRIE etching of borosilicate glass by LioniX

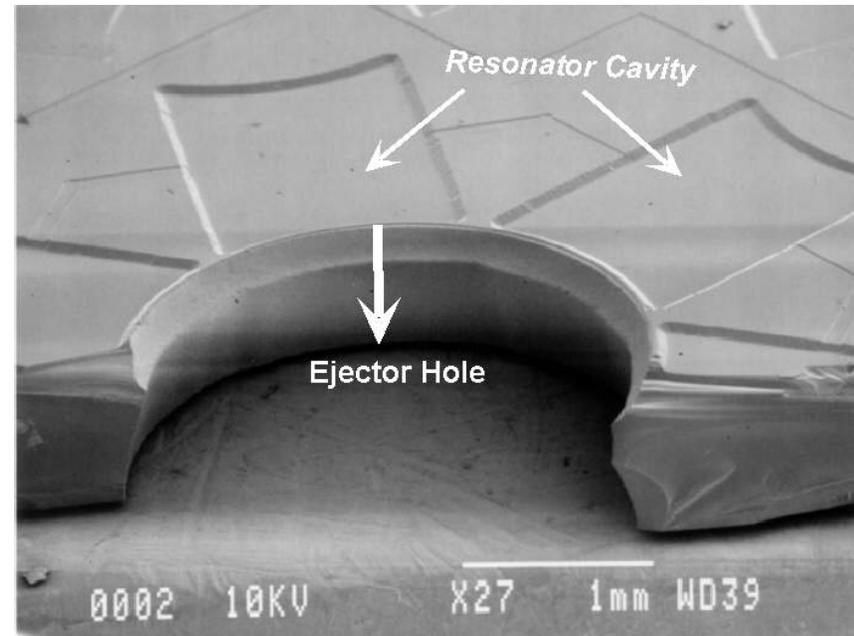
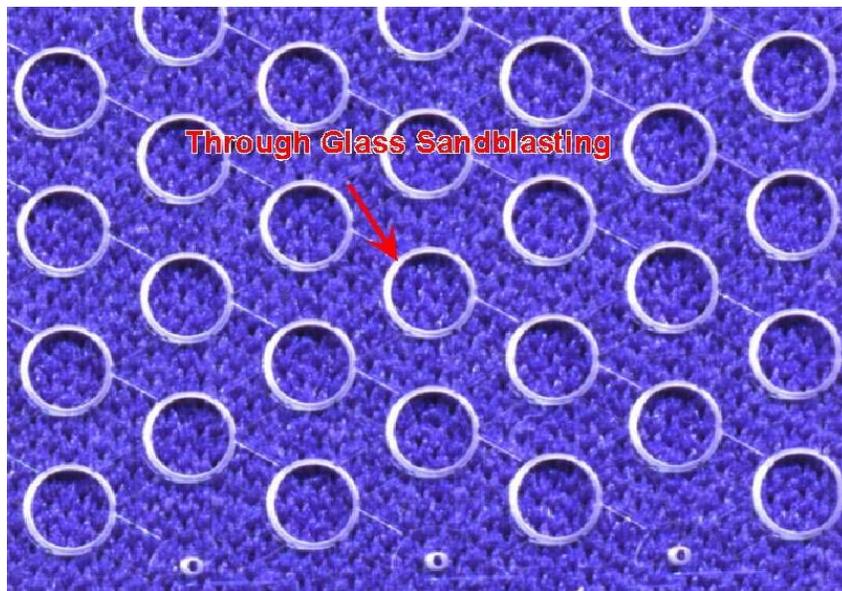
Glass Micromachining

- Wet Etching
 - HF:HNO₃:H₂O
 - Au or Si is usually used as etch mask



Sandblasting Technique

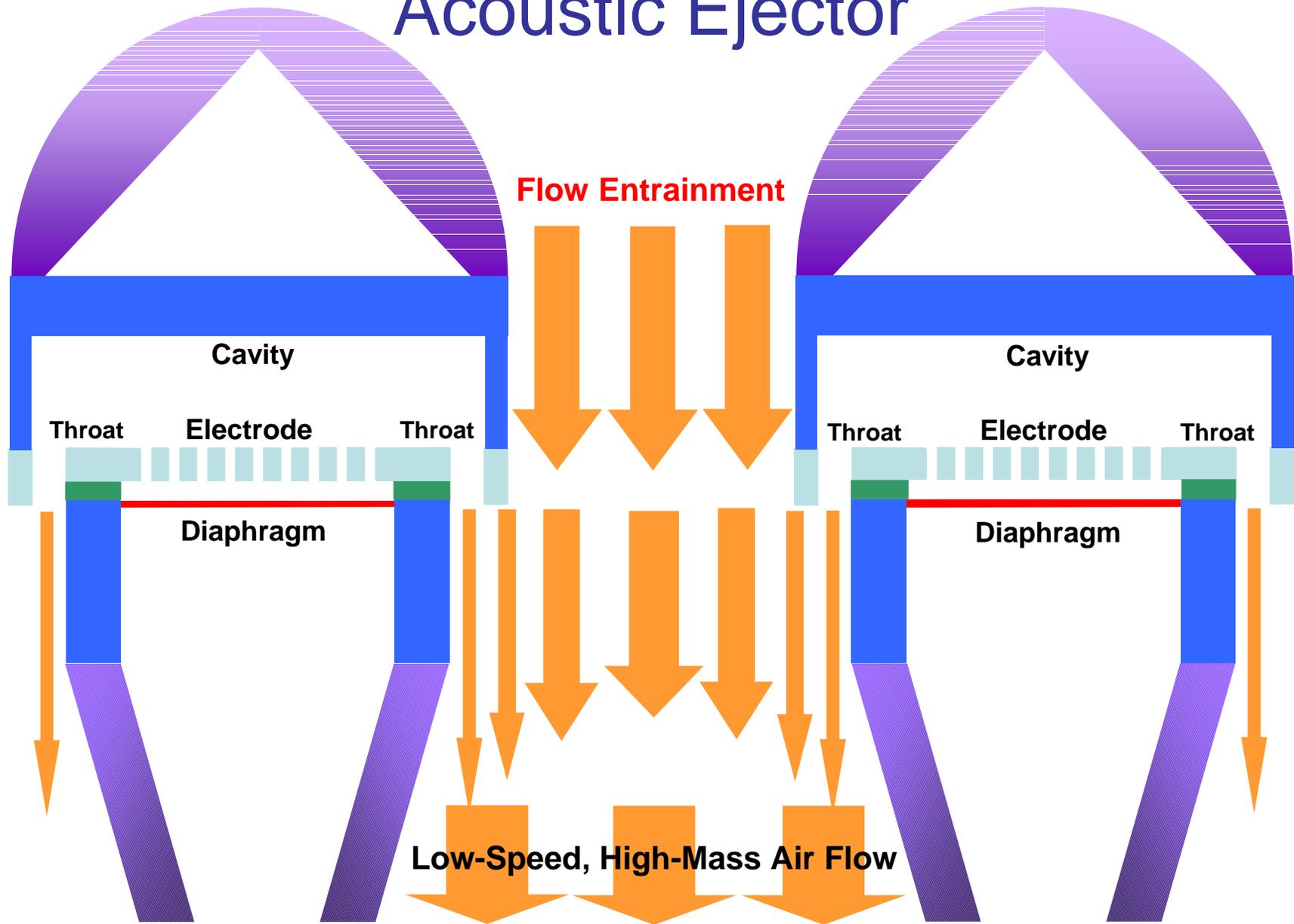
- Direct particle bombardment
- Low tech but effective
- Also works on Si substrate



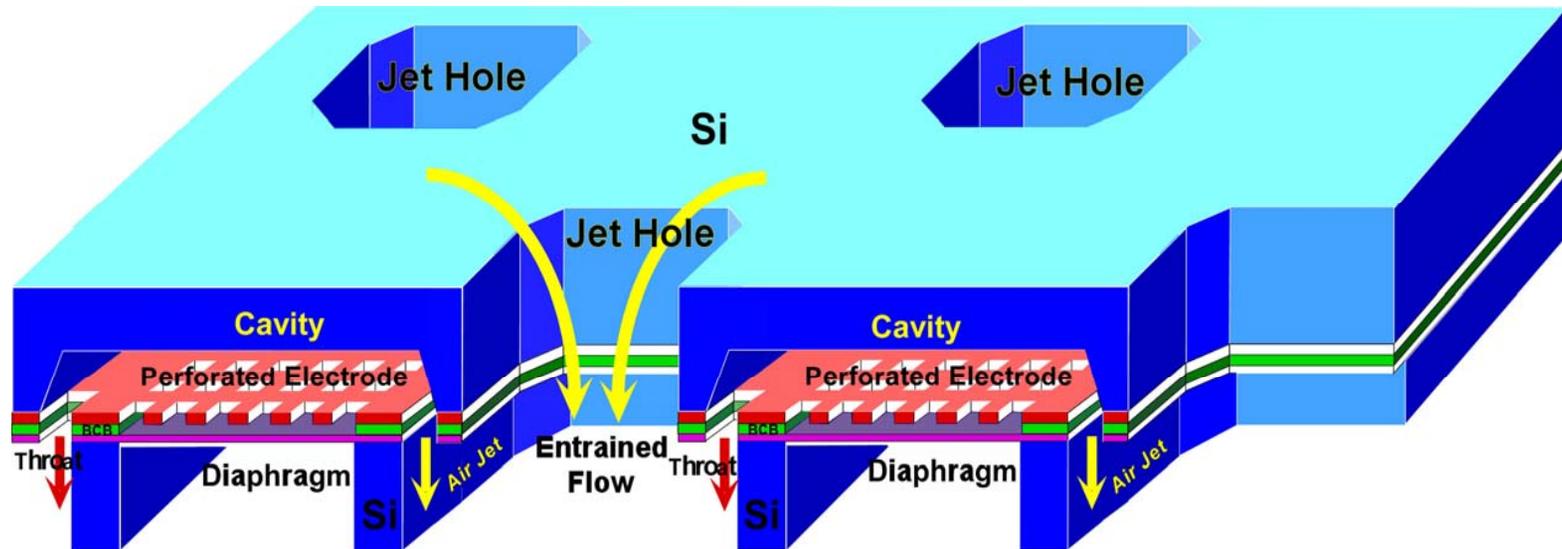
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- **3D MEMS structure and package**
 - Complex MEMS structures can be created by combination of various etching techniques
 - Through wafer via package
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Acoustic Ejector



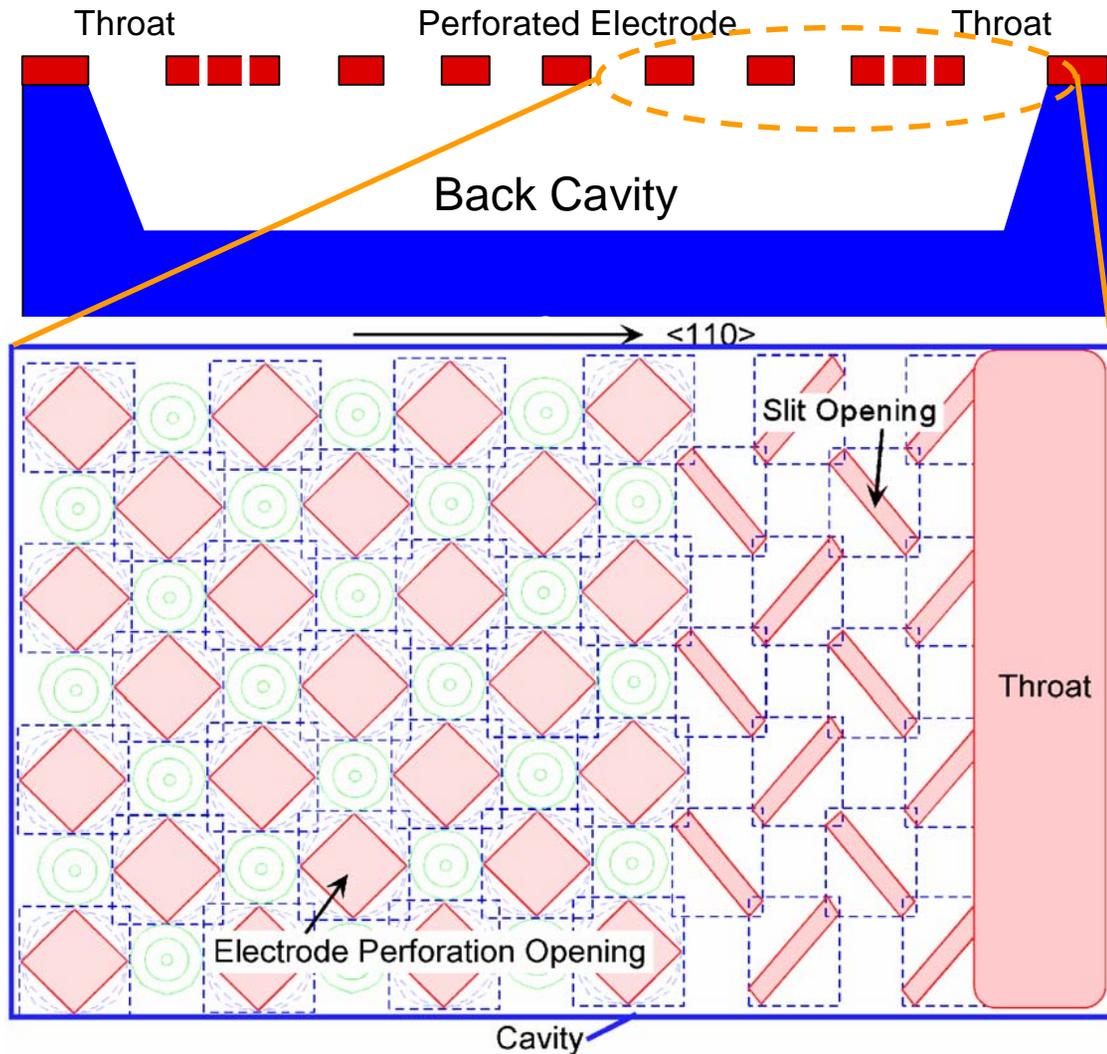
Micromachined Acoustic Ejector Array



- gas pumping
- micro propulsion
- thermal management

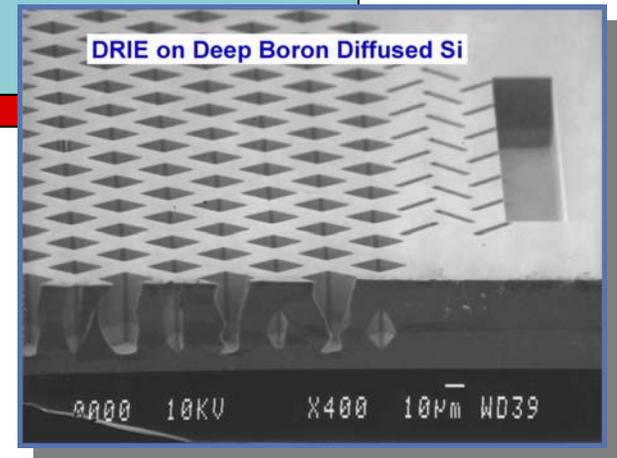
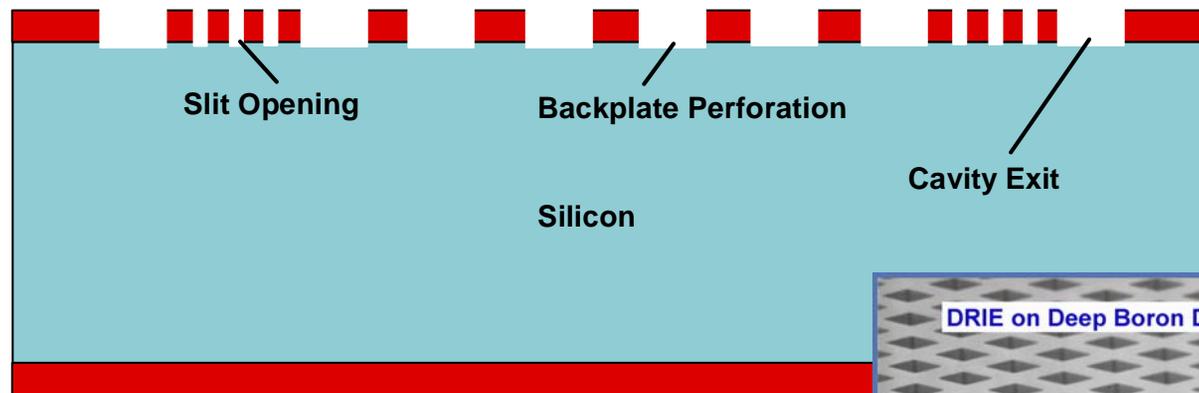
Design and Fabrication of Cavity With Integrated Perforated Electrode

- Deep boron diffused Si (~15 μm) serves as the electrode
- Perforation of electrode is done by DRIE through the deep boron diffused Si
- Electrode release and cavity formation are performed on the same wafer by anisotropic etching underneath the perforated electrode



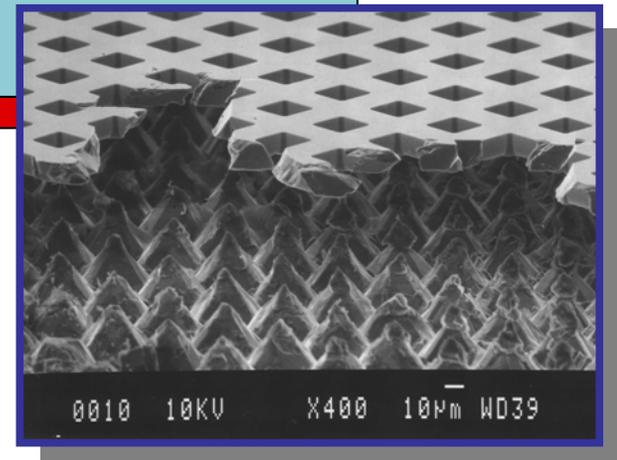
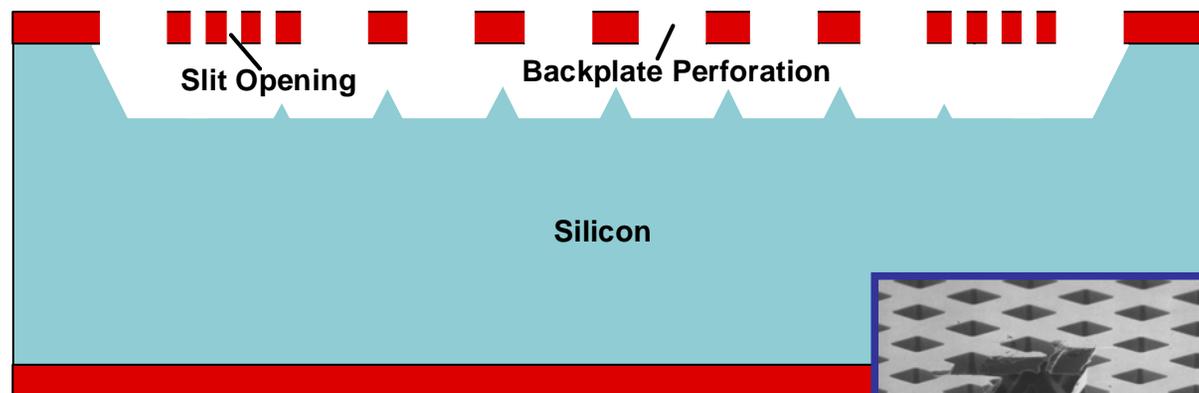
Formation of Buried Cavity with Perforated Electrode

b) DRIE through deep-boron diffused silicon layer



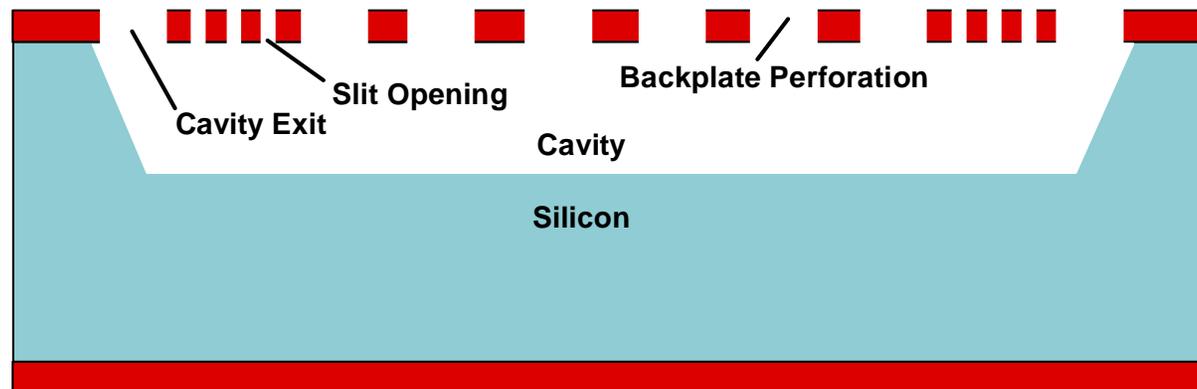
Formation of Buried Cavity with Perforated Electrode

c) Transient anisotropic Si etch



Formation of Buried Cavity with Perforated Electrode

d) Buried cavity formation

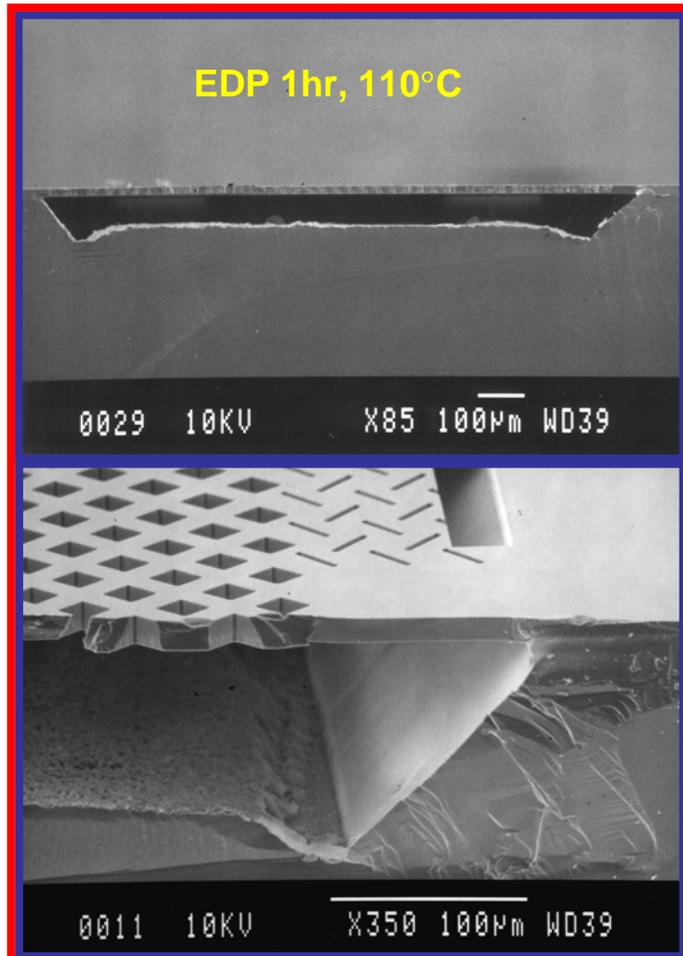


Back Cavity Formation By EDP and TMAH

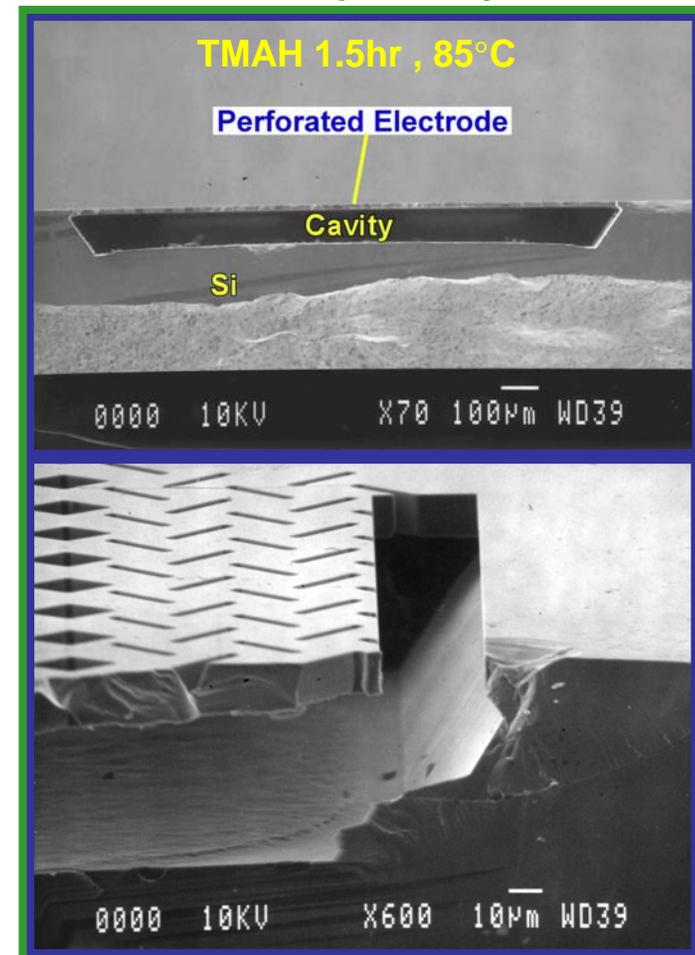
- Perforated electrode is released

- Continuous back cavity is formed

Rough etch profile by EDP



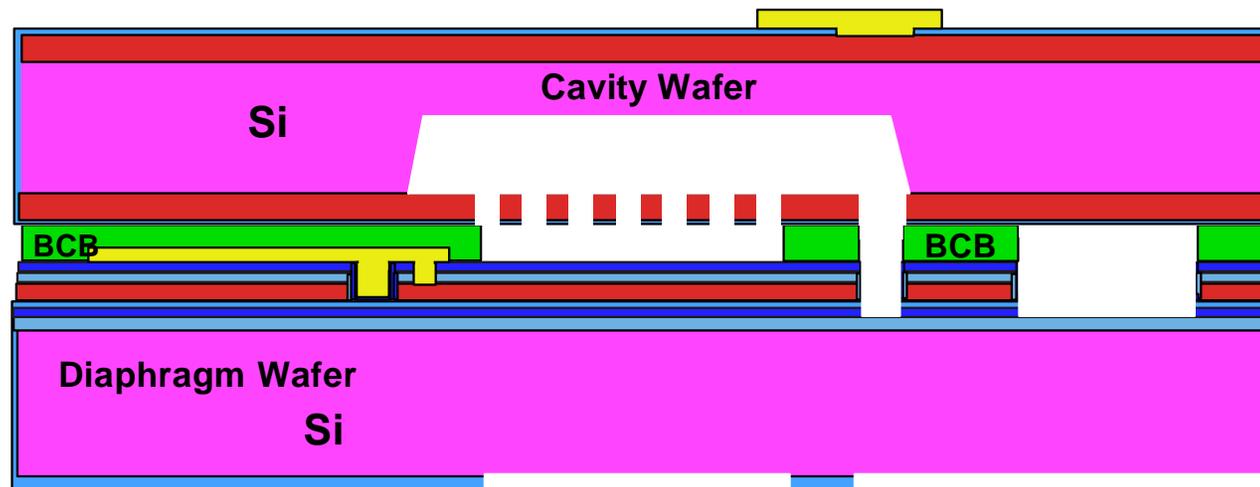
Smooth etch profile by TMAH



Batch Fabrication of All-Si MACE

- Wafer bonding (Cavity wafer & Diaphragm Wafer)

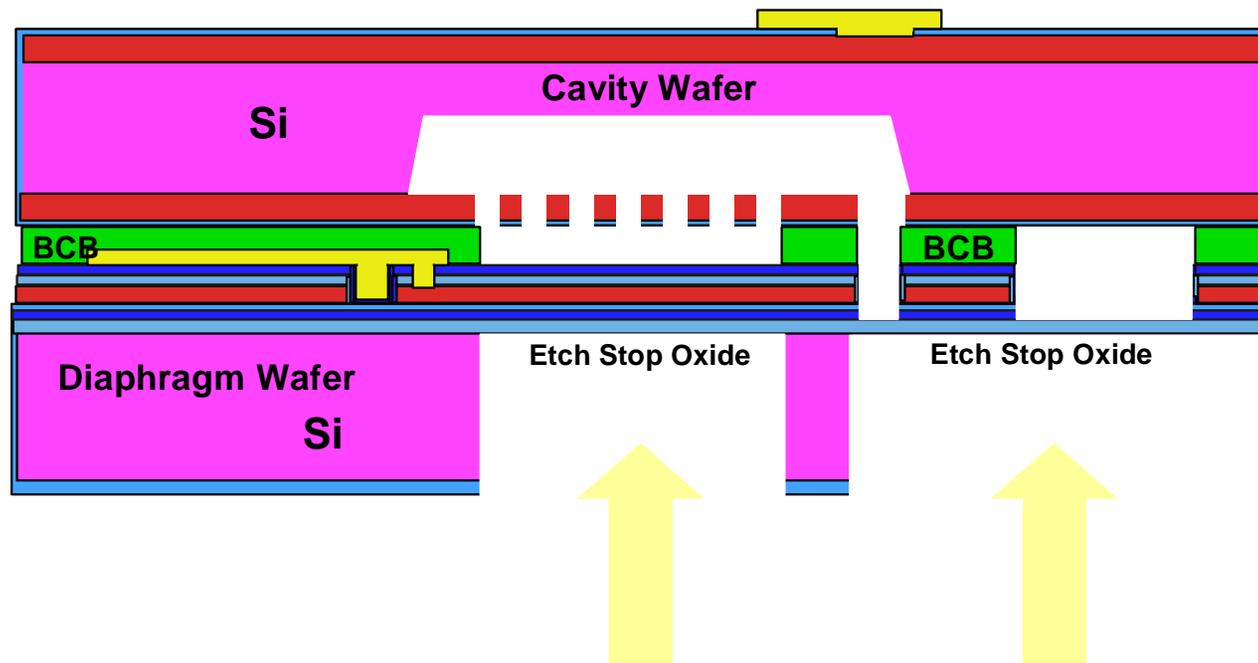
BCB Patterning and Localized Bonding with Cavity Wafer



Batch Fabrication of All-Si MACE

- Bonded Wafer

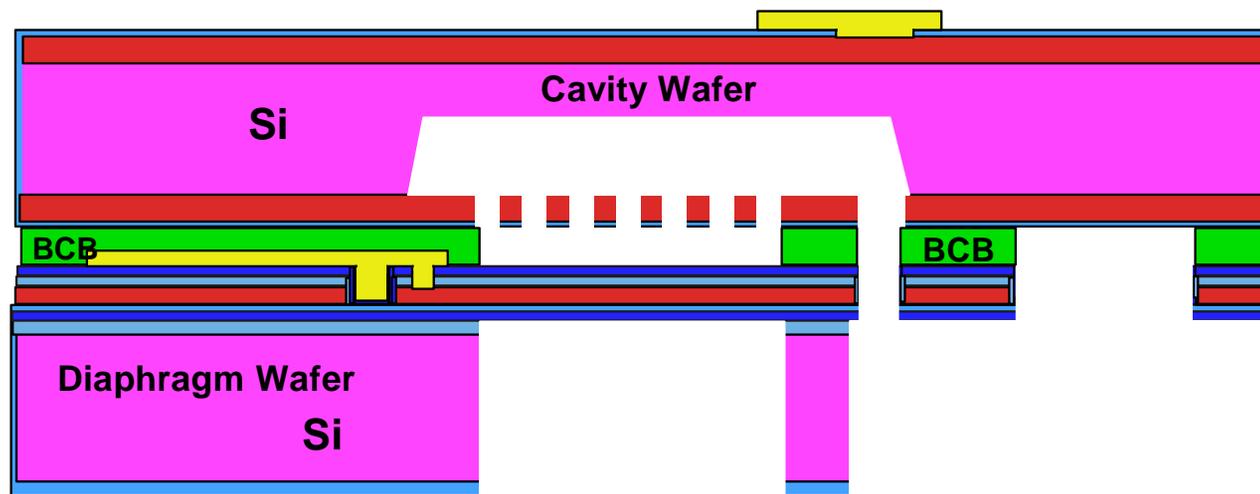
DRIE Membrane Release



Batch Fabrication of All-Si MACE

- Bonded Wafer

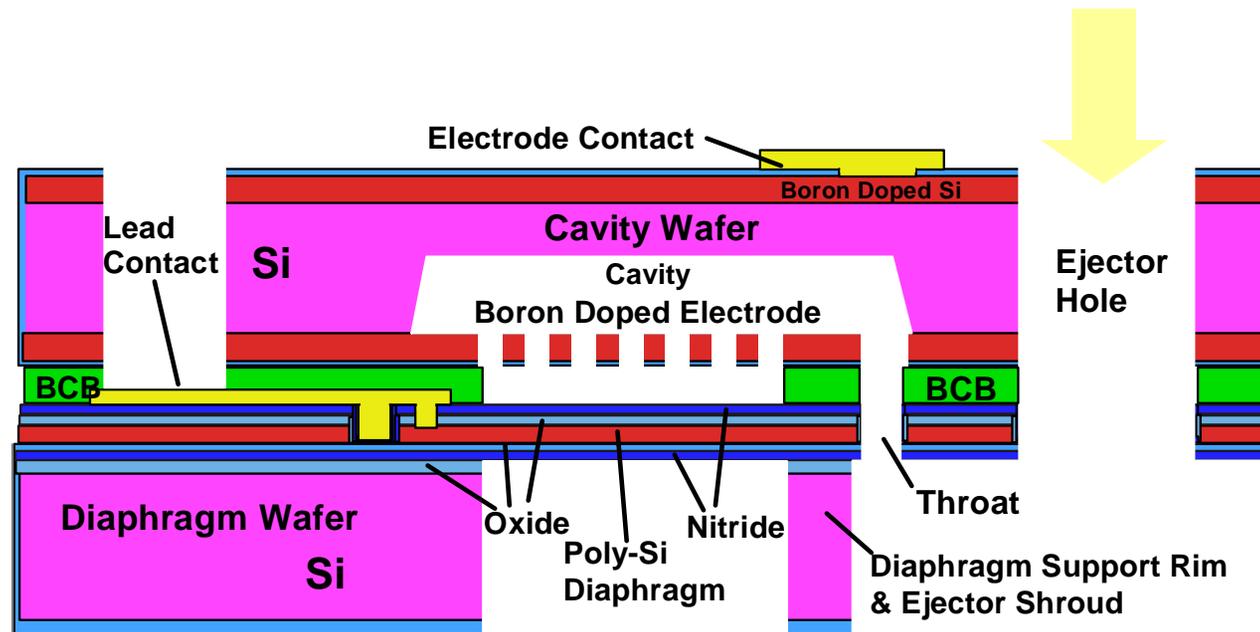
Etch Stop Oxide Removal



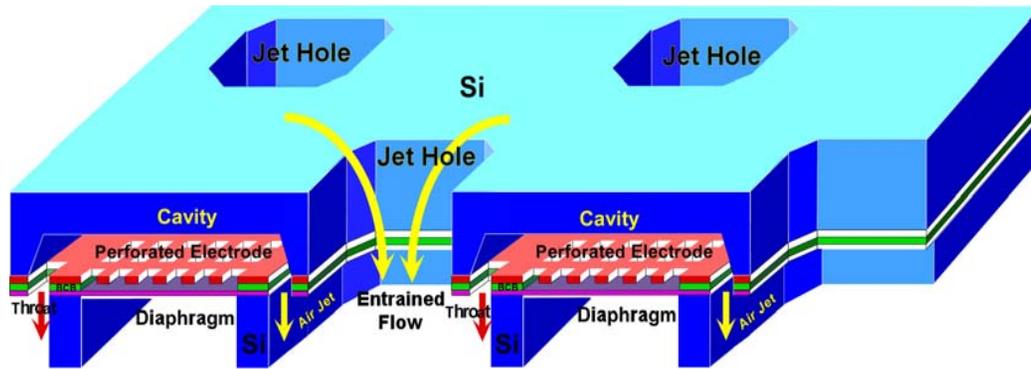
Batch Fabrication of All-Si MACE

- **Bonded Wafer**

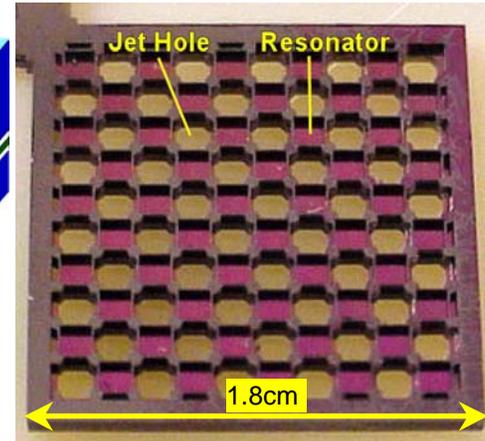
DRIE Ejector Hole and Chip Separation Etch



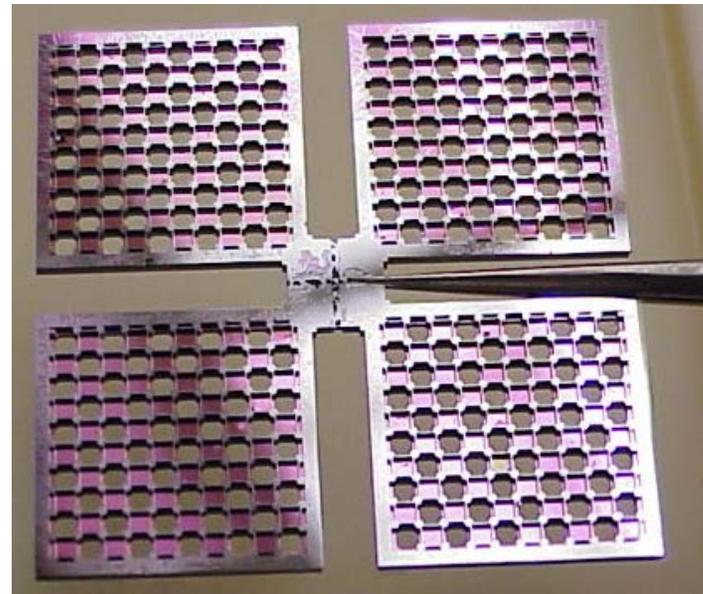
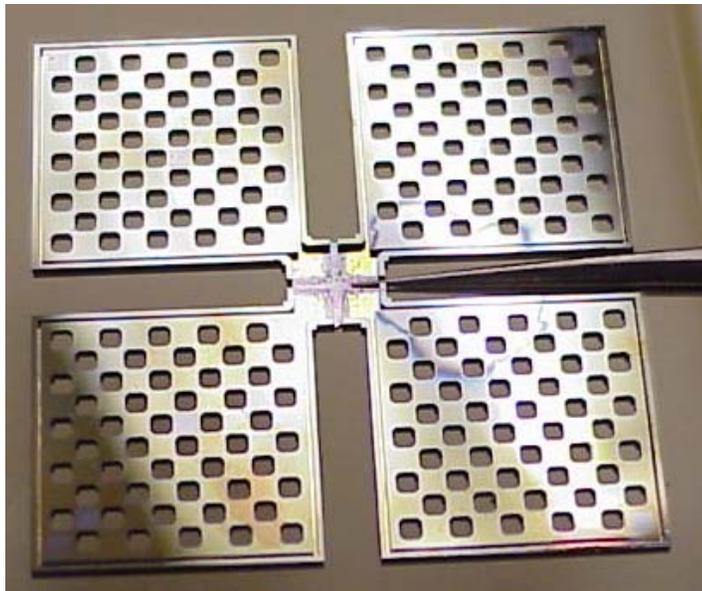
Fabricated MEMS Ejector Array Chip



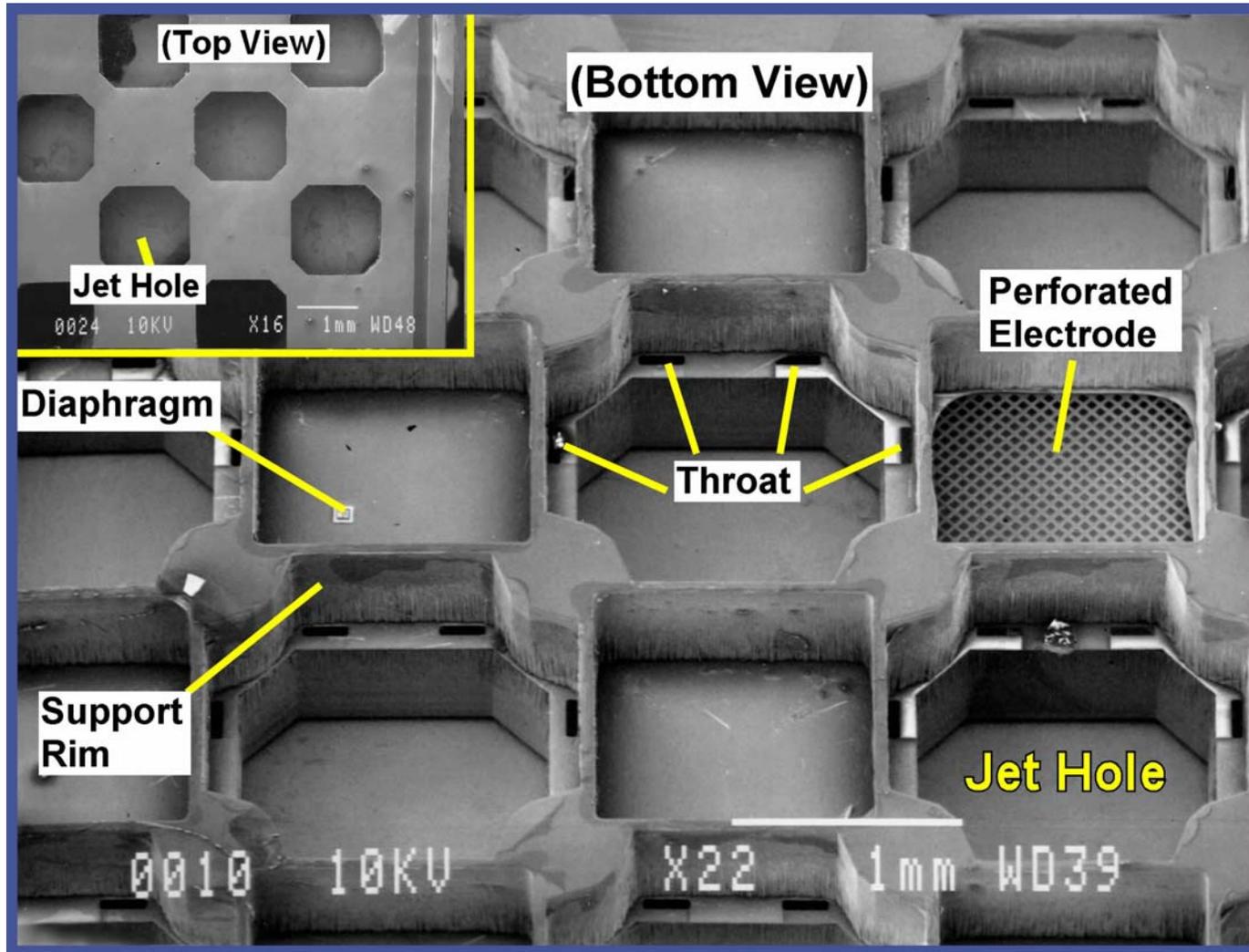
Top View



Bottom View

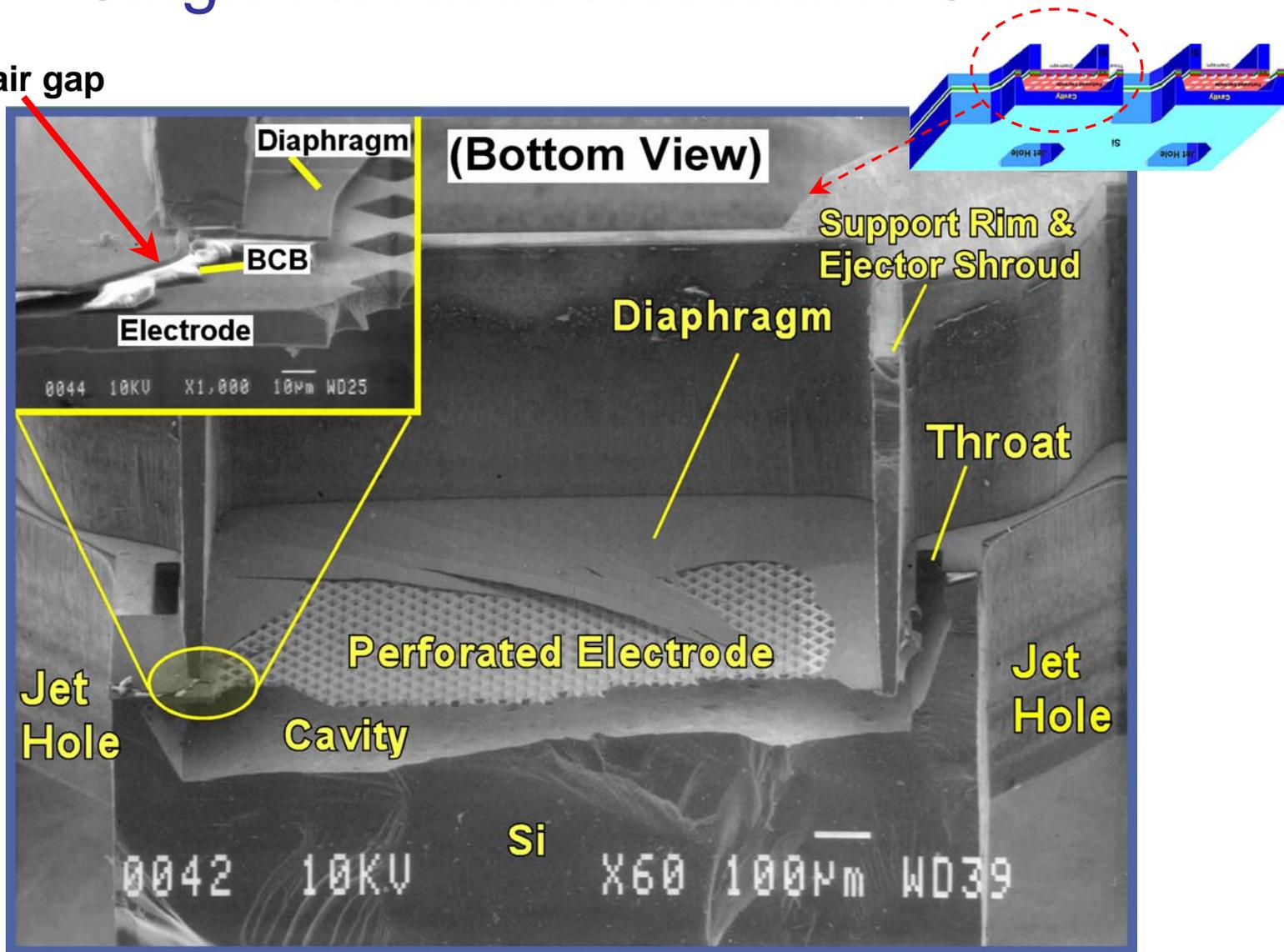


SEM of MEMS Ejector Array

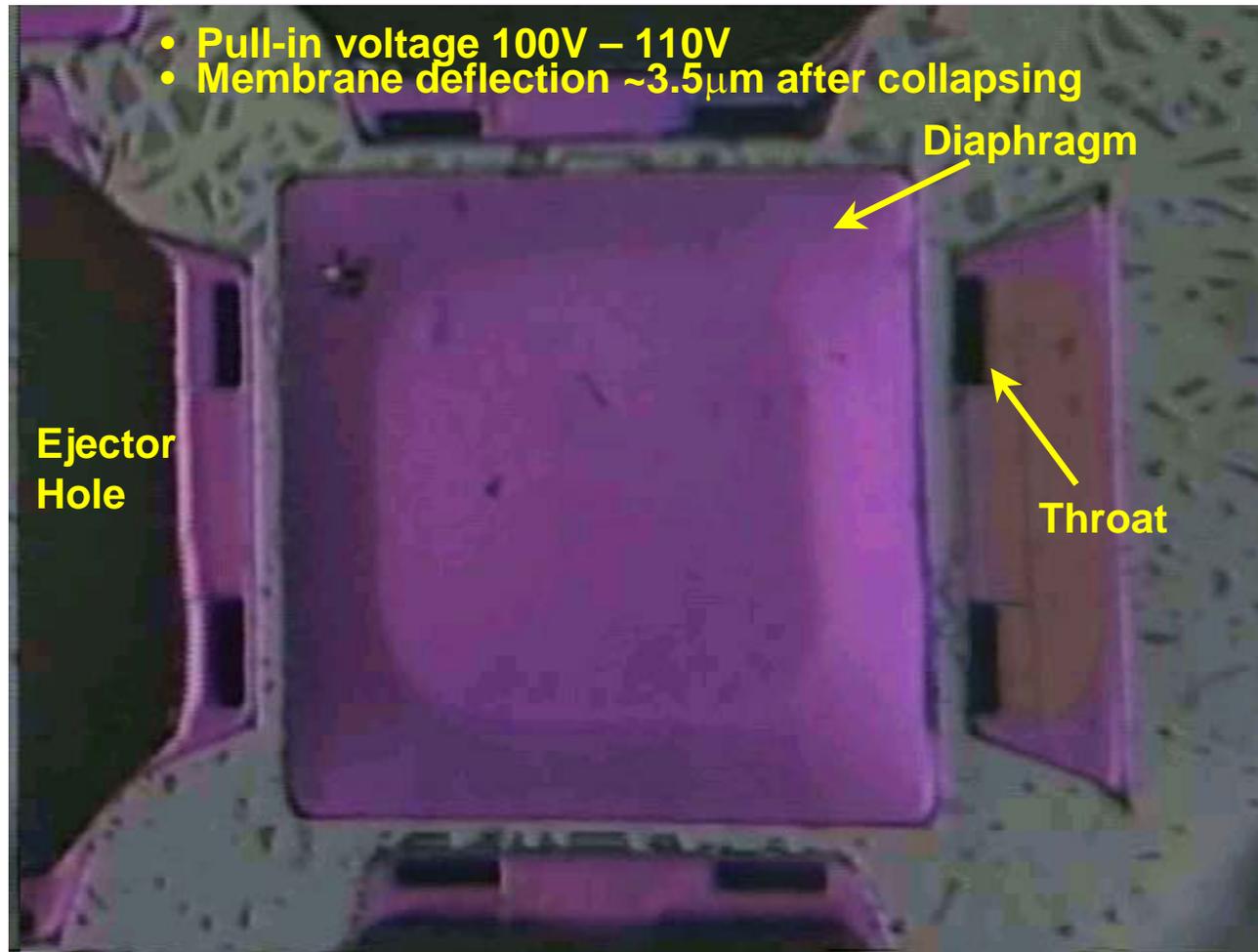


Single Acoustic Resonator Unit

Actual air gap
~5.5 μm



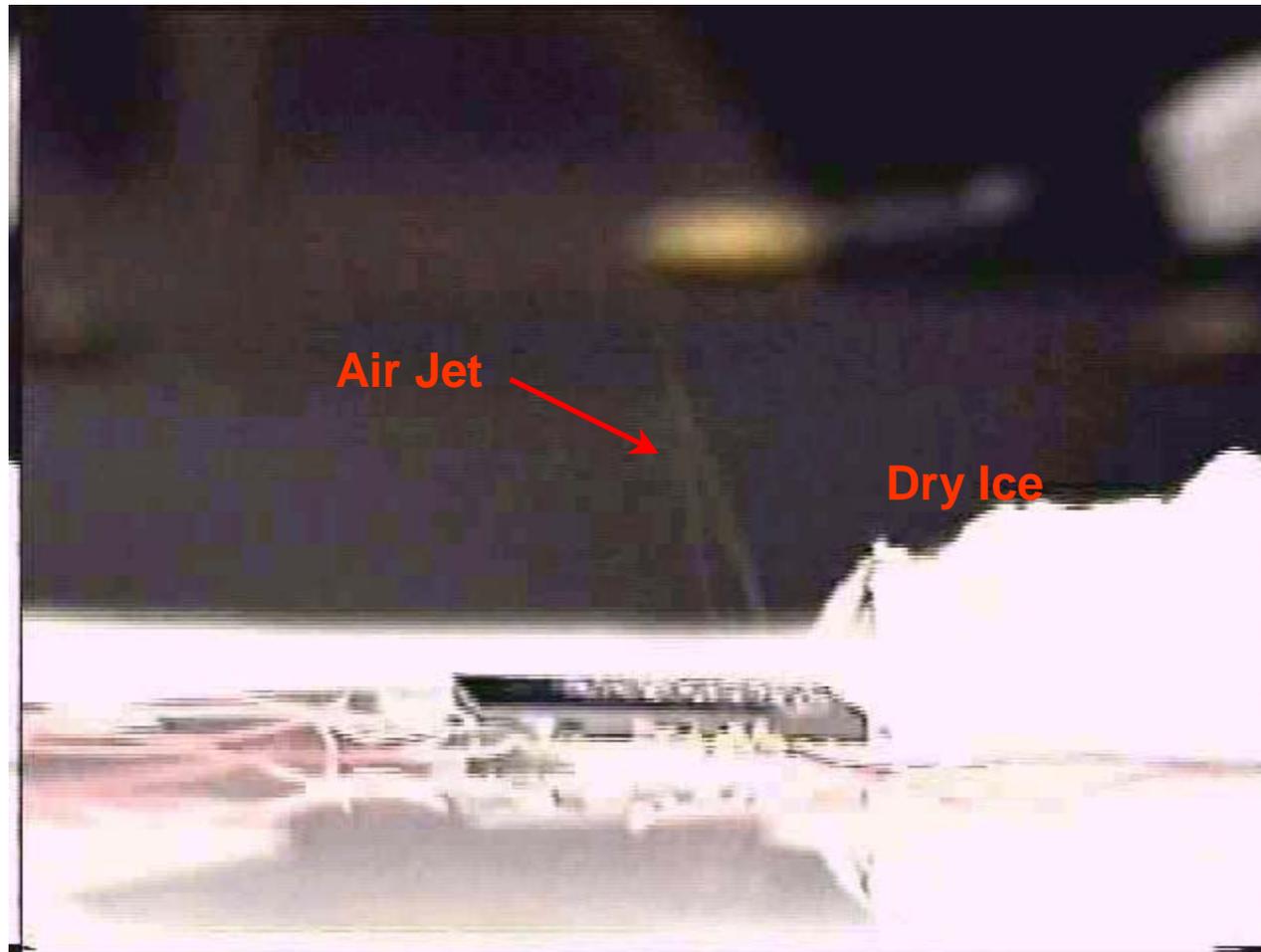
Actuation of Addressable Resonator



Dry Ice Flow Visualization and Particle Levitation

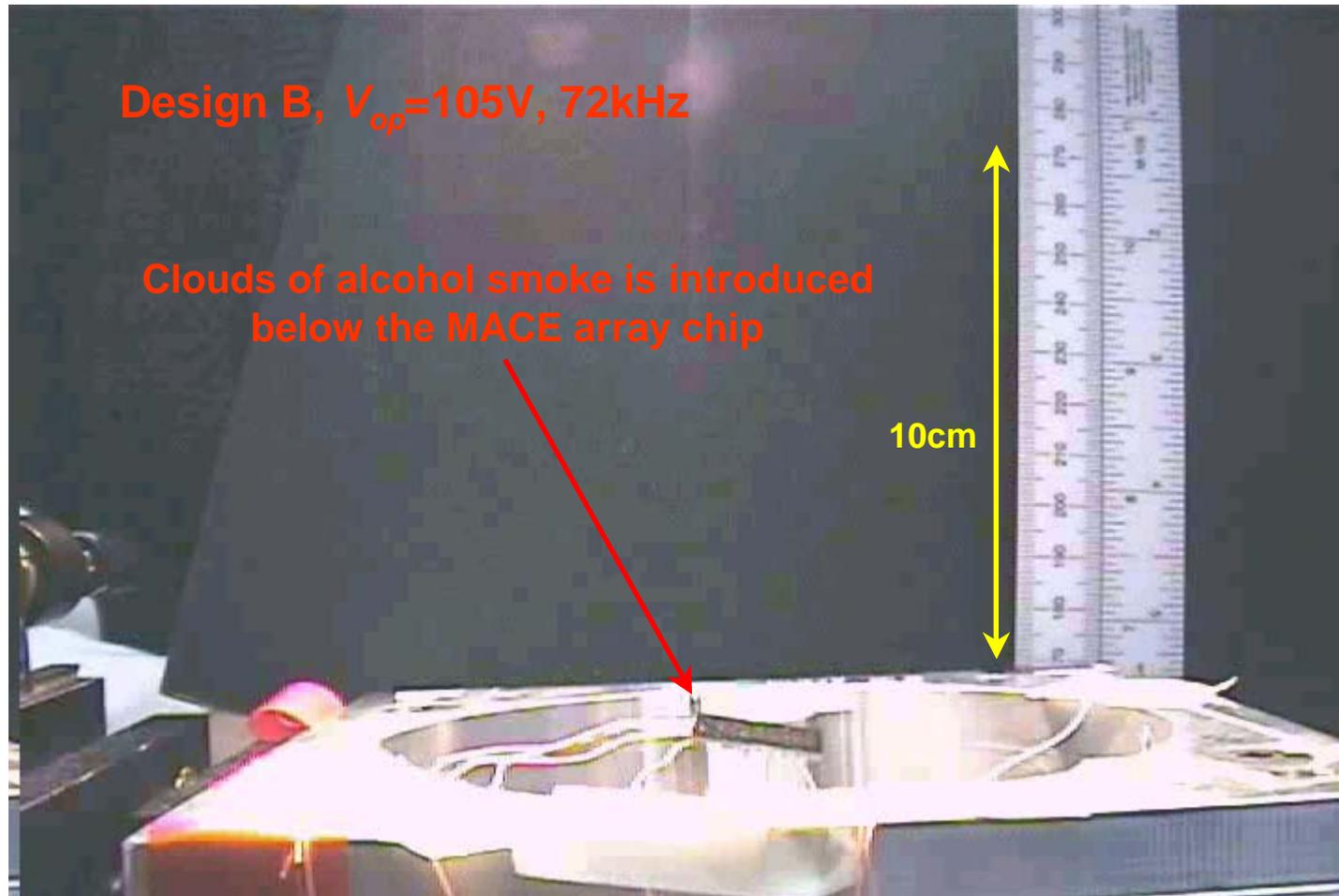
- $V_{op}=110V$, $f_{membrane}$: ~68kHz
- Dry ice particle velocity ~ 15cm/s

Design A
one row
addressed



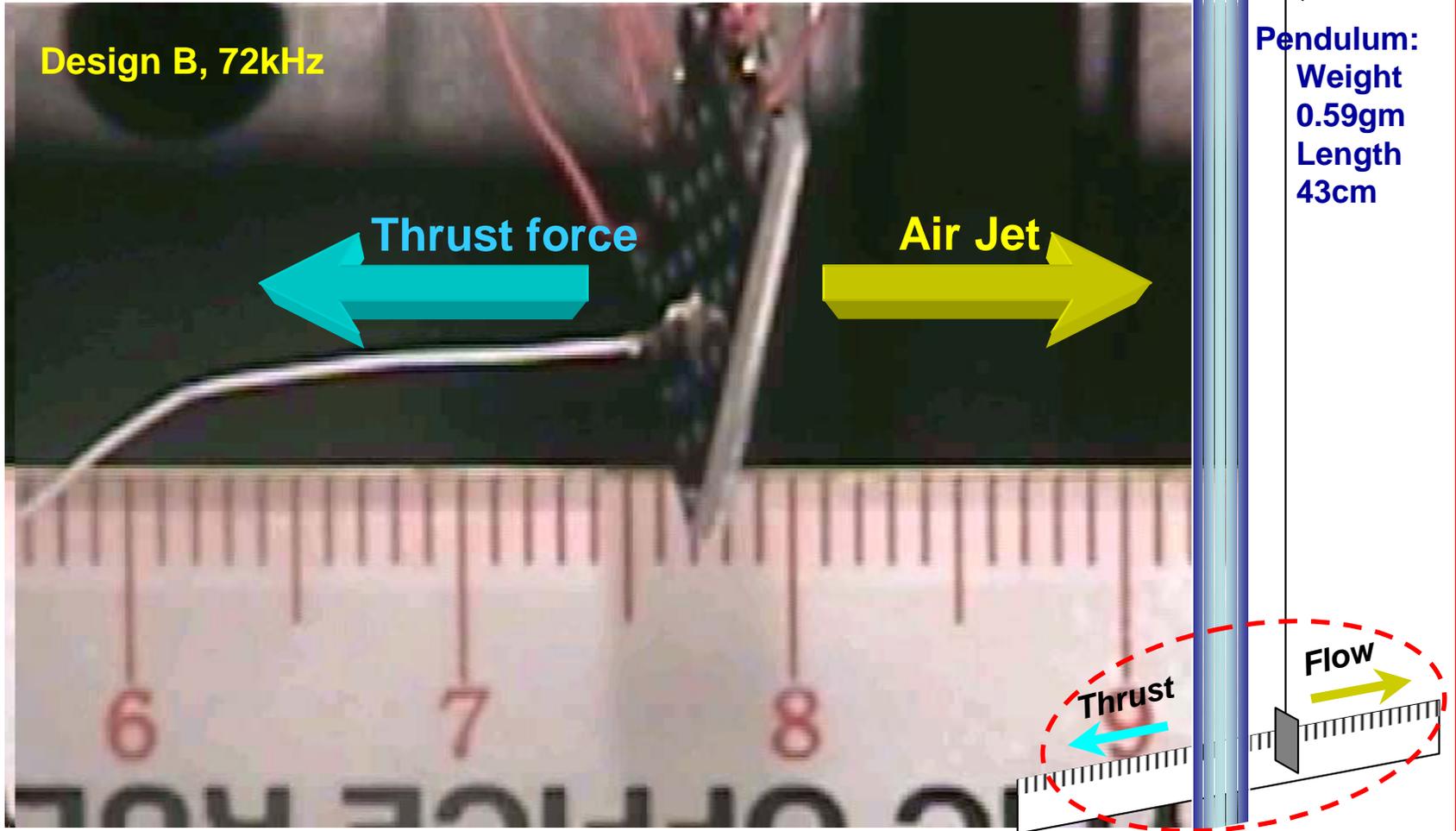
Air Pumping

Actuation of MACE array chip with 20 ejectors / resonators operating simultaneously.



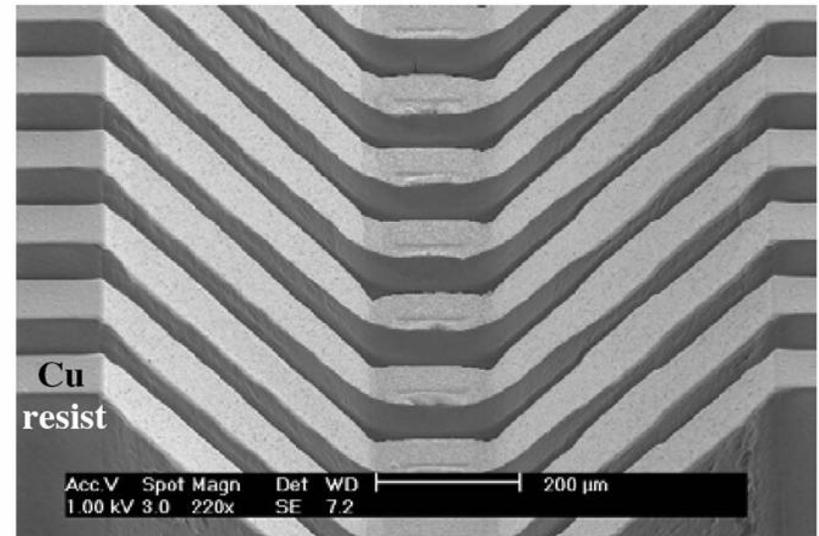
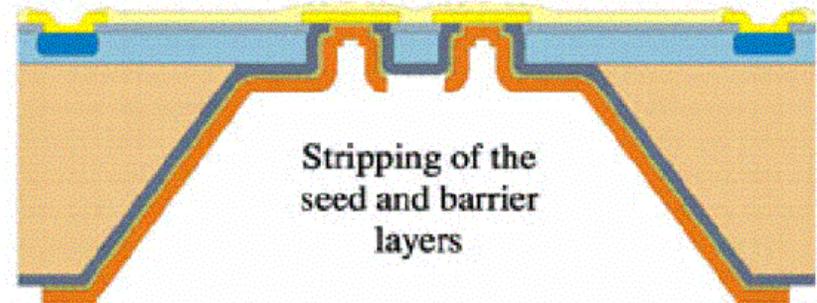
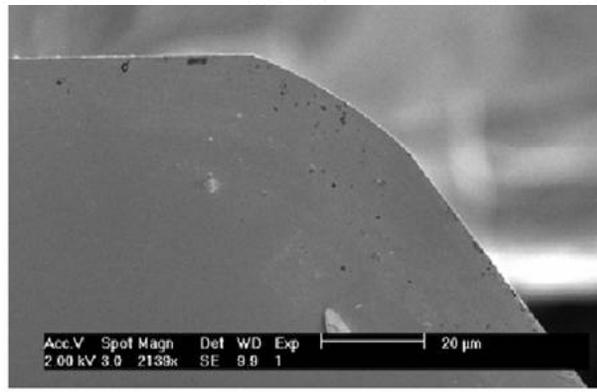
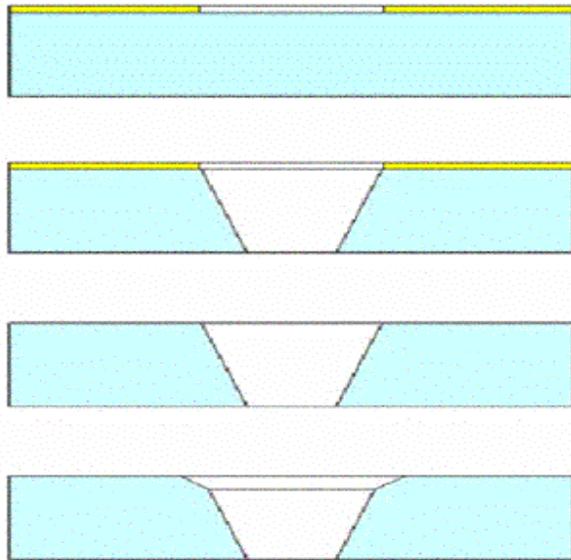
Thrust Demonstration

- 2mm displacement at Steady State
→ $27\mu\text{N}$ thrust



MEMS etching for CMOS via package

Through wafer via and corner rounding



DRIE for through wafer via package

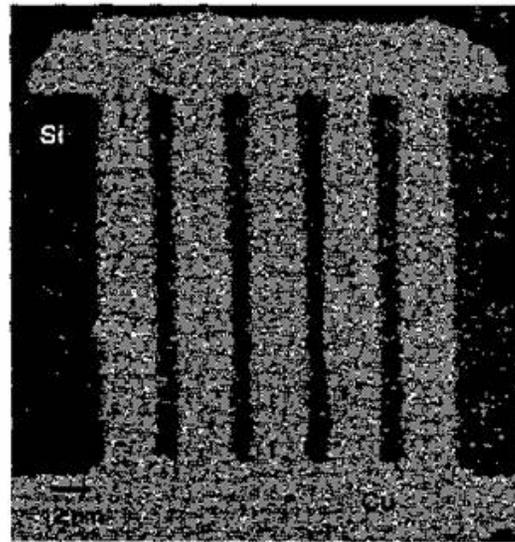


Fig. 4. SEM cross-section of substrate vias with an aspect ratio of 8. The substrate is 100- μm thick. Each via is 12- μm wide. These vias are overfilled.

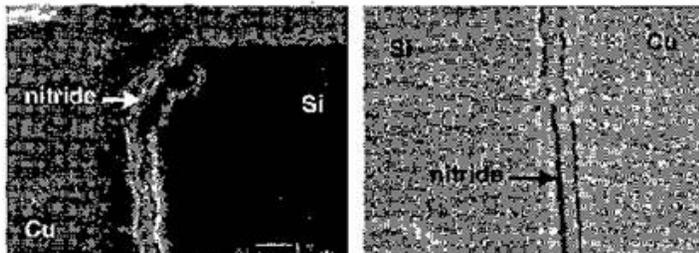
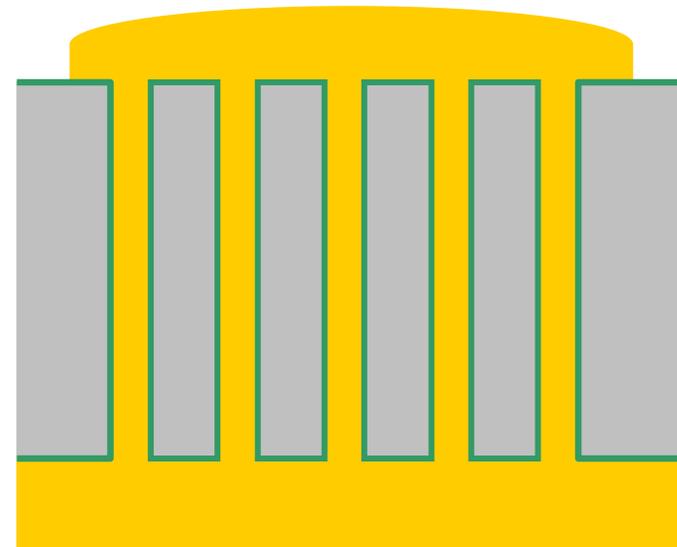


Fig. 5. Top: SEM cross-section of top-sidewall of a 14- μm wide x 103- μm deep via. The nitride liner is 550-nm thick at the surface and 500-nm thick 1 μm down from the surface. Bottom: cross-section of the mid-sidewall of a 38- μm wide x 106- μm deep trench. The nitride is 150-nm thick (260 nm at surface). Both are conformally lined with nitride and filled with Cu.

Summary

- MEMS etching technology has deviated from traditional CMOS process with various etching approaches and combinations
- Complex MEMS structures require new etching capability which cannot be provided by traditional CMOS technology
- Cost & Prospective
 - Wet etching technology
 - High throughput and Low cost
 - Limited MEMS structure
 - Some may need CPD for final release with adding cost
 - Dry etching
 - Low throughput and high cost (especially DRIE)
 - Much more freedom on MEMS structure for various applications
 - Direct final release feasible with no additional cost
 - Etching rate and throughput is the key for cost-effective commercial MEMS products
 - MEMS etching is no longer limited by the CMOS process and can become a solution to some future CMOS technology