MEMS Etching Technology

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Sep. 9, 2004
Outline

• Overview
• Etching in surface micromachining
• Etching in bulk micromachining
• 3D MEMS etching technology
  – Complex 3D MEMS machinery
  – Through wafer via package
• Summary
MEMS etching overview

- Then - MEMS etching technology initiated with CMOS etching technology
  - Fundamental pattern transfer
    - Lithography
  - Dry etching
  - Wet etching
  - Can re-use the depreciated CMOS equipments.
  - Final release process (for moving parts) is the key that deviates MEMS etching from CMOS technology (need to have good selectivity to other structure materials)
BiCMOS with surface micromachining

- A standard BiCMOS process follows by a final surface sacrificial layer (e.g., oxide) etching for final structure release.

Analog Devices BiMEMS integrated MEMS technology.

CMOS with bulk micromachining

- An infrared detector with standard CMOS process follows by a final bulk silicon etching for final structure release.

Tezcan et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, 2003

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MEMS etching overview

• Now and future – Complex MEMS structures and etching technology have advanced beyond CMOS
  – MEMS structures are not limited by simple surface or bulk micromachining etch step
  – Deep wafer etching becomes popular
  – Etching technology in MEMS diversifies MEMS into complex 3D structures
  – CMOS related process starts to use MEMS etching technique
  – Final release etching remains the key in MEMS process technology (need to have good selectivity to other structure materials)
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  - 3D MEMS package
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Etching in Surface Micromachining

- Etching to produce MEMS pattern as standard CMOS process
- Etching to remove sacrificial material for the MEMS structure release
  - Sacrificial material
    - Oxide – usually used for polysilicon structures (high temp. process).
      - 49% HF (>1um/min)
      - BHF (>0.1um min., depends on deposition of oxide)
      - Vapor HF (very slow ER~350A/min)
    - Metal (low temp. process)
      - Cu with Cu etchant
      - Al with Al etchant
    - Polymer/polyimide/photoresist (low temp. process)
      - Solvent (e.g., Acetone)
      - O2 plasma
    - Polysilicon (high temp process) - same etching approach as Si bulk etch
      - Si wet etchant
      - SF6 and XeF2 dry etchant
Vapor HF Release

Sacrificial polymer etch for surface micromachining

- Plasma release or solvent release with CPD

TI DMD (Digital Micromirror Device)
CPD

- CPD is needed in some MEMS structures due to stiction issue if it is done by wet etch release
- Dry etch release will not need CPD

G. T. Mulhern et. al., Transducers'93

a. 1) Exchange methanol with liquid CO2 (@ ~20°C and 1200 psi).

b. 1–2) Close off vessel and heat liquid CO2 to a supercritical fluid. There is no interface formed during this transition.

c. 2–3) Vent vessel at a constant temperature above Tc. The CO2 exists in gaseous form.
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Etching in Bulk microchining

• Si Etch to produce
  – Mold for MEMS structure
  – Si as sacrificial material for structure release
  – Package via
  – Microchannel

• Glass Etch to produce
  – Package cavity, Via
  – Microfluidic channel
Isotropic Si etch

- Wet etch (HNA, hydrofluoric acid, nitric acid, acetic acid)
  - HF+HNO3+CH3COOH+H2O
- Dry etch (usually for final release step)
  - SF6 RIE
    - Most common dry etch approach for sacrificial Si etch and release
  - XeF2 – receives attention
    - 2 XeF2 + Si \rightarrow 2 \text{Xe} \text{(g)} + \text{SiF}_4 \text{(g)}
    - Advantages:
      - Highly selective to silicon with respect to Al, photoresist, and SiO2.
      - isotropic, large structures can be undercut.
      - Fast (~10µm per hour)
      - Gas phase etching, no stiction between freed structure and substrate
Single Crystal Reactive Etching And Metalization (SCREAM)

Yao et al., JMEMS, 1992.
Si Anisotropic Wet etch

From Micromachined transducers sourcebook by Kovacs
Anisotropic Si etchant

- KOH, EDP, and TMAH are commonly used with SiO2 as etch mask
- All etchants have good selectivity to heavy boron doped Si
- TMAH is safer and IC compatible with less selectivity to oxide compared to other etchants

<table>
<thead>
<tr>
<th>Etchant/Diluent/Additives/ Temperature</th>
<th>Etch Stop</th>
<th>Etch Rate (100) (μm/min)</th>
<th>Etch Rate Ratio (100)/(111)</th>
<th>Remarks</th>
<th>Mask (Etch Rate)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KOH/water, isopropyl alcohol additive, 85°C</td>
<td>B &gt; 10^5 cm^-2 reduces etch rate by 20</td>
<td>1.4</td>
<td>400 and 600 for (110)/(111)</td>
<td>IC incompatible, avoid eye contact, etches oxide fast, lots of H2 bubbles</td>
<td>Photoresist (shallow etch at room temperature); Si,N (not attacked); SiO2 (28 Å/min); SiO2 (2-5 Å/min); Si,N (1 Å/min); Ta, Au, Cr, Ag, Cu</td>
</tr>
<tr>
<td>Ethylene diamine pyrocathecol (water), pyrazine additive, 115°C</td>
<td>≥5 × 10^5 cm^-2 reduces the etch rate by 30</td>
<td>1.25</td>
<td>35</td>
<td>Toxic, ages fast, O2 must be excluded, few H2 bubbles, silicates may precipitate</td>
<td></td>
</tr>
<tr>
<td>Tetramethyl ammonium hydroxide (TMAH) (water), 90°C</td>
<td>&gt;4 × 10^9 cm^-2 reduces etch rate by 40</td>
<td>1</td>
<td>From 12.5 to 50</td>
<td>IC compatible, easy to handle, smooth surface finish, few studies</td>
<td>SiO2 etch rate is 4 orders of magnitude lower than (100) Si LPCVD Si,N</td>
</tr>
<tr>
<td>NH4OH/water), isopropyl alcohol, 115°C</td>
<td>&gt;1.5 × 10^10 cm^-2 practically stops the etch</td>
<td>3.0</td>
<td>10</td>
<td>Toxic and explosive, okay at 50% water</td>
<td>SiO2 (≤2 Å/min) and most metallic films; does not attack Al according to some authors</td>
</tr>
</tbody>
</table>

From Fundamentals of Microfabrication by Madou.
Si DRIE

- Bosch passivation/etching process approach
- high aspect ratio Si etching
- Through Si wafer etch with close-to-vertical sidewall
- High etch rate (>5um/min.) can be achieved but only applies to small exposure area (e.g., <10%)
Combination of deep RIE and isotropic Si etch

Ayazi et. al., JMEMS 2000
DRIE Issue

- Scalloping is common at initial few um of etch
- RIE lag effect arises when aspect ratio $>\sim 2$

Scalloping

- Loading effect
  - Etching rate reduces drastically with exposure area
  - $\rightarrow$ lower throughput and expensive
- Dielectric charging affect etching direction
RIE for out-of-plane surface

• Turn the con to pro?
Etching technology for arbitrary out-of-plan surface formation

• (a) Si DRIE etch to create curved bottom profile
Etching technology for arbitrary out-of-plan surface formation

- (b) Isotropic Si etch to remove pillars

![Diagram of etching process with labeled areas](image-url)
Etching technology for arbitrary out-of-plan surface formation

- (c) Thermal Oxidation to smoothen surface
Etching technology for arbitrary out-of-plan surface formation

• (d) Maskless field Si etch
Etching technology for arbitrary out-of-plan surface formation

- (e) Thermal oxide removal
Out-of-plane curved electrode
Glass Micromachining

• DRIE
  - Etching of borosilicate glass
  - Up to 50 microns
  - Positive taper
  - Very smooth bottom

DRIE etching of borosilicate glass by LioniX
Glass Micromachining

- Wet Etching
  - HF:HNO3:H2O
  - Au or Si is usually used as etch mask
Sandblasting Technique

- Direct particle bombardment
- Low tech but effective
- Also works on Si substrate
Outline

• Overview
• Etching in surface micromachining
• Etching in bulk micromachining
• 3D MEMS structure and package
  – Complex MEMS structures can be created by combination of various etching techniques
  – Through wafer via package
• Summary
Acoustic Ejector

Flow Entrainment

Cavity

Low-Speed, High-Mass Air Flow

Throat

Electrode

Diaphragm
Micromachined Acoustic Ejector Array

- gas pumping
- micro propulsion
- thermal management
Design and Fabrication of Cavity With Integrated Perforated Electrode

- Deep boron diffused Si (~15µm) serves as the electrode
- Perforation of electrode is done by DRIE through the deep boron diffused Si
- Electrode release and cavity formation are performed on the same wafer by anisotropic etching underneath the perforated electrode
Formation of Buried Cavity with Perforated Electrode

b) DRIE through deep-boron diffused silicon layer
Formation of Buried Cavity with Perforated Electrode

c) Transient anisotropic Si etch

Slit Opening

Backplate Perforation

Silicon
Formation of Buried Cavity with Perforated Electrode

d) Buried cavity formation
Back Cavity Formation By EDP and TMAH

- Perforated electrode is released
- Continuous back cavity is formed

Rough etch profile by EDP

EDP 1hr, 110°C

Smooth etch profile by TMAH

TMAH 1.5hr, 85°C

Perforated Electrode
Cavity
Si
Batch Fabrication of All-Si MACE

- Wafer bonding (Cavity wafer & Diaphragm Wafer)

BCB Patterning and Localized Bonding with Cavity Wafer
Batch Fabrication of All-Si MACE

• Bonded Wafer

DRIE Membrane Release

Si
Cavity Wafer
Etch Stop Oxide
Etch Stop Oxide
Diaphragm Wafer
Si
BCB
BCB

DRIE Membrane Release
Batch Fabrication of All-Si MACE

- Bonded Wafer

Etch Stop Oxide Removal

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Batch Fabrication of All-Si MACE

- Bonded Wafer

DRIE Ejector Hole and Chip Separation Etch

[Diagram showing the fabrication process]
Fabricated MEMS Ejector Array Chip

Top View

Bottom View
SEM of MEMS Ejector Array

(Top View)

Jet Hole
Diaphragm
Support Rim

(Bottom View)

Perforated Electrode
Throat
Jet Hole

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Single Acoustic Resonator Unit

Actual air gap
~5.5μm
Actuation of Addressable Resonator

- Pull-in voltage 100V – 110V
- Membrane deflection ~3.5 μm after collapsing

Ejector Hole
Diaphragm
Throat
Dry Ice Flow Visualization and Particle Levitation

- $V_{op}=110\text{V}$, $f_{membrane} \approx 68\text{kHz}$
- Dry ice particle velocity $\approx 15\text{cm/s}$

Design A

one row addressed
Air Pumping

Actuation of MACE array chip with 20 ejectors / resonators operating simultaneously.

Design B, $V_{op}=105V$, 72kHz

Clouds of alcohol smoke is introduced below the MACE array chip.

10cm
Thrust Demonstration

- 2mm displacement at Steady State
  → $27\mu N$ thrust

Design B, 72kHz

Thrust force

Pendulum:
Weight 0.59gm
Length 43cm

Air Jet

Flow

Thrust
MEMS etching for CMOS via package

Through wafer via and corner rounding

Kutchoukov et al., J. Micromech. Microeng., 2004

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DRIE for through wafer via package

Fig. 4. SEM cross-section of substrate vias with an aspect ratio of 8. The substrate is 100-µm thick. Each via is 12-µm wide. These vias are overfilled.

Fig. 5. Top: SEM cross-section of top-sidewall of a 14-µm wide x 103-µm deep via. The nitride liner is 350 nm thick at the surface and 500 nm thick 1 µm down from the surface. Bottom: cross-section of the mid-sidewall of a 38-µm wide x 106-µm deep trench. The nitride is 150-nm thick (280 nm at surface). Both are conformally lined with nitride and filled with Cu.

Wu et al., IEDM 2000
Summary

- MEMS etching technology has deviated from traditional CMOS process with various etching approaches and combinations
- Complex MEMS structures require new etching capability which cannot be provided by traditional CMOS technology
- Cost & Prospective
  - Wet etching technology
    - High throughput and Low cost
    - Limited MEMS structure
    - Some may need CPD for final release with adding cost
  - Dry etching
    - Low throughput and high cost (especially DRIE)
    - Much more freedom on MEMS structure for various applications
    - Direct final release feasible with no additional cost
  - Etching rate and throughput is the key for cost-effective commercial MEMS products
  - MEMS etching is no longer limited by the CMOS process and can become a solution to some future CMOS technology