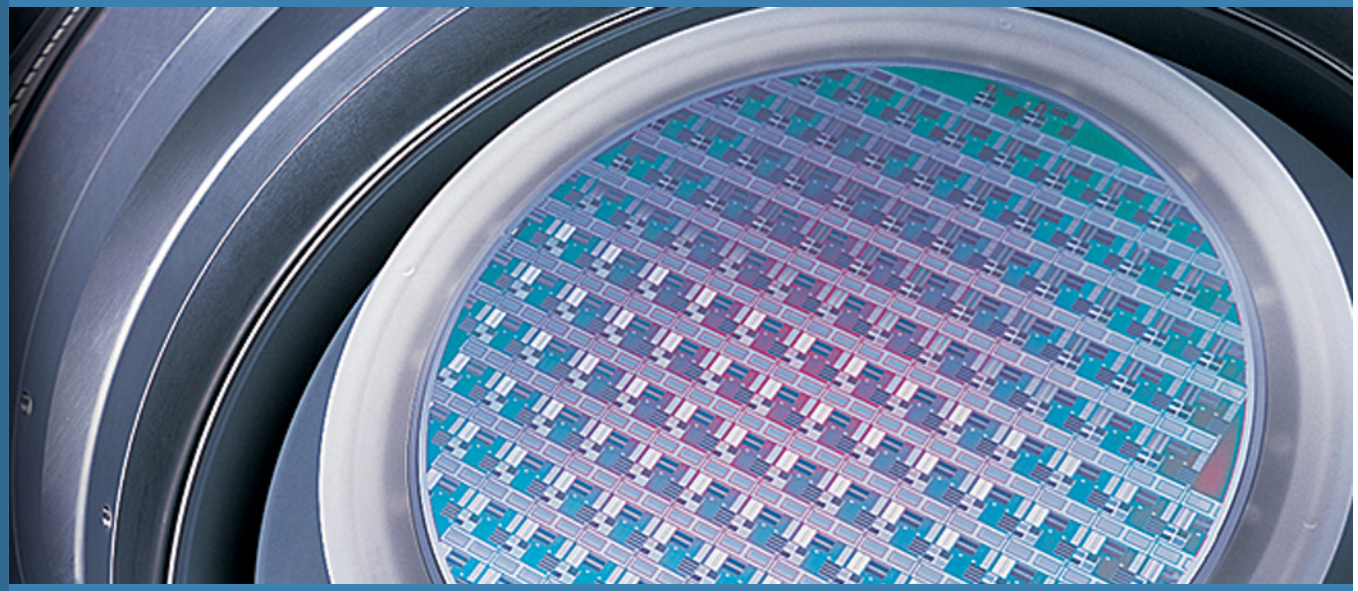
Etch Product Business Group



Plasma Induced Charging Damage: From An Semiconductor Equipment Vendor Point of View

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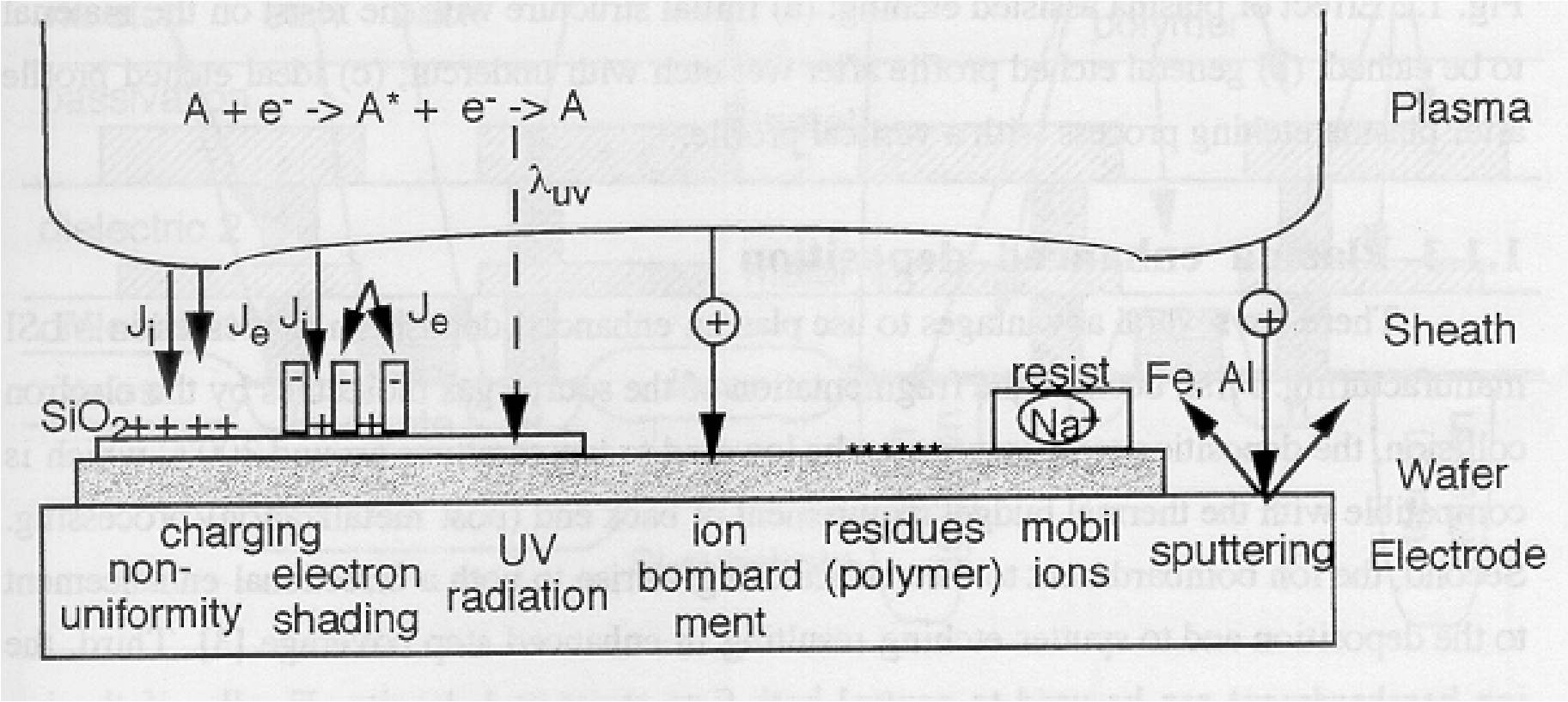
Outline and Questions

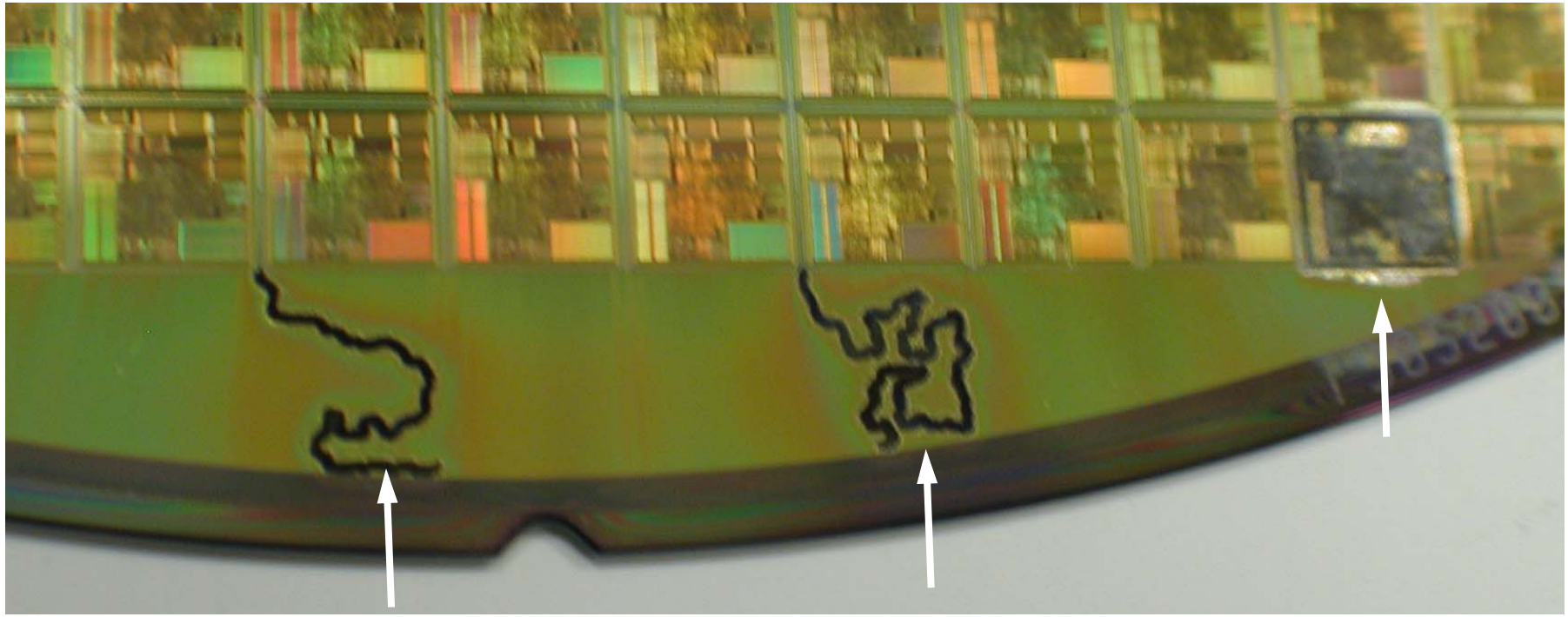
- How important is plasma charging damage?
- Who should be responsible for plasma charging damage?
- Do people really understand plasma charging damage?
- What characterization methods are used?
- Is damage getting better or worse as technology progress?
- Is it possible to make “damage free” process chamber?
- Why people talk less about this problem?
- What are the road blocks of resolving charging damage?

Plasma Process Induced Damage



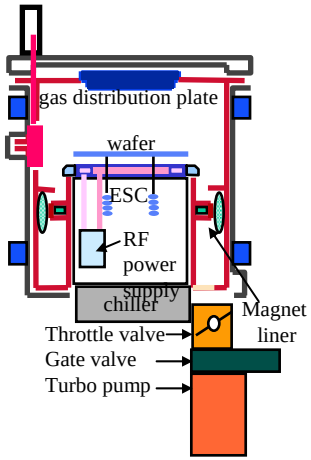
- Plasma charging damage is only one of the important plasma process induced damage phenomena
- Less than 40% for equipment vendor to work on plasma charging damage compare to other plasma damage mechanism

Definition of Wafer Arcing



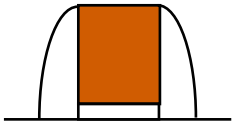
- “Snake” or “worm” type of arcing marks on wafers
- On dummy metal areas or within dies
- Results of wafer arcing: lost dies, low yield, particle increases, chamber utilization ratio decreases, operation cost increases

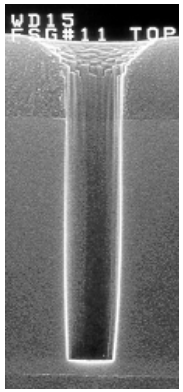
Plasma Charging Damage – Responsible Groups



Hardware
- chamber
- source
- cathode
- process kit

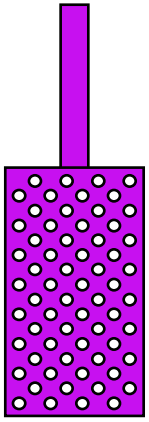
Device
- scaling
- integration
- reliability
- testing method





Process
- profile
- uniformity
- selectivity
- sequence

Layout
- design rule
- die stepping
- alignment mark
- edge exclusion

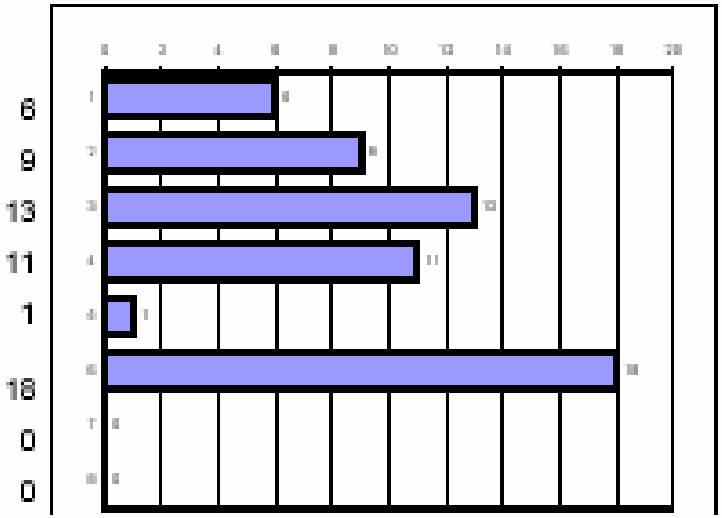


- Four different groups control plasma charging damage
- It is very difficult to understanding all details from all groups

From P2ID 2003 Industry Survey

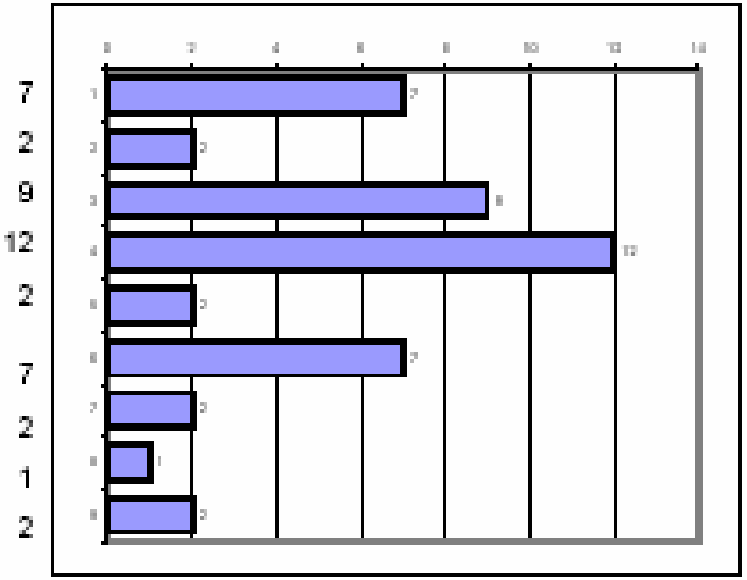
2 Who or which organization/department, do you think, actually has capability to solve PID:

- a Reliability engineer,
- b IC Circuit designer and/or CAD layout group,
- c Device manufacturer's Device or Process Integration engineer in R&D,
- d Device manufacturer's Fab Production or Process engineer,
- e Device manufacturer's Fab Yield engineer,
- f Equipment supplier's Process/Plasma equipment designer or Process engineer,
- g none of the above,
- h no comment or don't know.



3 In reality, who or which organization/department actually has burden/responsibility of solving PID:

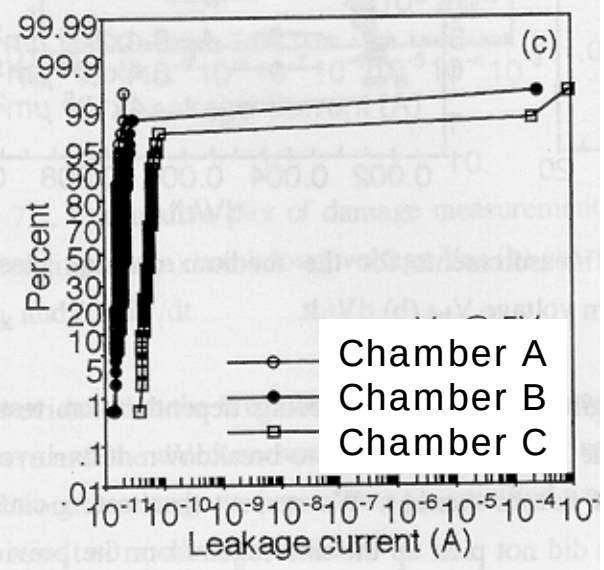
- a Reliability engineer,
- b IC Circuit designer and/or CAD layout group,
- c Device manufacturer's Device or Process Integration engineer in R&D,
- d Device manufacturer's Fab Production or Process engineer,
- e Device manufacturer's Fab Yield engineer,
- f Equipment supplier's Process/Plasma equipment designer or Process engineer,
- g The department which has least power,
- h none of the above,
- i no comment or don't know.



- Most people agree equipment manufacture has the power to fix plasma damage

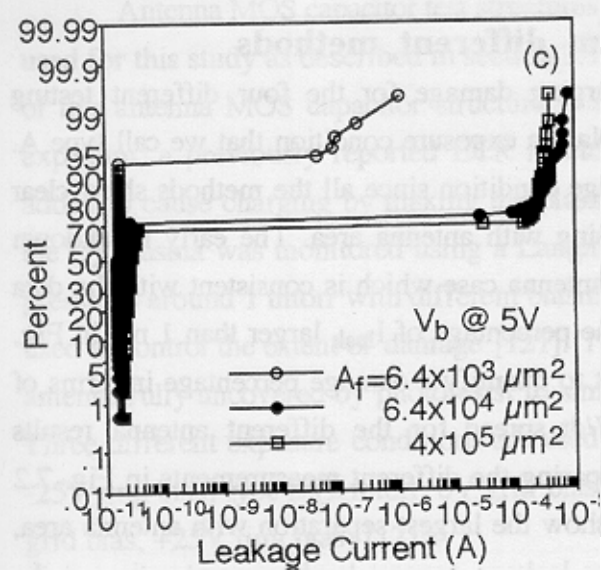
Definition of Plasma Charging Damage

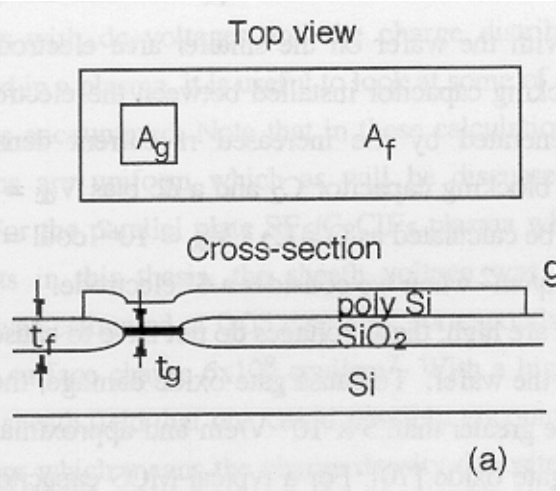
Same type device



Not plasma charging

Different antenna device





Yes, plasma charging

- Plasma charging damage measured by device degradation must increases with the antenna area or ratio increases
- Most people still does not know the fundamental definition of plasma charging damage

Role of Protection Diode on Charging Damage

- Widely use of protection diode or ESD (electro static discharge) structure reduces risk of plasma charging damage
  - Standard design for almost every logic/memory function cell
  - Local and system wide interconnect protection
  - Many IDM claimed they do not have plasma charging damage problem anymore due to this
  - Plasma induced wafer charging is still there but no damage
- Exceptions
  - When system level integration is so complicated that die size starts to be a limitation: fewer protection diode allowed in design
  - Process qualification always use test structure without protection
- For equipment vendor: antenna structure always no protection
  - Plasma charging is always a concern for all plasma tools
  - May run real product wafer with excellent yield but still suffer from plasma damage issue
  - Bottom line: what process window is needed? No one really know!

Myth and Reality of Gate Oxide Thickness

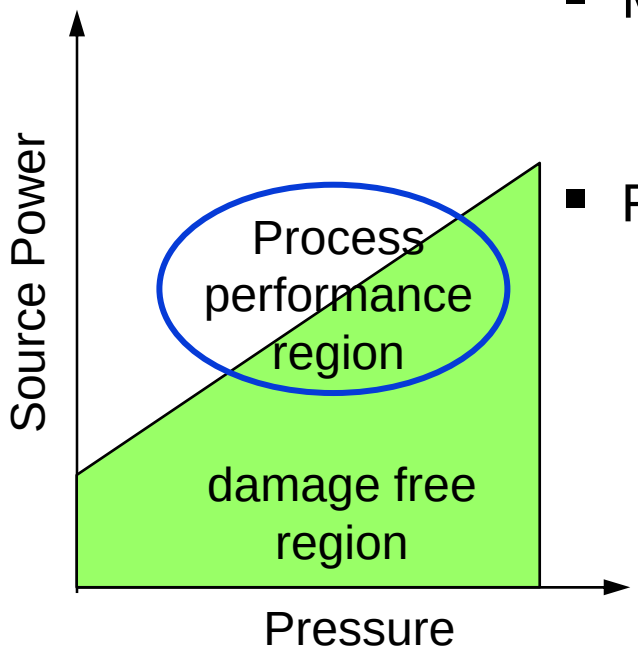
- Myth: as gate oxide thickness decreases below 30A, there are no plasma charging damage due to direct tuning through gate oxide

	Pfet	Nfet
1.6nm oxide	0.09nm	0.45nm
2.2nm oxide	0.10nm	0.55nm
5.2nm oxide	0.12nm	0.50nm

Table 1. Capacitive oxide thickness increase from moderately fluorinated to heavily fluorinated samples.

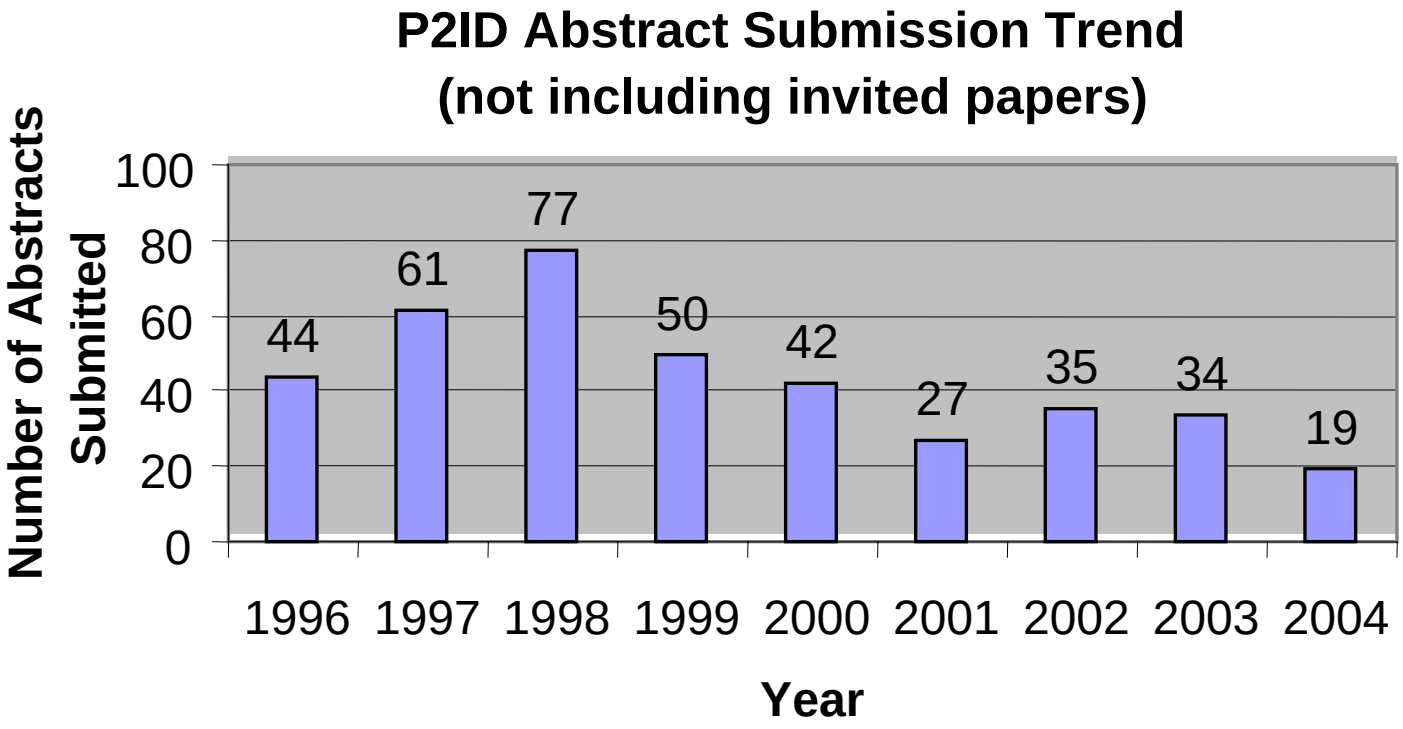
- Reality: gate oxide for the I/O circuitry is never reduced blow 40~70A because of driving current need and the oxide quality become worse due to multiple gate oxide thickness on the same chip
- Plasma charging damage always focus on gate oxide 40~70A on device test wafers

Plasma Charging Damage Performance Window



- Myth
  - So many marketing people like to use “damage free” to guarantee no damage
- Reality
  - Every plasma etcher can find plasma damage conditions
  - “Damage free” become “damage for free”
  - Plasma damage performance window is the real concern
  - Areas overlapped with process performance region are the real applicable window

Plasma Process Induced Damage Conference Paper Submission



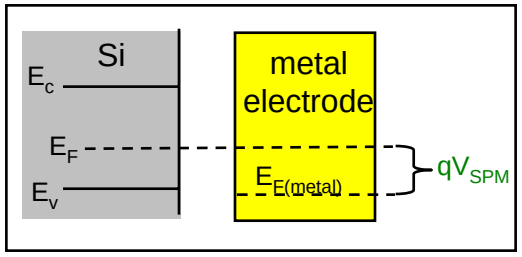
- People tend to talk less about the plasma damage over the years
- Lack of equipment vendor participation

Plasma Damage Characterization Tools

- Device Characterization
  - 200mm CHARM-2 wafers: EEPROM wafer
    - Measure threshold voltage shift after plasma exposure on various antenna EEPROM structure to calculate back local peak voltage and current during process
  - 200/300mm MOS Antenna Capacitor/Transistor wafers
    - Best for plasma damage characterization
    - **Most difficult and expensive to acquire for equipment vendor, especially 300mm!!**
- Wafer Surface Charge Characterization
  - 200/300mm CPD (Contact Potential Difference)
    - Use Blanket 1000A thermal oxide to measure residue charge before and after plasma exposure
    - Not good for oxide etch chemistry
- Chamber Characterization
  - Langmuir Probe: measure plasma density
    - Plasma density may not relate to real plasma damage
    - Can not be used in every process condition
  - Vdc Cathode: special cathode for Vdc uniformity measurement
    - Measure Vdc at different location and use ΔVdc to relate to damage

Contact Potential Difference (CPD)

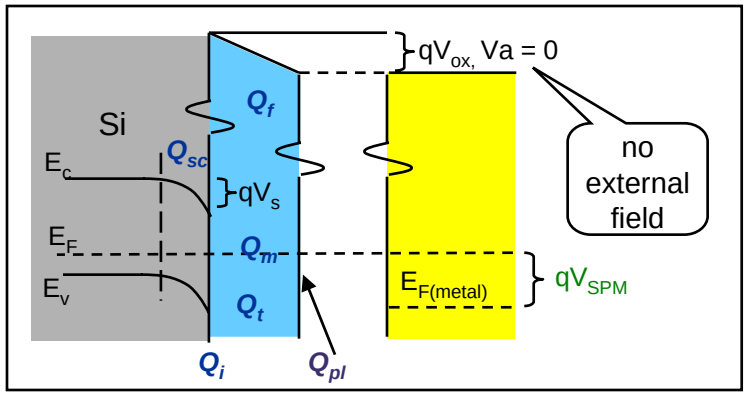
Name: PDM = CPD , concept based on the contactless work function measurement (Lord Kelvin – Kelvin probe, Monroe probe)



contact potential difference V_{SPM} = work function difference (const)

$f(E_F(Si)$, work function of the reference electrode)

space charge function relating surface barrier to the net charge



$$\mathbf{V_{SPM} = V_{ox} + V_s - const}$$

- $V_s = V_s(Q_{total})$, $Q_{total} = -Q_{sc}$

$$Q_{total} = \sqrt{2}\, kT/q\ \ \varepsilon_o\varepsilon_{Si}/L_D\ F(V_s)$$

- $V_{ox} = Q_{pl}/C_{ox} + (1-\gamma_t)Q_t/C_{ox} + (1-\gamma_m)Q_m/C_{ox}$

$$C_{ox} = \varepsilon_{ox}/d_{ox}$$

describe spatial distribution

- Non-contact capacitance measurement with Kelvin probe

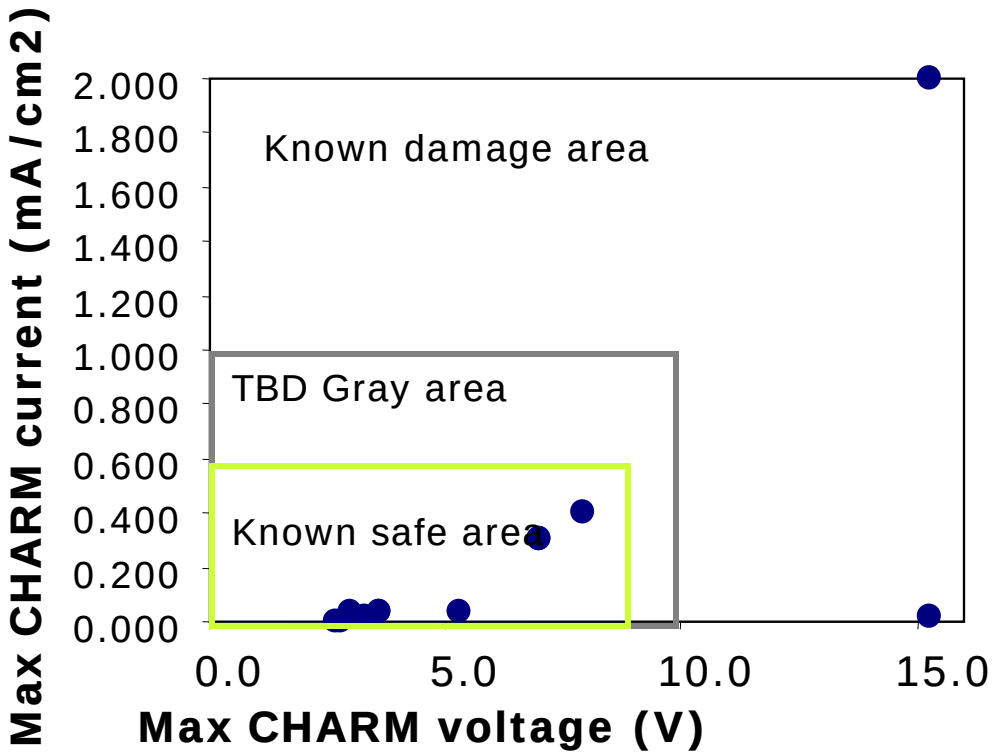
Generally Confused Nomenclature

- CPD-Contact Potential Difference
  - Correct description of the method, scientific name (like MERIE)
- PDM-Plasma Damage Monitor
  - Commercial name of this technique by some vendor who sells the characterization machine (like Super-e)
- SPM-Surface Photovoltage Measurement
  - Generic name for this measurement category
  - Mis-leading "name" for plasma damage characterization

CPD Limitation for Damage Characterization

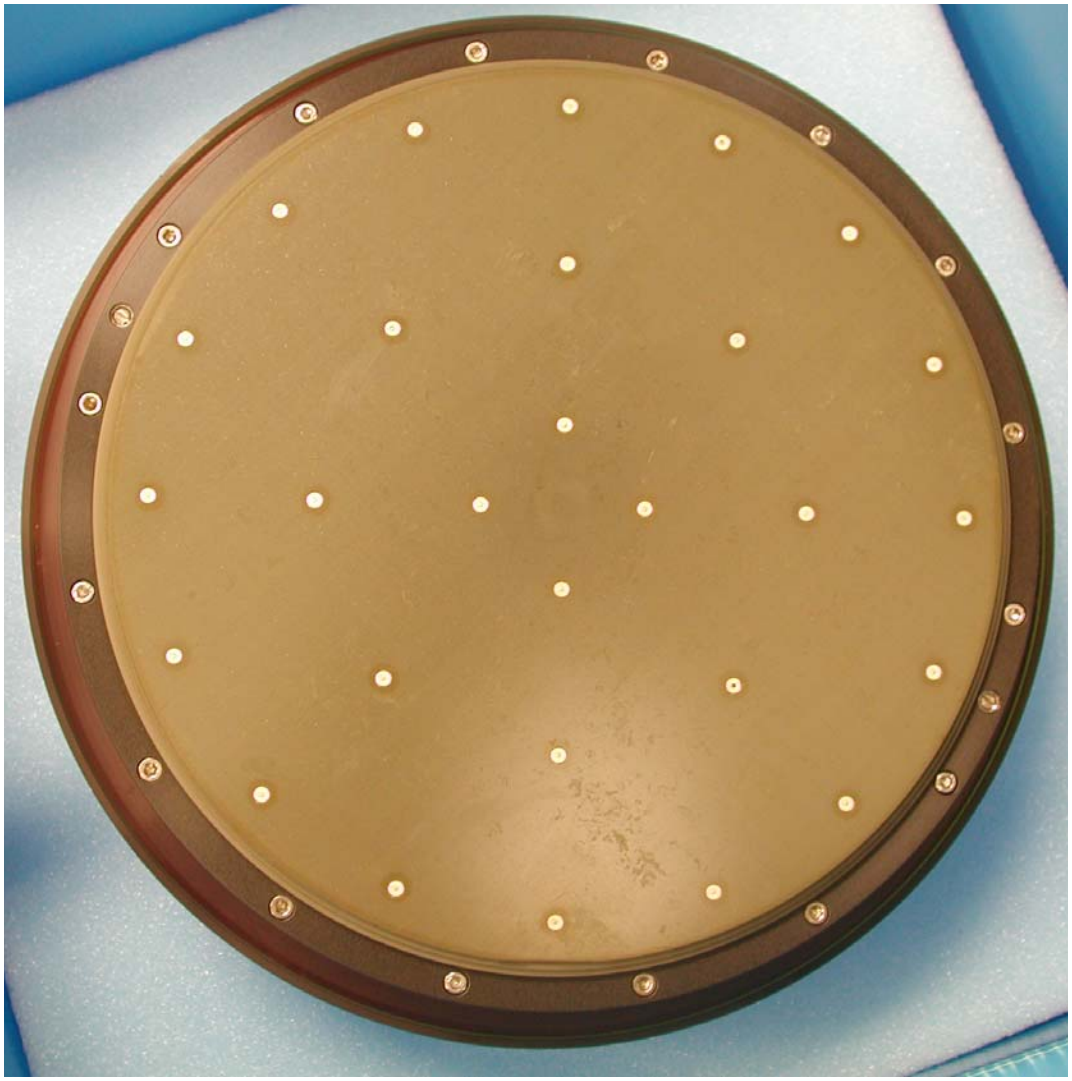
- CPD is only sensitive to the plasma status before rf is off
  - Only capture instantaneous charge deposition on wafer
  - Can not measure the “average” or “integrated” charging effect
- Measured V_{pdm} is not plasma charge voltage on wafer V_c
  - V_{pdm} is believed to be proportional to V_c which causes real damage
  - Standard deviation, maximum V_{pdm} are also good indicator on plasma induced charge deposition on wafer
- Requires calibration between V_{pdm} and the real plasma induced device damage
  - Empirical value of on-set value of V_{pdm} to see device damage is around 5V for 1000A T_{ox}

CHARM-2 Test Calibration to Device Damage



- CHARM wafers results are consistent with device wafer results
- Expensive and only 200mm wafer available

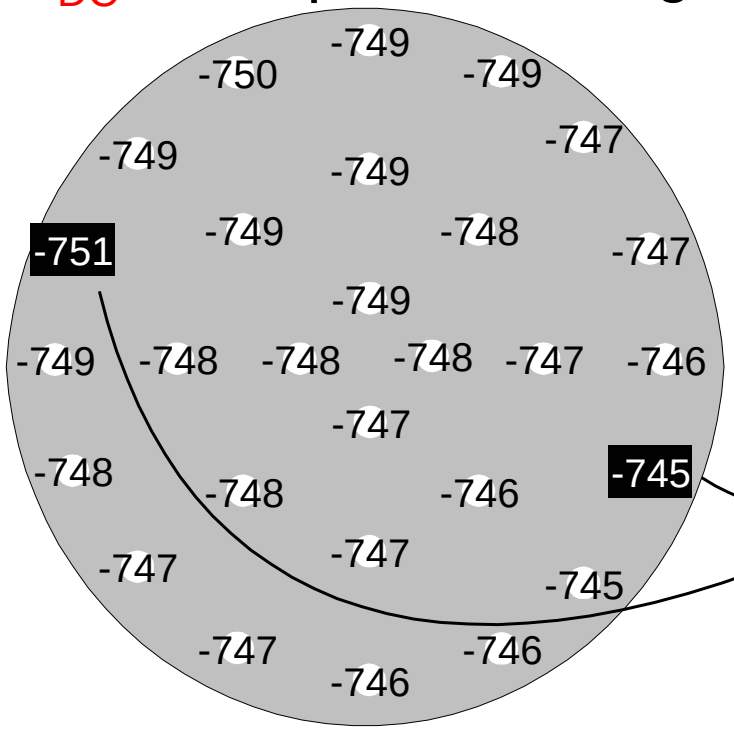
300mm eMAX ΔV_{DC} Cathode

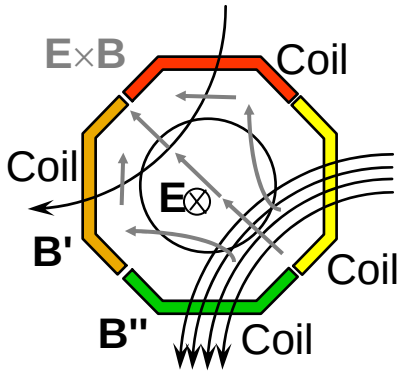


- Fully swappable with standard rev.2 eMAX cathode
- Bias voltage measured using 100 MΩ / 200:1
- Resistive dividers and computer data acquisition system
- Tested up to 3200W cathode power and -2000V DC bias
- Withstands large variations in DC bias across the pedestal

ΔV_{DC} Data Analysis

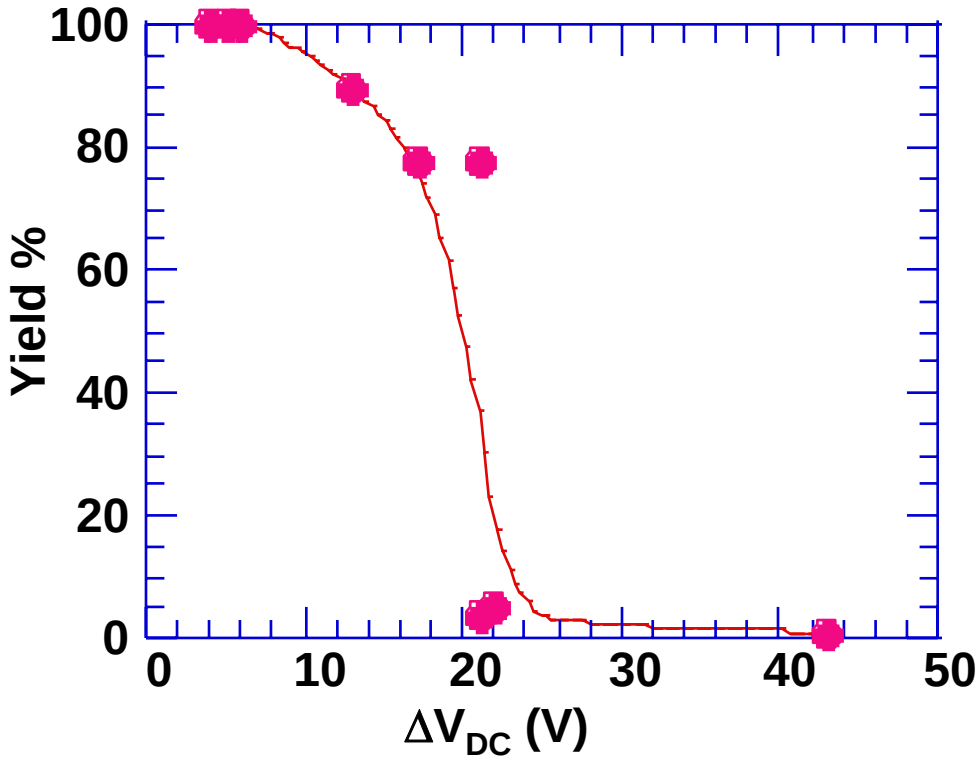
- $\Delta V_{DC} \equiv V_{DCmax} - V_{DCmin}$
- ΔV_{DC} repeatability (1σ) ~ ± 3 V
- ΔV_{DC} has been identified to be the driving force of damage
- ΔV_{DC} is not plasma charging voltage V_c, but proportional to



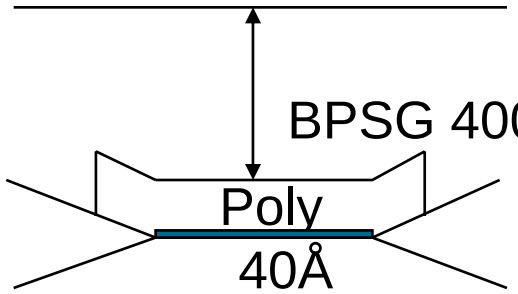


ΔV_{DC} = -745 V -751 V = 6 V

Previously Established Critical ΔV_{DC} Threshold and Device Plasma-Damage Yield Relationship



Poly Antenna MOS capacitor structure for oxide etch back process



Antenna Ratio 333333:1

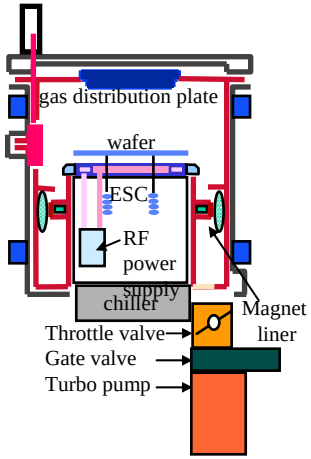
Performed on 200mm eMAX™

- Threshold of ΔV_{DC} is ~15-20V for plasma damage
- Threshold voltage depends on customer's device

Limitation of Equipment Vendor to Work on Plasma Charging Damage

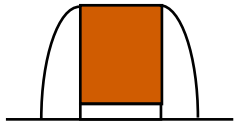
- In general, it is very difficult for equipment vendor to discuss plasma damage
  - Any public “damage” materials can be used by competitor’s as negative marketing purpose
    - Amazing brain-washing technique
  - Only after solution has been found then the issue can be discussed outside
- Availability of device test wafer is always an issue
  - Chicken or egg first issue: equipment development or test wafer for charging damage
  - Must rely on internal characterization tools but still needs calibration to the device wafers
  - Cost of device wafers is still a concern

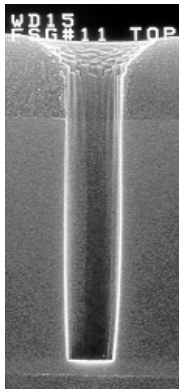
Plasma Induced Damage-Missing Links



Hardware
- chamber
- source
- cathode
- process kit

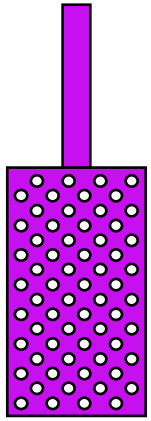
Device
- scaling
- integration
- reliability
- testing method





Process
- profile
- uniformity
- selectivity
- sequence

Layout
- design rule
- die stepping
- alignment mark
- edge exclusion



- Needs all the links to resolve plasma damage problem

Conclusion

- Plasma charging damage is a permanent issue for all plasma processing chamber: no one can claim “damage free” chamber
- Most people still do not understand plasma charging damage
- Availability of device wafer (especially 300mm) for damage characterization is the biggest issue for equipment vendor to evaluate plasma damage
- People often use wrong method to measure plasma charging damage to get wrong conclusion
- It is still a long way to go to resolve plasma charging damage
- Four groups of people (equipment, process, device and design) need to work together to resolve plasma charging damage issue. Neither one of them can resolve it alone.

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