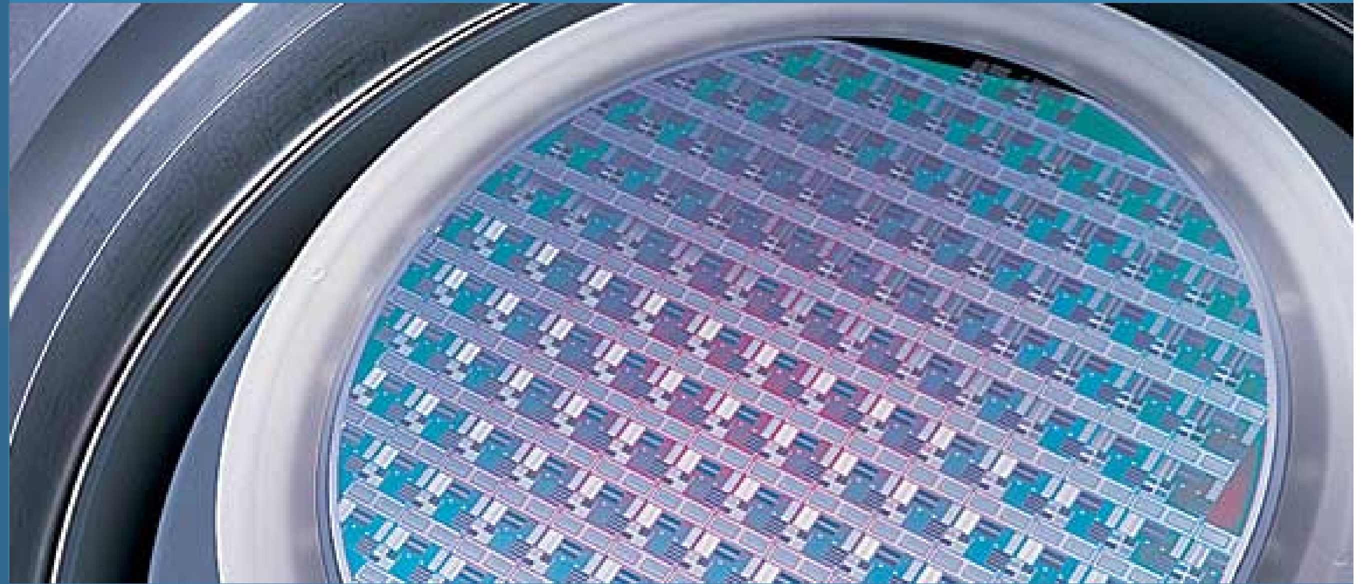


Integrated Dual Damascene Etching for 65nm Technology and Beyond

Yan Ye, Ph.D.
Dielectric Etch Technology Development
Applied Materials,
PEUG Meeting, Aril 13, 2004

Content

- Trends in dual damascene development
- Integrated dual damascene etch process
- Challenges for integrated etch process.
- Feasibility of integrated dual damascene etch process.

Integrated etch process is one of major challenges for dual damascene etch applications of 65nm technology and Beyond

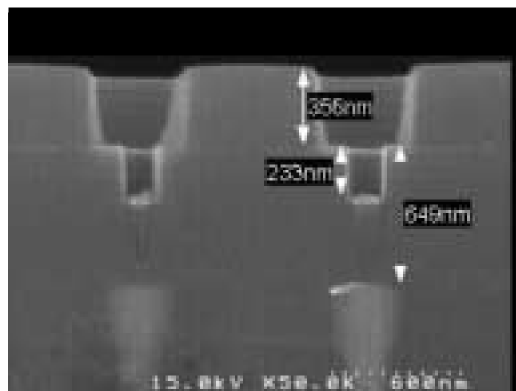
Low-K Dual Damascene Trends Observed

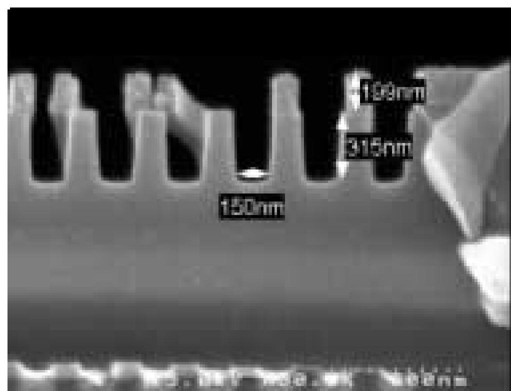
Trench First	**Via First**	**New DD structure?**
Via first	Trench first	Via First

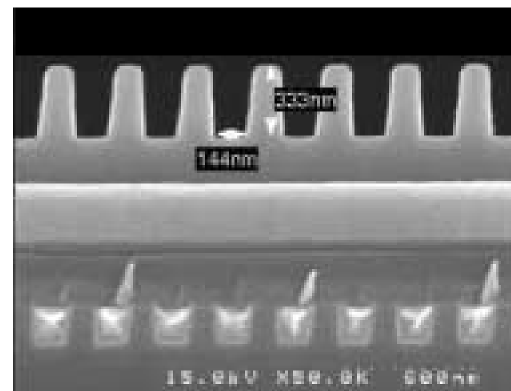
Both low-k material and lithography are the driving forces for new dual damascene schemes

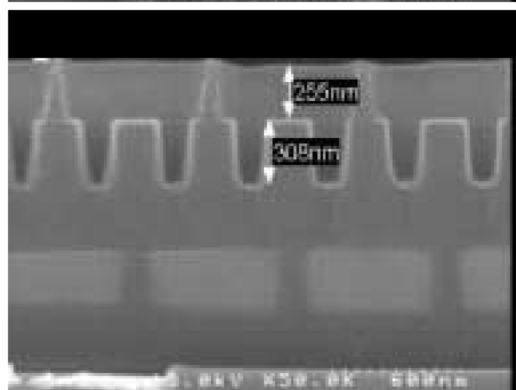
BARC Etchback Approach

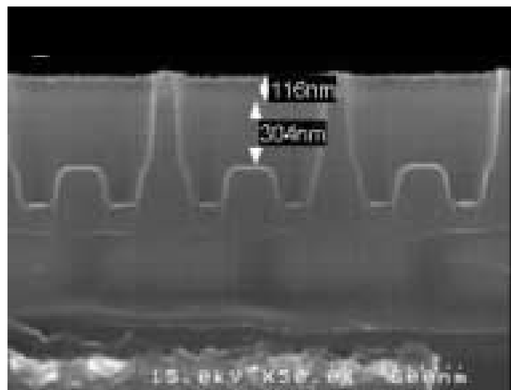
Pre	M2 etch	Ash+ Barrier open

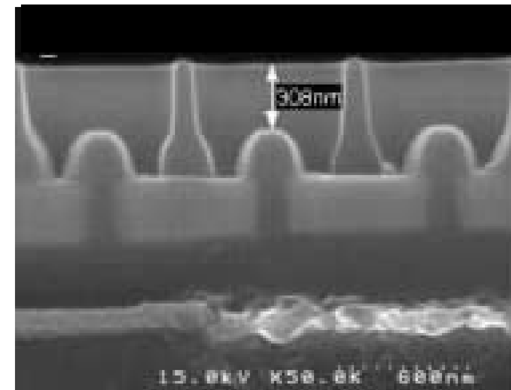




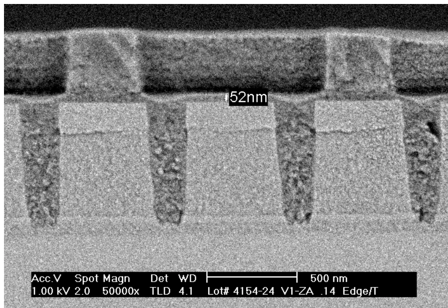
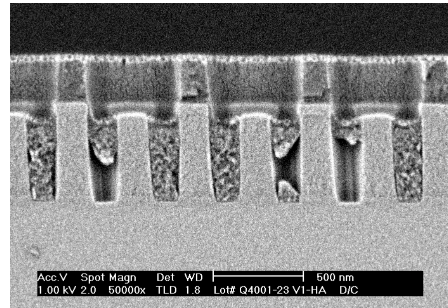
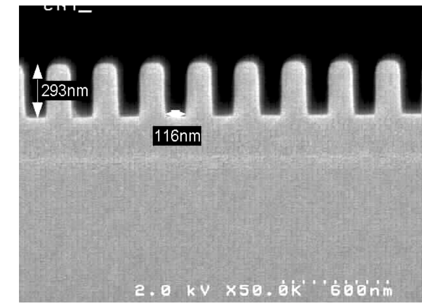
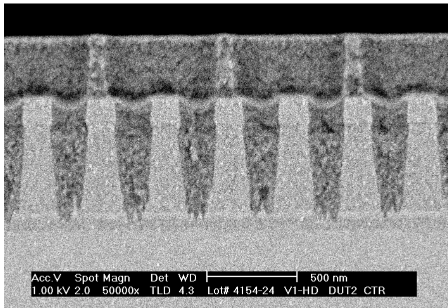
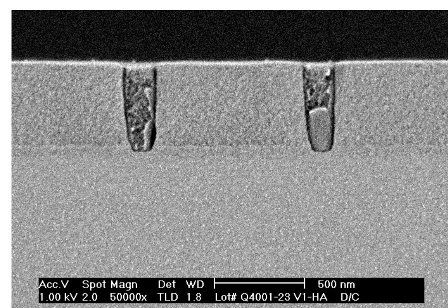
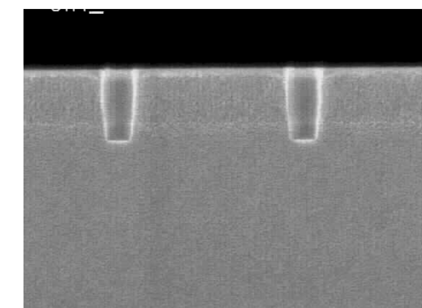






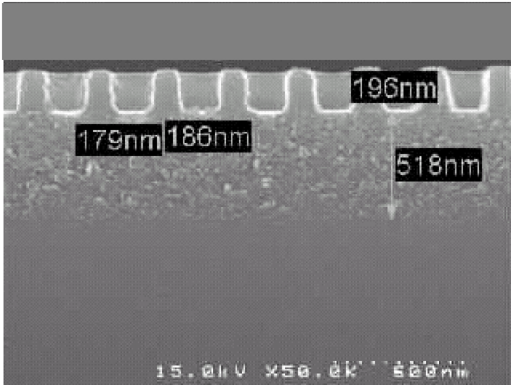


Dual Damascene with Full-Filled BARC

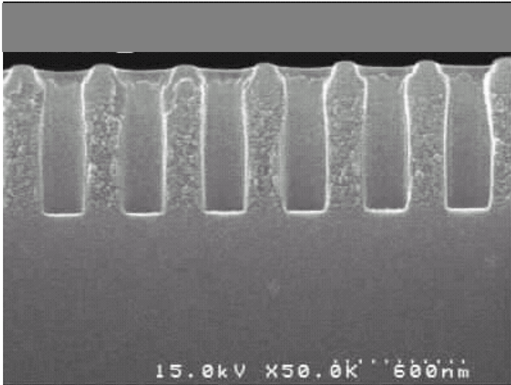
Pre	BARC etch	M2 etch 2
		
		

Dual Damascene with Bi-layer Resist

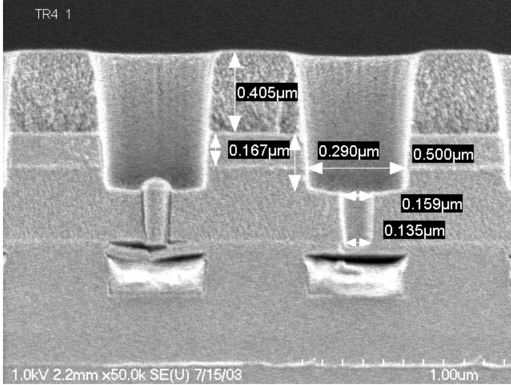
Pre



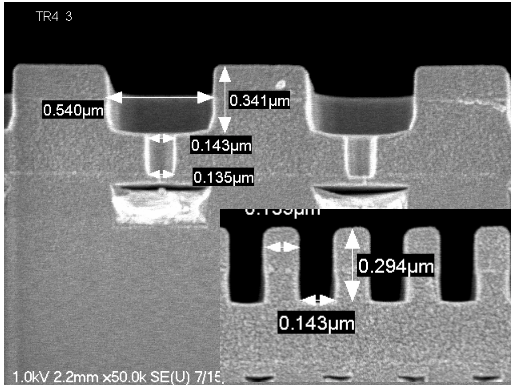
Mask etch



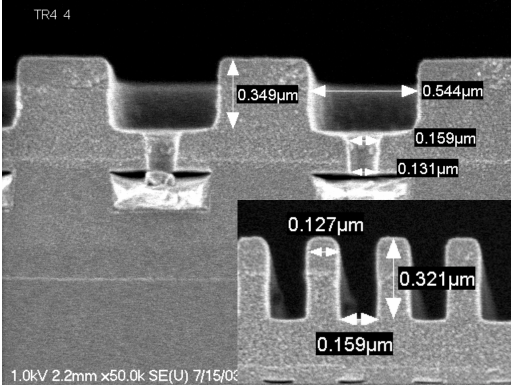
Trench etch



Ash

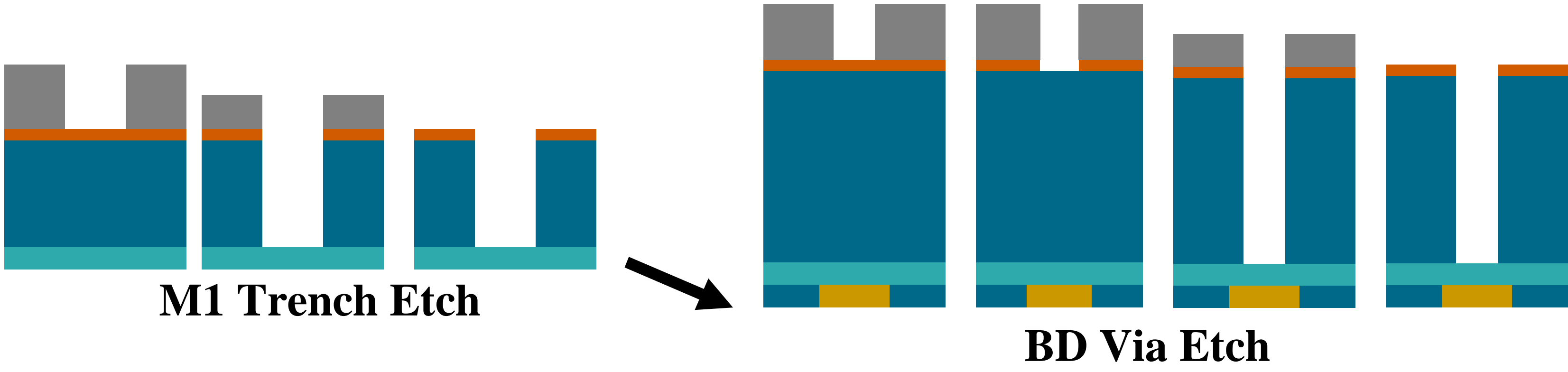


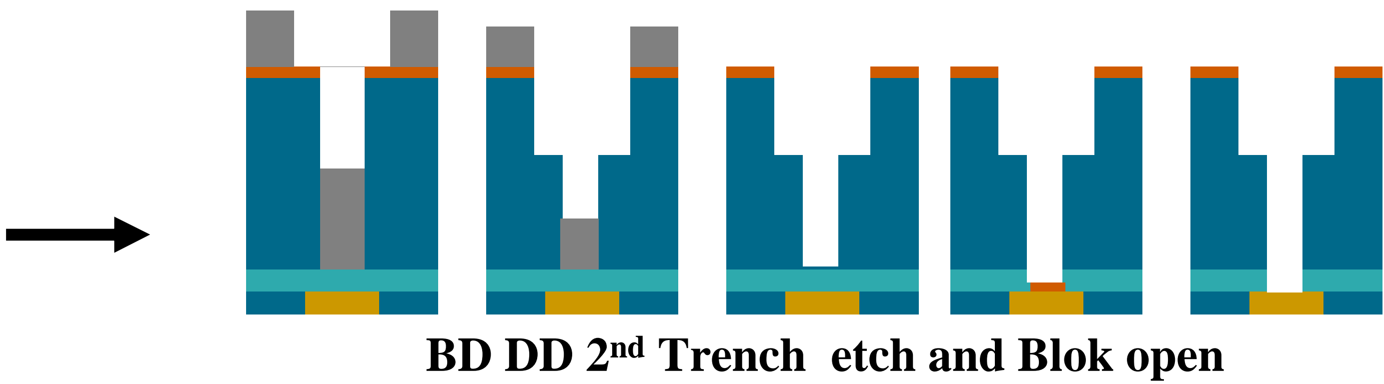
Barrier open



Why Integrated Etch Process is Needed

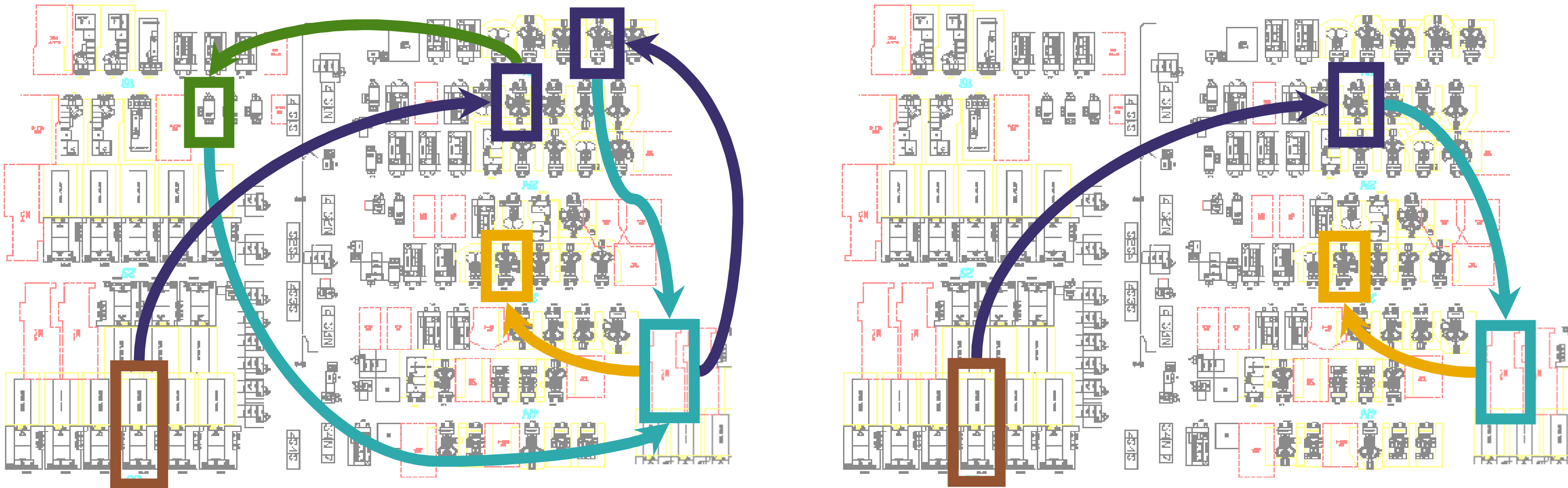
Low-K Dual Damascene Process





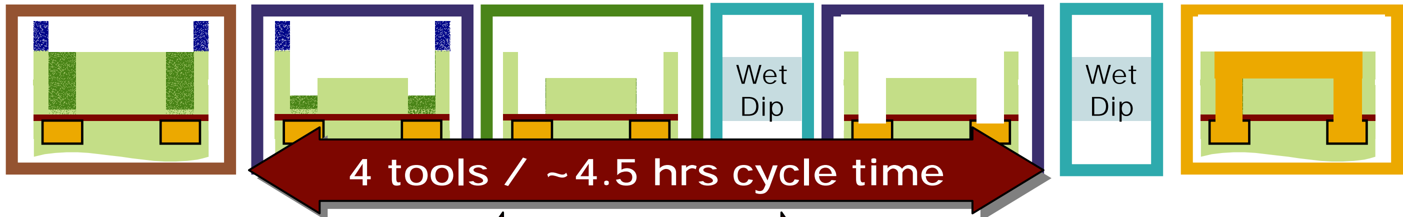
Enabler: Cycle Time Advantage

Representative Fab Layout



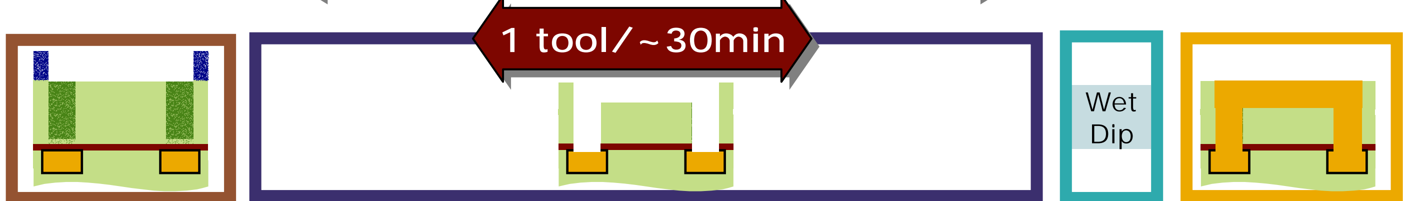
Lithography | *Trench Etch* | *PR Strip* | *Dip* | *Barrier Open* | *Dip* | *Cu Deposition*

Traditional Etch Scheme



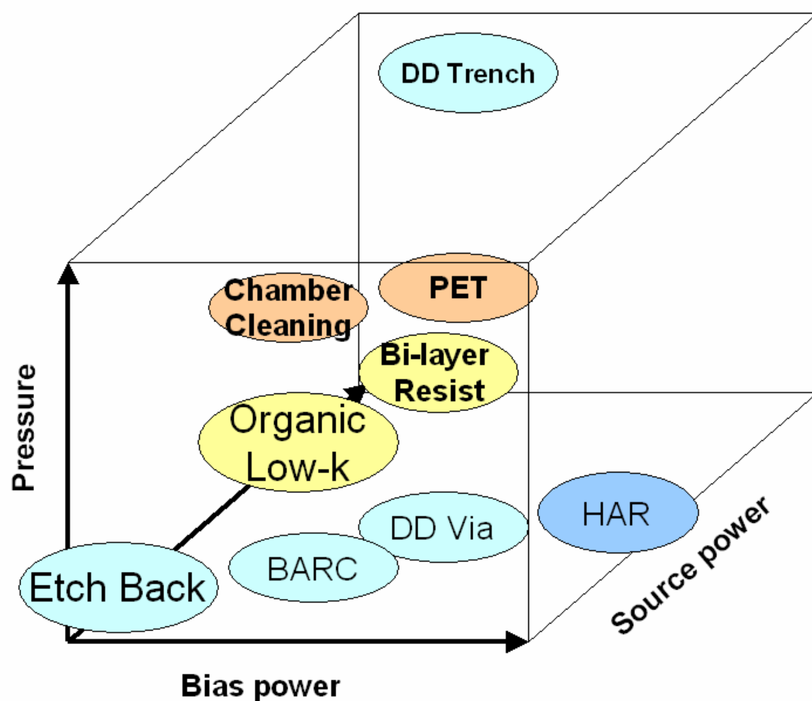
ENABLER

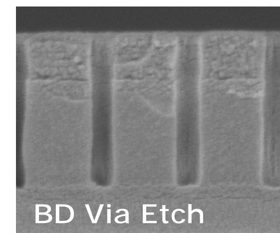
All-in-One

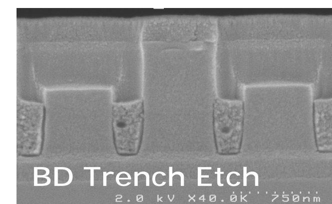


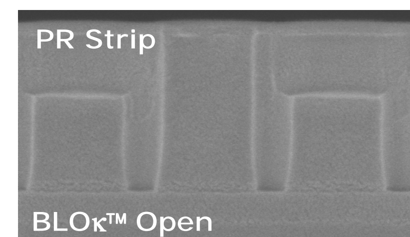
Challenges Faced For Integrated Etch Process

Large Operation Window is Required for an All-in-One Dual Damascene Process



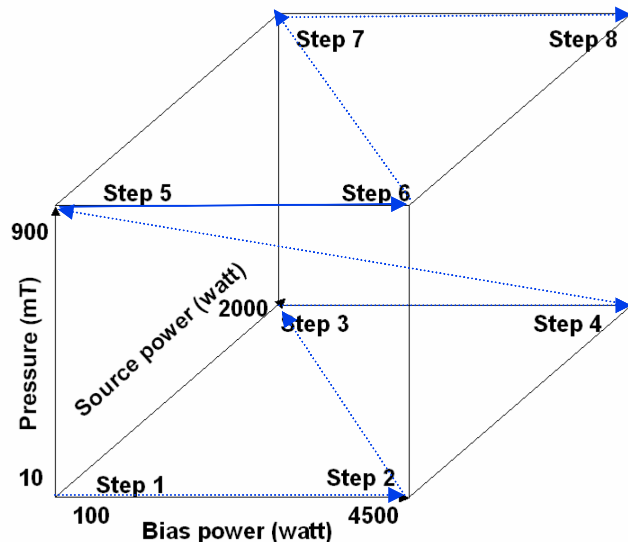




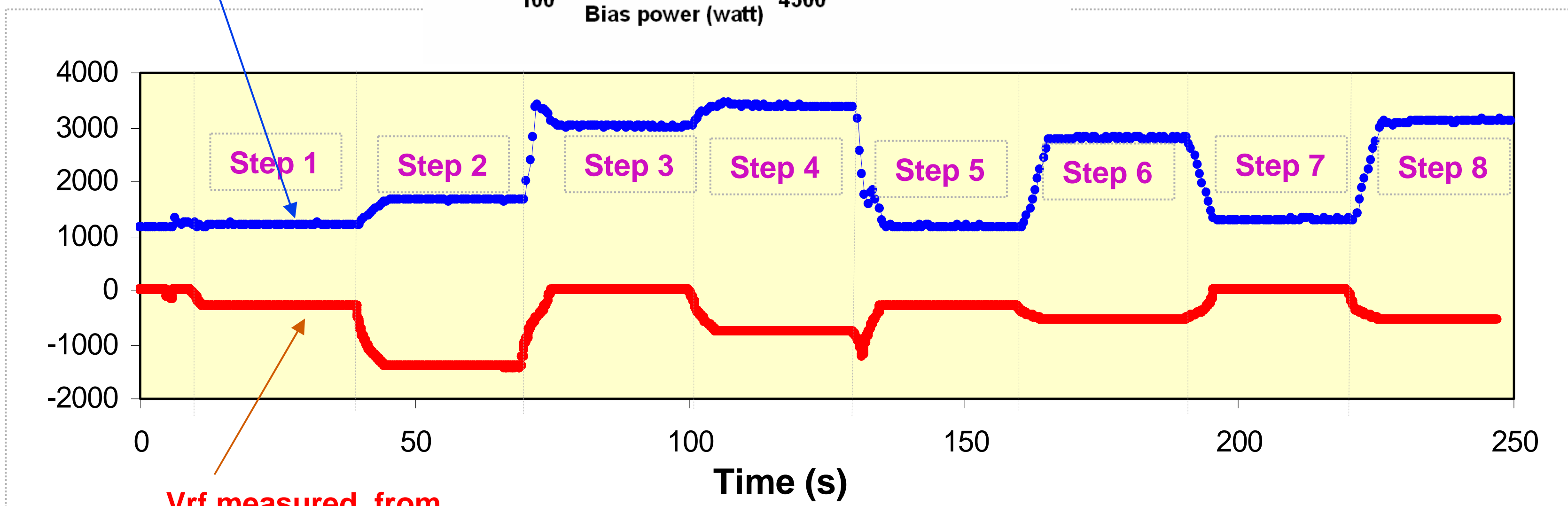


Etch of Diverse Low-κ Materials and Integration Schemes is Required

Fast transition between steps is Required for an All-in-One Dual Damascene Process

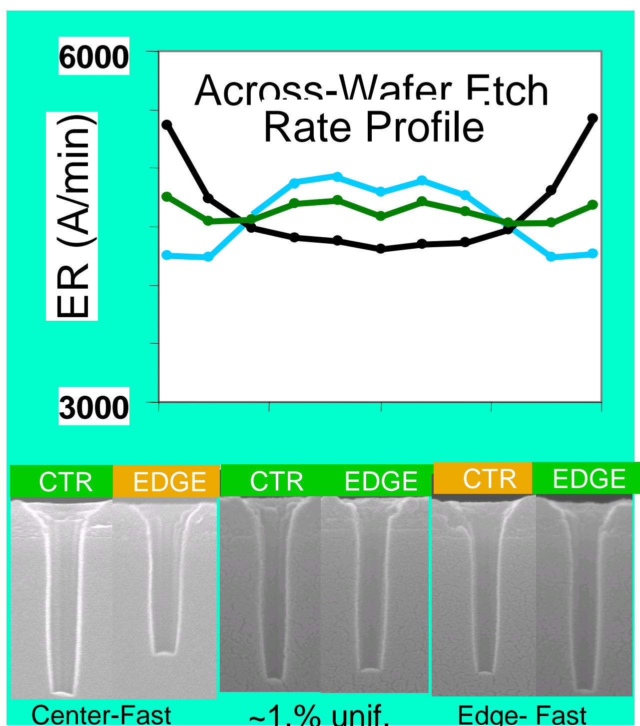


500O2/10-900mT/
100-4500Wb/0-2000Ws

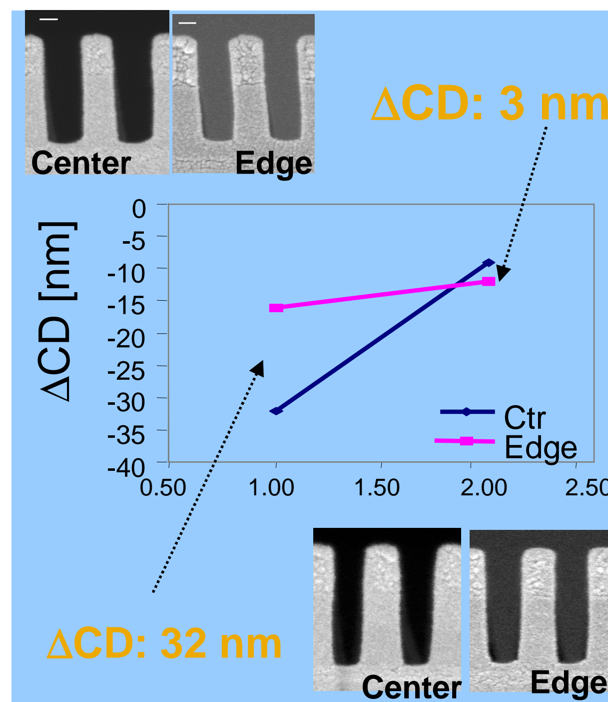


All-in-1 Process Requires Tunability for Both Charged Species and Neutral Species Distribution in Each Step

Effect of Charged Species Distribution Tuning



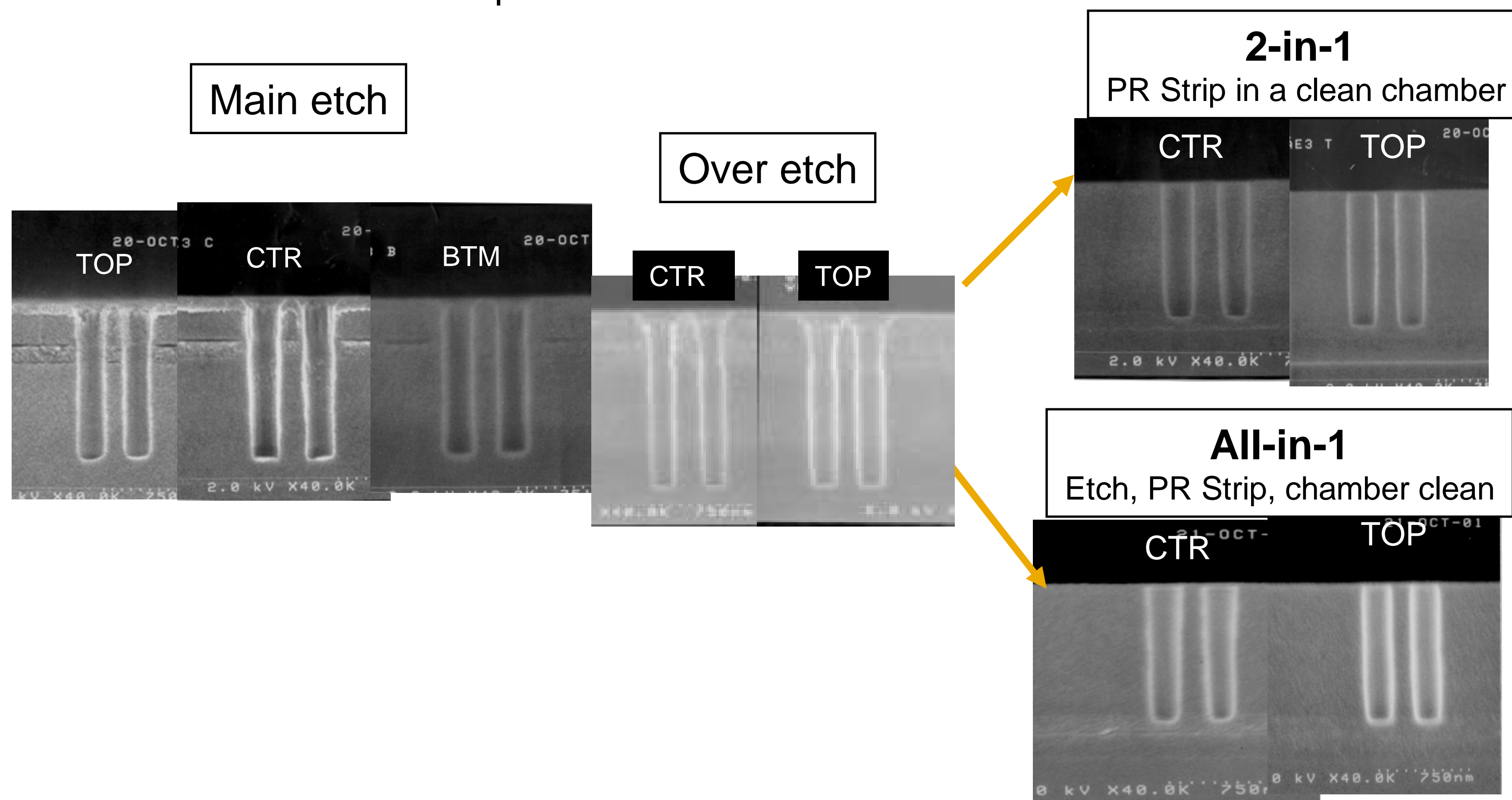
Effect of Neutral Species Distribution Tuning



Independent control of both charged and neutral species distribution is necessary to achieve complete tunability of etch rate uniformity and profile/CD uniformity

Integrated Etch Process Requires Process Transferable:

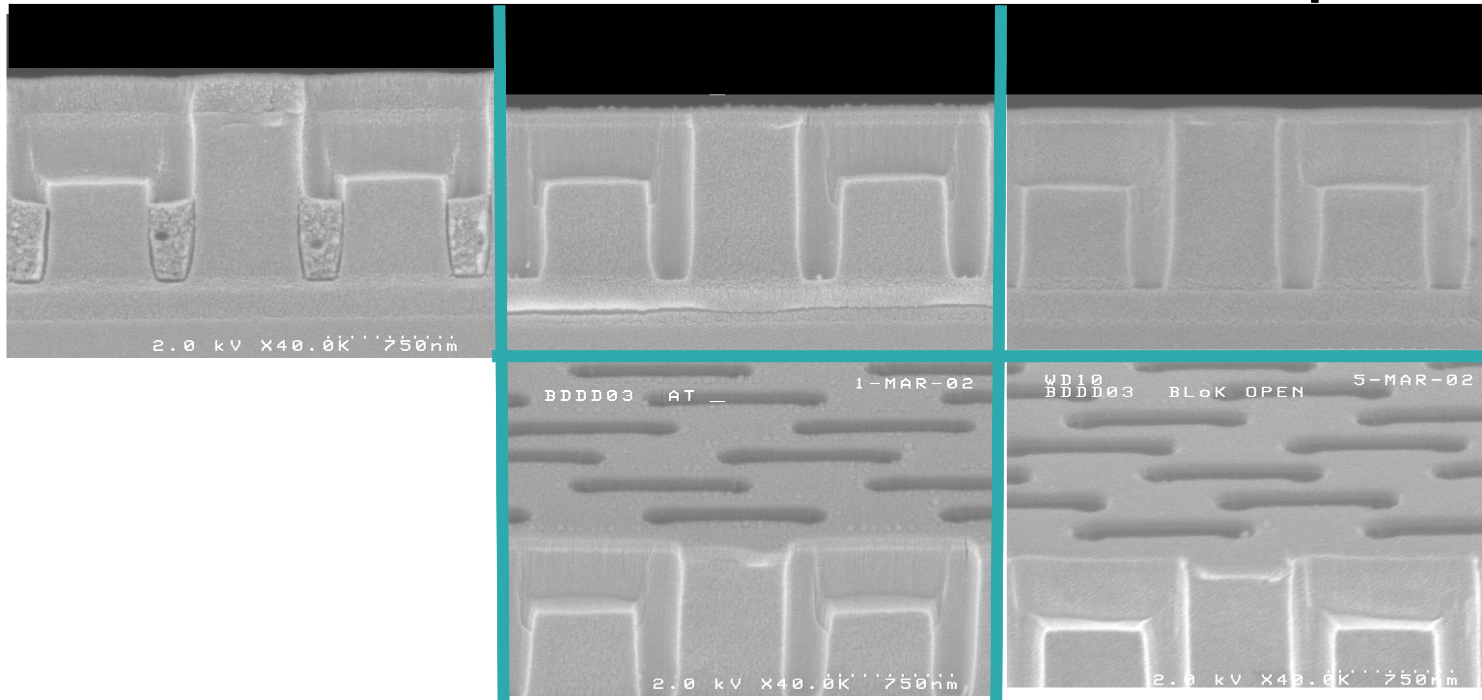
All-in-1 via etch comparison with 2-in-1 etch



Identical process performance is required

Feasibility of Integrated Etch Process

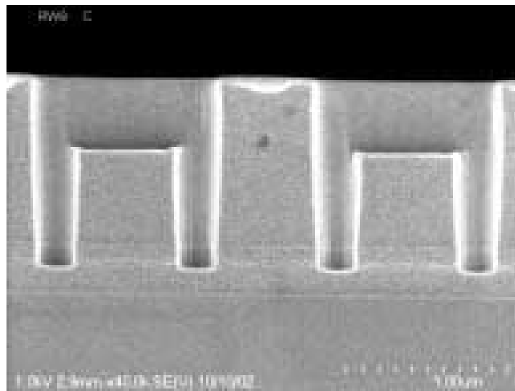
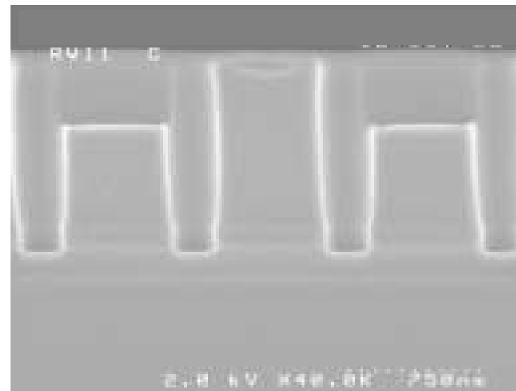
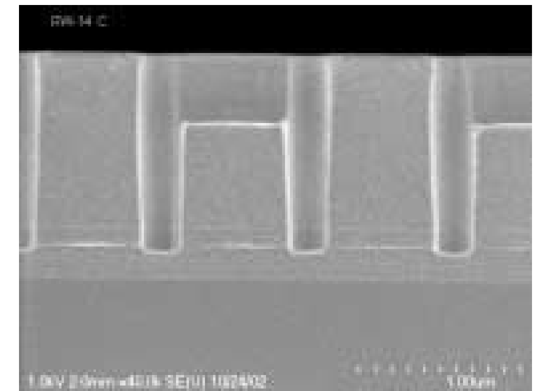
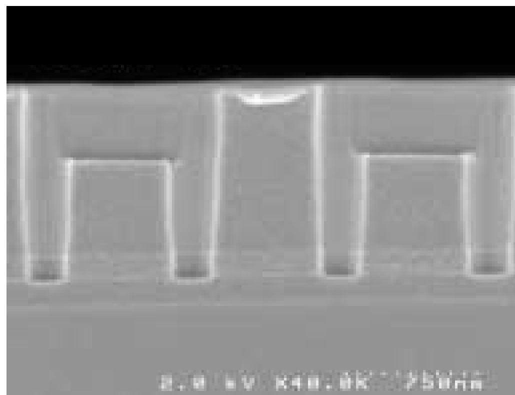
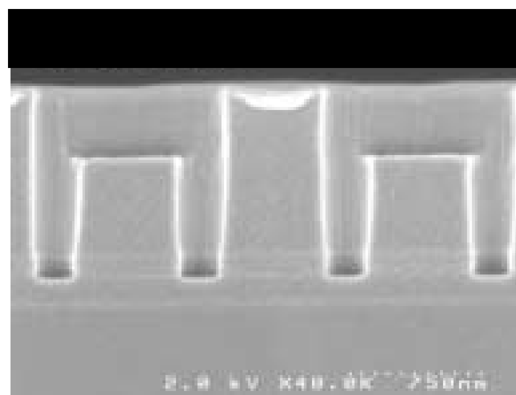
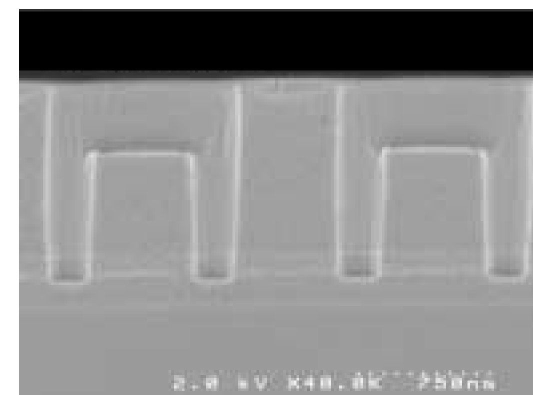
Integrated BD Dual Damascene M2 Trench Etch



All-in-1 BD Dual Damascene Trench etch is Demonstrated

All-in-1 Low-K Film Integrity Repeatability Test:

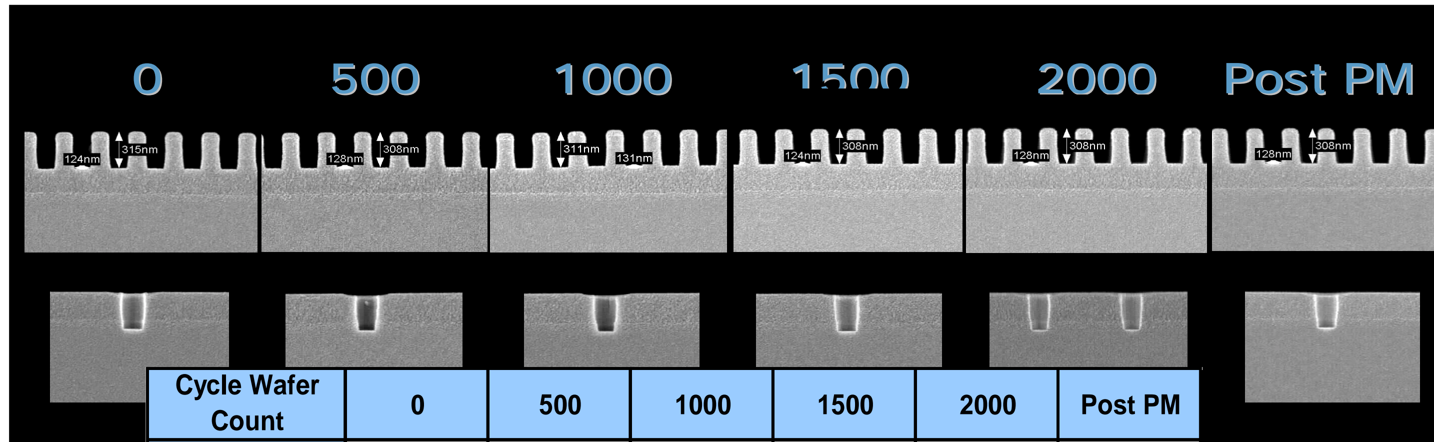
BD I M2 etch profile after ash & HF dip

	Wafer #1	Wafer #200	Wafer #1000
Ash			
HF Dip			

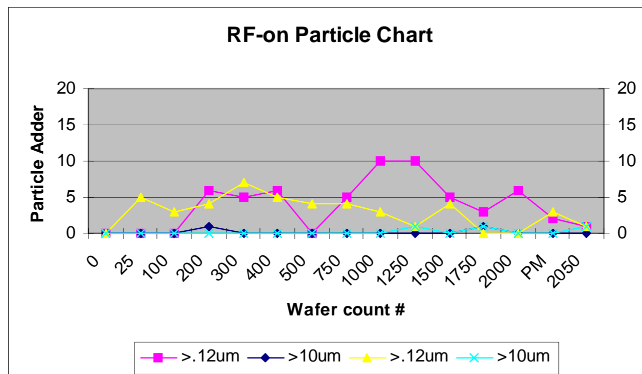
No Low-k film integrity change in 1000 wafer burn-in

2000 Wafer Burn-in Result for All-in-1 BD M2 Trench:

Process and Particle Performance



Cycle Wafer Count	0	500	1000	1500	2000	Post PM
Fence (A)	0	0	0	0	0	0
U-loading (%)	-2.6	-1.6	-2.9	0.3	-0.6	-2.1
ED (A)	3180	3120	3180	3080	3100	3100
NonU(%)	3.3	1.8	2.9	2.4	1.1	2.4

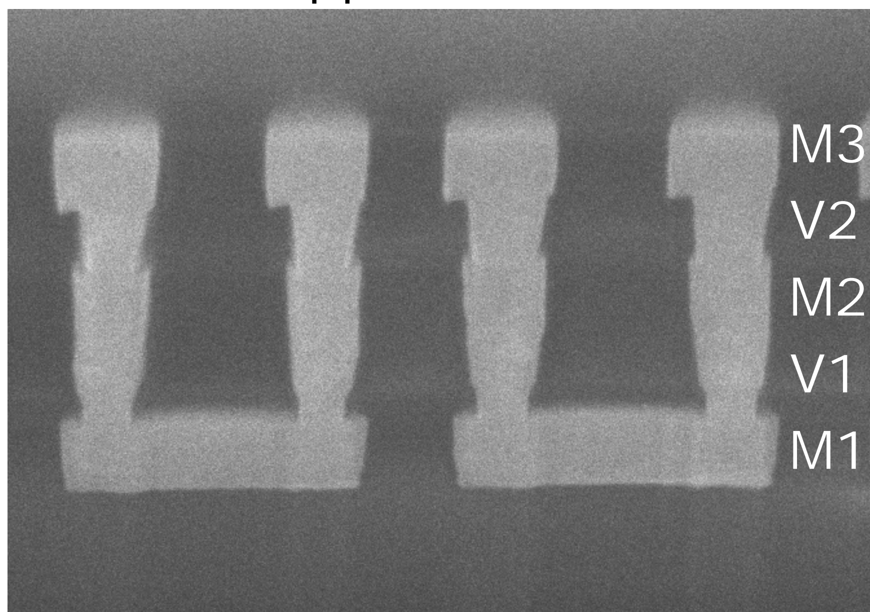


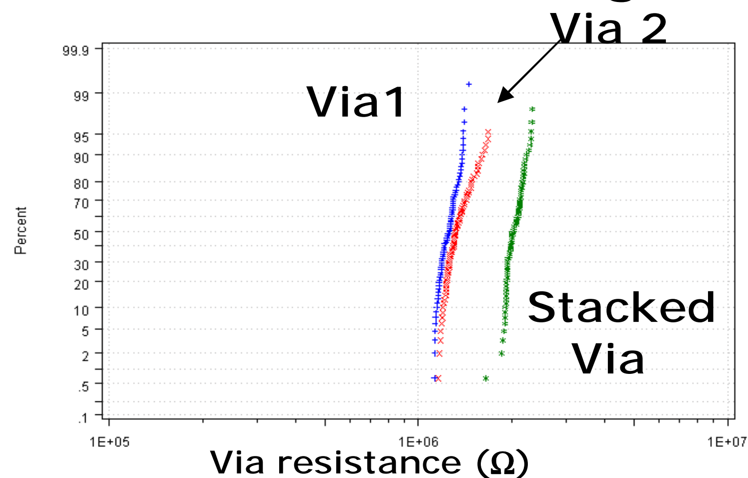
The average particle adders are 3.9 and 2.9 for >.12um and >0.20um

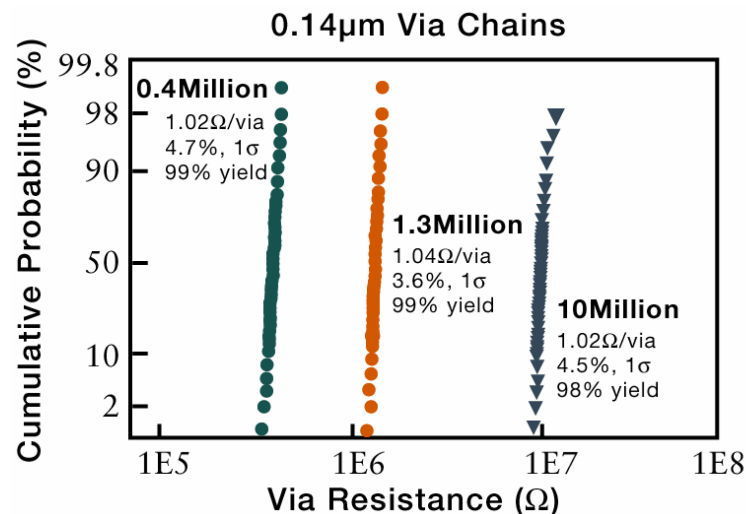
Process and particle performance are stable through 2000 wafers burn-in.

3 Level Metal Copper BD Interconnect Built Through Integrated Etch process

3 level Copper Interconnect



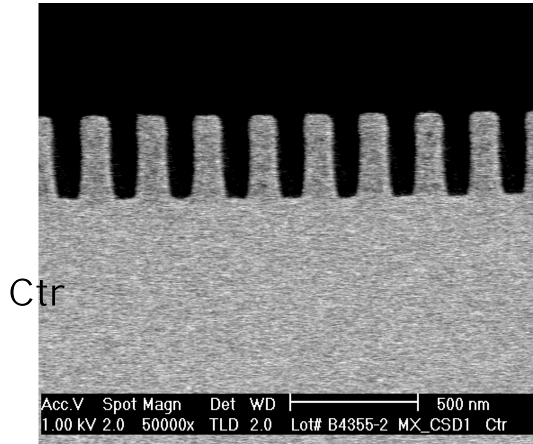




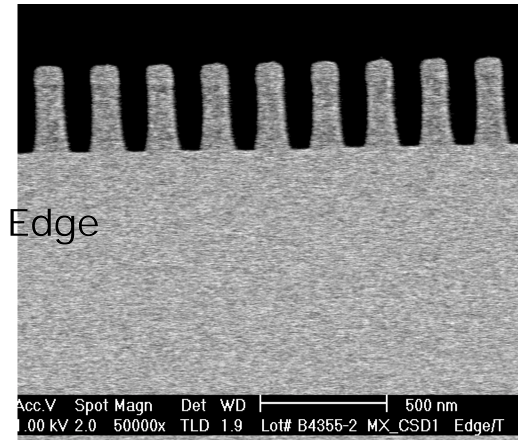
3 level Copper Interconnect with 95-99% yield 10 Million via chain as well as stacked 1 Million Via Chain

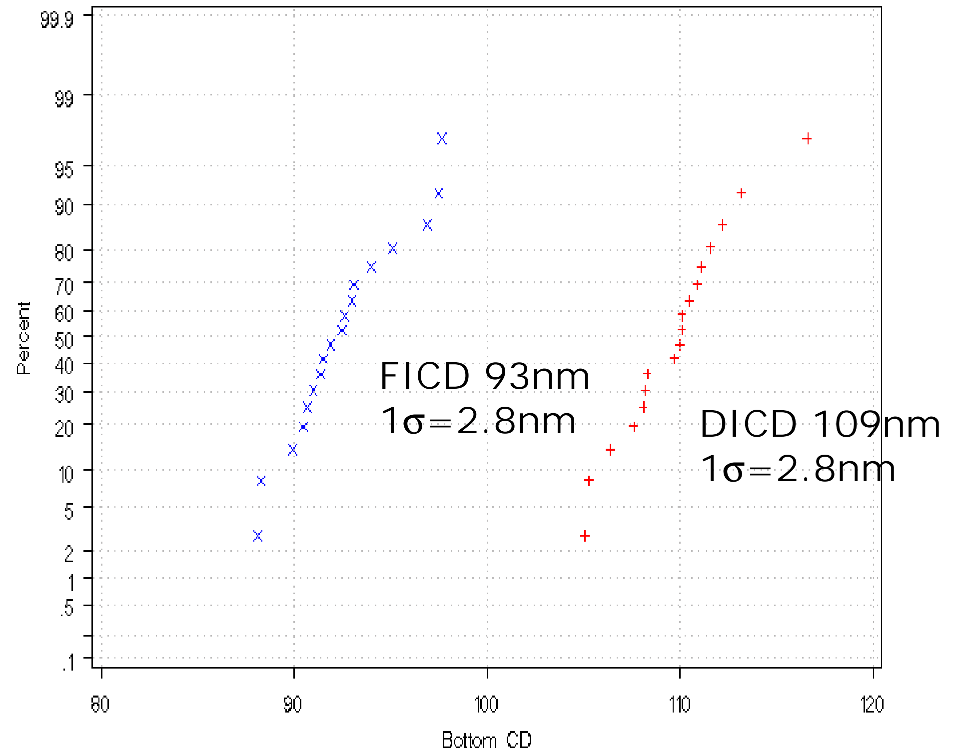
All-in-1 CDO (k~2.3) Trench Etch with 193nm PR

Ctr



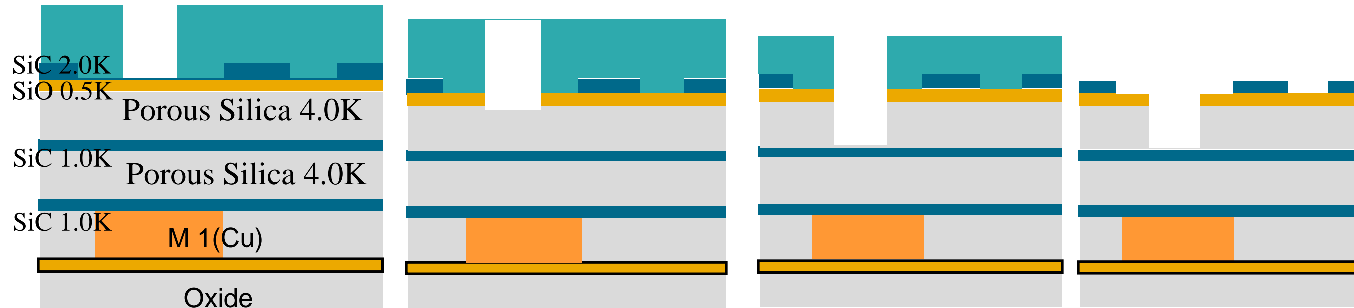
Edge

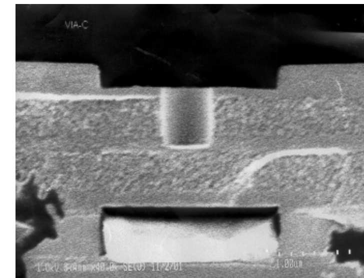


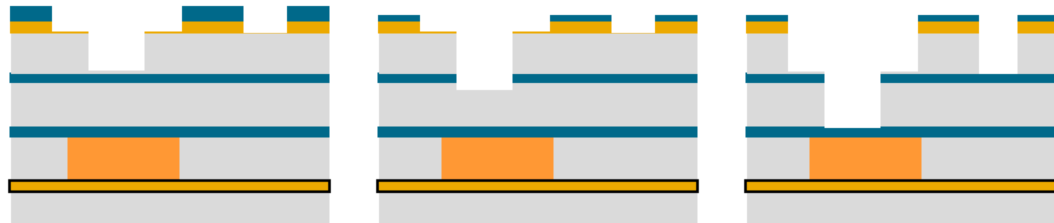


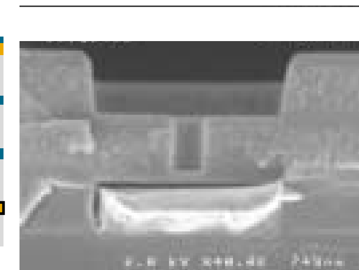
APPLIED MATERIALS®

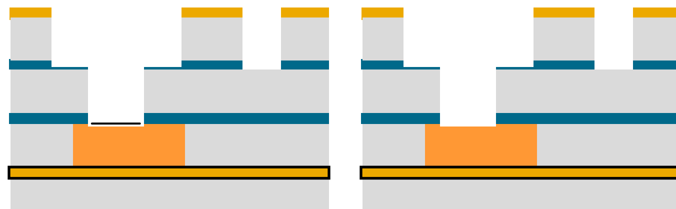
Integrated Porous OSG (ELK) Etch

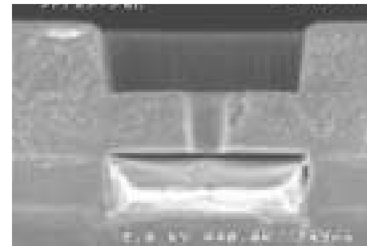




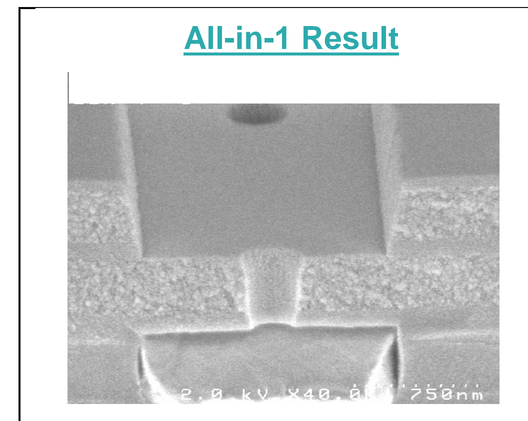








All-in-1 Result

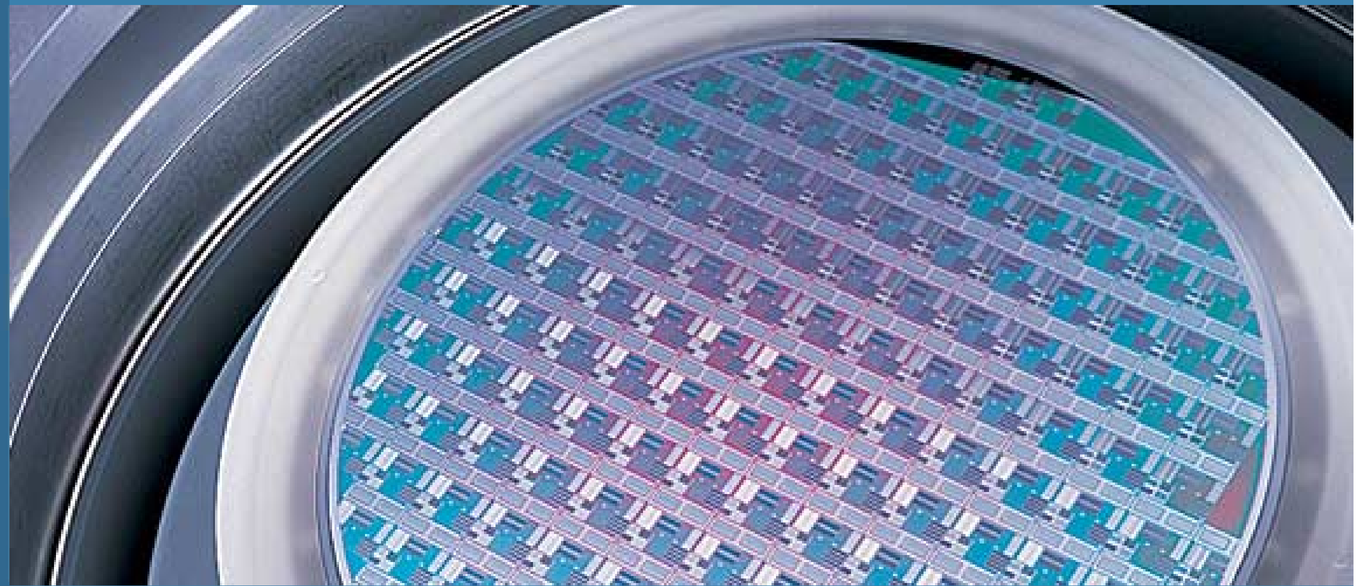


Demonstrated all-in-1 capability

Summary

- Requirement for integrated dual damascene etch processes has been observed. It requires new etch tool with large process window, better tunability for both charge species and neutral species in each step, smooth step transition, effective clean without low-k film damage, and so on. Feasibility to achieved required etch performance for several integrated dual damascene scheme has been demonstrated.

Etch Products Business Group



APPLIED MATERIALS®