Dual Damascene Etch; Challenges at the 65nm Node and Beyond

Makarem Hussein
Portland Technology Development
Intel Corporation
email: makarem.hussein@intel.com

intel®

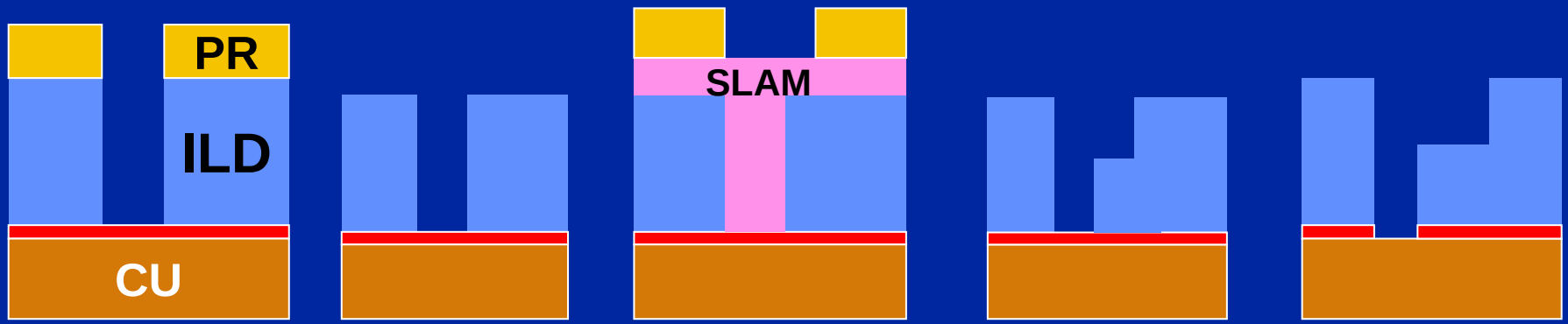
Outline

- Integration Scheme
- About the “environment”
- Selectivity during etch stop layer etch
- Conclusions

Outline

- **Integration Scheme**
- About the “environment”
- Selectivity during etch stop layer etch
- Conclusions

Via-First Patterning

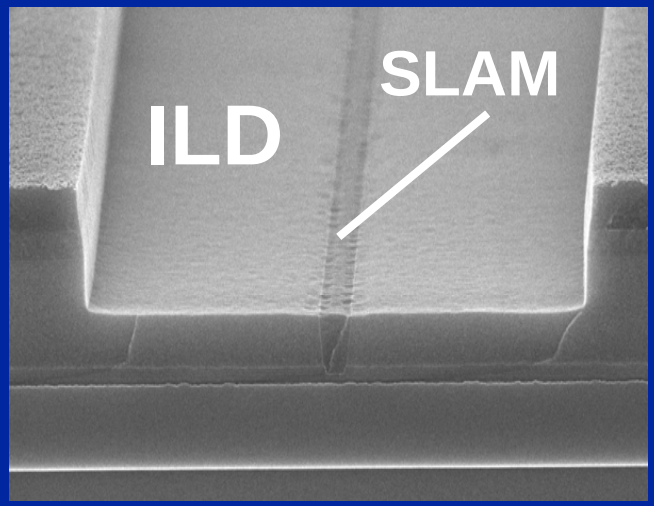


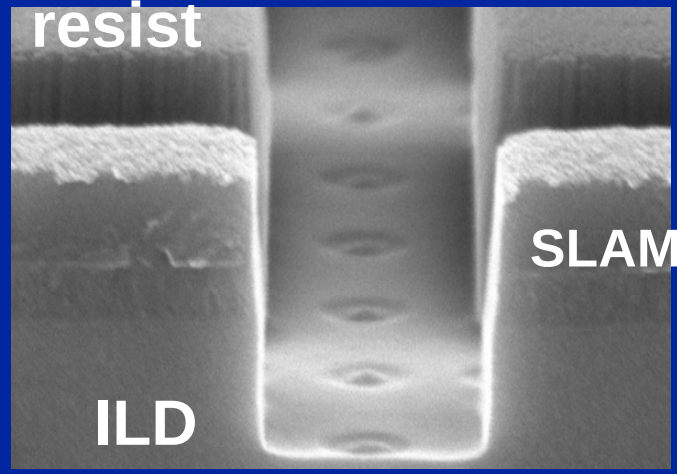
1. Via Patterning

2. Trench Patterning

3. Etch-stop layer etch

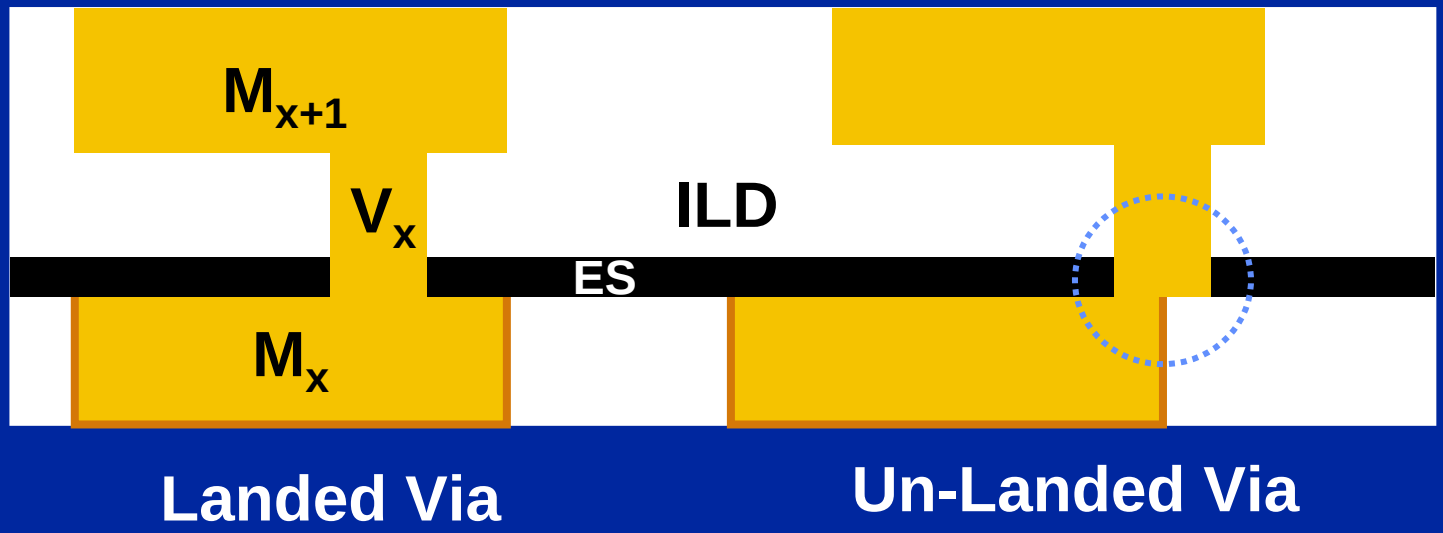
Post Trench Etch





- SLAM fills the vias and protect the ESL during trench etch→ No ES selectivity needs
- SLAM etch characteristics → Control via profile

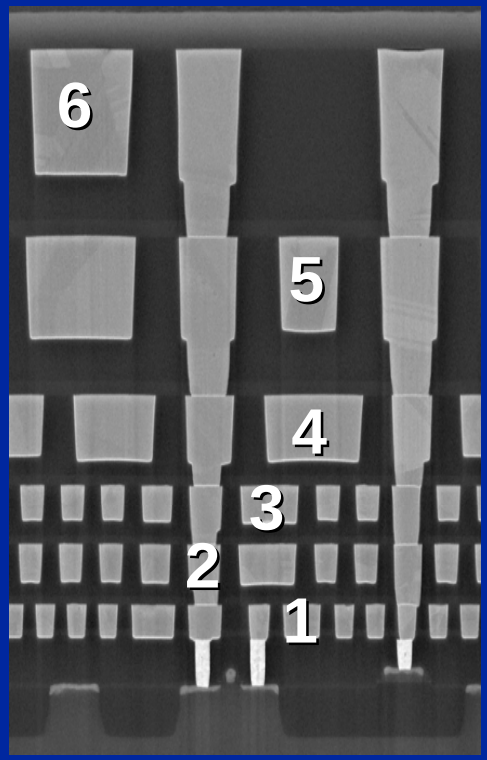
Role of Etch-Stop



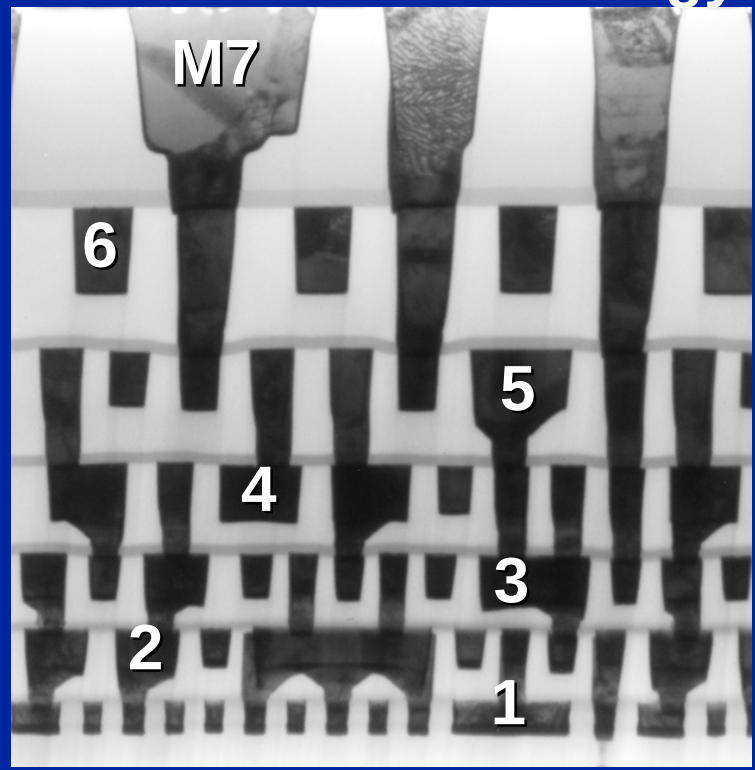
- Copper diffusion barrier
- Protect copper during processing
- A layer on which via etch terminates

Proven Technology

Intel's 130nm Technology



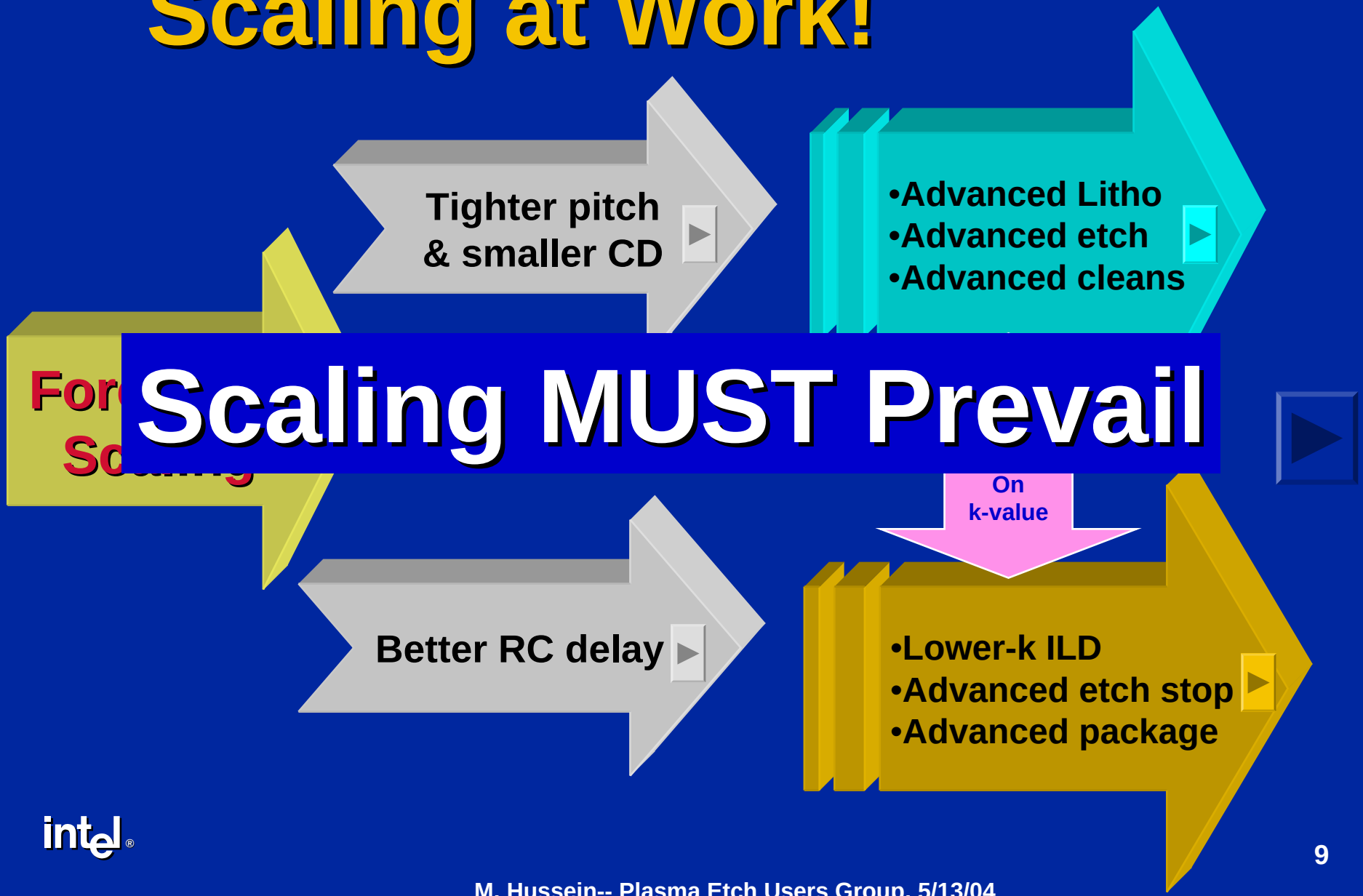
Intel's 90nm Technology



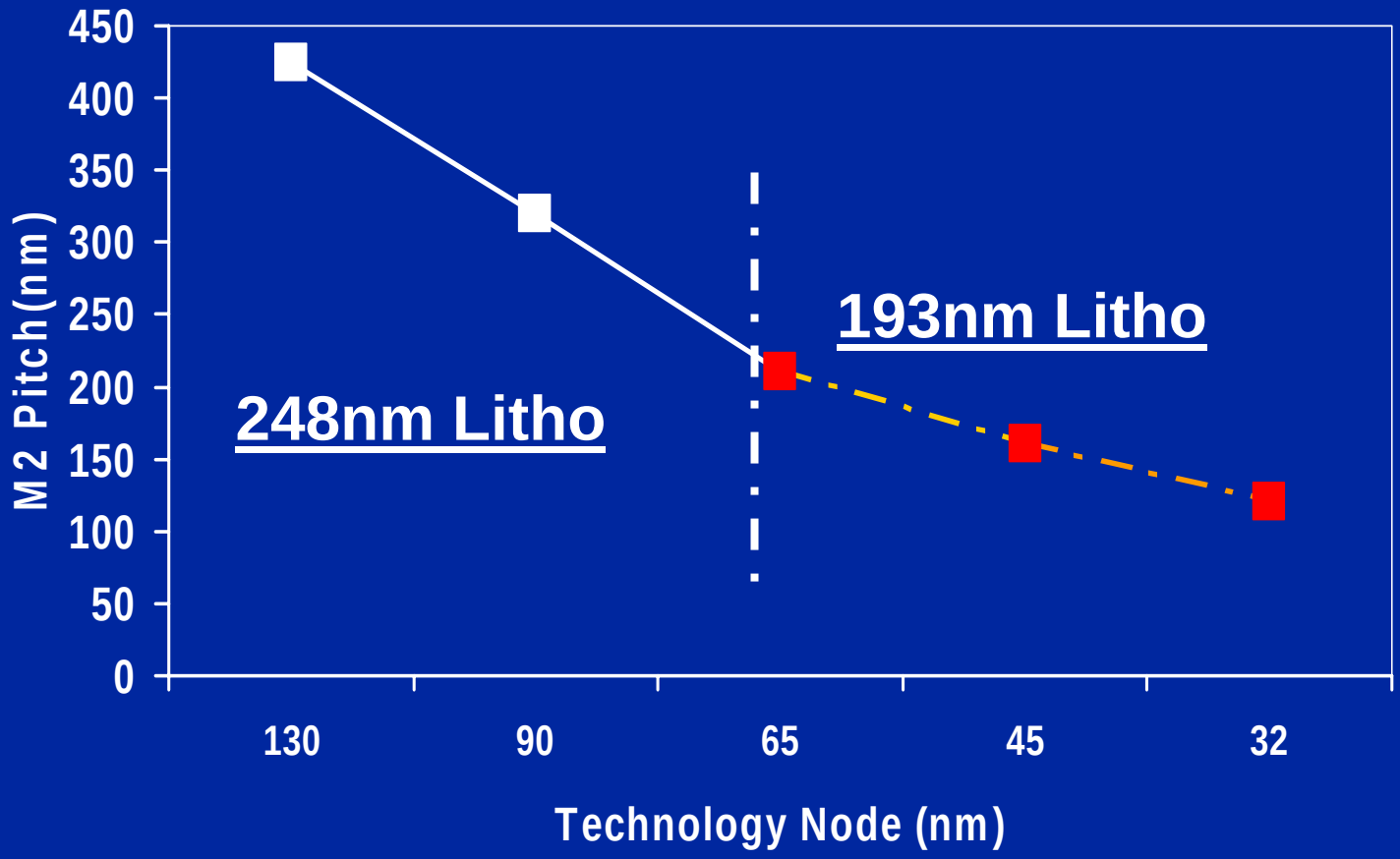
Outline

- Integration Scheme
- **About the “environment”**
- Selectivity during etch stop layer etch
- Conclusions

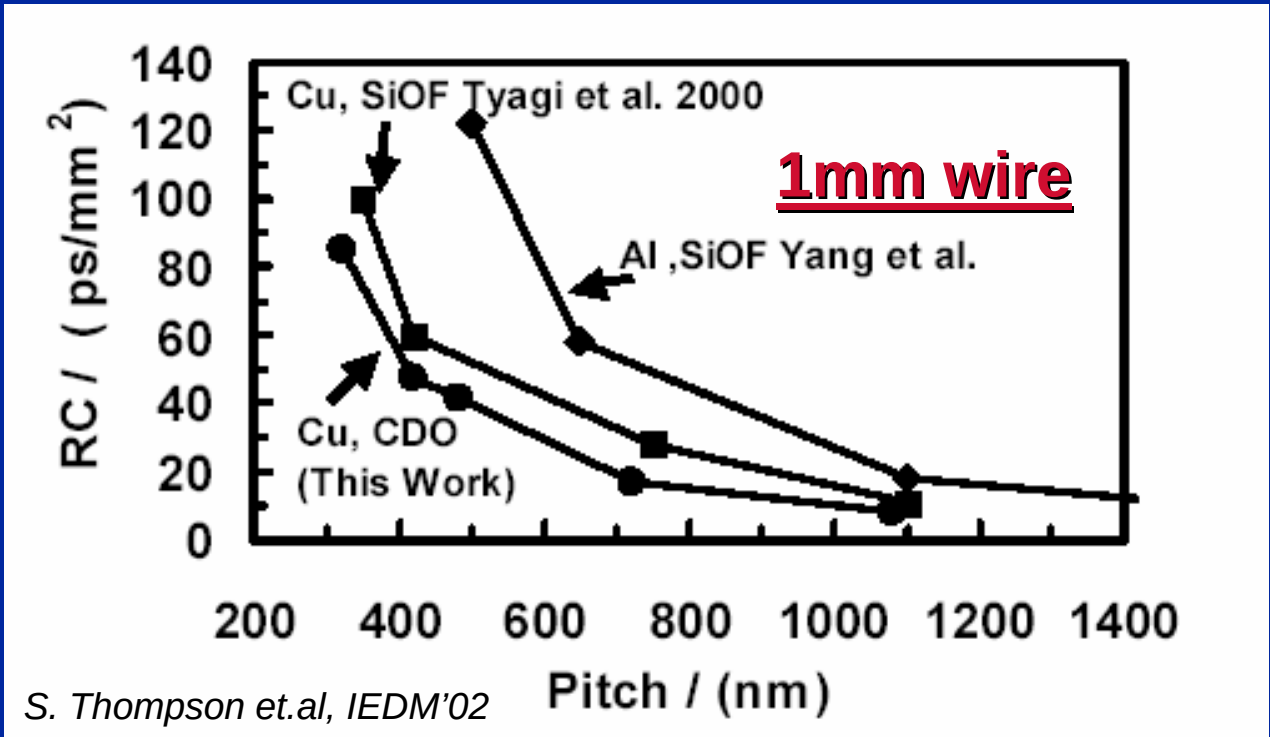
Scaling at Work!



Always ~30% Smaller



Quest for Shorter RC-Delay



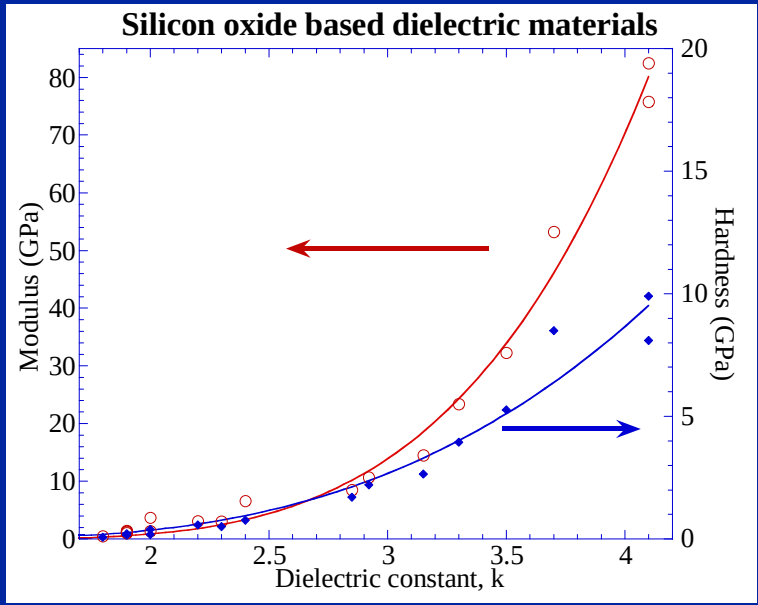
S. Thompson et.al, IEDM'02

Shorter delay → (1) Low resistivity metal
(2) Low-k ILD

Conductor? Anyone?!

- Copper becomes more resistive as metal line width decreases below 200nm
- Liner is occupying a “significant” portion of the metal wire area

What Does Low-k Mean?



- Low-k ILDs possess a lower dielectric constant and weak mechanical properties
- Weak mechanical properties
  - Negatively impact etch and cleans
  - Limit packaging choices

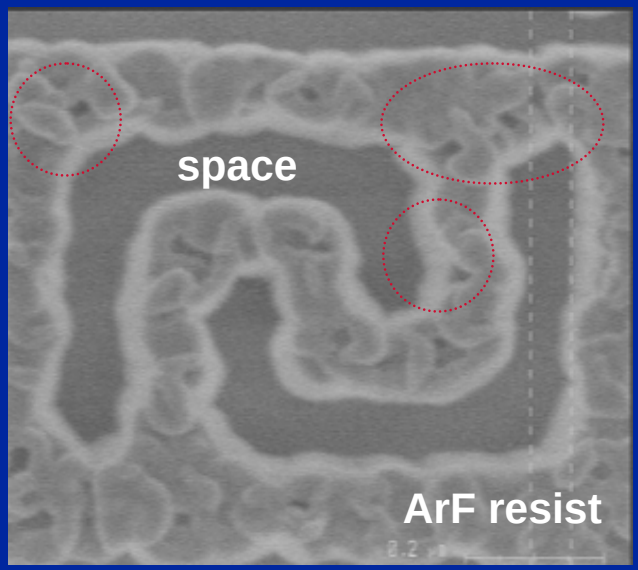
Processing Vs. k- Value Degradation

- Low-k ILD has a “memory”!
- Ashing post via and trench etch:
  - Impacts the out come of the dual damascene patterning
  - May affect k-value

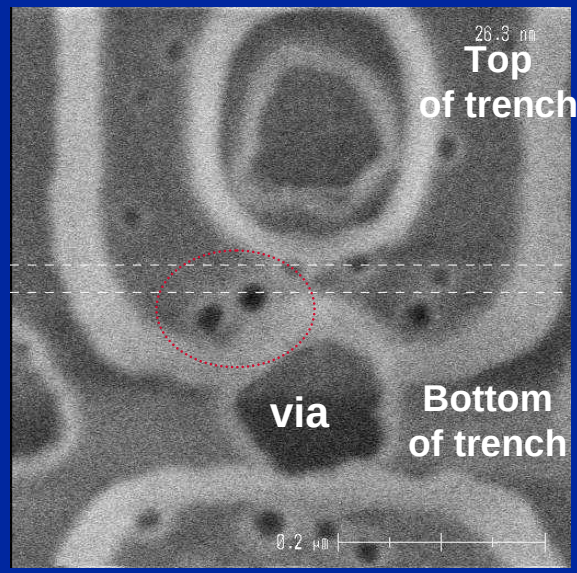
No impact to ILD’s k-value adds to etch complexity

intel®

Harder Patterning with ArF Litho



Before etch

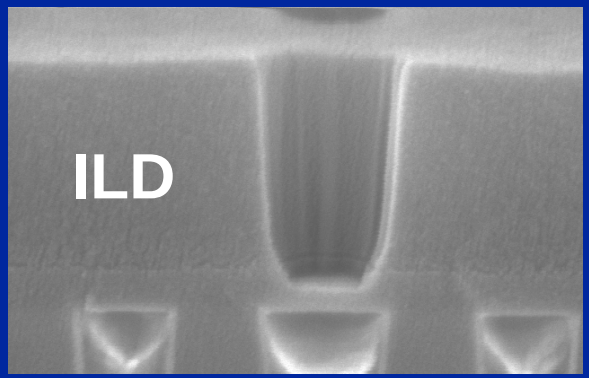


Post trench etch & cleans

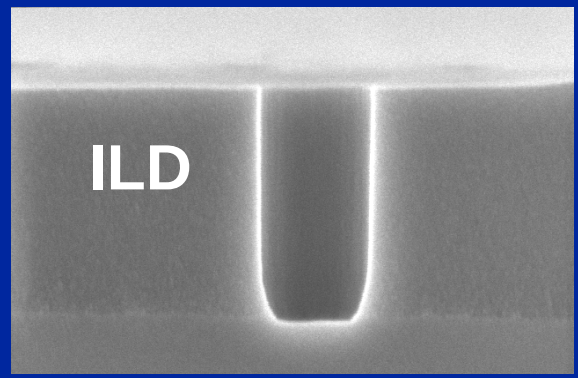
- ArF resist is needed for λ=193nm lithography
- ArF resist "agglomerates" under plasma conditions
- Etch performance of ArF resist is poor

Harder Patterning with ArF Litho

ArF Patterning



KrF Patterning



SAME Via etch process. SAME cleans.

- **Etching under ArF resist is more susceptible to generating deep striations in the ILD**
- **Balancing selectivity to etch-stop and maintaining profile and CD is getting harder**

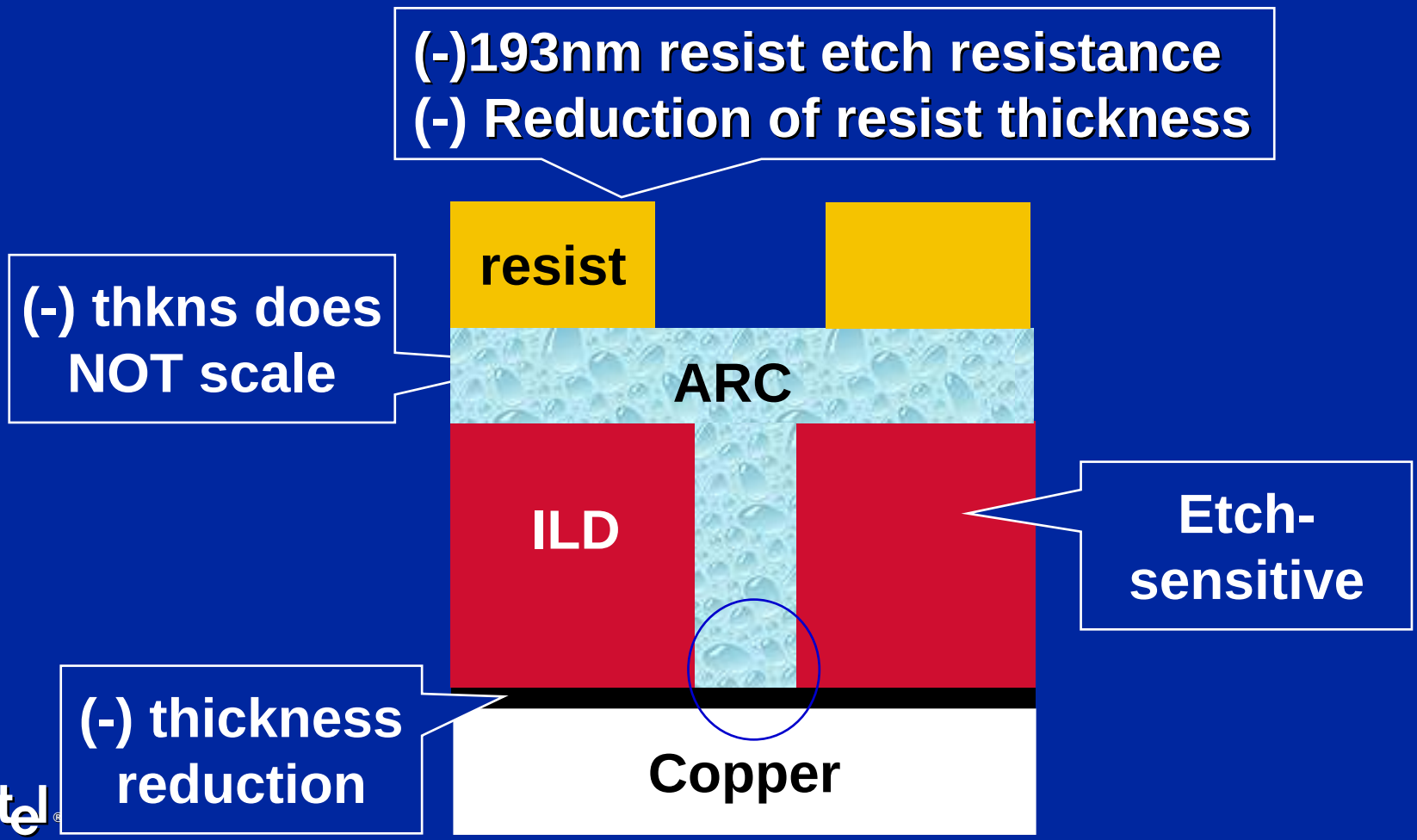
More Challenging Cleans

- Cleans are influenced by:
  - Nature of the ILD
  - Dry etch chemistry / strategy
- Dealing with low-k ILD and ArF resist significantly complicates the cleans

Outline

- Integration Scheme
- About the "environment"
- **Selectivity during etch stop layer etch**
- Conclusions

Have Enough Selectivity?

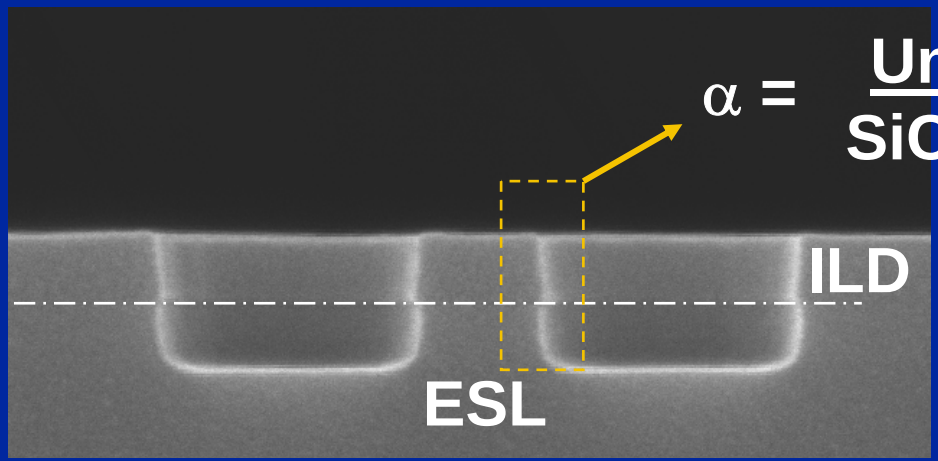


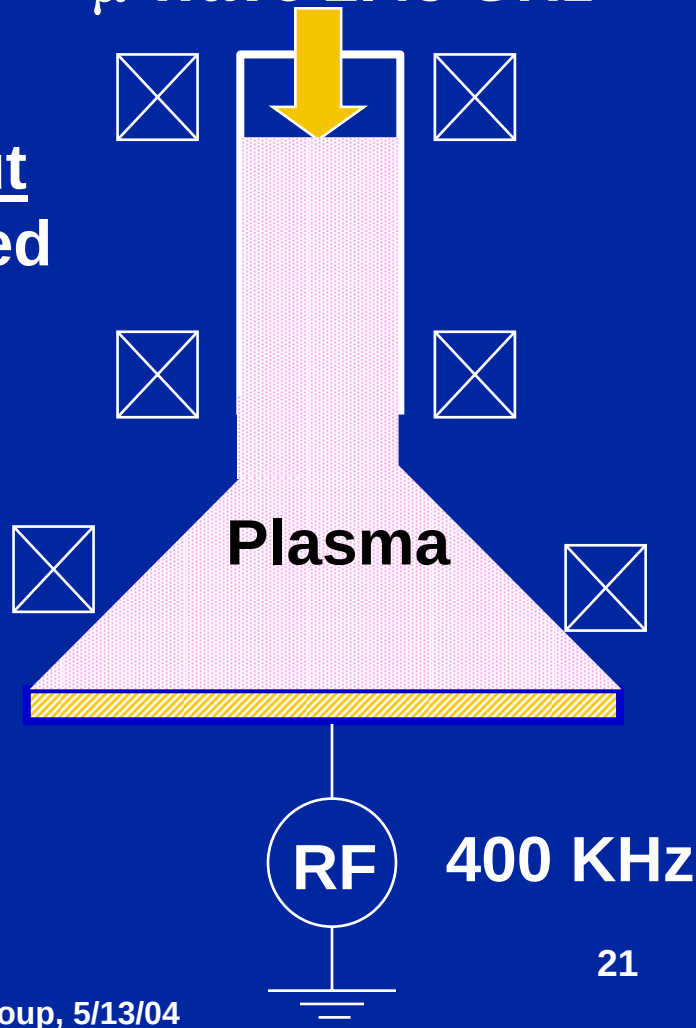
More Selectivity Demands

- Etch-stop layer (ESL) etch is performed with dual damascene pattern as MASK
- Requires etch rate of ESL >> Etch rate of ILD
- Minimum to erosion of exposed edges

Experimental Set-up

Substrate: 300mm Wafer

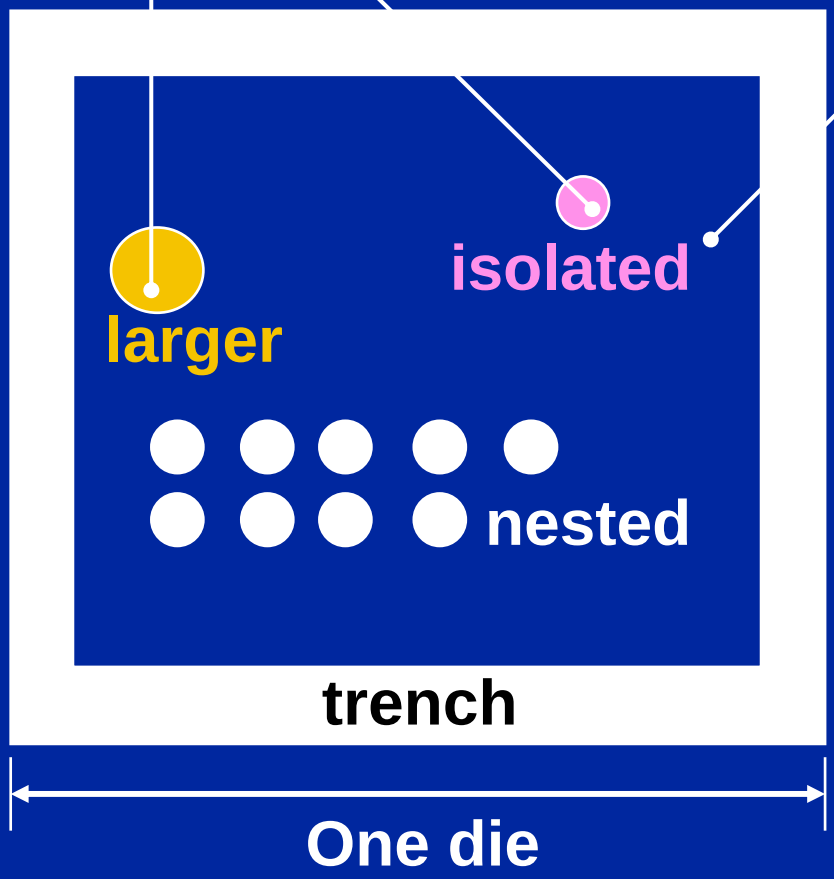




ILD: Low-k, carbon-doped oxide
ESL: Silicon carbide

Experimental Design

ESL ER: X-section



ILD ER: Optical

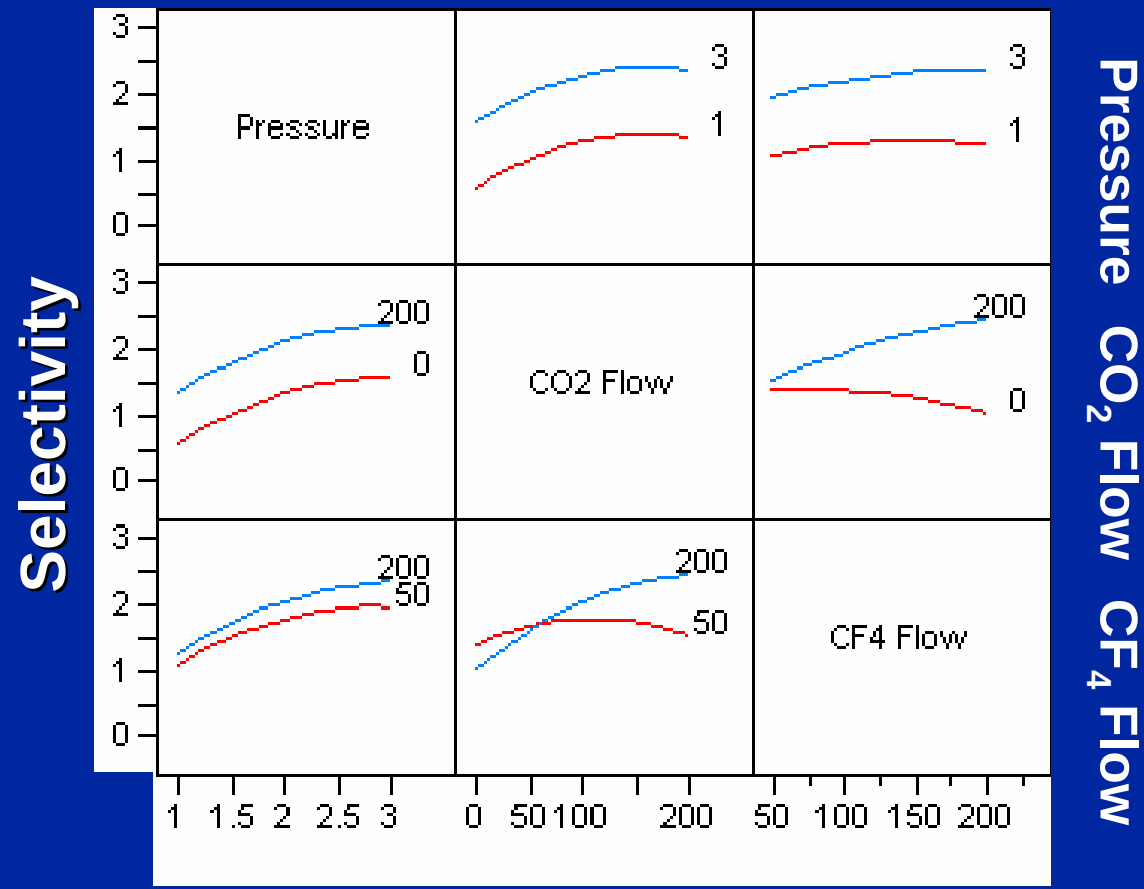
	-	+
CF4 (sccm)	50	200
CO2 (sccm)	0	200
Pressure (Pa)	1	3

- **Design:** Three factors, central composite with on-face axial points
- **Response:** ILD ER, ESL ER, under-cut in ESL

intel

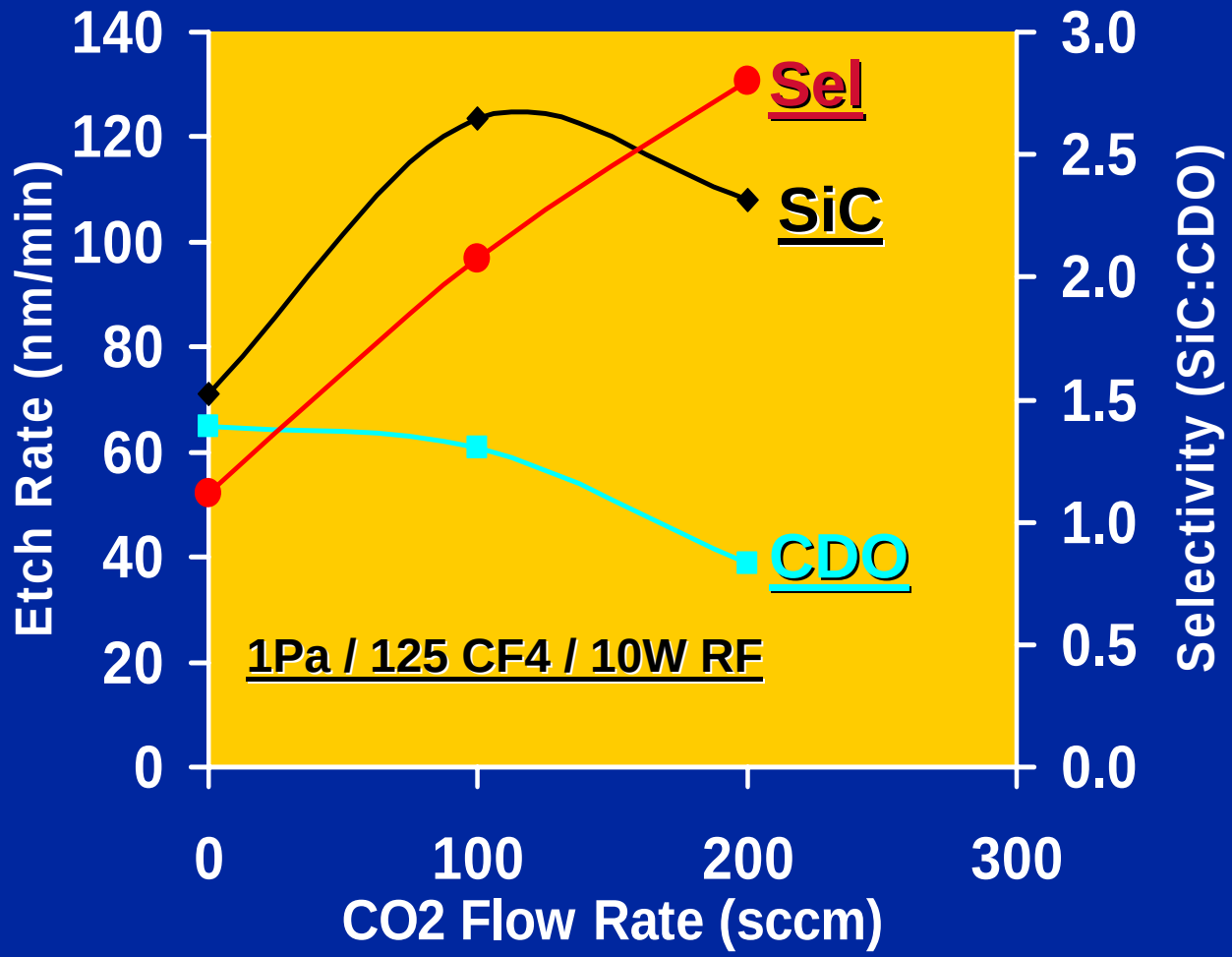
Selectivity: Interactions

High pressure and High CO_2 flow enhance selectivity



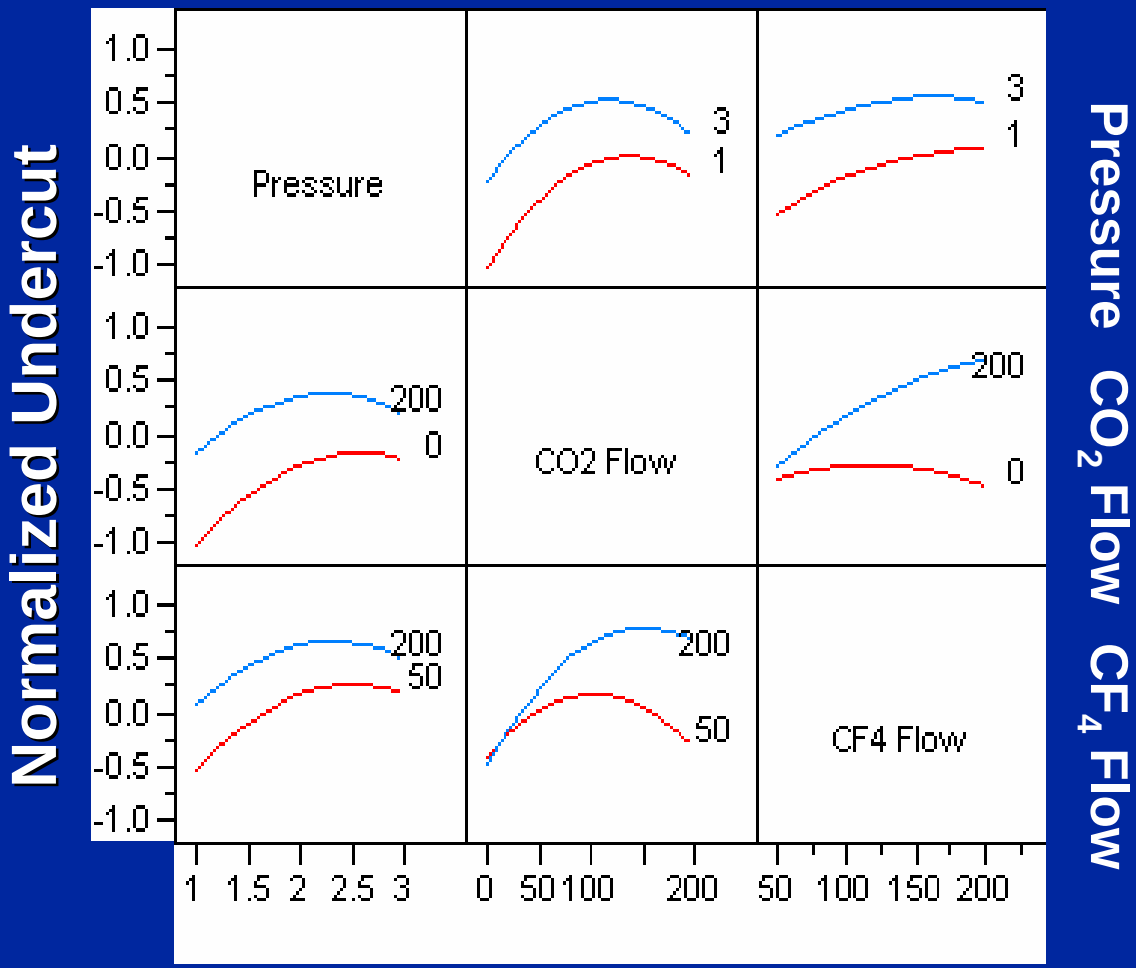
Effect of CO_2 Addition

SiC ER is more responsive to oxygen addition than CDO

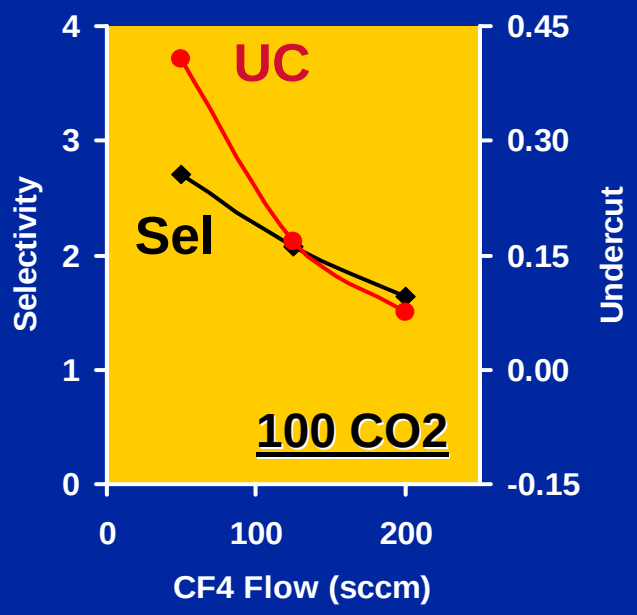


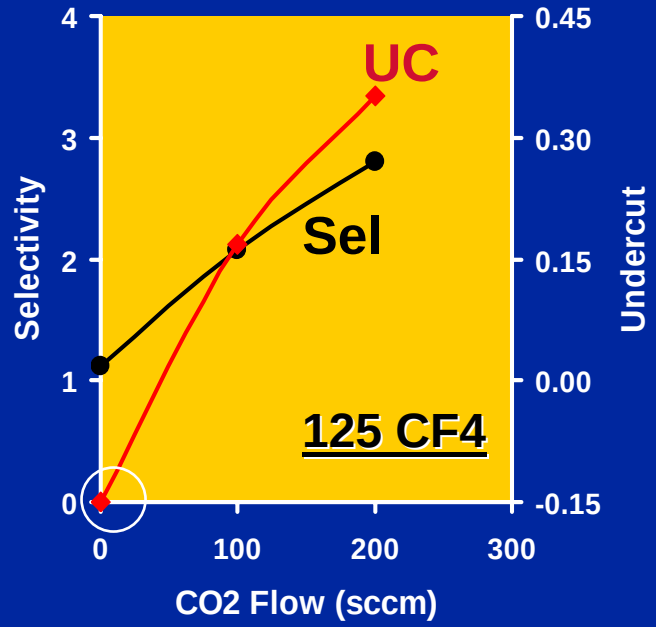
Under-Cut: Interactions

High pressure and CO_2 flow enhance undercut



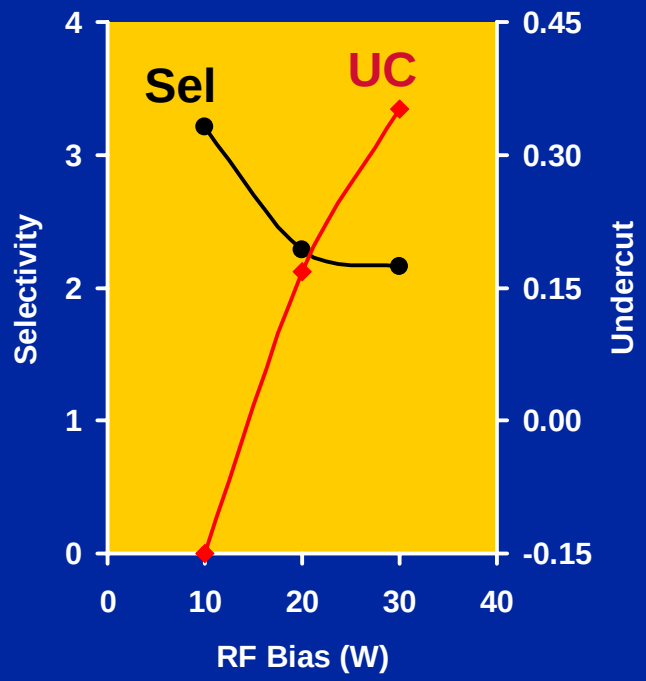
General Trends: Flows

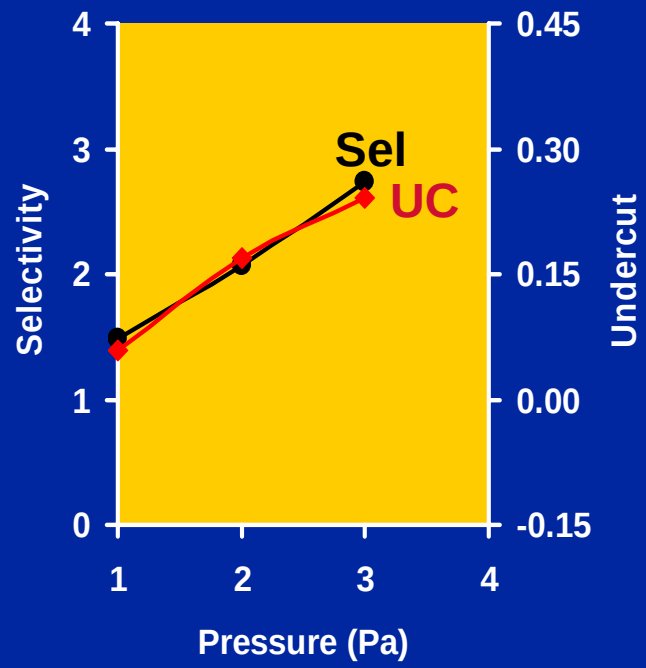




Addition of CO2 improves selectivity at the expense Of undercut

General Trends: RF & Pres

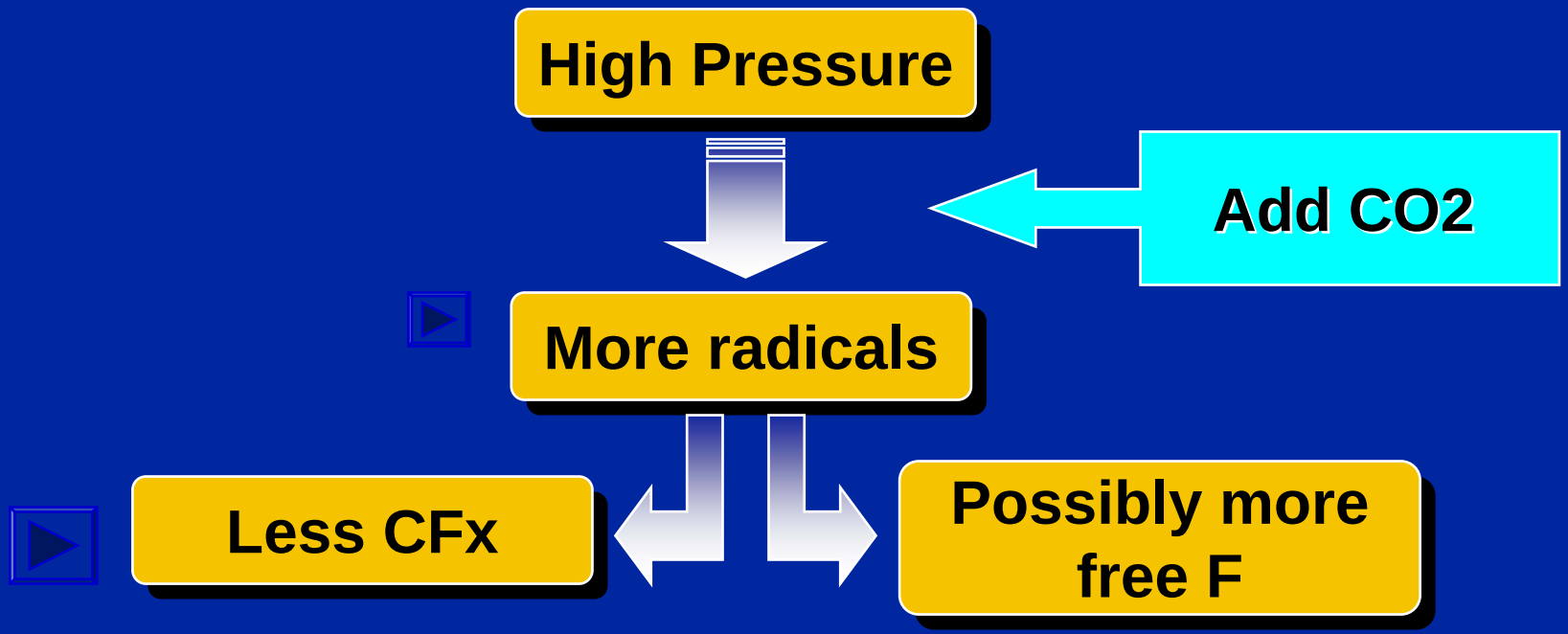




Selectivity improves at higher pressure
Undercut increases with RF bias

intel®

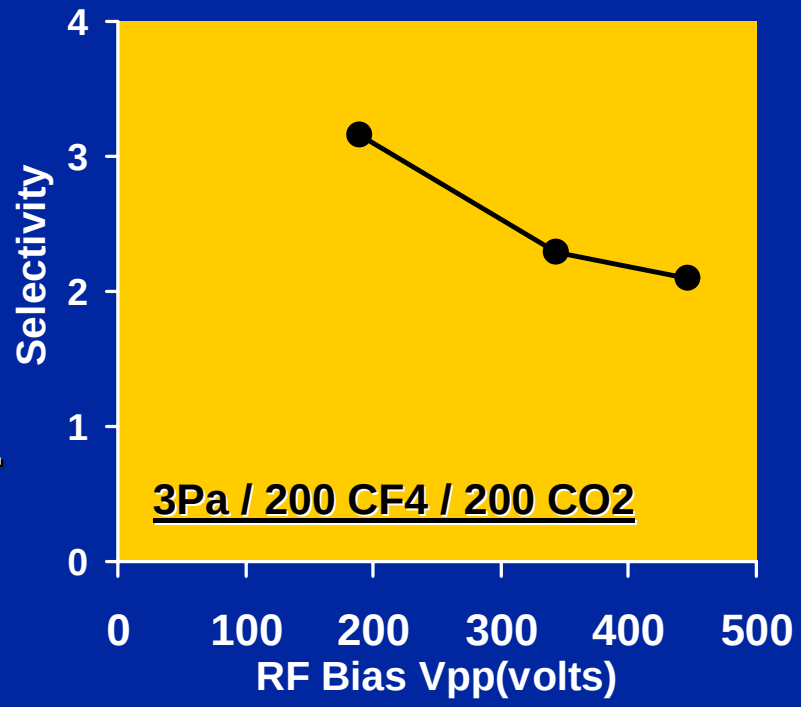
Model: Selectivity & UC



Less wall passivation → undercut CDO ER

On The Role Of RF…

- **Observations:**
  - Undercut increases with RF
  - Selectivity degrades with RF
  - ER increases with RF bias
  - No threshold for ER of either SiC or CDO



- **Conclusions:**
  - SiC etching exhibits appreciable chemical behavior
  - Passivation, rather than ion bombardment, is the source of anisotropy

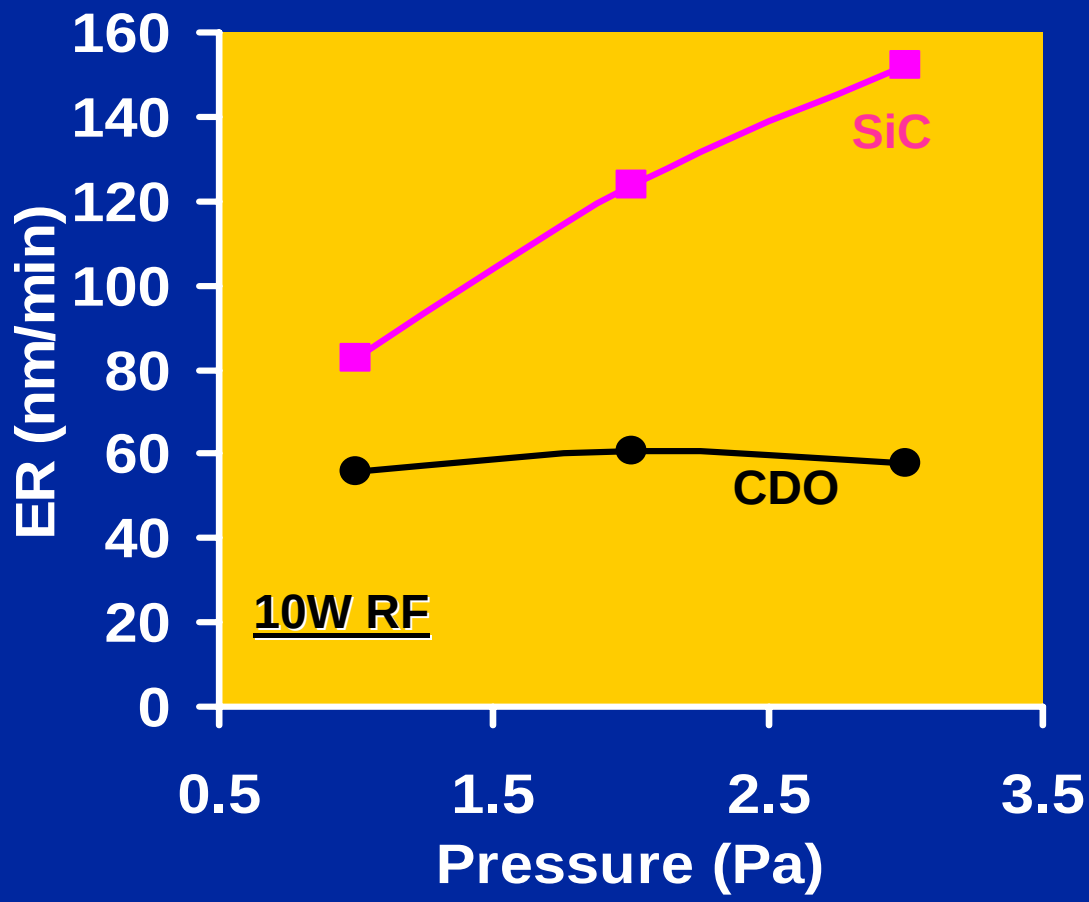
Conclusions

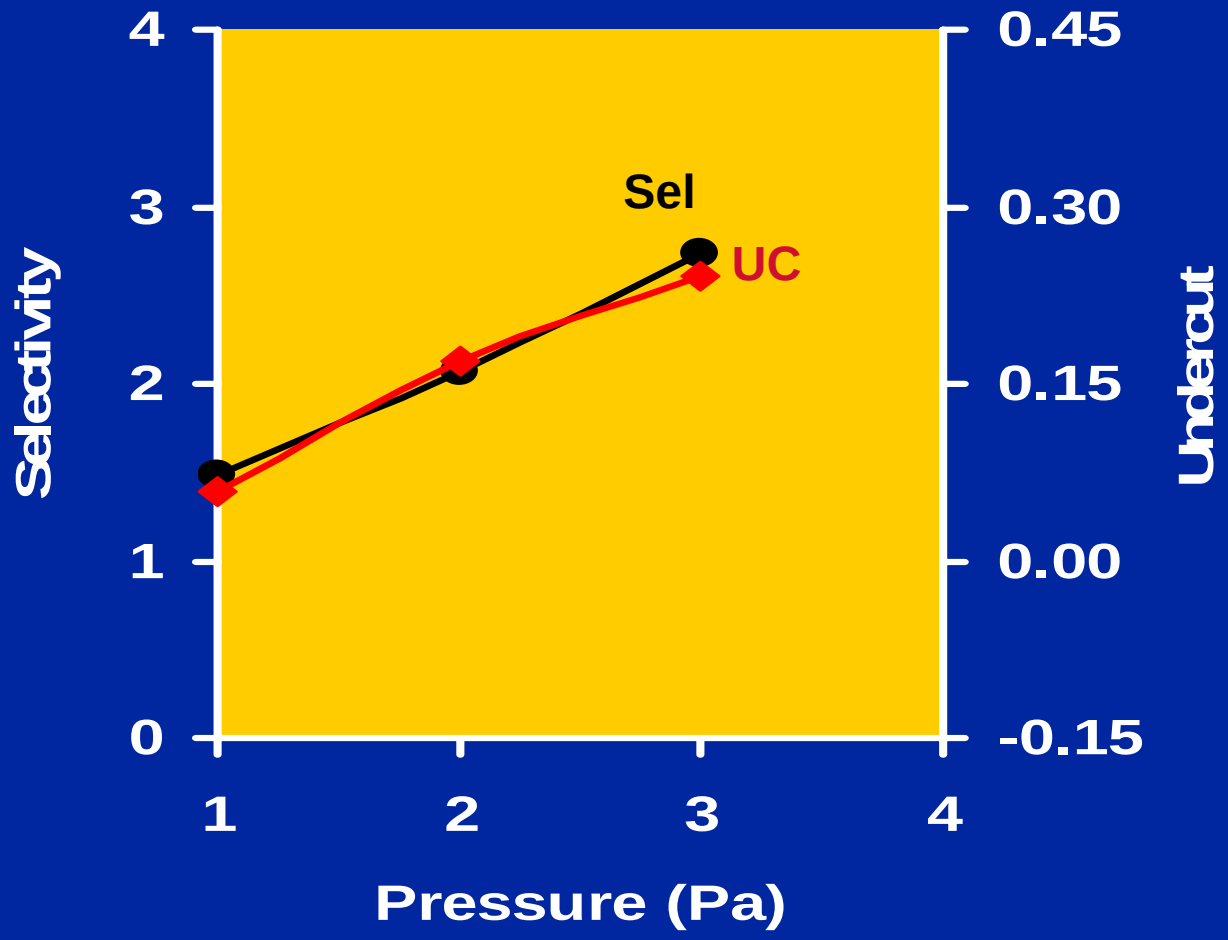
- Scaling will prevail, making patterning more challenging than ever.
- In a downstream high density etch system, it is difficult to attain high selectivity without undercut between CDO ILD and SiC ESL.
- Selectivity is becoming a serious challenge and basic understanding is much needed:
  - Impact of plasma on ArF resist
  - Selectivity modulation

Acknowledgement

- Data and discussions with the following colleagues significantly contributed to this work:
  - **Dry Etch:** Satyarth Suri, Max Heckscher, and James Jeong
  - **Wet Etch:** Lourdes Dominguez, Lana Jong, and Mike Nashner
  - **Integration:** Phucahn Nguyen, and Peter Moon
  - **Quality & Reliability:** Jun He and Barbra Miner

Back-up


160
140
120
100
80
60
40
20
0
ER (nm/min)
SiC
CDO
10W RF
0.5
1.5
2.5
3.5
Pressure (Pa)


Selectivity
Undercut
Pressure (Pa)
Sel
UC
4
3
2
1
0
0.45
0.30
0.15
0.00
-0.15
1
2
3
4