Self-aligned Contact Etch Development for 90 nm Technology Node

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Background

- Industry demand for high density memory products and quest for packing more dies/wafer have driven the memory cell size shrink.

- Self-aligned and borderless contacts, by relaxing lithography alignment requirements, have been two of the most powerful engines for cell size reduction.

- Self-aligned contacts (SAC) are used to form contacts to source and drain area.

- General electrical requirements for SAC:
  - Low contact resistance
  - No break-down to gate at operating Vcc
  - No leakage at corner of STI

- Self-aligned characteristics are obtained by employing chemistries that:
  - Anisotropically etch PMD (i.e. undoped or lightly doped glass)
  - Does Not etch the spacer and gate protection cap (i.e. Si$_3$N$_4$)
  - Stops on a thin liner (i.e. Si$_3$N$_4$)

- Contacts to S/D are subsequently formed by:
  - Removal of the liner by employing a plasma etch selective to Si and STI (HDP SiO$_2$).
  - Liner and plug deposition followed by CMP to polish to PMD surface.
**Stack and Architecture**

- Cypress SAC architecture increases contact area (reduces cell size) by eliminating liner.
- It requires to etch doped glass and stop on HDP oxide.
- It introduces the so-called “flower patterns”, hard to etch (possibly due to back-sputtered Si).
**SAC Etch. Characteristics vs. Requirements**

**Characteristics**
- Soft and thin 193 nm P.R.
- Organic BARC
- Highly doped PMD
- No stop liner
- Flower Pattern

**Requirements**
- Minimum +ve CD Bias (< 15 nm)
- Straight Profile (>87°)
- No P.R. Necking
- No striation
- Maximum SiN shoulder loss <400 A
- Maximum STI gouge <300 A
- No sensitivity to flower pattern
- Ability to etch O.L. trenches (1x20 μm)

*not drawn to scale*
Performance of PTOR (Super-E/C4F8-CO)

Problems:
• Severe profile tapering
• P.R. Pinch off
• Severe top contact striation

Solutions:
• Migrate to high flow-low pressure region
• Use lower temperature process
• Use alternative chemistry with higher P.R. selectivity
Next Generation Technology (eMAX): Characteristics

- High flow-low pressure region: high C:F chemistry in starving mode
- Temperature controlled liners: better polymer deposition
- Wider range B-field: control uniformity and ion energy
- Wider range backside He pressure: independent interstep temperature control

Source: AMAT
eMAX Process Capability (C4F6-O2)

- $C_4F_6-O_2$ process in eMAX improved the profile, reduced P.R. pinch off (not eliminated).
- Overall process also achieved acceptable $Si_3N_4$ and $SiO_2$ selectivity.
- Contact profile tilting observed at the wafer edge (<6 mm edge exclusion).
- Sensitive to flower pattern.
**eMAX Process Capability (Striation)**

- Striation was reduced by using eMAX and $C_4F_6O_2$ chemistry.
- Using low temperature, however, not viable due to $SiO_2/Si_3N_4$ selectivity requirements.
- Achieving an acceptable process requires further hardware modifications.

*C$_4$F$_6$O$_2$ Chemistry not viable in Super-E*
Striation Root Cause

- Directional bombardment by energetic ions: $V_{rf} = f$ (B-field, pressure, RF power)
- Insufficient sidewall polymer deposition: wafer temperature, $C:F$

![Image showing different plasma conditions and their effects on striation]

Scale: 0 - 5

Source: AMAT Internal Presentation Jan 2002
eMAX CIP: eMAX-CT

- 200mm CT adopted modifications from 300 mm CT hardware.
- 300mm CT intended for improving uniformity (narrow gap+RF delivery+ B-field+SGD)
- CT design also improves PR selectivity/Striation by employing narrow gap and SGD
- Cypress was the first customer for eMAX-CT 200 mm (Pre-α to manufacturing release).

SGD reduces gas species velocity and produces more uniform plasma thereby reducing striation.
Reduction of Vrf

20V to 90V difference on Vrf is seen between eMAX (high gap) and eMAX-CT (low gap)
**eMAX-CT: Process Characteristics**

C₄F₆/O₂/40mT

- **4011 Å/min** 7.32 % (1σ)
- **4345 Å/min** 7.66 % (1σ)
- **4751 Å/min** 4.16 % (1σ)
- **5197 Å/min** 4.48 % (1σ)

**eMAX-CT simultaneously improves uniformity and etch rate**
eMAX-CT: Process Characteristics

*eMAX/\text{C}_4\text{F}_6-\text{O}_2/20\;\text{C}*

*eMAX-CT/\text{C}_4\text{F}_6-\text{O}_2/20\;\text{C}*

*eMAX-CT improved P.R. selectivity and striation using \text{C}_4\text{F}_6-\text{O}_2\;\text{chemistry} @ 20\;\text{C}*

eMAX-CT: Process Characteristics

- Eliminated P.R. pinch off, acceptable profile, good within wafer uniformity
**eMAX-CT: Process Characteristics**

- Process is selective to $\text{SiO}_2$ and $\text{Si}_3\text{N}_4$
- Some sensitivity to flower pattern and nonuniform $\text{SiO}_2$ gouge

![Images of process characteristics with labels: Crown, Center, Notch, and remaining glass on the spacer sidewall.](image-url)
Optimization Challenges

Trade off:
- Contact deformation vs. CD bias/striation (ARCE)
- Etching open area vs. CD bias/striation (M.E. I)
- \( \text{Si}_3\text{N}_4/\text{SiO}_2 \) vs. Remaining PMD on spacer sidewall (M.E. II)

Required extensive optimization to develop a robust and manufacturable process
Optimized Process: Physical Verification

- Eliminated remaining glass on spacer sidewall and improved landing profile by:
  - Optimizing transition from M.E. I to M.E. II
  - Optimizing B-field/RF power in M.E. II
- Verified process window over incoming variable limits (CD, thickness, etc...) 
- Verified process performance over tool controllability limits.
Optimized Process: Physical Verification

- Reduced CD bias to allowable limit by TDR, etched overlay marks (1x20 um) and eliminated striation and contact deformation by:
  - Optimizing CHF₃/CF₄ RF power, B-field, and pressure in ARCE
  - Optimizing reactive gas/inert, C₄F₆/O₂ and wafer temperature (backside He pressure)
**Optimized Process: Electrical Verification**

All critical electrical parameters are met and tightly controlled (high CpK/low Z) within EDR spec.
Next Generation SAC Etch Challenges

- More severe striation and higher CD bias for 70 nm and beyond due to thinner 193 nm P.R., tighter pitch, smaller CD and higher AR:
  - Require further reduction of Vdc/Vrf w/o affecting etch rate (dual frequency?)
  - Require robust ESC design to enable chucking at low RF powers/high backside He pressure (eliminate chucking instability => new ESC design)
  - May need to switch to inorganic BARC and/or alternative architecture

- Backside He cooling range with current ESC design will NOT be sufficient to independently control etch substeps temperatures:
  - Require more efficient cooling system

- Trade-off between profile and SiO₂ selectivity due to pitch reduction (flowers will pinch off!):
  - Move to different flow-pressure region (current tool capable?)
  - May require alternative architecture

- Chamber matching/process transfer/process mixing characterization become more critical:
  - More systematic efforts to address issues before transferring to manufacturing

- CD variation within wafer, wafer-to-wafer and lot-to-lot are approaching acceptable limits:
  - May require APC

03/11/04 Recommendations on this page are solely CY point of view on the subject
Summary

- Completed qualification of eMAX-CT thru pre-α (prototype testing) to β-testing and manufacturing release.
- Developed a Rev 0 process on prototype HW to enable technology development.
- Optimized the process and eliminated all the captured failure modes.
- Verified process window over incoming variable and tool controllability limits.
- Verified electrical performance of final process.
- Successfully transferred process to manufacturing (Q2’03).
- Identified challenges for SAC etch on 70 nm technology node.
- Currently working with integration, CAD, design teams as well as AMAT dielectric etch division to appropriately address 70 nm requirements.
Acknowledgement

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