

Self-aligned Contact Etch Development for 90 nm Technology Node

Mehran Sedigh, Jie Zhang, Harry Lee Cypress Semiconductor, R&D Division

James Stinnett, Ajey Joshi Applied Material, Dielectric Etch Customer Technology

> AVS PEUG March 11, 2004



<u>Outline</u>

- Background
- Stack and Architecture
- SAC Etch Characteristics vs. Requirements
- *Performance of PTOR (Super-E/C*₄ F_8 -CO)
- Next Generation Technology (eMAX)
 - Characteristics
 - Process Capabilities
- Striation Root Cause
- eMAX CIP: eMAX-CT
- *Reduction of Vrf*
- eMAX-CT: Process Characteristics
- Optimization Challenges
- Optimized Process
 - Physical Verification
 - Electrical Verification
- Next Generation SAC Etch Challenges
- Summary



Background

- Industry demand for high density memory products and quest for packing more dies/wafer have driven the memory cell size shrink.
- Self-aligned and borderless contacts, by relaxing lithography alignment requirements, have been two of the most powerful engines for cell size reduction.
- Self-aligned contacts (SAC) are used to form contacts to source and drain area.
- General electrical requirements for SAC:
 - Low contact resistance
 - No break-down to gate at operating Vcc
 - No leakage at corner of STI
- Self-aligned characteristics are obtained by employing chemistries that:
 - Anisotropically etch PMD (i.e. undoped or lightly doped glass)
 - Does Not etch the spacer and gate protection cap (i.e. Si_3N_4)
 - Stops on a thin liner (i.e. Si_3N_4)
- Contacts to S/D are subsequently formed by:
 - *Removal of the liner by employing a plasma etch selective to Si and STI (HDP SiO*₂).
 - Liner and plug deposition followed by CMP to polish to PMD surface.



Stack and Architecture



- Cypress SAC architecture increases contact area (reduces cell size) by eliminating liner
- It requires to etch doped glass and stop on HDP oxide
- It introduces the so called "flower patterns", hard to etch (possibly due to back-sputtered Si)



SAC Etch. Characteristics vs. Requirements





Performance of PTOR (Super-E/C4F8-CO)



Problems:

- Severe profile tapering
- P.R. Pinch off
- Severe top contact striation

Solutions:

• *Migrate to high flow-low pressure region* Adjust residence time

- Use lower temperature process
- Use alternative chemistry with higher P.R. selectivity



Next Generation Technology (eMAX): Characteristics



- *High flow-low pressure region : high C:F chemistry in starving mode*
- Temperature controlled liners: better polymer deposition
- Wider range B-field: control uniformity and ion energy
- Wider range backside He pressure: independent interstep temperature control



eMAX Process Capability (C4F6-O2)



- C_4F_6 - O_2 process in eMAX improved the profile, reduced P.R. pinch off (not eliminated).
- Overall process also achieved acceptable Si_3N_4 and SiO_2 selectivity.
- Contact profile tilting observed at the wafer edge (<6 mm edge exclusion).
- Sensitive to flower pattern.



Driving the Communications Revolution™

eMAX Process Capability(Striation)



- Striation was reduced by using eMAX and C_4F_6 - O_2 chemistry.
- Using low temperature, however, not viable due to SiO₂/Si₃N ₄selectivity requirements.
- Achieving an acceptable process requires further hardware modifications.



Striation Root Cause

- > Directional bombardment by energetic ions: Vrf = f (B-field, pressure, RF power)
- > Insufficient sidewall polymer deposition: wafer temperature, C:F





Source: AMAT Internal Presentation Jan 2002



Driving the Communications Revolution™

eMAX CIP: eMAX-CT



- 200mm CT adopted modifications from 300 mm CT hardware.
- 300mm CT intended for improving uniformity (narrow gap+RF delivery+ B-field+SGD)
- CT design also improves PR selectivity/Striation by employing narrow gap and SGD
- Cypress was the first customer for eMAX-CT 200 mm (Pre-a to manufacturing release).

CYPRESS Driving the Communications Revolution™

<u>Reduction of Vrf</u>



20V to 90V difference on Vrf is seen between eMAX (high gap) and eMAX-CT (low gap)

Source: AMAT Internal Presentation Jan 2002



453 171







eMAX-CT improved P.R. selectivity and striation using C_4F_6 - O_2 chemistry @ 20 C



453 1 21

..



Eliminated P.R. pinch off, acceptable profile, good within wafer uniformity



252 1 71

11



Process is selective to SiO_2 and Si_3N_4

Some sensitivity to flower pattern and nonuniform SiO₂ gouge



Optimization Challenges

953 1 71



03/11/04



Optimized Process: Physical Verification

35317



- Eliminated remaining glass on spacer sidewall and improved landing profile by:
 - Optimizing transition from M.E. I to M.E. II
 - Optimizing B-field/RF power in M.E. II
- Verified process window over incoming variable limits (CD, thickness, etc...)
- Verified process performance over tool controllability limits.



Optimized Process: Physical Verification







• *Reduced CD bias to allowable limit by TDR, etched overlay marks (1x20 um) and eliminated striation and contact deformation by:*

- Optimizing CHF_{3}/CF_{*} RF power, B-field, and pressure in ARCE
- Optimizing reactive gas/inert, $C_4 F_6 / O_2$, and wafer temperature (backside He pressure)



Optimized Process: Electrical Verification



All critical electrical parameters are met and tightly controlled (high CpK/low Z) within EDR spec



Next Generation SAC Etch Challenges

- More severe striation and higher CD bias for 70 nm and beyond due to thinner 193 nm P.R., tighter pitch, smaller CD and higher AR:
 - *Require further reduction of Vdc/Vrf w/o affecting etch rate (dual frequency?)*
 - Require robust ESC design to enable chucking at low RF powers/high backside He pressure (eliminate chucking instability => new ESC design)
 - May need to switch to inorganic BARC and/or alternative architecture
- Backside He cooling range with current ESC design will NOT be sufficient to independently control etch substeps temperatures:
 - Require more efficient cooling system
- Trade-off between profile and SiO₂ selectivity due to pitch reduction (flowers will pinch off!):
 - Move to different flow-pressure region (current tool capable?)
 - May require alternative architecture
- Chamber matching/process transfer/process mixing characterization become more critical:
 More systematic efforts to address issues before transferring to manufacturing
- CD variation within wafer, wafer-to-wafer and lot-to-lot are approaching acceptable limits:
 May require APC



<u>Summary</u>

- Completed qualification of eMAX-CT thru pre-**a** (prototype testing) to **b**-testing and manufacturing release.
- Developed a Rev 0 process on prototype HW to enable technology development.
- *Optimized the process and eliminated all the captured failure modes.*
- Verified process window over incoming variable and tool controllability limits.
- Verified electrical performance of final process.
- Successfully transferred process to manufacturing (Q2'03).
- Identified challenges for SAC etch on 70 nm technology node.
- Currently working with integration, CAD, design teams as well as AMAT dielectric etch division to appropriately address 70 nm requirements.



<u>Acknowledgement</u>

- We would like to thank:
 - Cypress manufacturing personnel (production and maintenance), integration and FA teams.
 - *AMAT*....