Integration of Modeling and Simulation into Process Development

Northern California AVS Section Joint

- Plasma Etch Users Group
- Thin Films Users Group

Meeting

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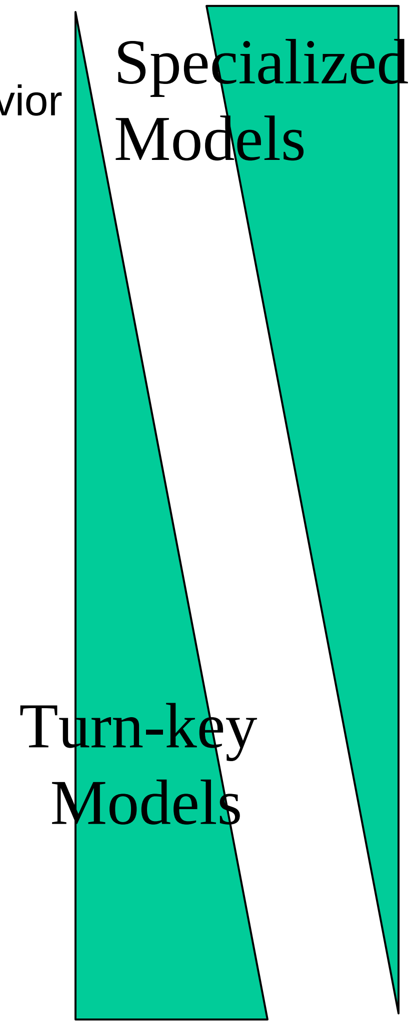
AGENDA

- Perspective on how modeling and simulation fit as a value propositions in the semiconductor industry.
- Computational process integration
  - **Process integration tool-kit at Motorola**
  - **Plasma Chemistry**
  - **Surfaces**
- FEOL Example
- BEOL Example

Simulation and the Manufacturing Life-Cycle

- **New Materials**
  - New devices and new materials. Understanding material behavior dependencies on unit processes.
  - *“Materials science calculations”*
- **Concept and Feasibility**
  - Tool design and the mating of tools to next technology nodes
  - *“Equipment simulation”*
- **New Product Development**
  - Unit process development
  - Process integration
  - *“Linked equipment and feature scale models”*
- **Manufacturing**
  - Yield enhancement, troubleshooting
  - *“Calibrated models”*
- **Re-use**



Barriers to Integration of Modeling and Simulation into Development Culture

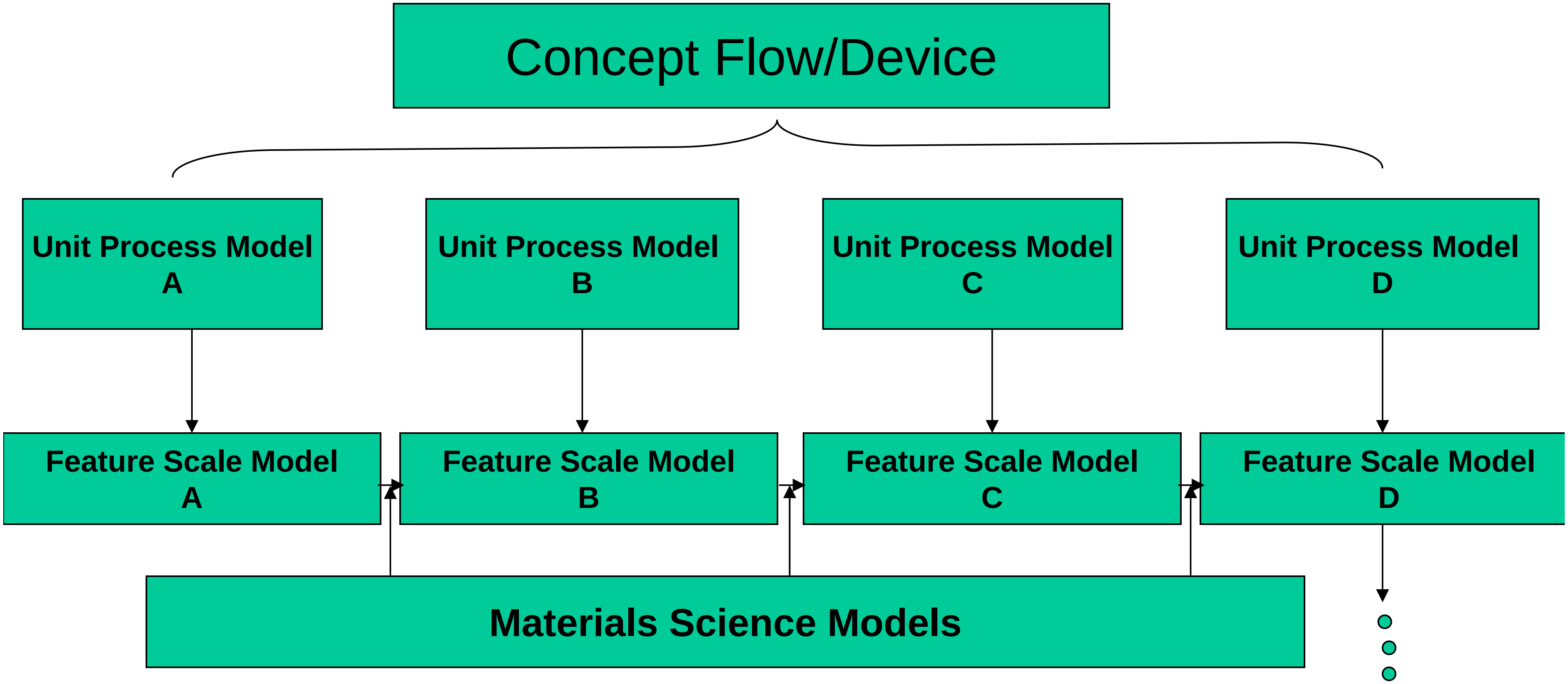
- Credibility and timeliness issues
  - Late results, replication vs. truly predictive
- Not quantitative enough
- Undersized development groups in industry and university
  - Downsize of traditional research sources
  - Small nature of many end users of M&S
- Communication gap between interested parties: chip makers, vendors
- Communication gap between funding agencies that would fund research , researchers and “customers”.

Means to Integration of Modeling and Simulation into Development Culture

- **Focus on predictive work (as much as possible)**
- **Strive to be quantitative – no corner cutting from fundamental physics data to tool details.**
- **Critical mass group or extended group**
- **As much as possible, engage vendors in joint projects**
- **Take an international view regarding research partners**

- **Aim where need is greatest: integration.**
  - **Point process studies while insight providing have limited value add potential.**
  - **The ensemble of unit processes or process integration is our view of where impact is greatest.**

Process Integration



Sequences of unit process models threaded together can replicate what is observed on Silicon.

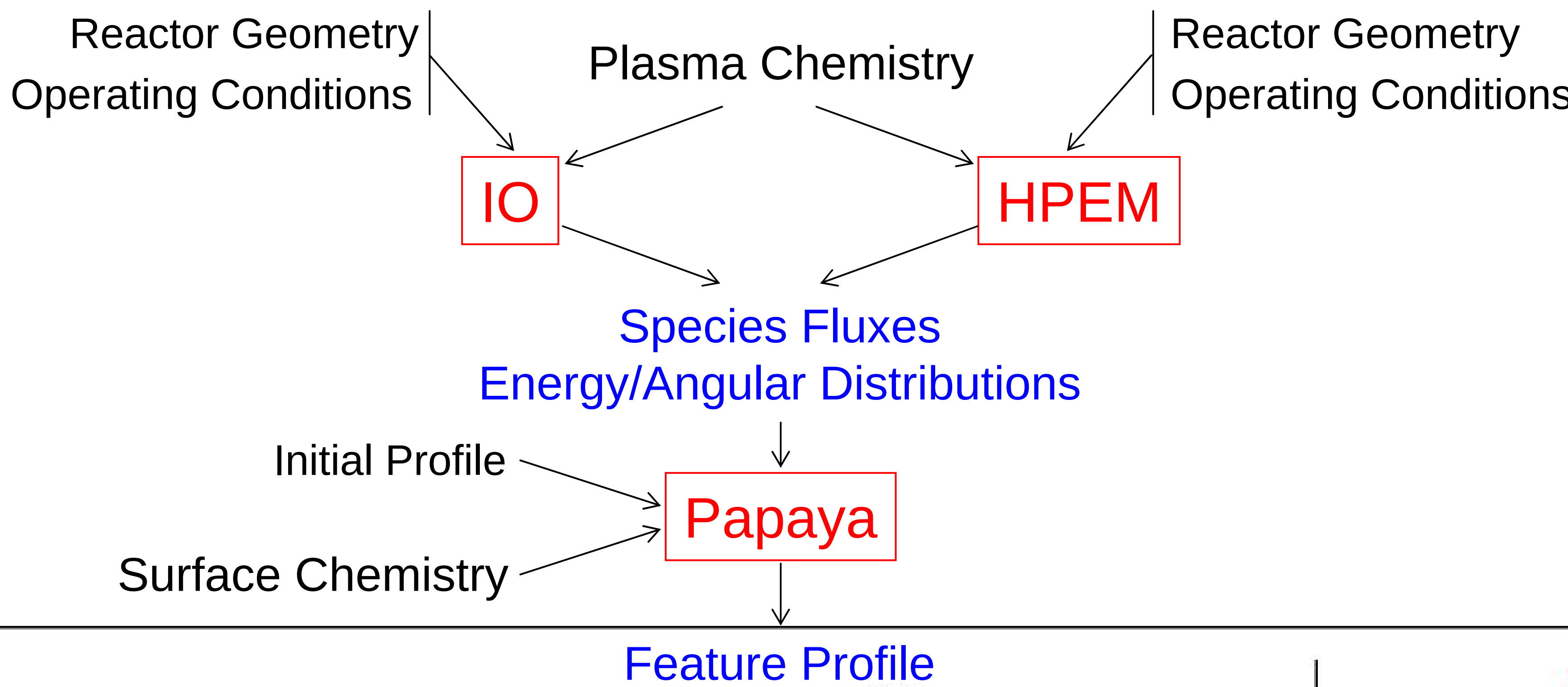
Yield Enhancement and Superior Reliability, Electrical Performance

Computational Integration Tool Kit

- Models for most commercial tools (AMAT, Lam, TEL) developed in-house.
- Plasma chemistry database assembled through internal computational environment.
- Plasma-surface interaction database developed through internal and external efforts.
- In-house simulations for both chamber and feature scale simulations.

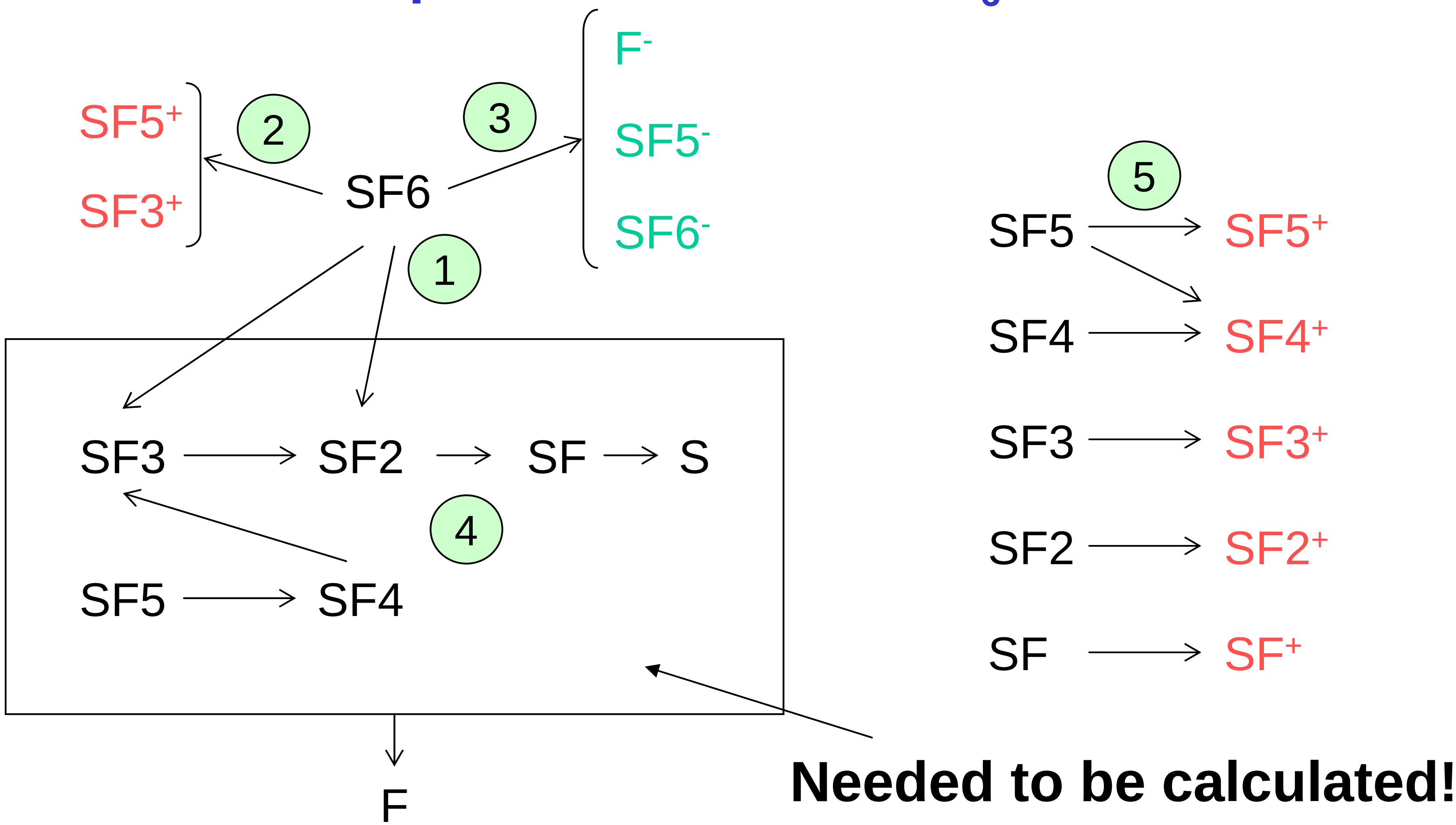
Computational Infrastructure

- Following codes have been utilized for the studies reported here:
  - IO:[1] 2-d fluid model for capacitive plasma simulation,
  - HPEM:[2] 2-d fluid model for inductive plasma simulation,
  - Papaya:[1] 3-d Monte Carlo based feature scale model.



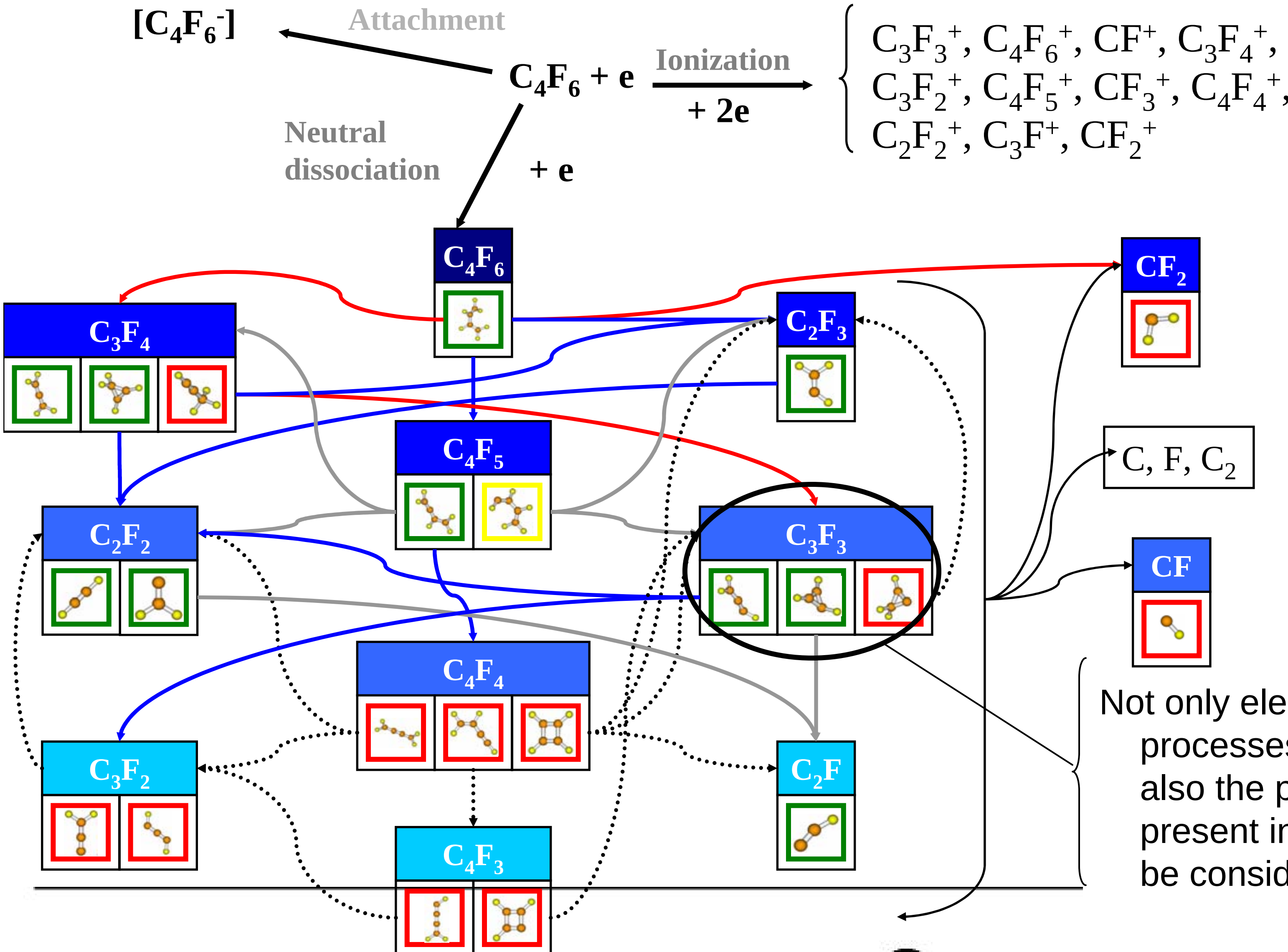
[1]Motorola; [2]University of Illinois

Electron Impact Processes In SF_6 Plasmas



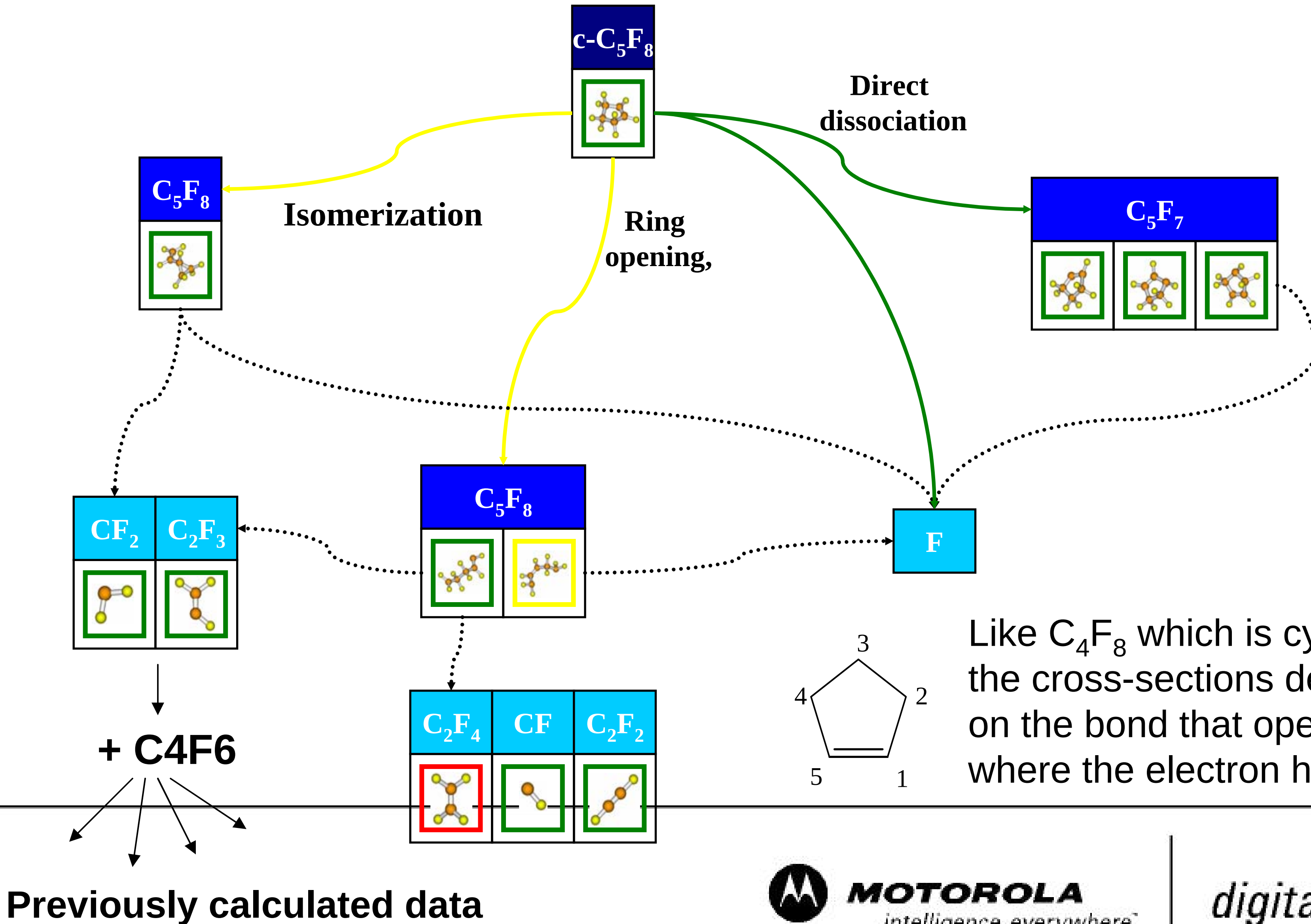
Processes (4) were calculated by us in 2000 to be bale to optimize critical deep Si etch processes used for e-beam lithography.

C_4F_6 Plasma Chemistry in Detail



Not only electron impact processes for the parent but also the plethora of radicals present in the system must be considered.

Neutral Dissociation Processes in C_5F_8 plasmas



Like C_4F_8 which is cyclic, the cross-sections depend on the bond that opens and where the electron hits.

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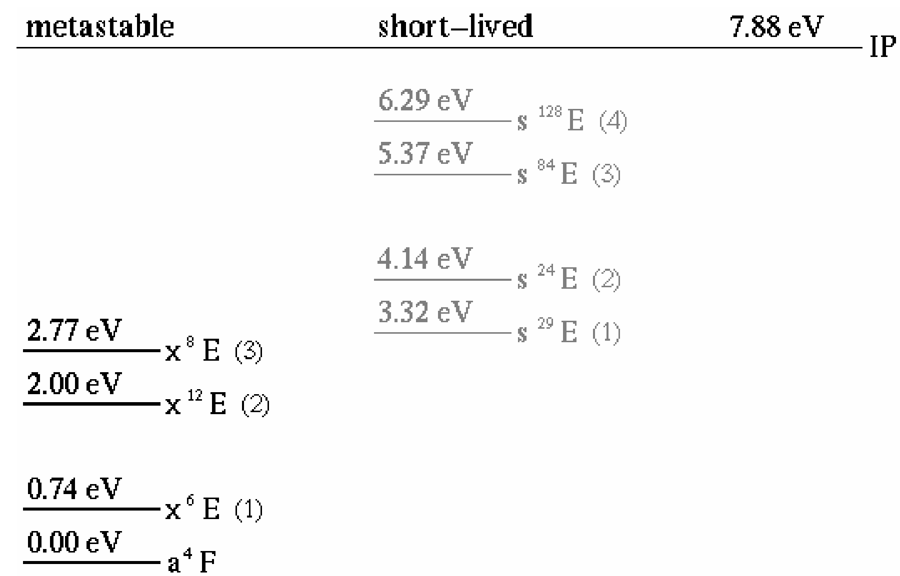
Metallization: Complex Excited State Plasma Chemistry

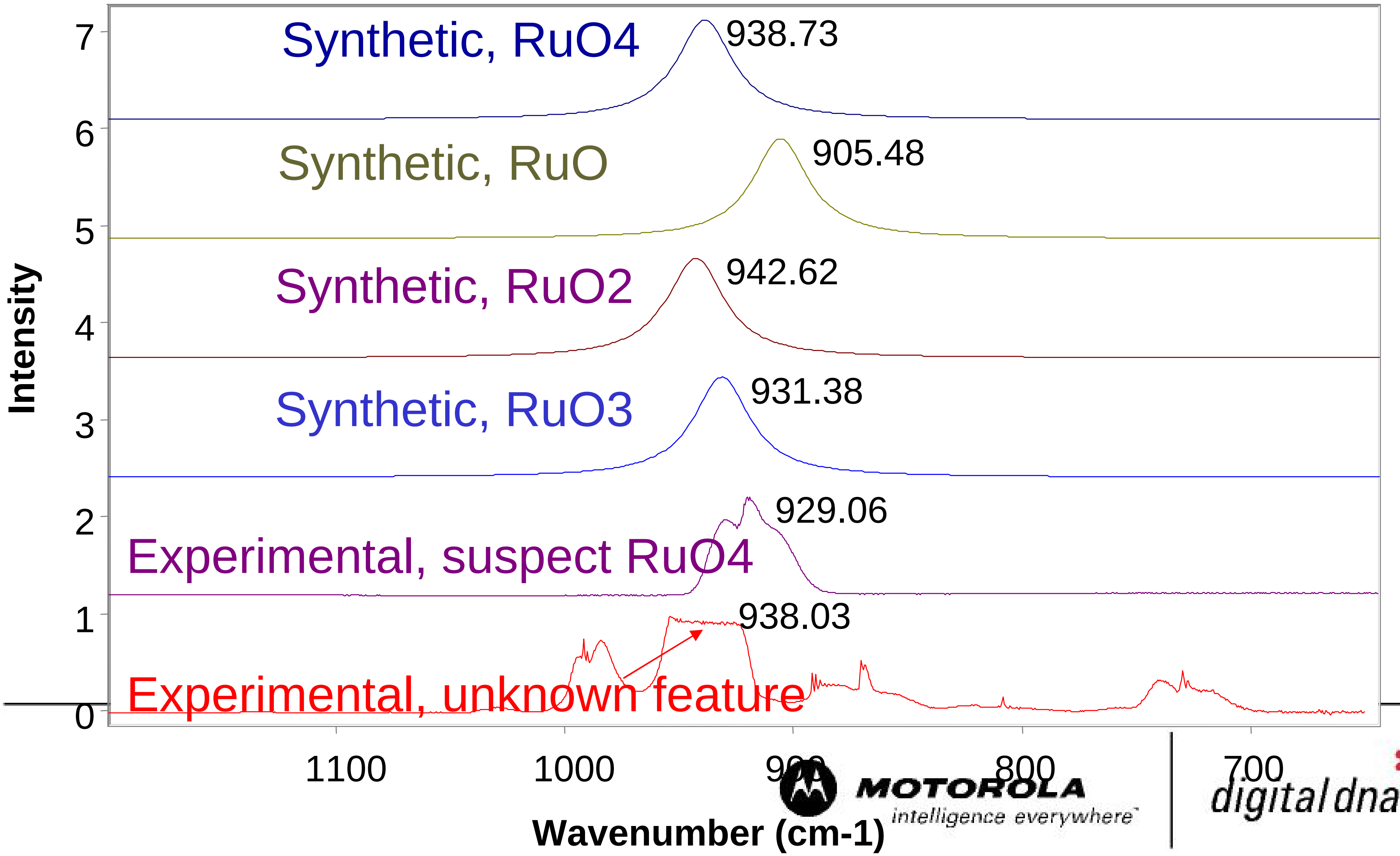
	Relevant Levels	"*Effective*" Metastable Levels	Short-Lived Levels
Ta	>300	4	4
Fe	>480	6	4
Co	>320	3	4
Ni	>200	3	4
Sn	>100	4	3
Mg	>80	1	3
B	>40	1	3

e.g., Co reduced energy level scheme



By Product: Data for Plasma Diagnostics

FTIR spectra/cross section study for RuOx Etch:



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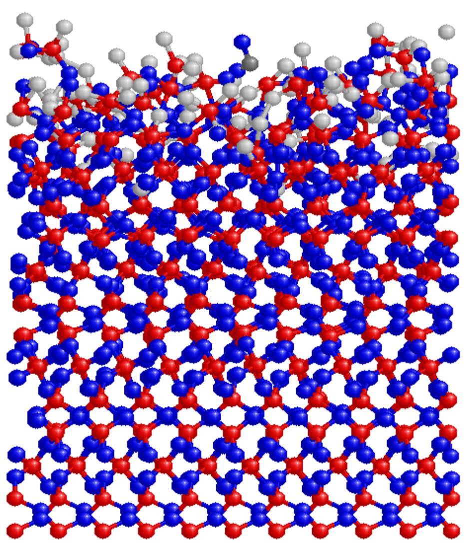
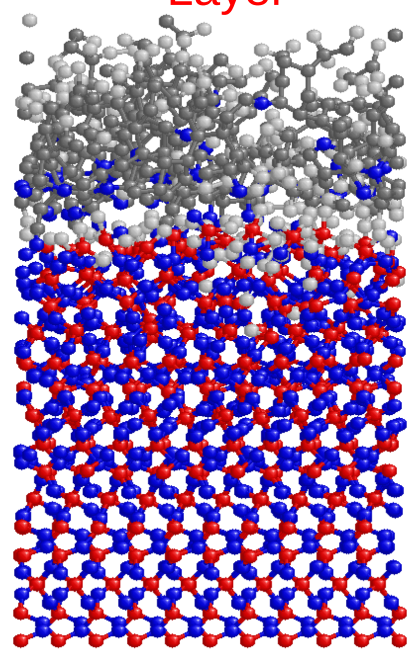
Plasma-Surface Interactions

- We are using molecular dynamics following the approach of Graves and Hamaguchi to develop plasma-surface interaction datasets.

Crystal Passivated with CF_2^+ Ions



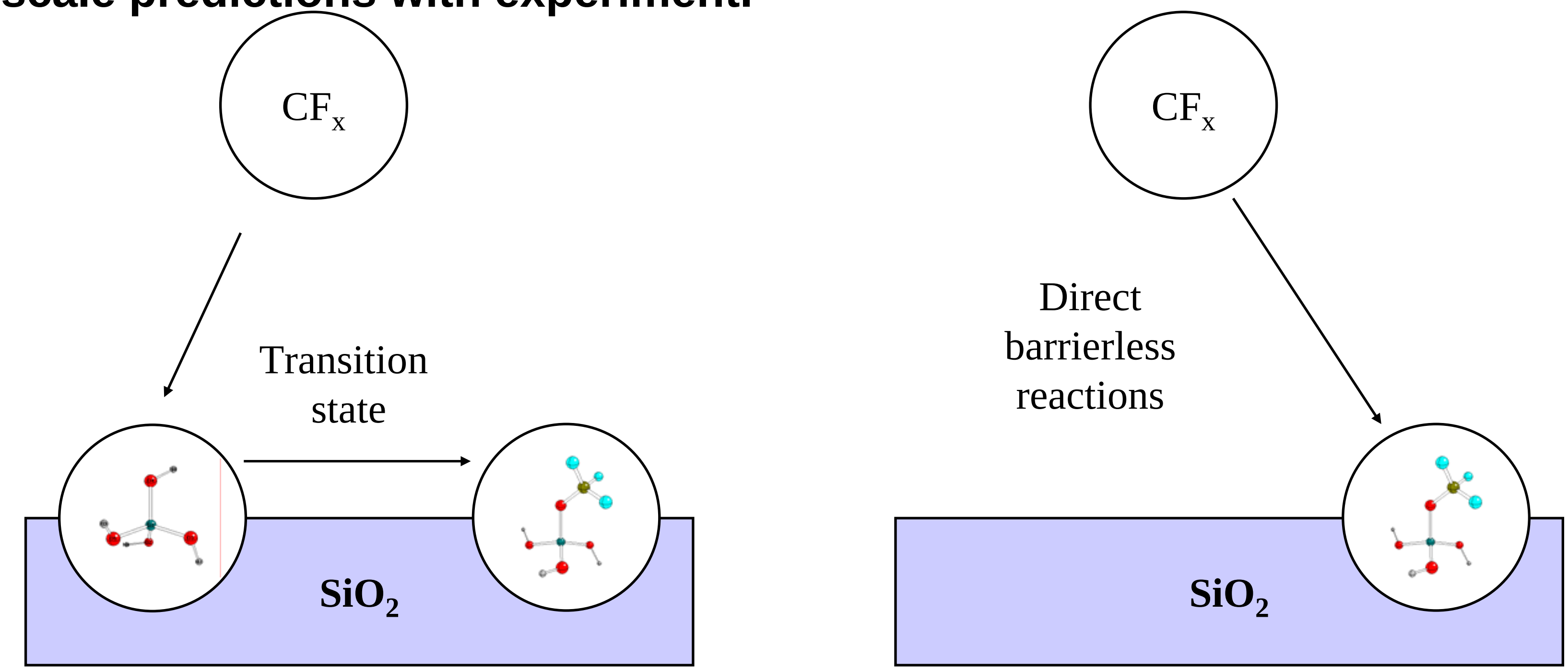
Crystal with Polymer Layer



Red – Si, blue – oxygen, light gray – F, dark gray - C

Plasma-Surface Interactions: Thermal Processes

- **Very complex problem!**
- **We seek relative sticking coefficients and reactions and try to cover a large parameter space using quantum chemistry calculations and small clusters. The final arbiter on these parameters is ultimately comparison of feature scale predictions with experiment.**

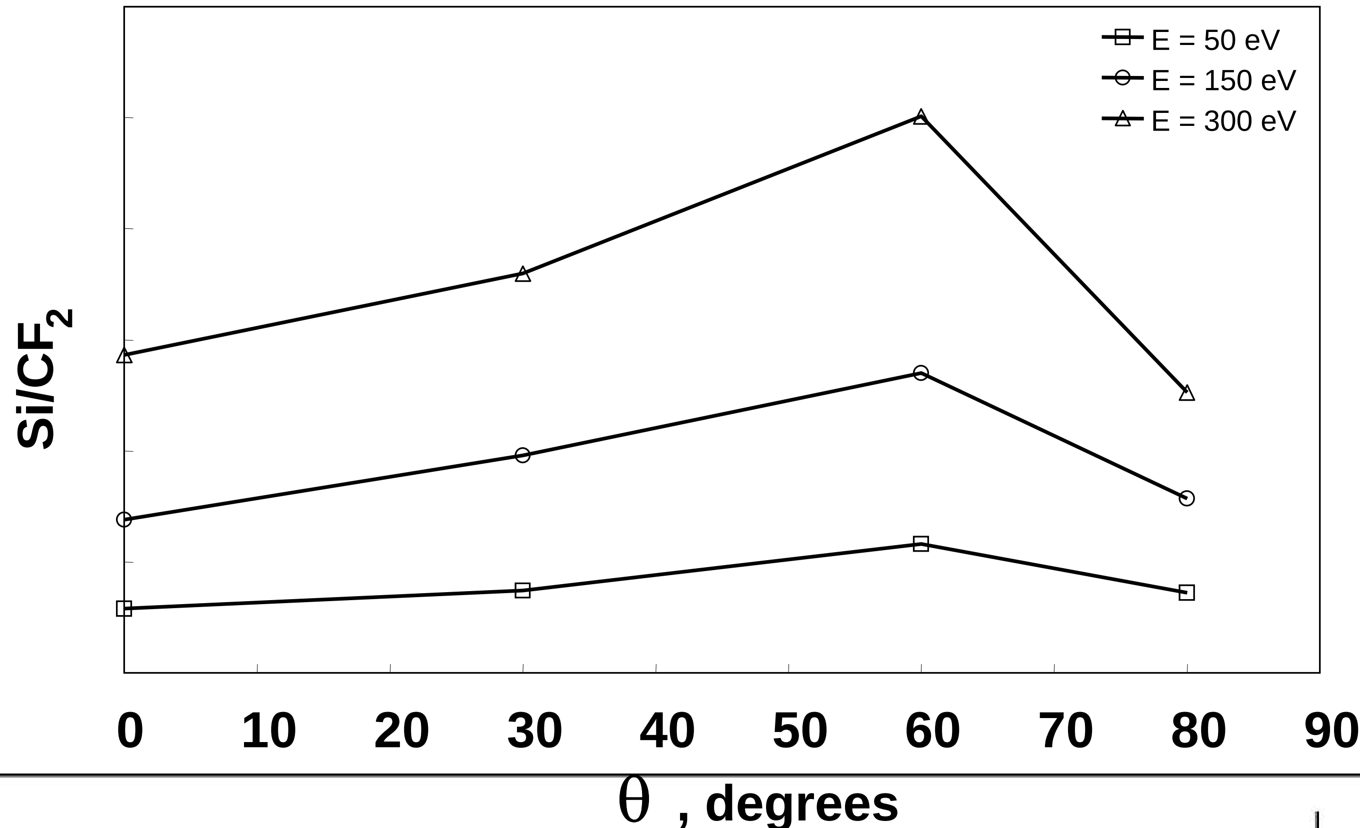


$$s = \gamma(1-\theta)$$

Plasma-Surface Interactions: Yields

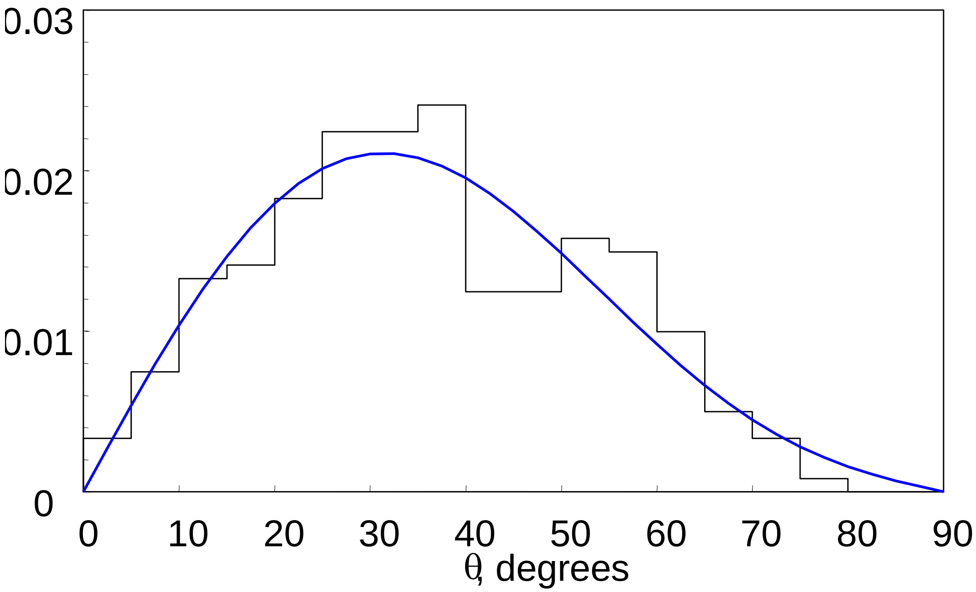
- **An example of macroscopic parameters that are inserted into our models. This constitutes a part of an ever-evolving array of species-surface parameters.**

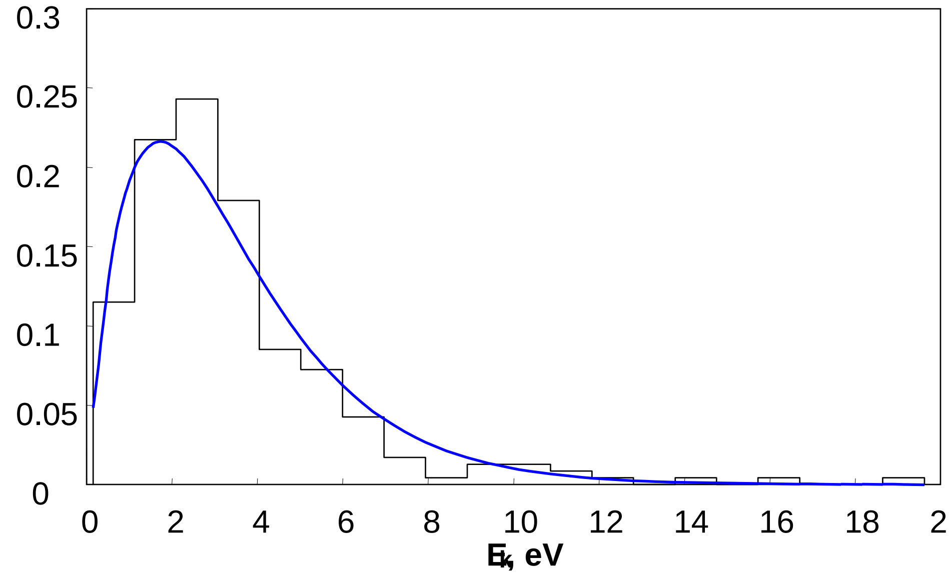
Si atoms removed per incident CF_2^+ ion



Plasma-Surface Interactions: Kinetics

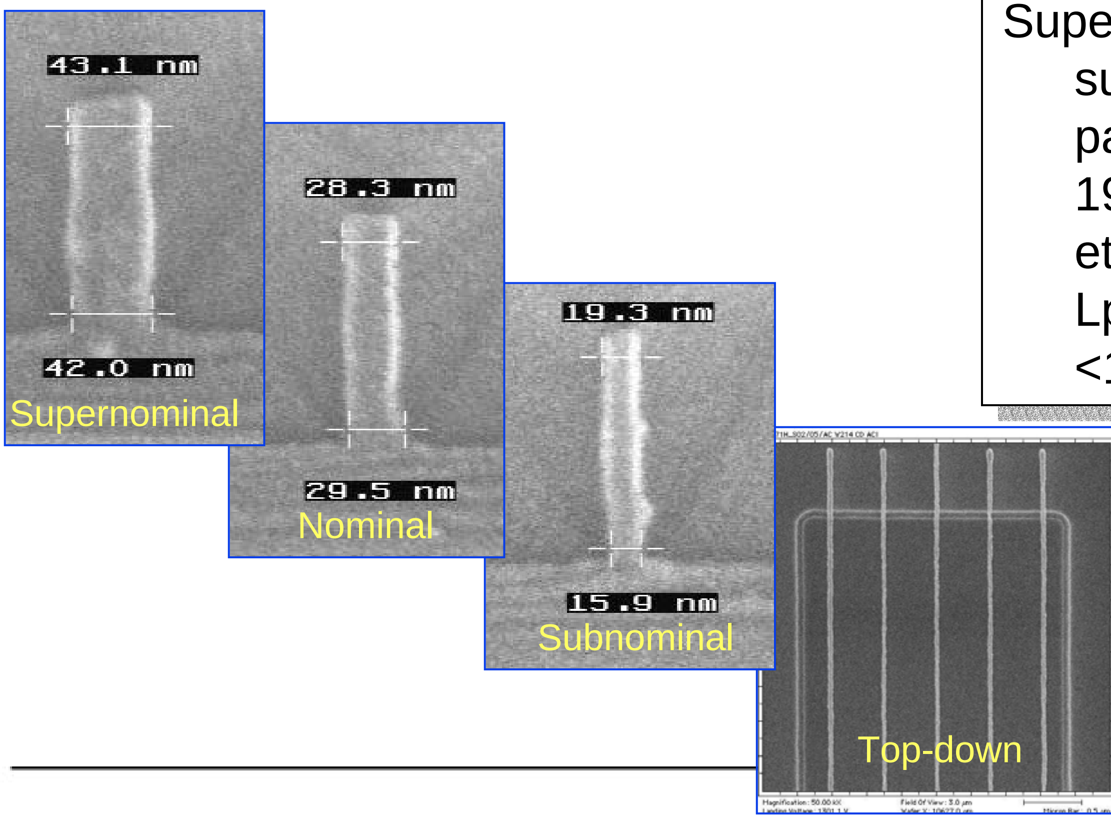
- **Example angular and energy distribution functions for SiF associated with polymer bombardment. Both are needed for feature scale simulations. Understanding the energetics of ejected species (even apart from their nature) is important for the thermal and chemical properties of the plasma.**





Dry Etch Achievements- Transistors

- At the heart of a CMOS transistor's performance is the gate patterning process. Product requirements demand innovative patterning techniques which produce gate lengths far smaller than the theoretical limits of lithography wavelengths.

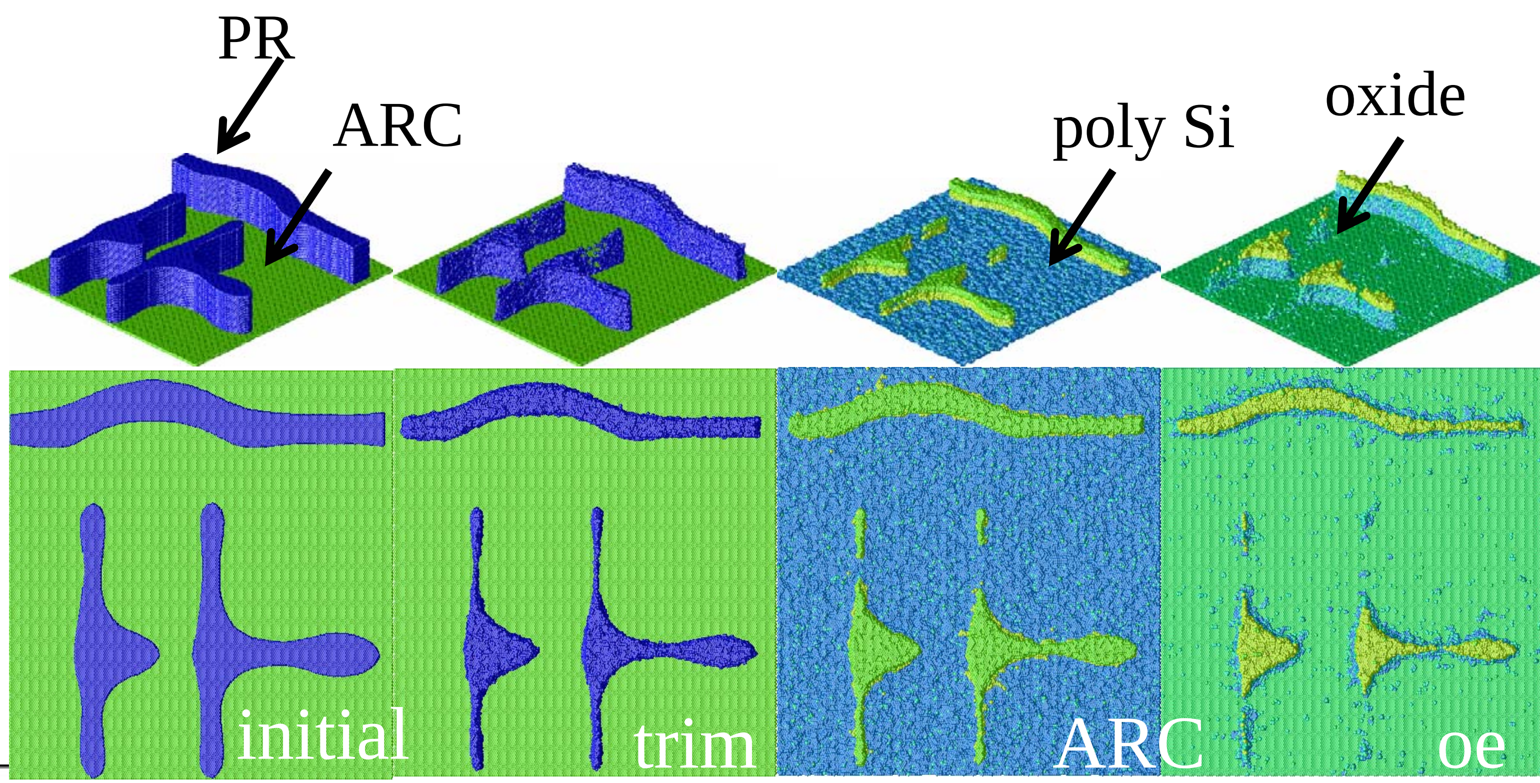


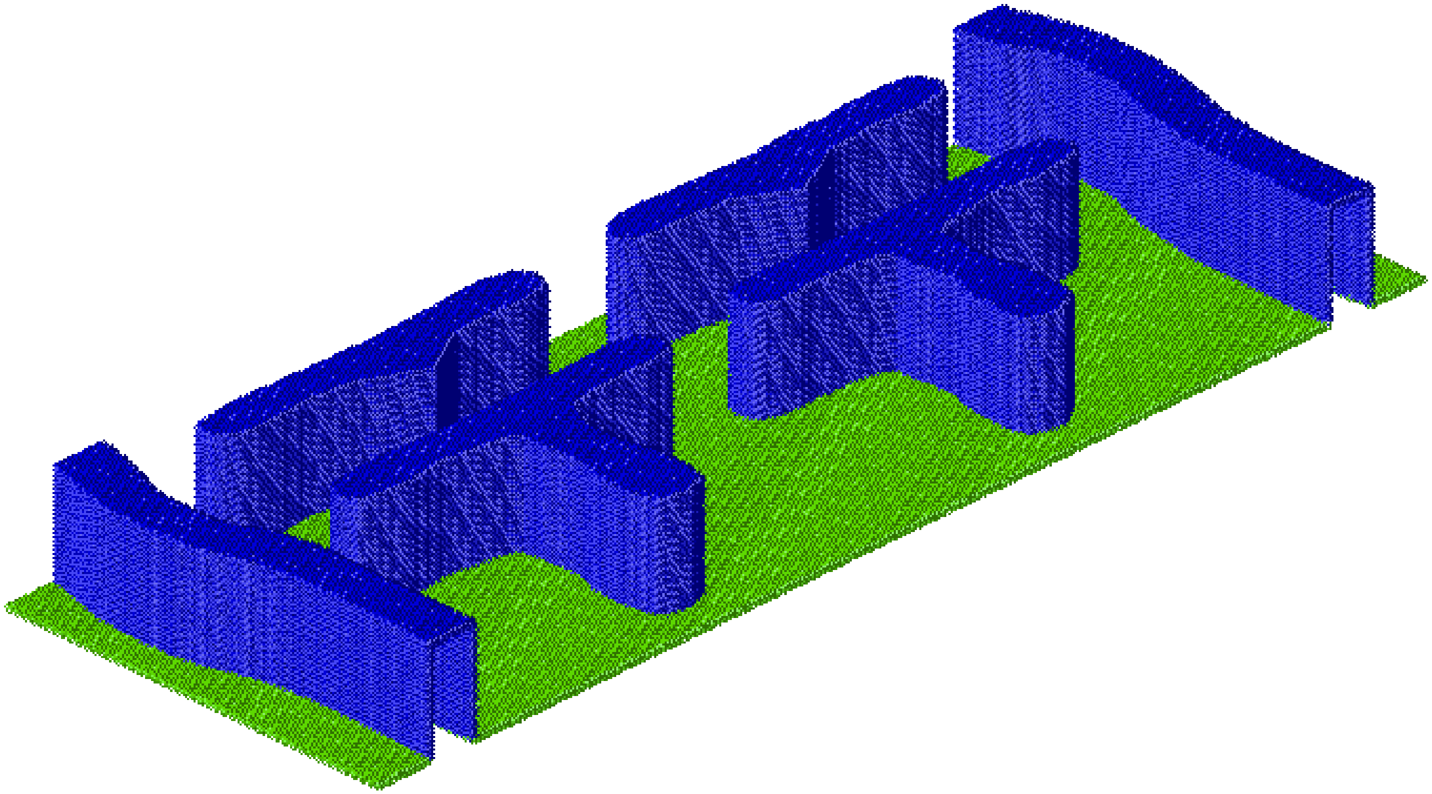
Supernominal, nominal, and subnominal Poly-Si lines patterned with conventional 193nm lithography, and etched down to <20nm Lpoly. Gate dielectric is <13Å oxynitride.

Advent of novel structures and new materials brings huge challenges

FEOL Computational Integration

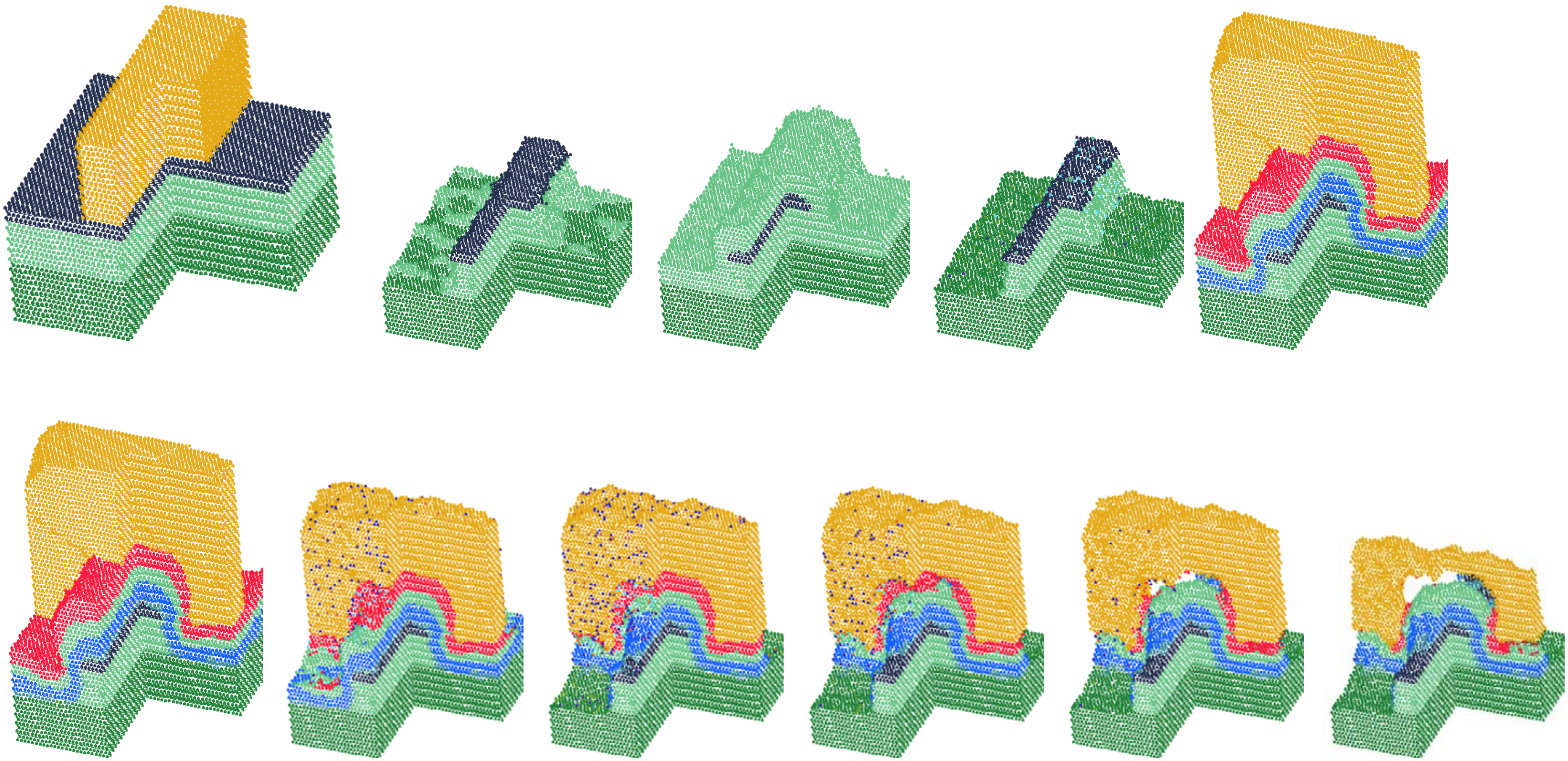
- **Calculated (w/ Papaya) evolution of an SRAM gate after 7 etch steps.**
- **Shown here is an over aggressive trim blows out the gates. These would be dealt with through lithographic adjustments or etch engineering.**





Applications to Process Development for Novel Devices

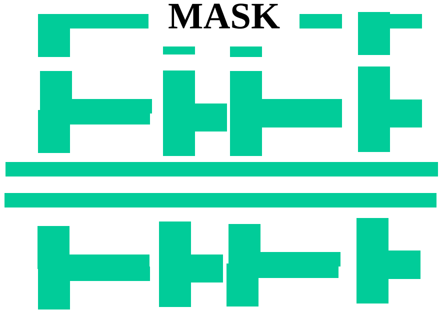
An example of fin process step gone awry!



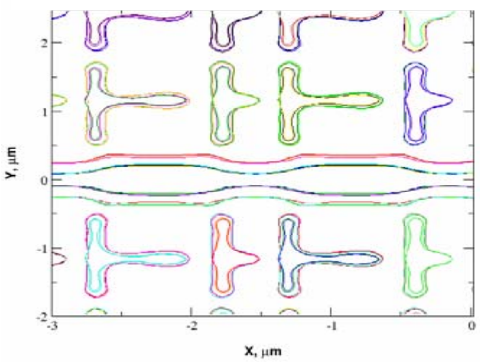
Computational Process Integration (FEOL)

Mask-to-Etched Feature Predictions

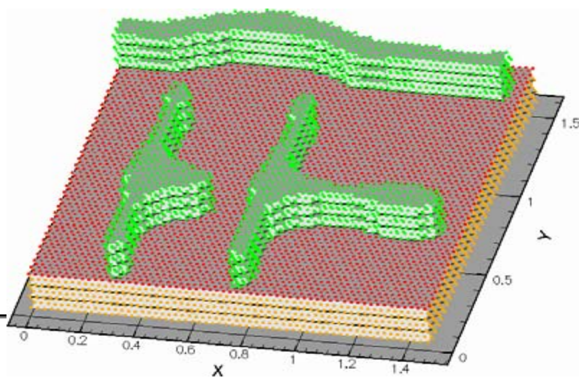
MASK



LITHOGRAPHY-ST-LITH



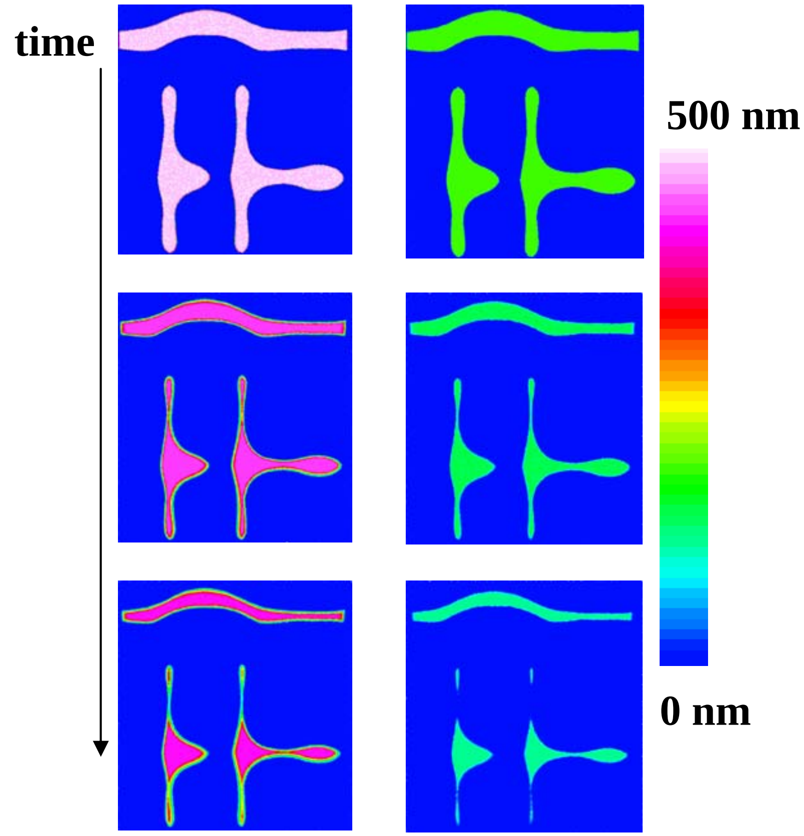
TRIM ETCH-PAPAYA



Mask Manufacture and Design

Initial Height

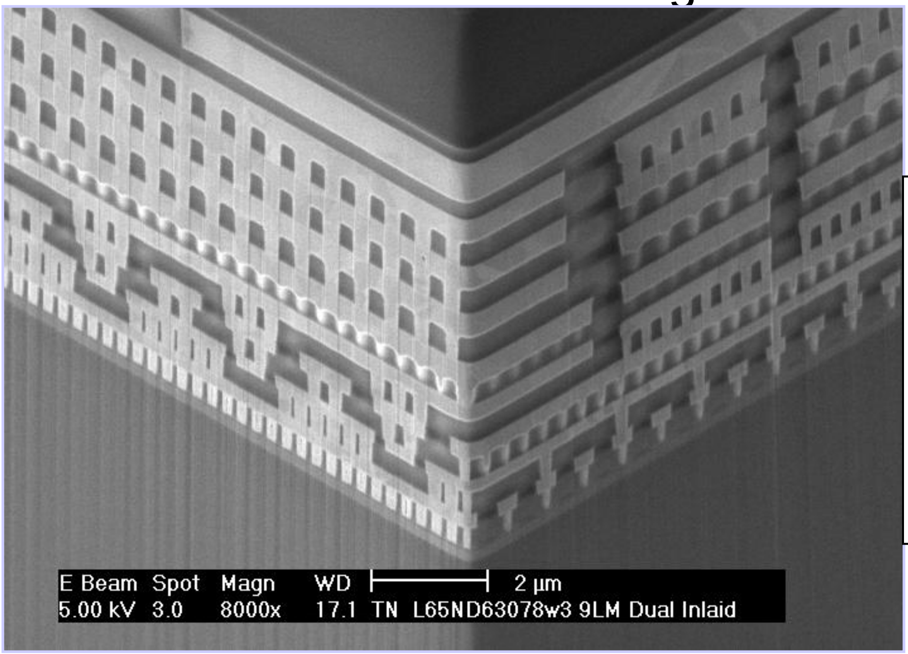
500 nm 200 nm



Example of Trim Etch for Different Initial Resist Heights

Dry Etch Achievements- Interconnect

- Advanced technologies bring a new host of challenges in interconnect processing: more metallization layers using novel materials, dual-inlaid metallization integrations for cost savings, as well as further shrinking of the feature dimensions.

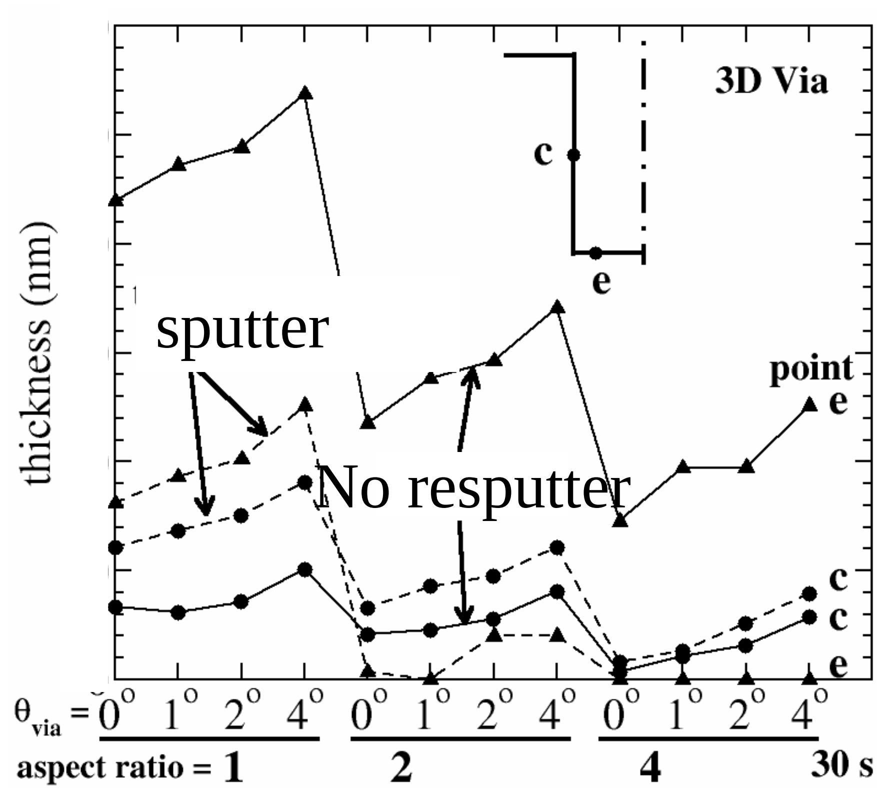


Motorola's HiPerMOS7 SOI product features nine levels of metal utilizing low-K dielectrics, implementing dual-inlaid processing at every layer.

Etch-Metallization Integration: Text-book view

Dual-inlaid structure with straight side-walls and well defined sidewall angles. Fill is as-expected.

Scaling for idealized cases is well defined as a function of via side-wall angle and aspect ratio.



BUT!

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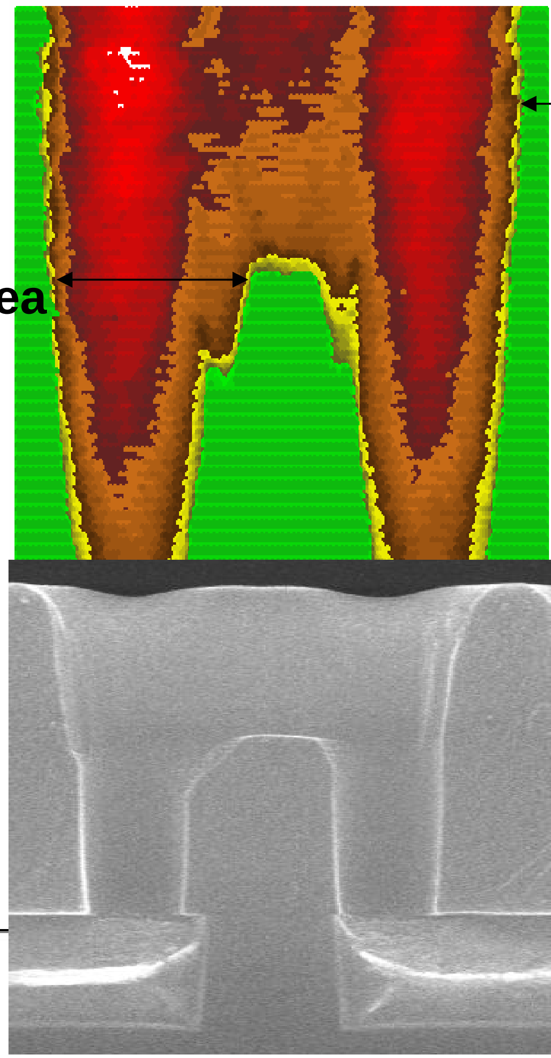
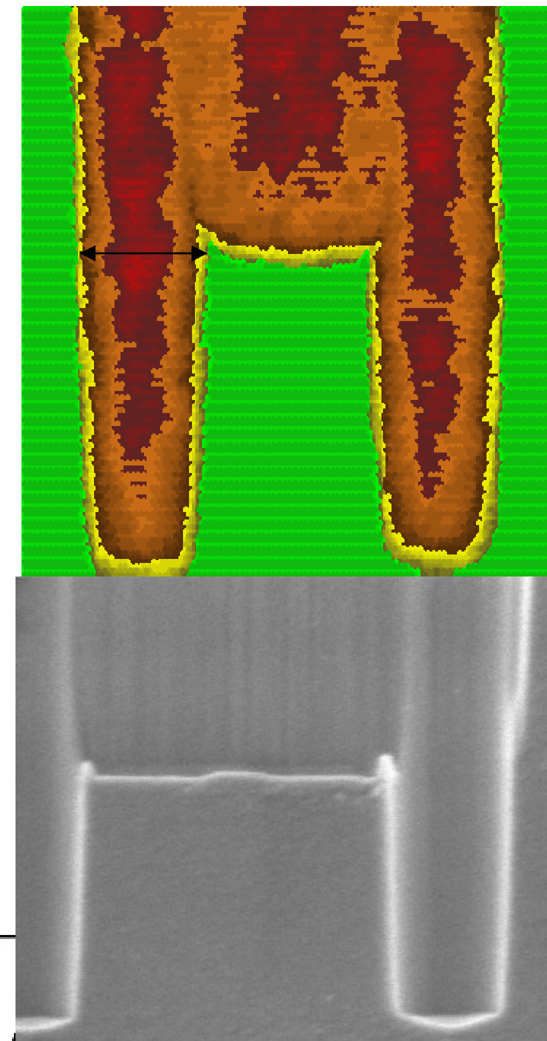
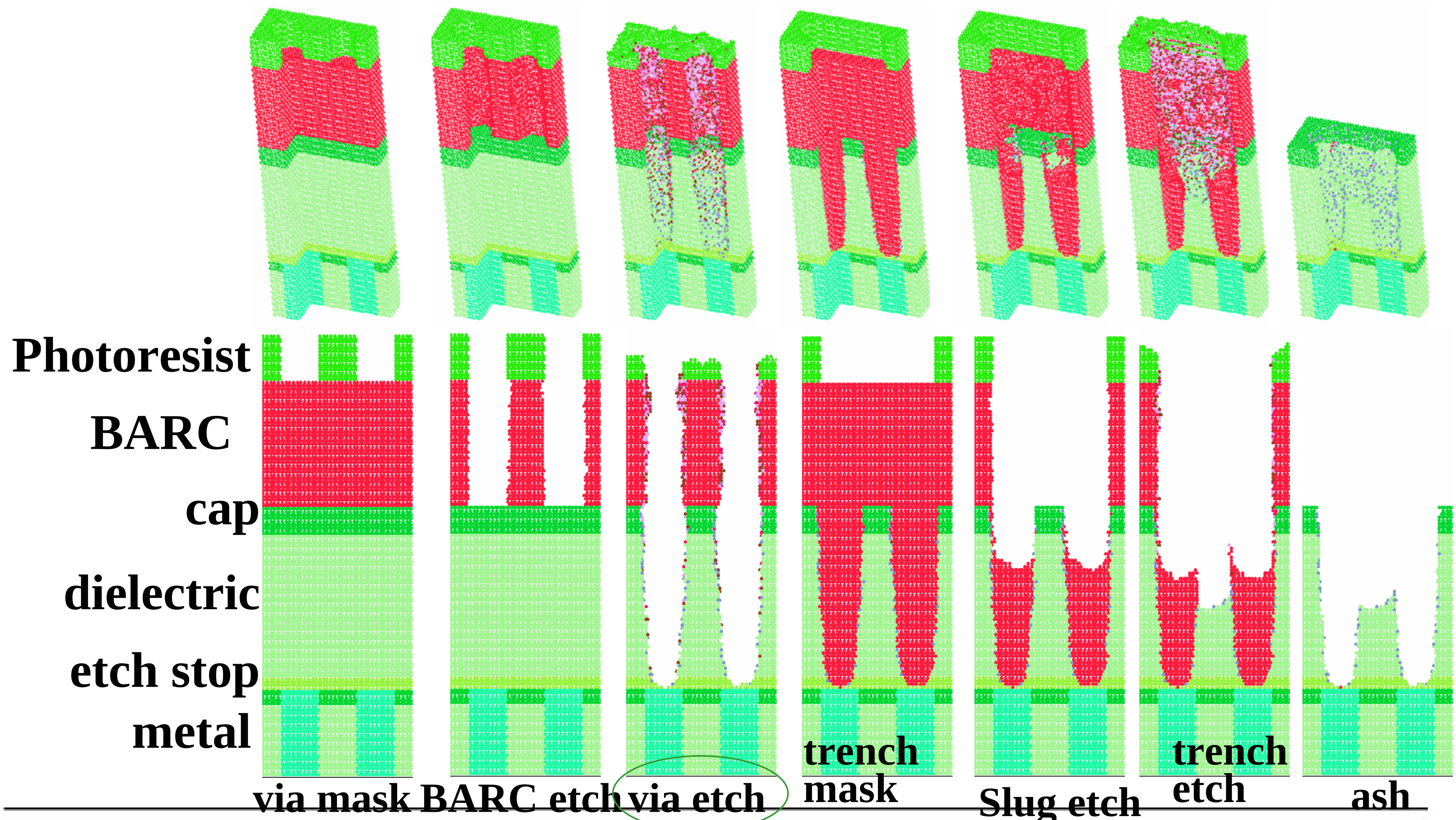
BEOL Computational Integration

Less polymerizing chemistry vs More polymerizing chemistry



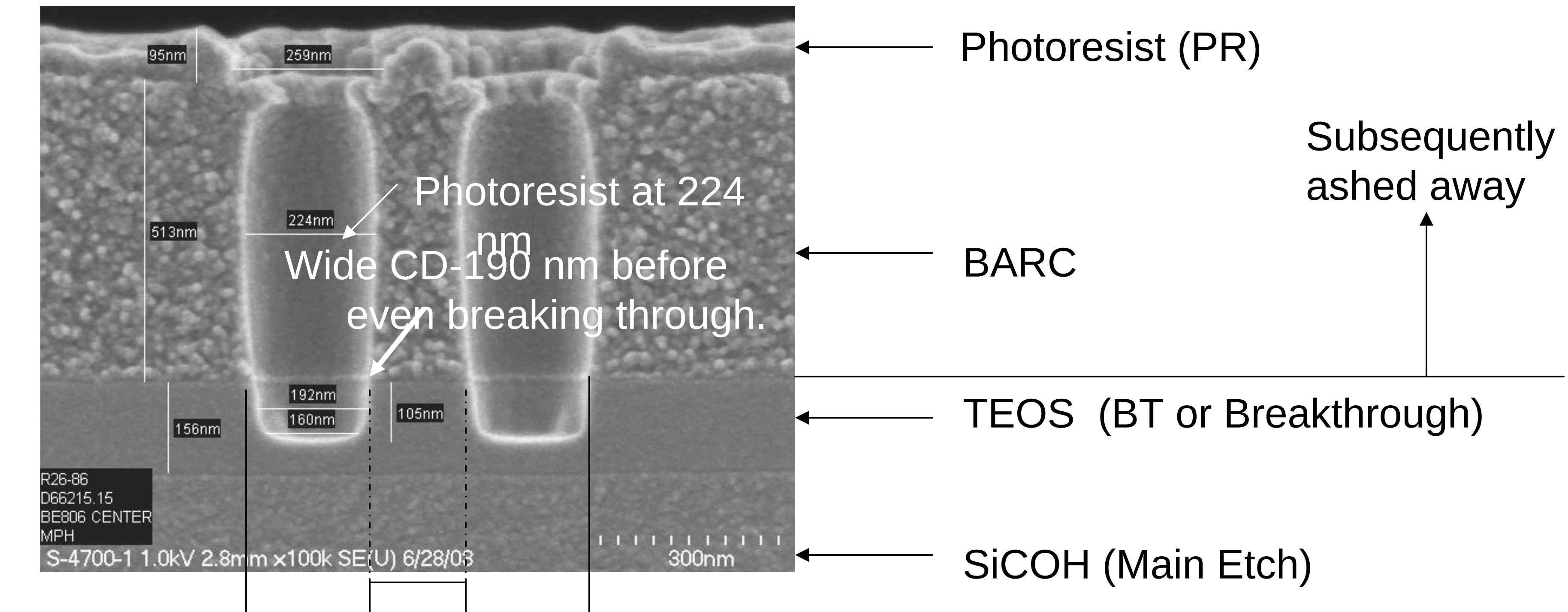


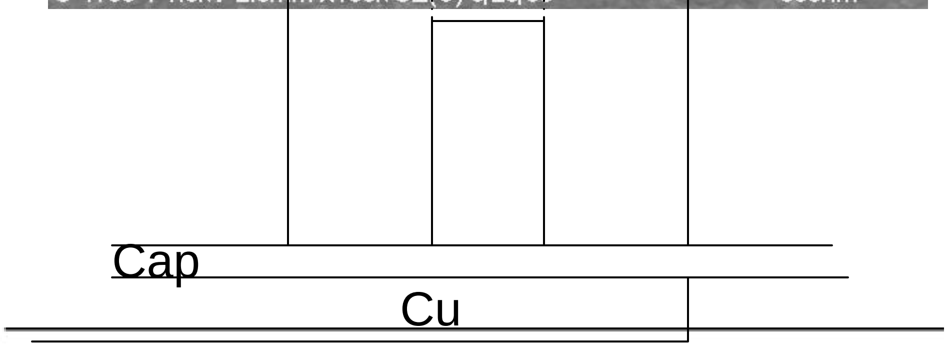
BEOL Computational Integration



- See Next Slide

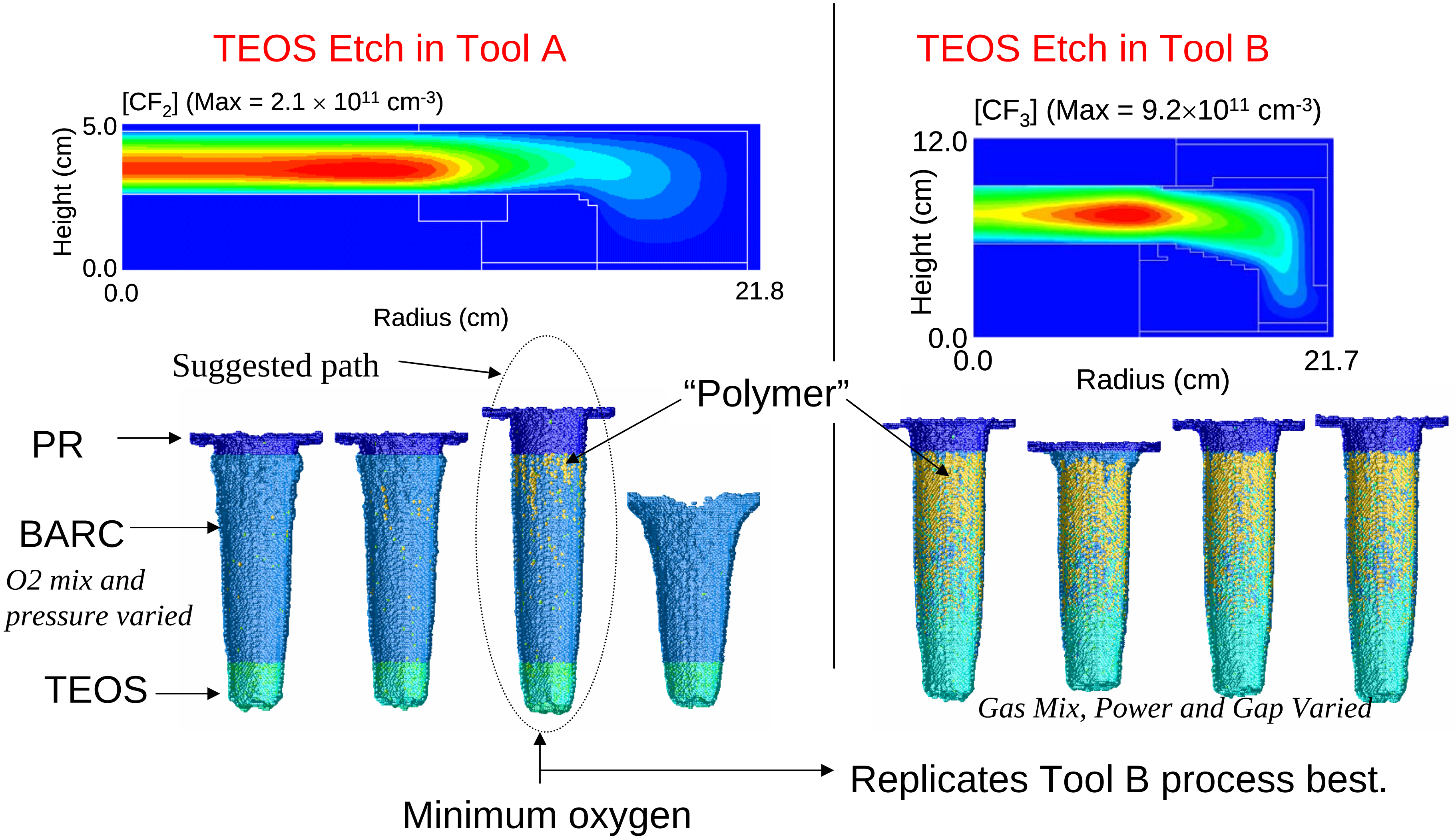
First Stab at BT Process from Vendor



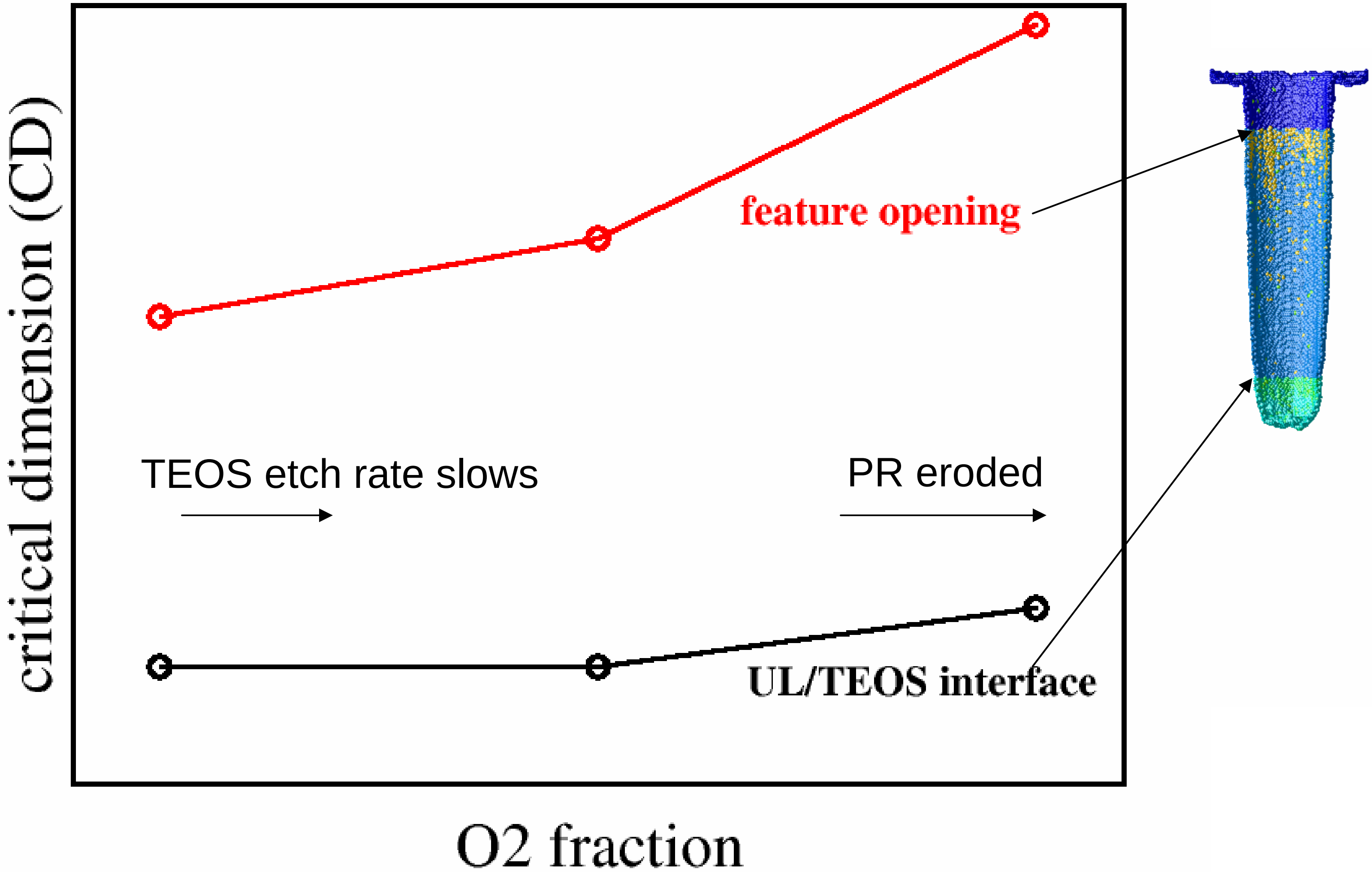


- **Slow etch that attacks PR dimension.**
- **Lost sidewall (CD) cannot be recovered in subsequent steps!**
- **7 degrees of freedom.**

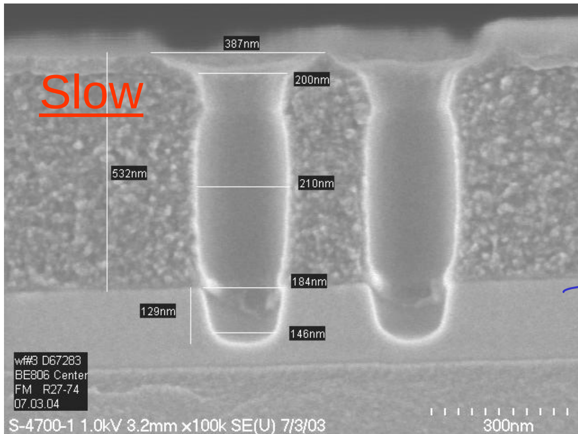
Two Tools - Two Processes



O_2 in Process Critical to CD Control

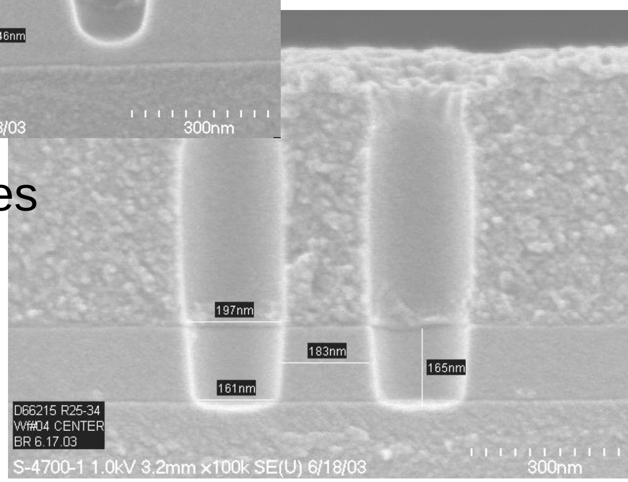


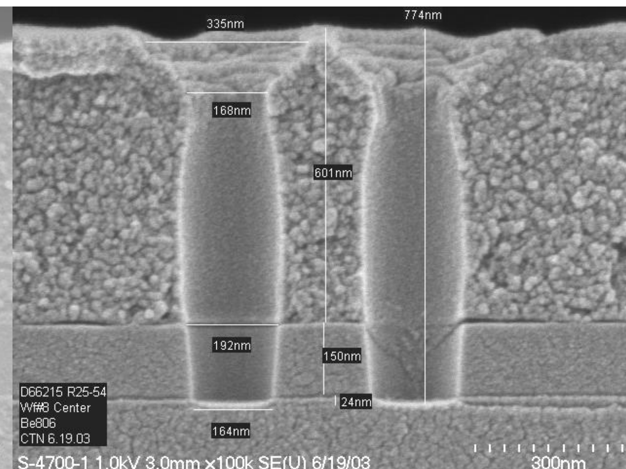
Experimental Verification



Demonstrates O_2 need

Optimal

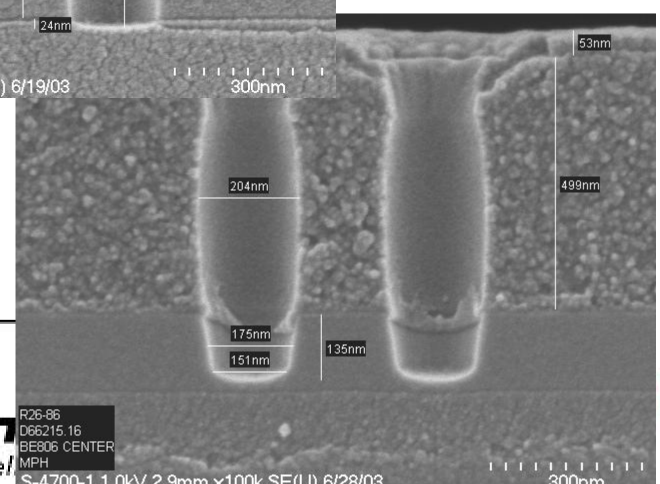




Needs Ar and more polymer

Poor CDs

Slow



Summary

- Fundamentals based simulations can and do have an engineering impact in unit process and process integration development.
- The physics, chemistry and materials interactions problems remain complex but are tractable enough to warrant tackling them inside the semiconductor manufacturing industry.
- Developmental activities remain critical to making the leap to “predictive” simulation and fulfilling the promise of simulation adding value.