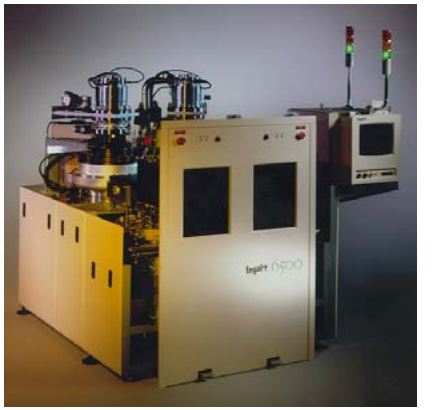
Abstract

There is renewed interest today in employing medium density capacitively coupled reactors for plasma etch applications in advanced semiconductor manufacturing processes, like creating trenches and vias for damascene structures in complex stacks of dielectric films and low k materials, or patterning noble metals and perovskite ferroelectrics for nonvolatile memory storage capacitors. One of the critical attributes in any plasma reactor design is the inherent symmetry of the reactor. A highly symmetrical plasma etch reactor will prove itself again and again across almost all of the ways we measure plasma etch performance. Gas flow symmetry in the reactor, for example, will influence etch nonuniformity, critical dimension control, and particle performance; electrical and, where applicable, magnetic field symmetry, will reveal itself in those three areas and will be an important factor in contributing to and propensity toward plasma etch-induced damage. Additionally, the thermal symmetry of the wafer electrode, along with the symmetry of the electrical field superimpose in the plasma reactor by RF-biased wafer electrodes (and by electrostatic wafer electrodes), can have profound effects on plasma etch reactor performance.

We will report and provide data on the design and performance of Tegal's sixth generation capacitively coupled plasma etch reactor, and demonstrate how the inherent symmetry and uniformity of the source design, reactant flow, magnetic confinement, RF wafer bias, ESC construction, and thermal profile across the wafer electrode can be usefully applied to the etching of ferroelectric stacks. We will also present data on agile control of elevated wafer temperatures during etching of ferroelectric stacks.

tegal



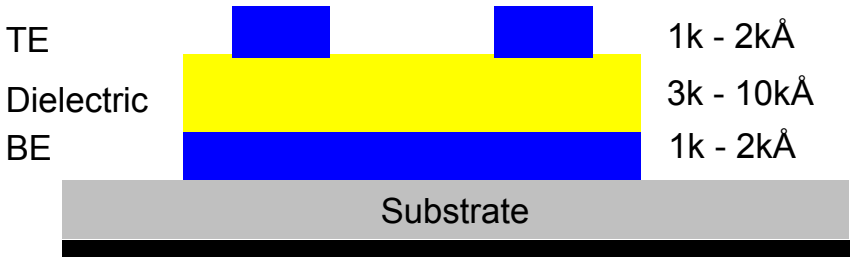
A Highly Symmetrical Capacitively Coupled High Density Plasma Reactor with Agile Wafer Heating for Ferroelectric Stack Etch

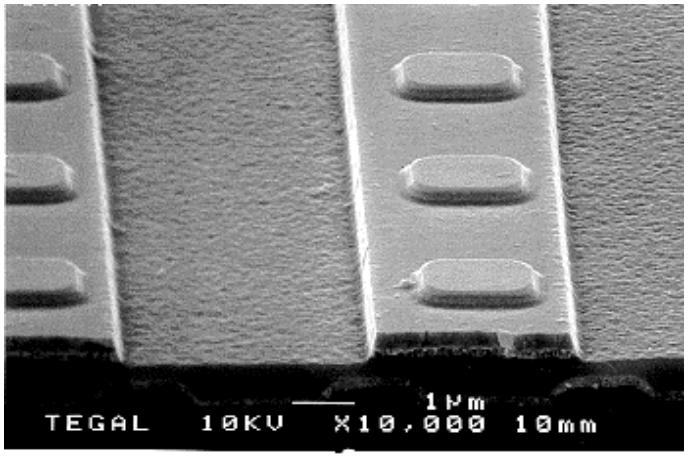
Geneviève Béïque, Steven Marks, John Almerico, Paul Werbaneth

Outline

- Introduction
- Highly symmetrical capacitively coupled reactor design
  - Dual frequency RF configuration
  - Magnetic confinement
  - ESC
  - High pumping speed
- High Temperature Features
  - High Temperature ESC
  - Wafer Temperature Control
- Examples of Ferroelectric stack etch
- Conclusion

What are we etching?





- Example of MFM stack etch
- There are many variations (in materials choice and approaches)
- Key etch results are profile, residue, selectivity, rate
- SEM: Pt top electrode, PZT dielectric, Pt bottom electrode

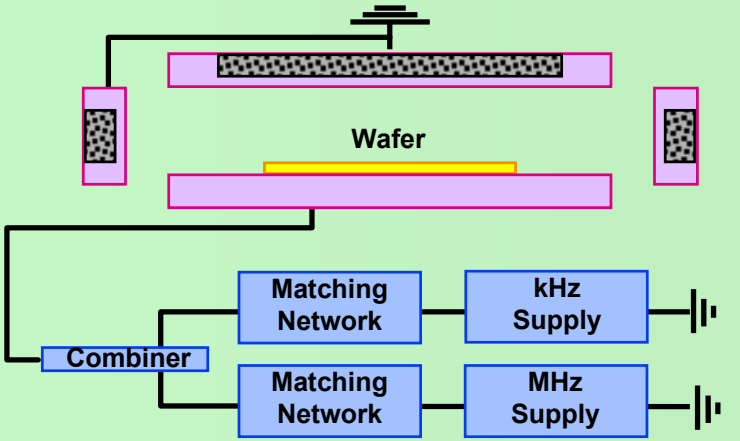
Introduction

- Description of Tegal CCP reactor
- Description of Tegal ICP reactor
- Highlights of the benefits of CCP reactor for FeRAM application

Evolution of Tegal CCP Reactors

Generation Model / Year	Reactor	RF	Pumping	Chemistry	Wafer Temp
I 700 / 1979	Diode (Top Powered)	HF	Rotary	Inert	Heated
II 701 / 1981	Diode	HF	Rotary	Inert	Water Cooled
III 802 / 1983	Diode	LF, HF	Rotary + Blower	Reactive	Water Cooled
IV 1500 / 1985	Triode	LF, HF	Rotary + Blower	Reactive	Water Cooled
V 6000 / 1991	Triode	LF, HF	Turbo	Reactive	He Cooled
VI 6510 / 1994	Triode	LF, HF	Turbo	Reactive	He Cooled
VII 6540 / 1998	Triode	LF, HF	Turbo	Reactive	Heated w/ Agile Control

Tegal HRe- 4 ™ Plasma Technology

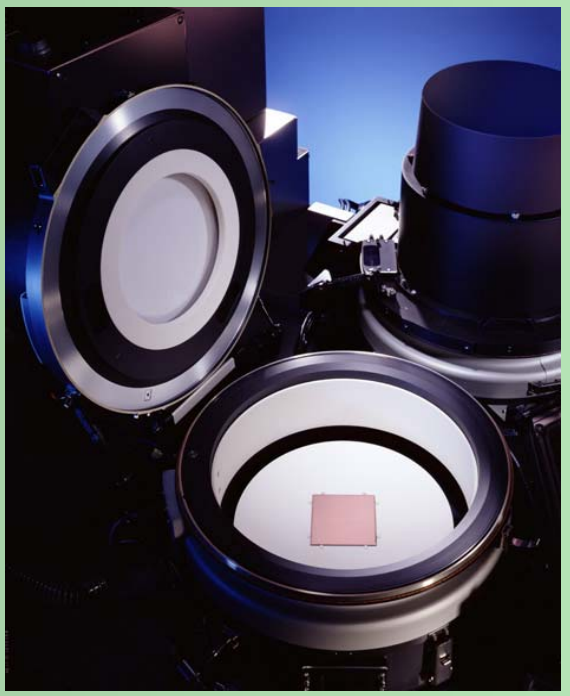


- Medium Plasma Density
- Dual Frequency
- Permanent Magnet Confinement
- Top Pumped - 30 sccm/mT
- 200 mm
- -40º to 200ºC
- Heated ESC up to 500ºC

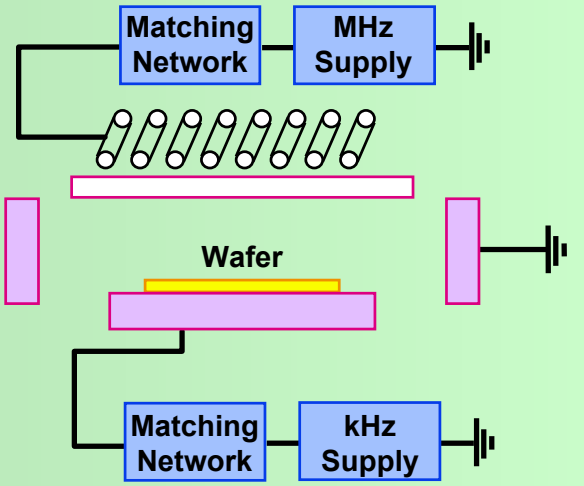
HRe⁻

Pt, Ir/IrO_2 , Ru/RuO_2 electrode etch
PZT and Y-1 (SBT) ferroelectric etch
BST high-k dielectric etch

Tegal Spectra™ Plasma Technology



Spectra



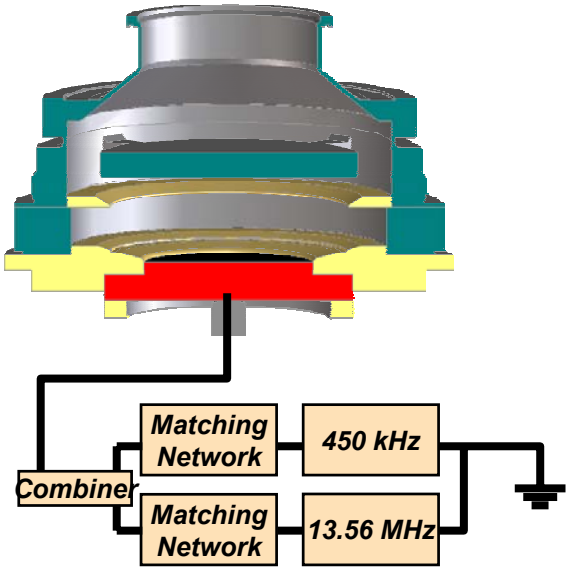
- Medium to High Plasma Density
- Dual Frequency
- Bottom Pumped - 60 sccm/mT
- 300 mm
- -40°C to 200°C

MRAM etch
GMR etch
TMR etch
Alumina etch

Why HRe- for FeRAM applications?

- **Process stability regardless of number of wafer processed in the chamber.**
  - Power is not attenuated from conductive by-product over time
- **High Mean Wafer Between Clean**
  - No sputtering of internal chamber surface
  - Temperature control of all chamber surfaces
- **High ion energy**
  - All power through the wafer produces highest available ion energies
- **High temperature ESC**.

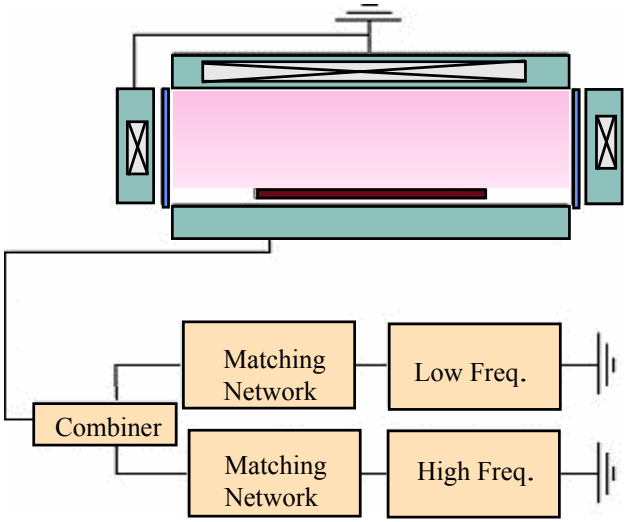
1- Highly Symmetrical Capacitively Coupled Reactor Design

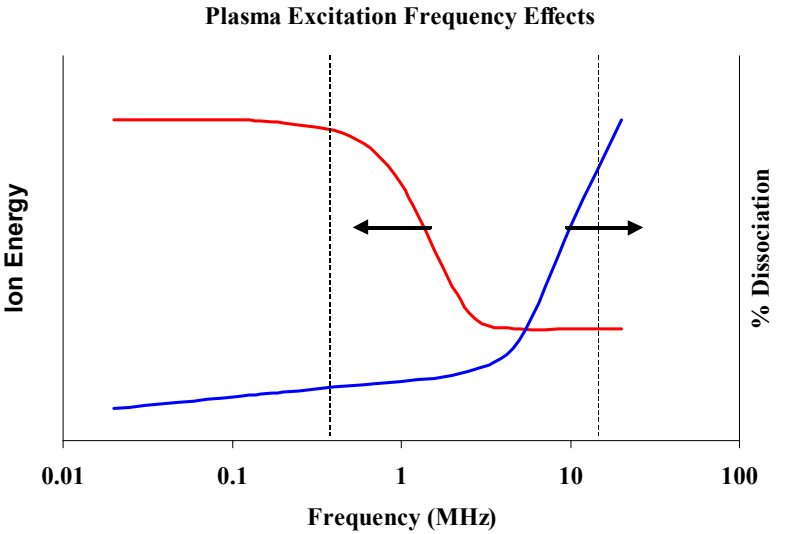


Symmetry is scrupulously maintained in the HRe- reactor design

- Gas injection
- Dual frequency RF configuration
- Magnetic confinement
- Axial symmetric pumping

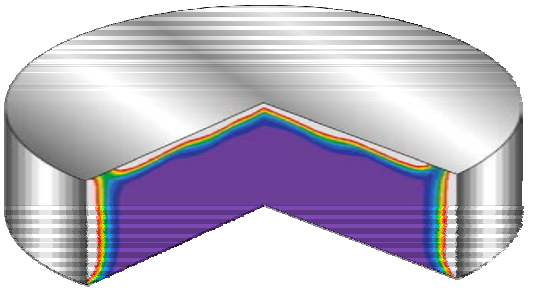
Patented dual-frequency HRe-

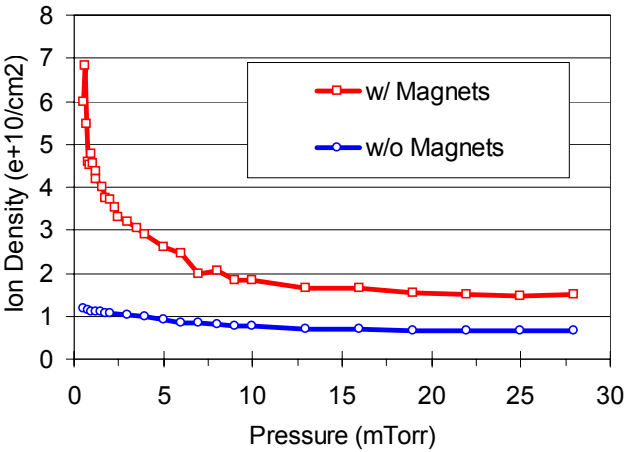


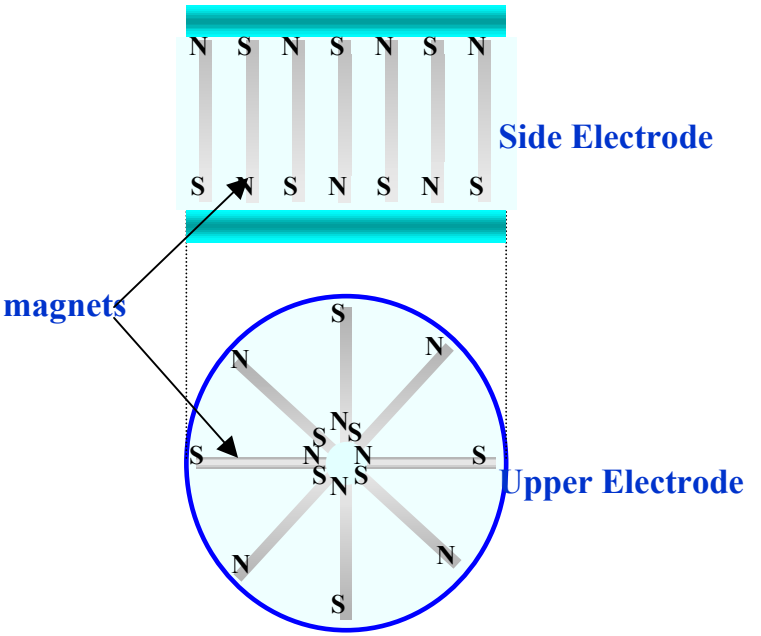


- Symmetry is maintained with the RF coupling.
- Tegal uses a patented dual-frequency RF design to drive the plasma at 13.56 MHz and 450 kHz simultaneously for maximum **ion bombardment and plasma generation** efficiency.
- The ion energy controlled by low frequency RF; Plasma density controlled by high frequency RF.

High-density Reflected Electron reactor



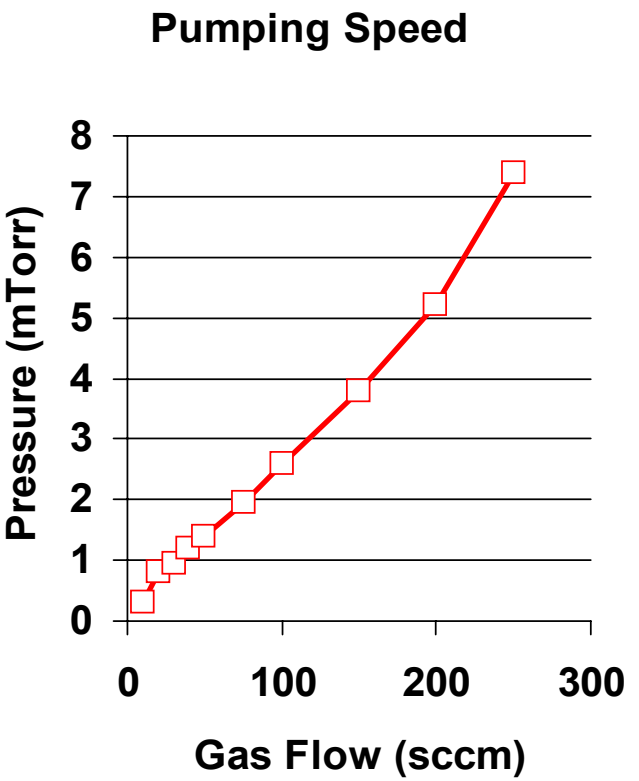




Permanent SmCo magnets are embedded in the upper and sidewall electrodes; alternating poles faces creates magnetic fields that reflects electrons back into the plasma volume.

This enhances plasma density at low pressure.

HRe- Pumping Speed



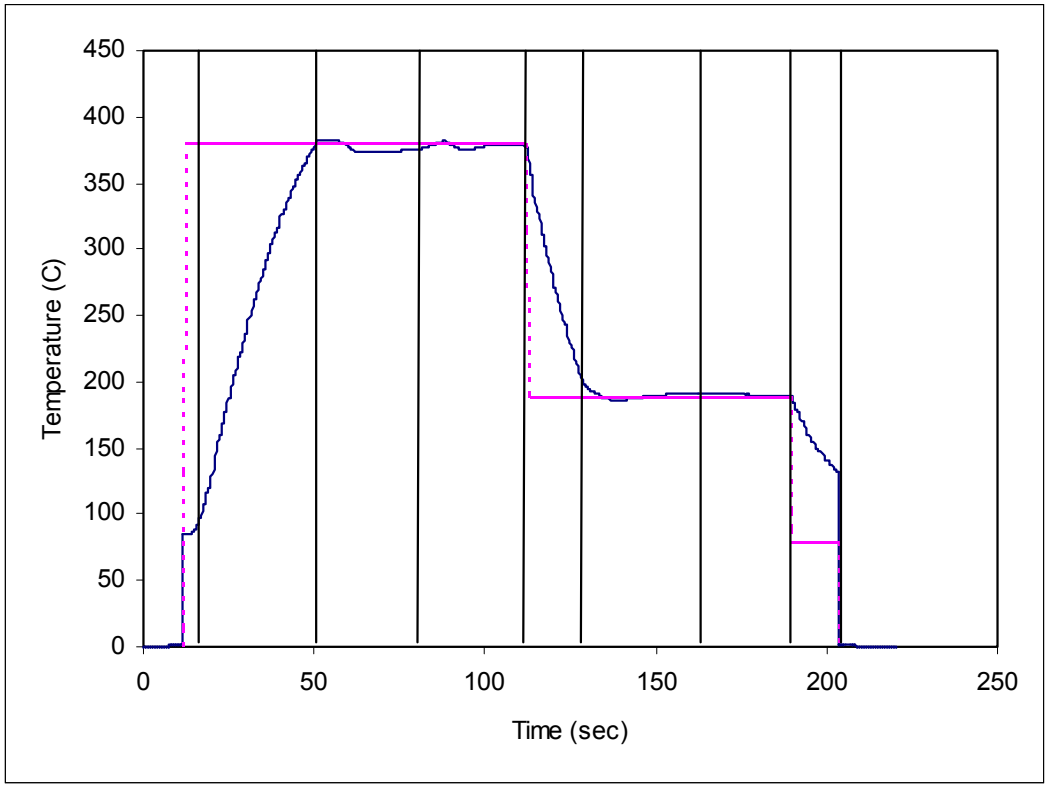
- High conductance design with axial-symmetric pumping
- Nominal operating pressure: 2 to 5 mTorr
- >35 sccm/mTorr

Electro Static Chuck Features

- Johnsen-Rahbek monopolar Ceramic ESC Design Accommodates Any Material or Wafer Backside
- Tegal Patented ***Auto Clamp*** Assures Each Wafer is Optimally Clamped
- Self Calibrating Backside Wafer Temperature Sensing in addition to chuck temperature sensing
- Tegal Patented ***Wafer Temperature Control***
- Wafer Temperature is a Process Recipe Parameter.

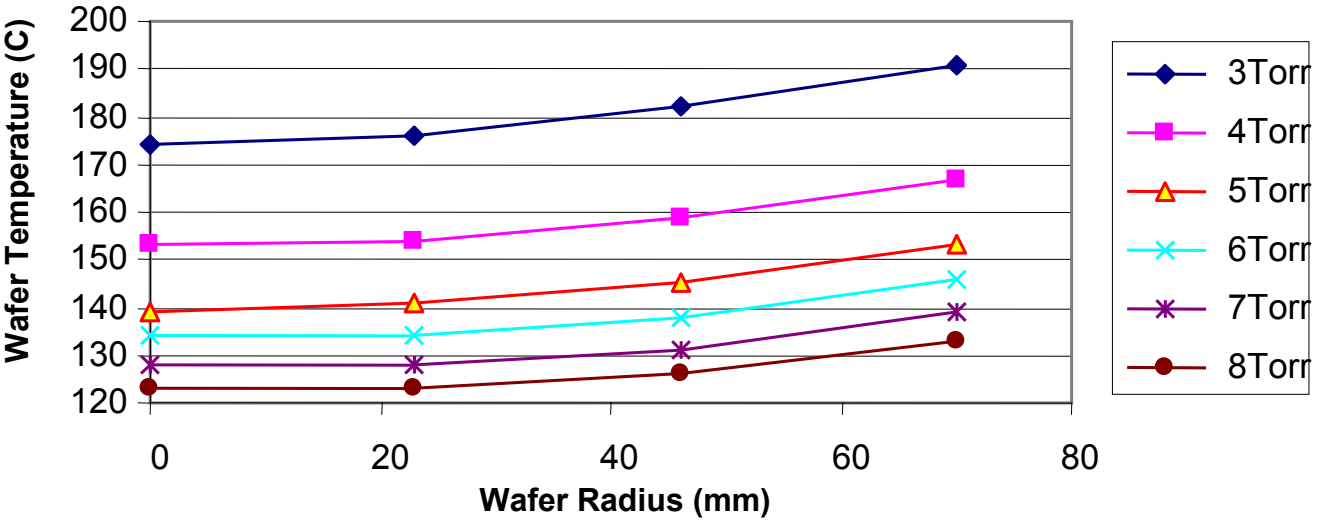
Wafer Temperature Control

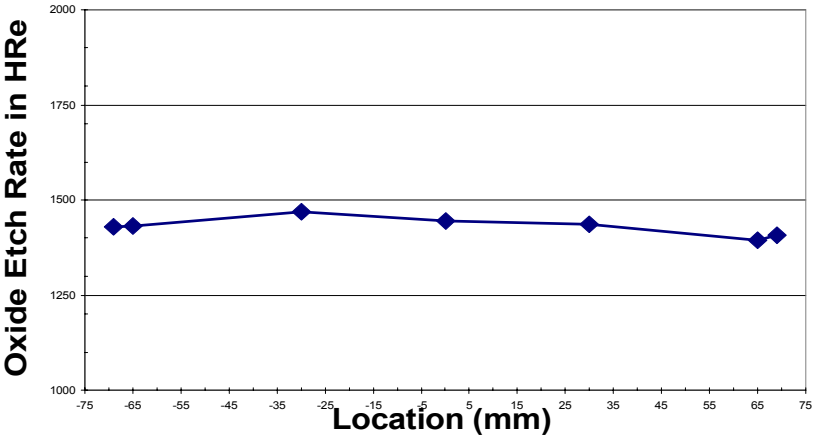
For these processes wafer temperature is a critical process parameter that must be monitored and controlled in order to achieve acceptable process control.



Non Uniformity Data

Non Uniformity
< 5%





Non Uniformity
< 5%

2- High Temperature Features

- FeRAM requirements
- Benefits of high temperature processing

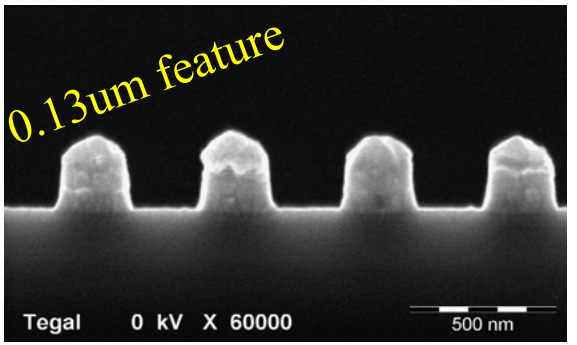
By-Product Volatility Enhancement

Element	Chloride Boiling Point (°C)	Fluoride Boiling Point (°C)
Si	58	- 86
Al	70	
Pb	**360**	**1290**
Zr	**331**	**58**
Ti	**136**	**284**

Benefits of High Temperature Processing (> 350ºC)

- High Temperature (> 350ºC) improves FeRAM etch performance for virtually all electrode, ferroelectric, and high-K materials (Ir, IrO_2, Pt, PZT, SBT, BST)
  - Higher Profile Angles
  - Reduced Sidewalls & Residues
  - Higher Etch Rates & Selectivities
- The combination of Dual Frequency HRe$^-$ with High Temperature ESC **allows 0.13 micron features to be etched with steep profiles.**

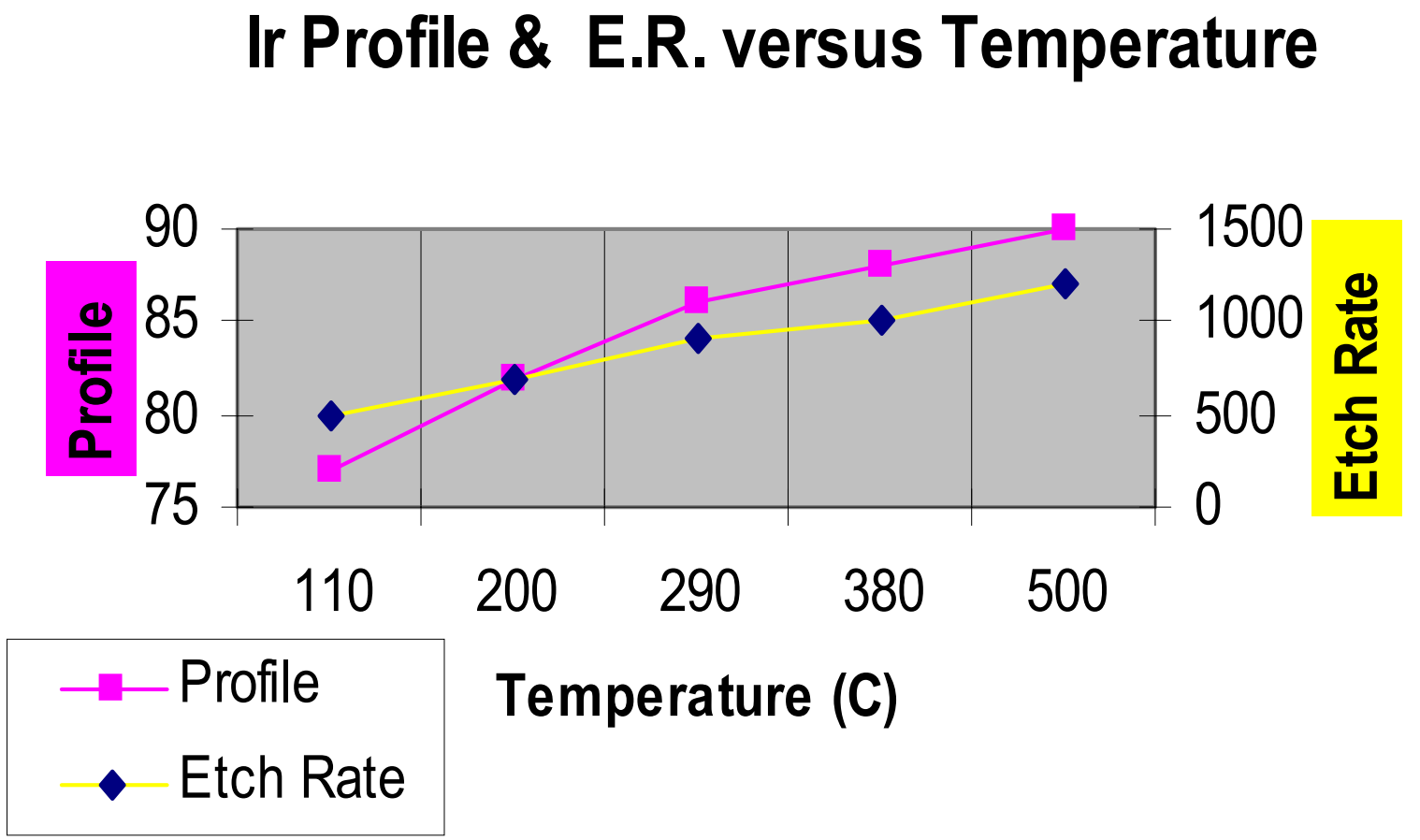
3- Etch Performance of the Reactor



The combination of Dual Frequency HRe- with High Temperature ESC results in enhanced etch capability to the 0.13 micron device node.

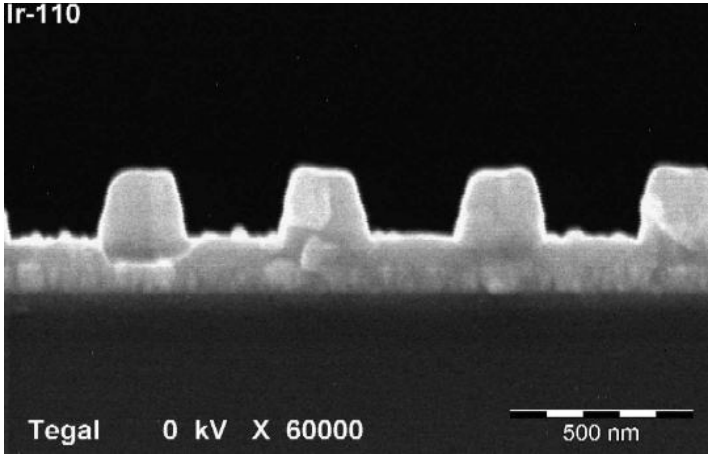
- Ir
- PZT
- Ir/PZT/Ir
- $Ir/IrO_2/PZT$

High Temperature Improves Etch Performance for Ir

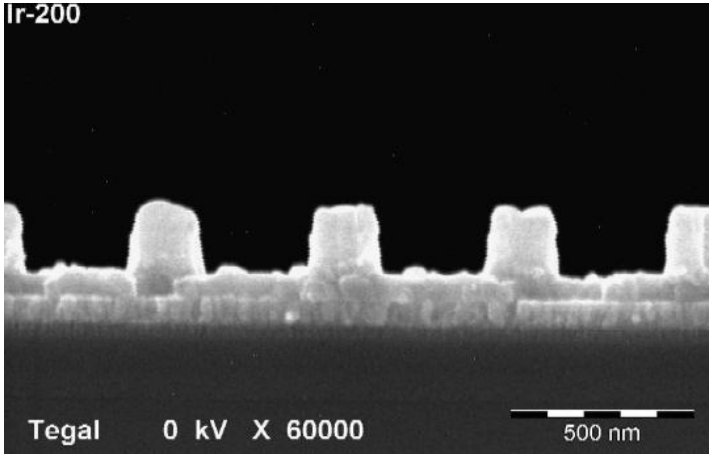


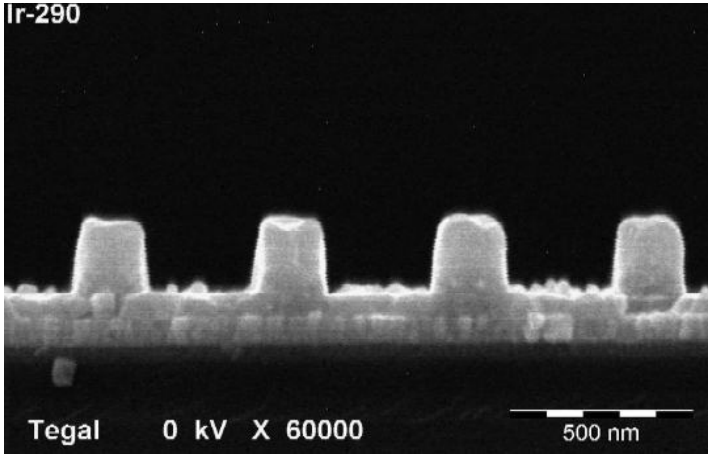
Temperature Dependence of Ir Profile

110 ˚C: 77deg, 500 Å/min.

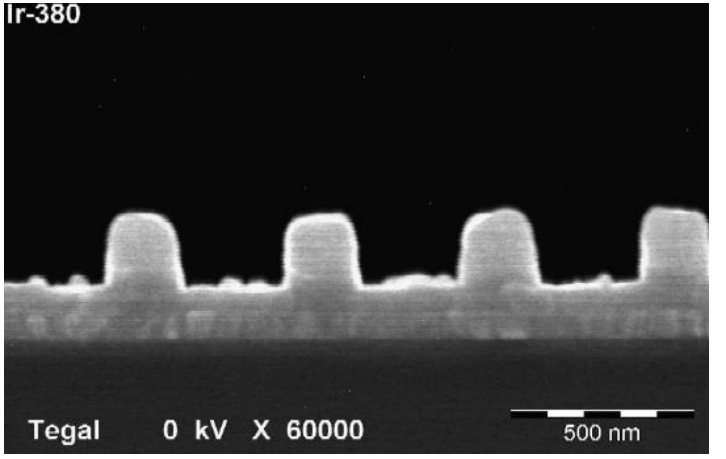


200 ˚C: 82deg, 700 Å/min.



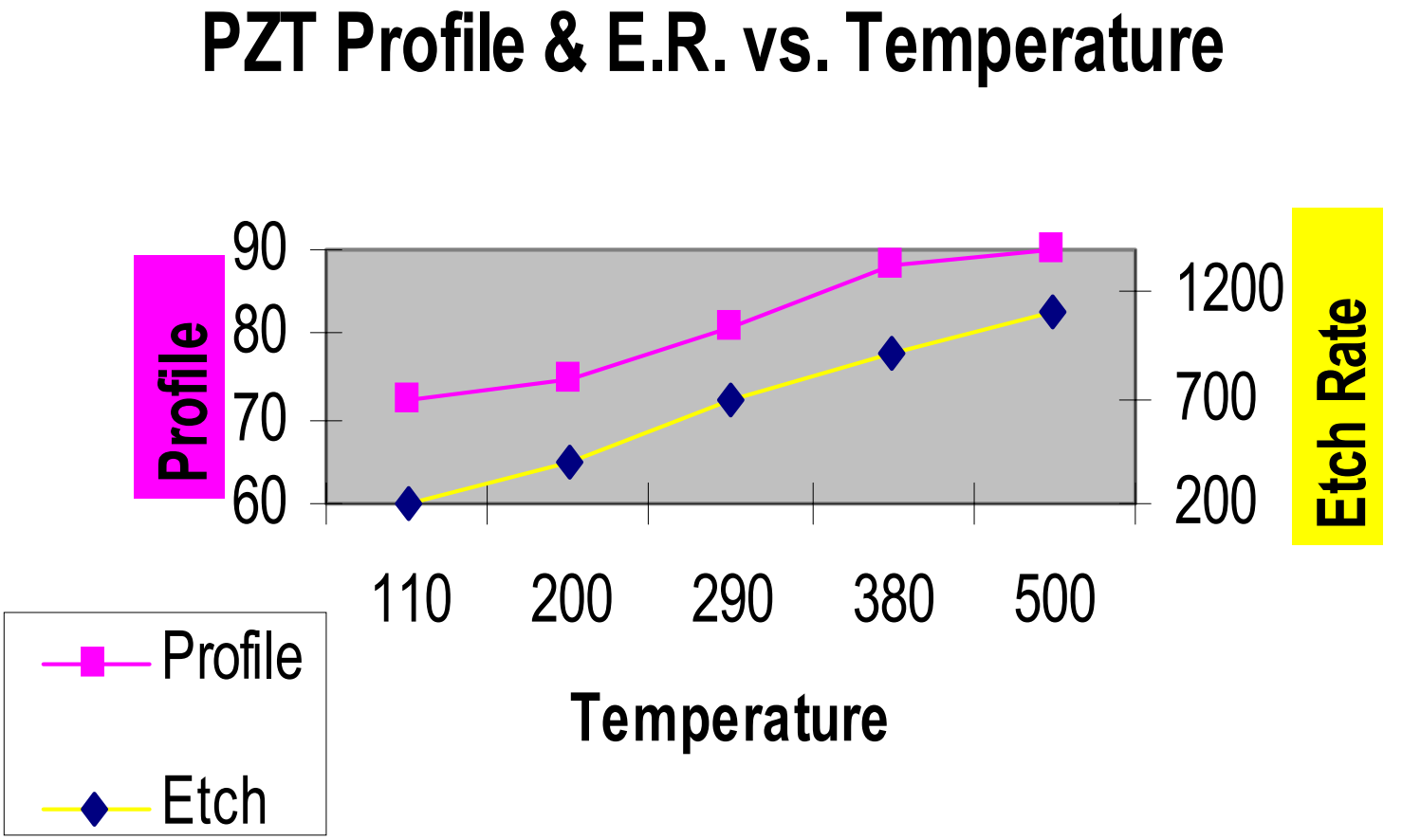


290 ˚C: 86deg, 900 Å/min.



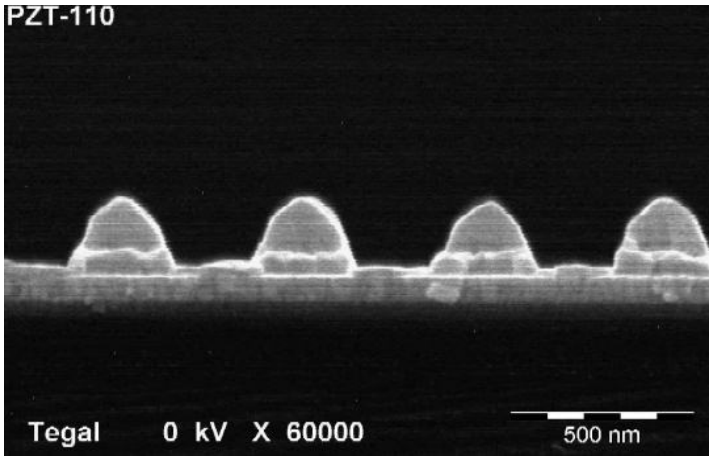
380 ˚C: 88deg, 1000 Å/min.

High Temperature Improves Etch Performance for PZT

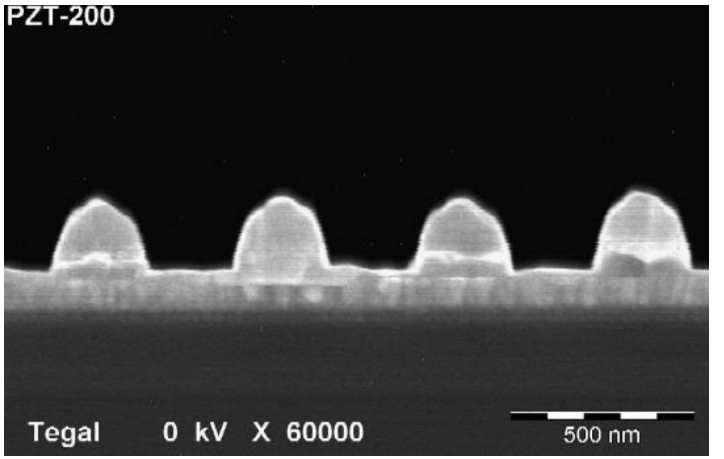


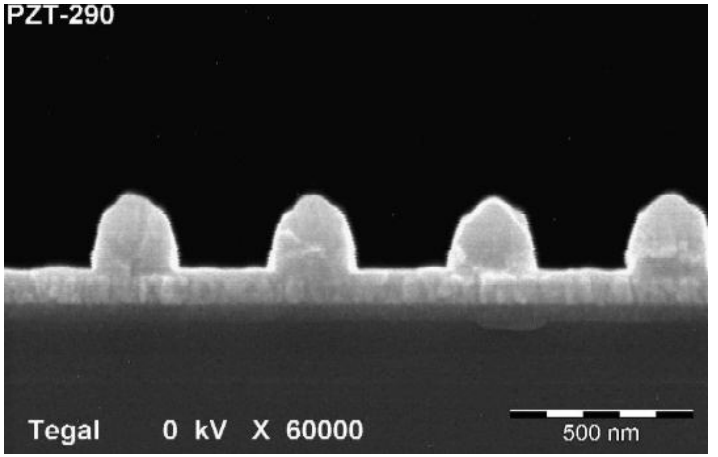
Temperature Dependence of PZT Profile

110˚C: 72deg, 200 Å/min.

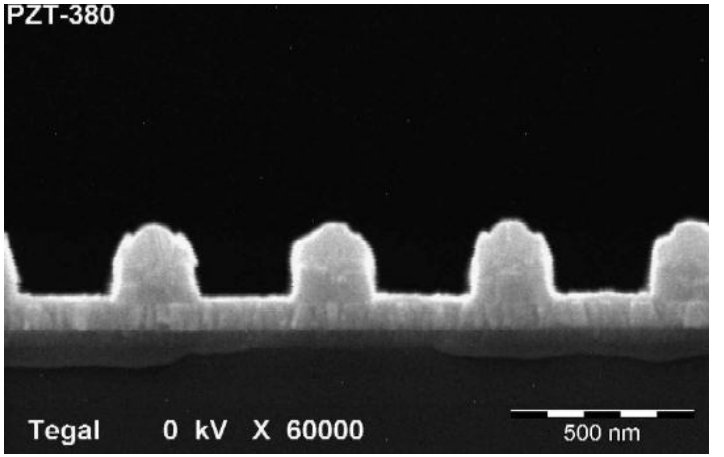


200˚C: 75deg, 400 Å/min.



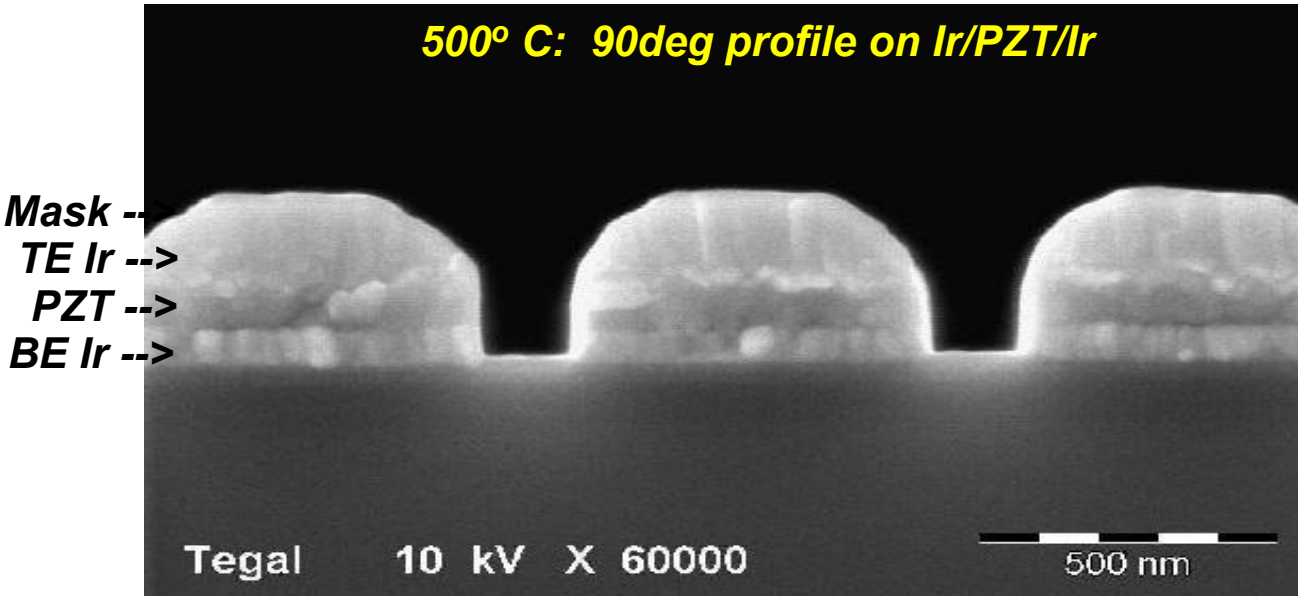


290˚C: 81deg, 700 Å/min.



380˚C: 88deg, 1100 Å/min.

High Temperature Improves Etch Performance for Ir/PZT/Ir Stack

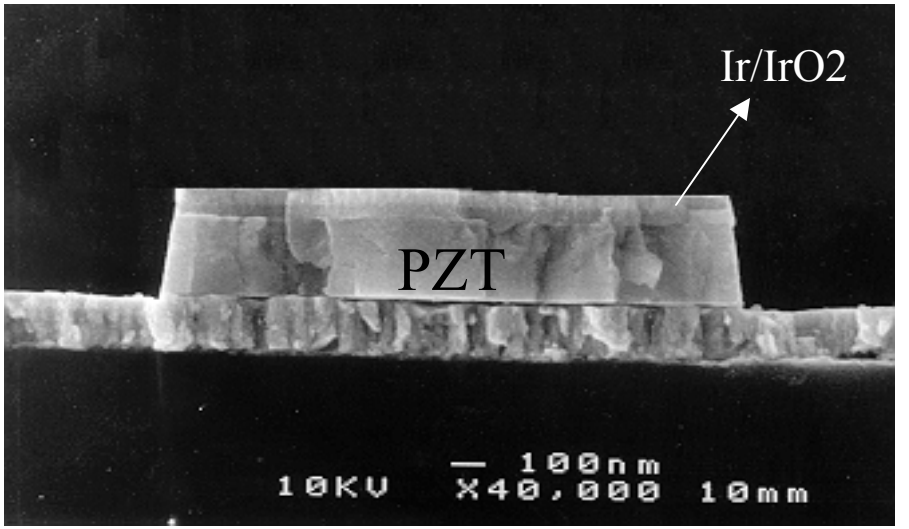


- 90 degree Stack Profile!
- 0.13 micron spaces

Full Capabilities of HRe$^-$ demonstrated with 500 °C

High Temperature Improves Etch Performance for Ir/IrO2/PZT Stack

Ir / $Ir0_2$ / PZT Stack After Hard Mask Removed



- Higher Profile Angles
- Reduced Sidewalls & Residues
- Higher Etch Rates & Selectivities

Conclusions

- HRe- is the configuration of choice for etching FeRAM structures
- Capacitive coupling is required to maintain process stability in an FeRAM plasma etcher.
- Symmetry is scrupulously maintained in the HRe- family
  - gas injection
  - pumping
  - magnets configuration
  - monopolar ESC

  these produce a very uniform etch environment
- Elevated wafer temperatures in the range of 350-500 °C are required to meet production FeRAM fabrication patterning requirements for capacitor stack spacing below 0.13µm.