Manufacturing Qualification of Plasma Wafer Cleaning Processes for FEOL and BEOL Applications

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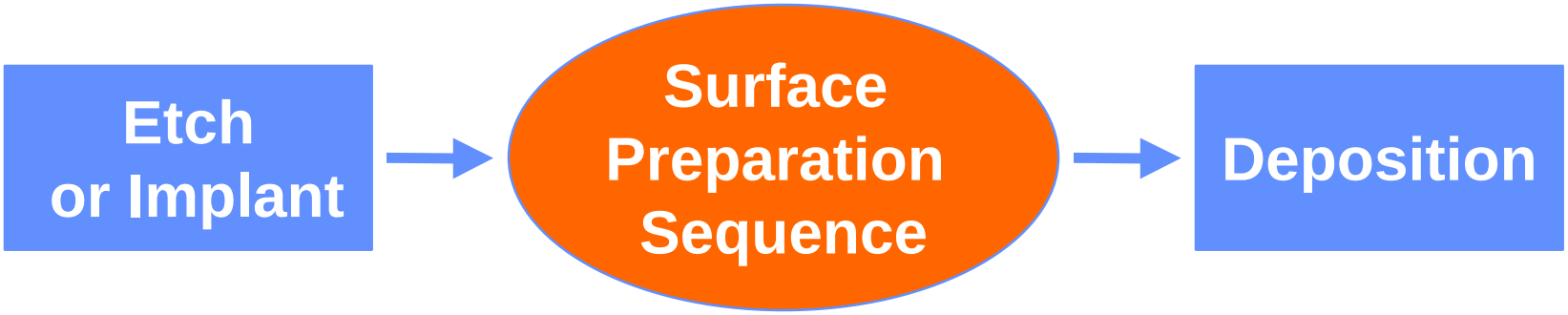


- **Surface preparation is needed between every etch (or implant) and deposition step**
- **Conventional surface preparation sequence uses plasma to ash resist and wet chemicals to clean residues**
- **The strip/clean sequence can be very extensive and costly**

Examples:

Ash → H_2SO_4/H_2O_2 → HF → H_2SO_4/H_2O_2 DI → Rinse

Ash → Hydroxylamine → IPA → DI Rinse → Re-ash

Motivation to develop plasma wafer cleaning processes:

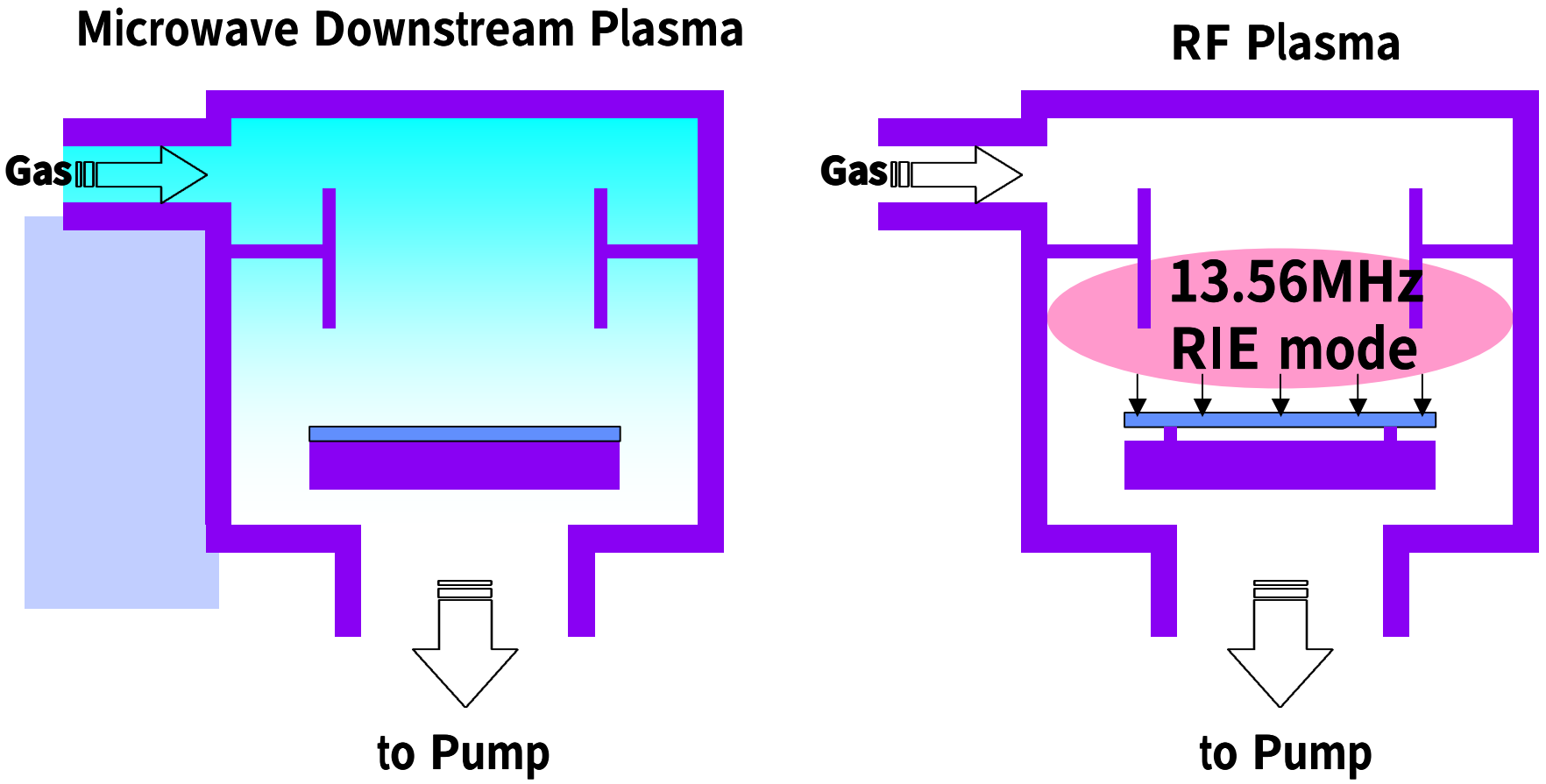
* Resist strip & residue clean in one plasma tool
* Eliminating or reducing wet clean steps
* Improving clean process robustness
* Reducing manufacturing cost
* Reducing cycle time

Two case studies will be discussed:

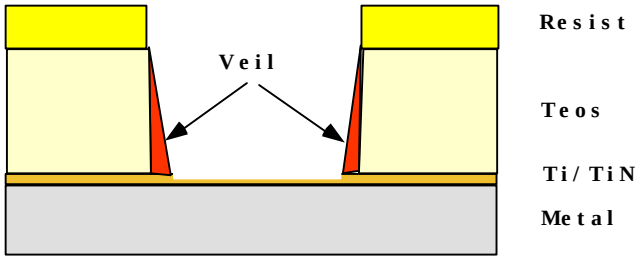
For BEOL, post via etch clean (in collaboration with Motorola, results published in Solid State Technology, April 2001)

For FEOL, post HDI ash clean (in collaboration with LSI Logic, results published in Micro, March 2003)

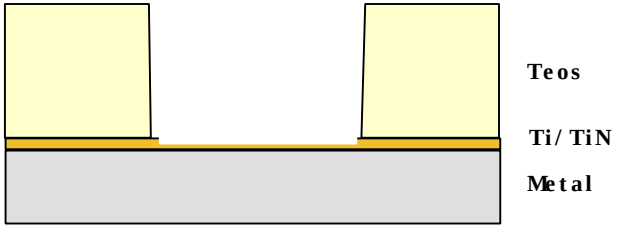
ENVIRO™ Reactor with Dual Plasma Sources



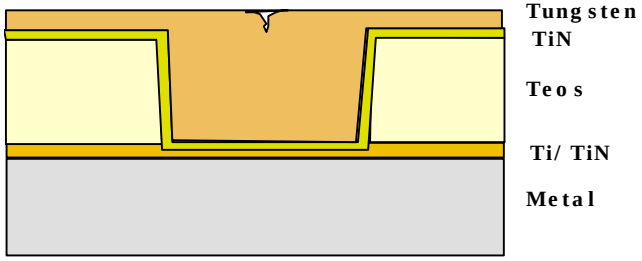
Via Process Integration



Post Via Etch



Post Ash/ Deveil

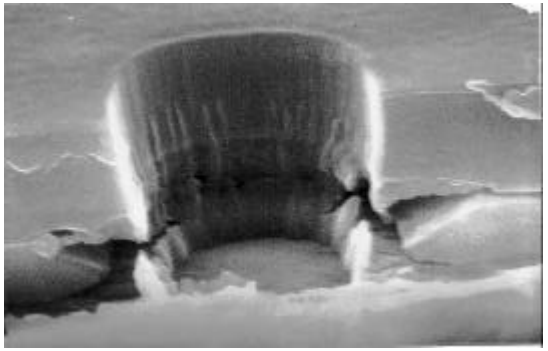


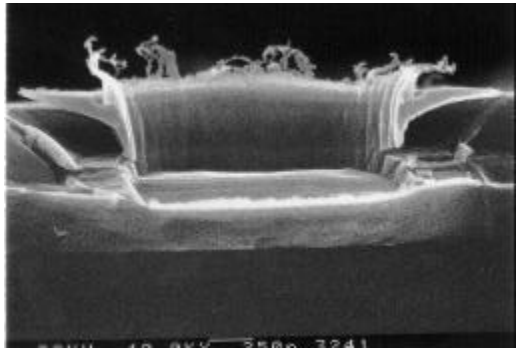
Via Metal Fill

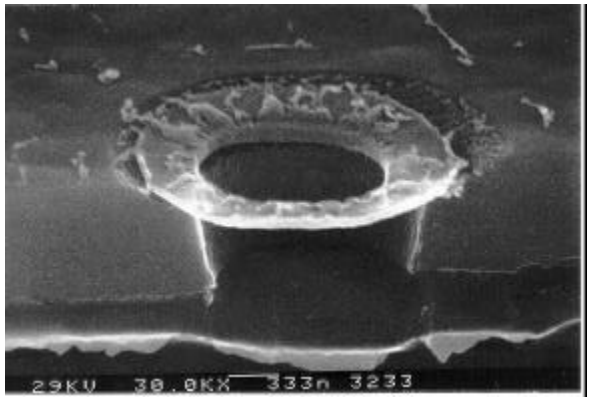
Problem Statement

Via veil, or metallized polymer, is an unwanted by-product of via etch. Traditionally, these veils are removed with organic or inorganic solvents. Inorganic solvents, while effectively dissolving veils under ideal conditions, are costly and inconsistent under non-ideal conditions. Solvents are also environmentally incompatible. For these reasons, a dry solution has been explored.

The Problem: Via Veils

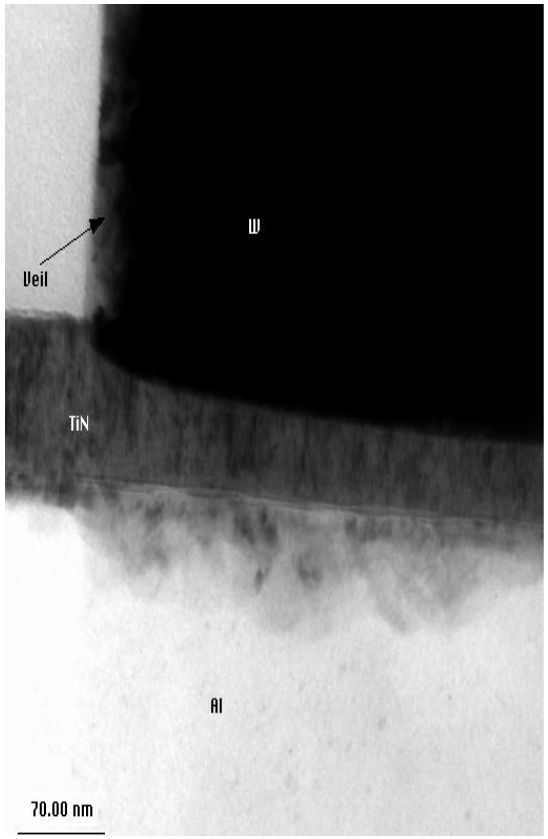






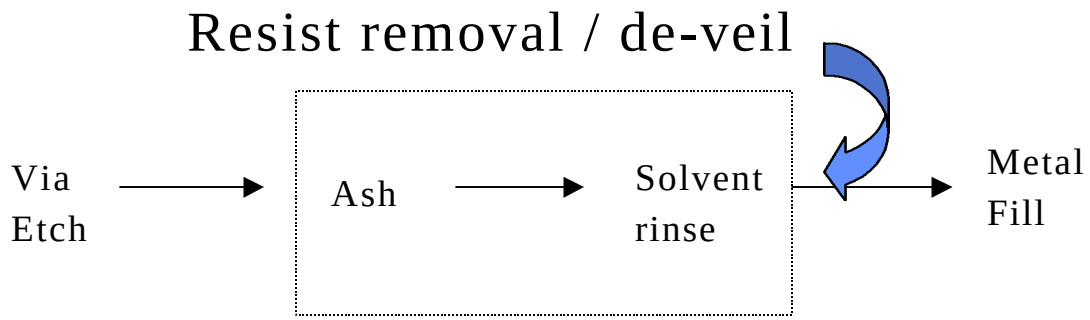
* veils produced using stop-on-Al via test structures

Via Veil: Stop-on-TiN Via



* ash only processing no de-veil.

Solvent De-veil Process



1. O_2/N_2 ash to remove resist. >240 ^{O}C process temp
2. Hydroxyl amine (HA) solvent de-veil done in hood or spray tool.

Spray Process: HA (80 ^{O}C) rinse followed by isopropyl alcohol and DI water rinse.

Solvent De-veil Process, cont'd

- HA chemical effectiveness dependent on temperature and water concentration.
- Spray tools are difficult to control and to monitor. Hoods require large floor space.
- Aggressive nature of HA tends to pit AlCu and degrade valves and seals.
- Chemicals, chemical facilities, and chemical management are costly and relatively unfriendly to the environment.

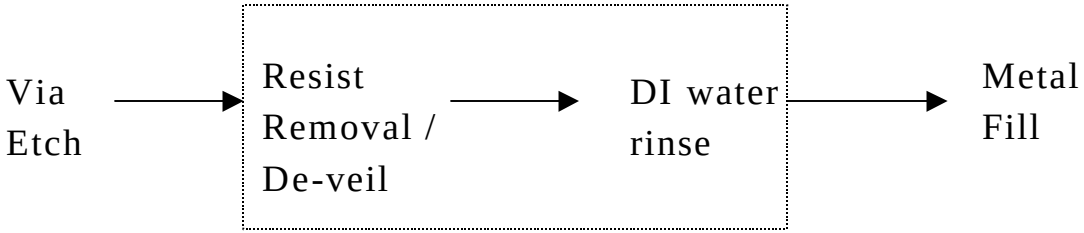
These difficulties lead to product variation, scrap, high cost and environmental burden.

Solvent Spray Tool and Handling Facility

* Solvent spray tool

* 5700 gal chemical reclaim tanks

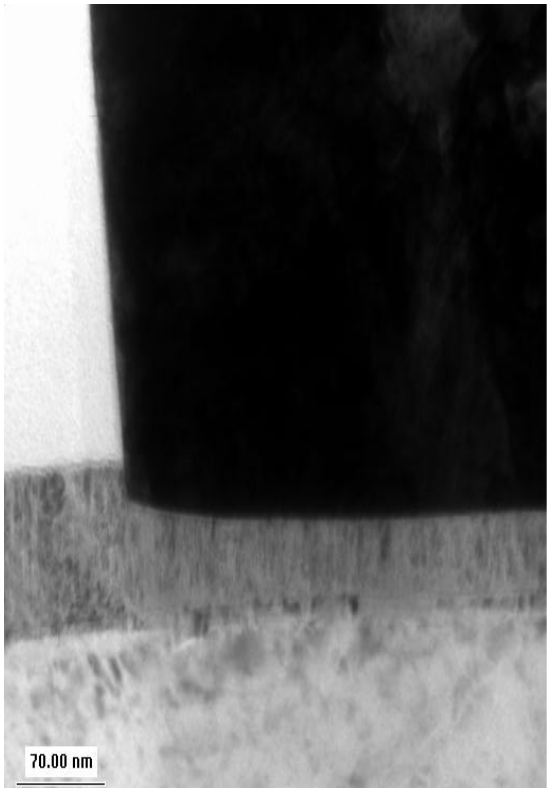
Dry De-Veil Process



- Dual process steps: bulk resist removal and veil treatment
- Chemistry: NF_3 or CF_4, O_2, N_2 or H_2N_2 (forming gas, 3%H_2)
- Dual power sources:
  - Downstream microwave: 0-2000W
  - RF for reactive ion etch: 0-650W
- Low temperature processing: 25-90 ^{O}C
- Optical Endpoint
- Room temperature DI water rinse

Dry De-Veil Results

- Product yield and resistance data is equivalent or better than solvent process
- Metal fill glue deposition is more uniform
- Solvent failure mechanisms have been eliminated.
- Product has been running with the new process since Q4'99.



Dry De-Veil Process Tools

Single chamber ENVIRO™ dry de-veil tools and DI water Spin/Rinse/Dry tool

Dual chamber ENVIRO™

Yield Comparison of Dry and Solvent Deveil

Process	Process Yield Difference	Std. Dev.	# of wfrs
Solvent		8.777	20
Dry Deveil	+1.7%	6.89	5
Solvent		6.44	19
Dry Deveil	+0.4%	5.35	6
Solvent		9.44	19
Dry Deveil	+9.77%	10.27	6
Solvent		4.9	8
Dry Deveil	+1.13%	5.23	17
Solvent		15.25	3
Dry Deveil	+21.94%	3.69	3
Solvent		4.14	13
Dry Deveil	+1.84%	2.66	12
Solvent		5.92	13
Dry Deveil	+1.12%	5.38	12

Cost Comparison for Via Deveil

Process Cost Items	Conventional Solvent Process	ENVIRO™ Dry Deveil Process
HA Solvent	$ 2,080,728	$ 0
Isopropyl Alcohol	$ 2,741,566	$ 0
DI Water	$ 4,498	$ 3,632
Process Gas	$ 8,786	$ 98,758
Process Power	$ 969	$ 765
Waste Disposal	$ 17,153	$ 0
Total Process Cost	$ 4,853,700	$ 103,155
Process Cost/Wafer Pass	$ 4.66	$ 0.10
Process Cost/Wafer	**$ 9.33**	**$ 0.20**
Required Equipment	5 SST, 4 Ash	5 ENVIRO™, 2 SRD
Annual Amortization (5 year)	$ 860,664	$ 802,800
Idling Power Cost	$ 10,000	$ 15,085
Annual Component Replacement	$ 400,000	$ 91,000
Tool Set Floor Space	243 Square Feet	117 Square Feet
Total Annual Overhead Cost	$ 1,270,664	$ 908,885
Annual Overhead Cost/Wafer Pass	$ 1.22	$ 0.87
Overhead Cost/Wafer	**$ 2.44**	**$ 1.74**
Total Annual Cost/Wafer	**$ 11.77**	**$ 1.94**

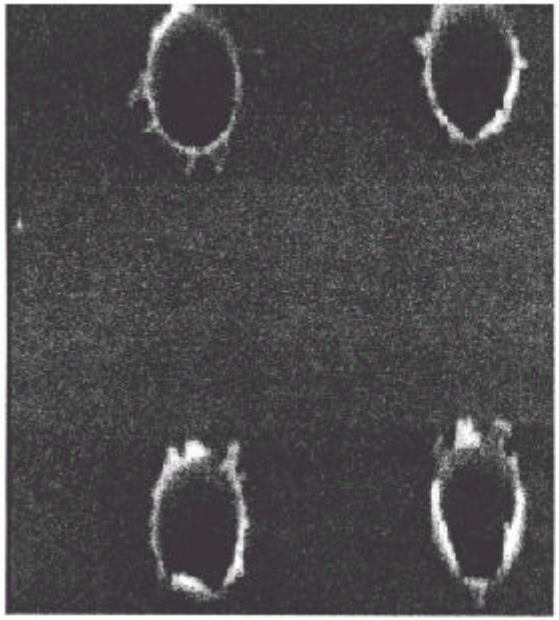
*** 10K wafer/week,2 via layers**

For tough veil of stop on Al via:

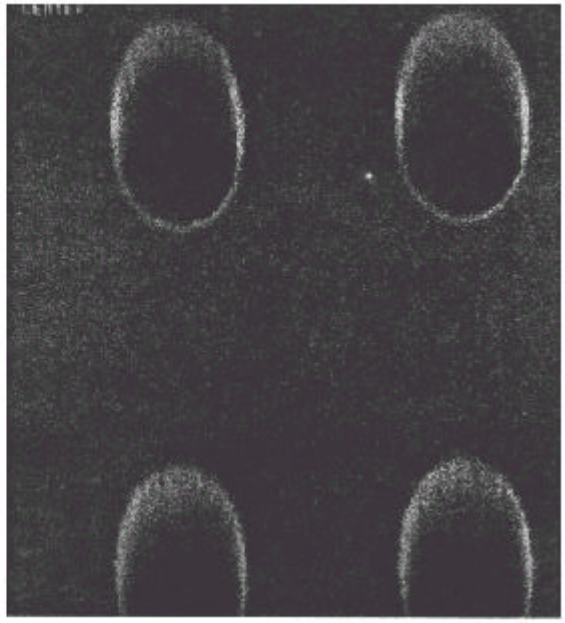
Dry ENVIRO™ process can

- Widen wet process window
- Reduce wet chemicals usage (>50%)
- Eliminate wafer scrap

After ENVIRO™ process, solvent deveil under non-ideal condition (10min ACT935 @ 30C) is still effective



O_2/N_2 Ash



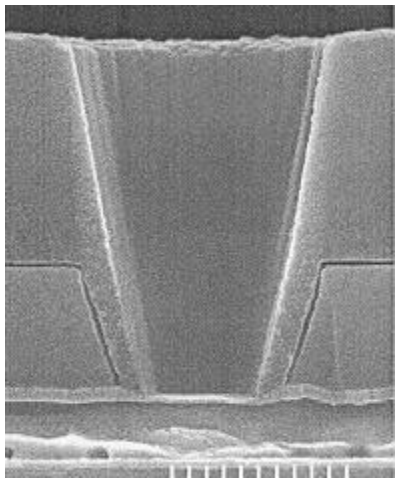
ENVIRO™

Standard solvent deveil condition: 20min @ 80C

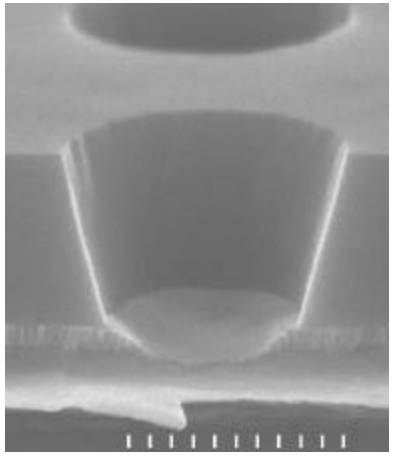
ULVAC
Ultimate in Vacuum since 1952

Dry Deveil Example

Before Enviro Process



After Enviro Process



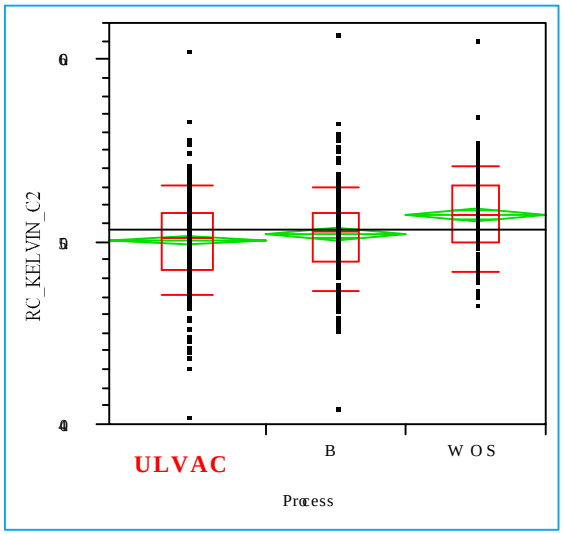


Figure 9. Kelvin contact performance of the Ulvac wafers, process A.

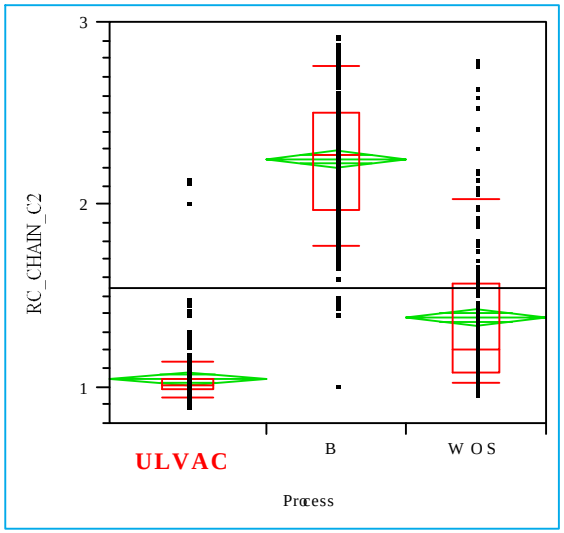
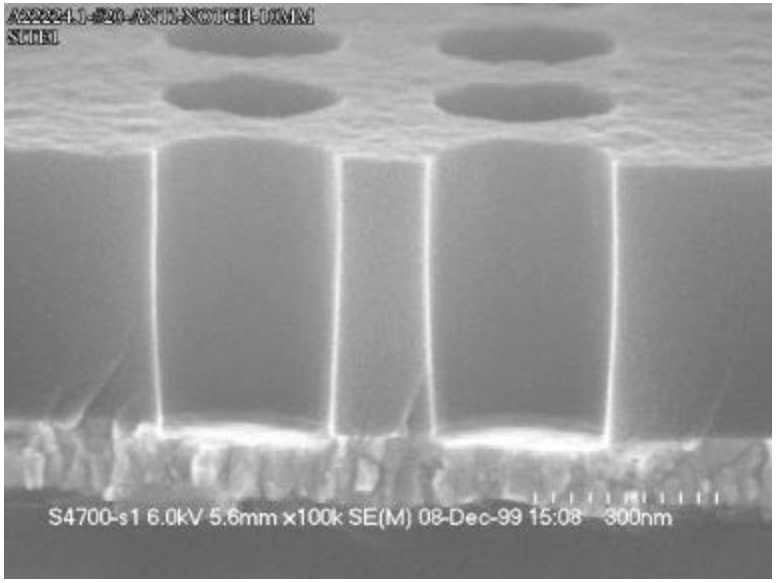


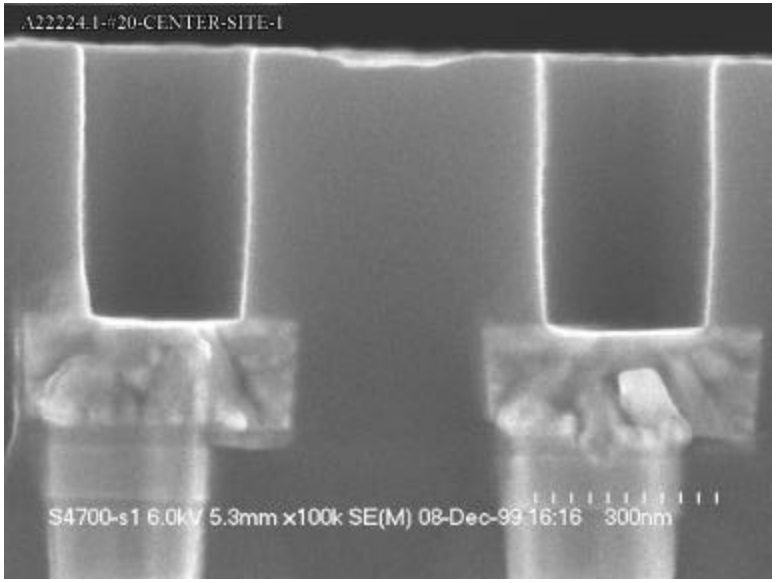
Figure 10. C2 chain contact resistance performance for the Ulvac wafers, process A.

Stop-on-TiN Via

Dry Deveil Example

After Enviro Process plus DI Water Rinse





Stop-on-W Via

Via Deveil Summary

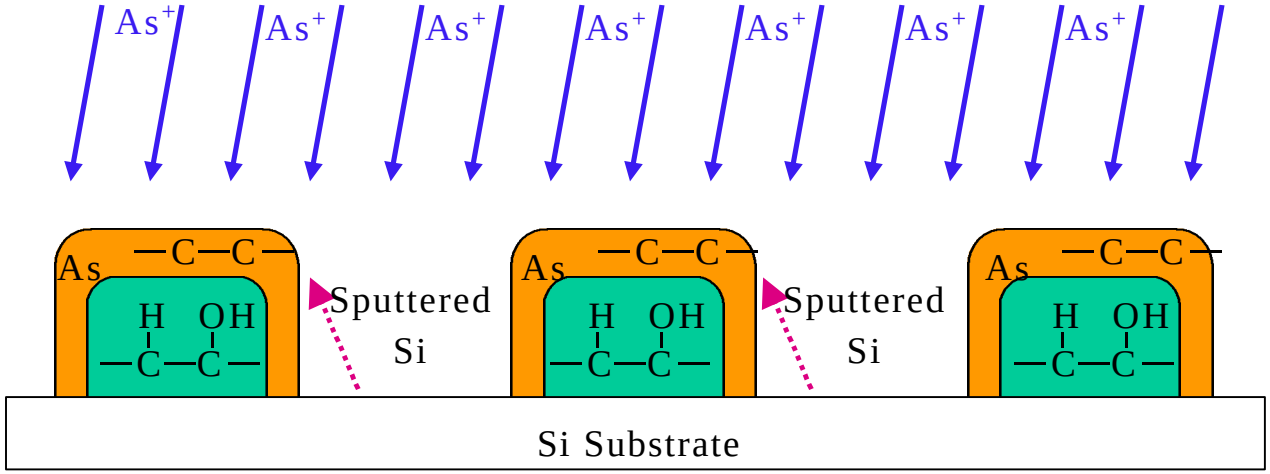
• A reliable, cost effective alternative to solvent de-veil processing has been developed.

- Same or improved yield and device performance
- Solvent failure mechanisms have been eliminated
- Process wafer cost is reduced to <15% of the solvent process

• Dry De-veil technology is better for safety and less overall burden to the environment

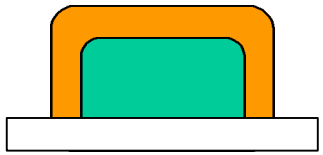
- Eliminates hazardous waste disposal
- Reduces overall DI water consumption
- Requires less safety equipment

Impact of Implant on Resist

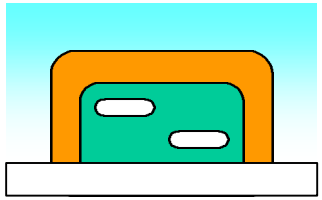


- **High dose implant drives out H and OH groups from resist resulting in a carbonized crust layer formed on resist**
- **Crust layer also contains inorganic species, such as, back sputtered Si and implanted As, P or B**

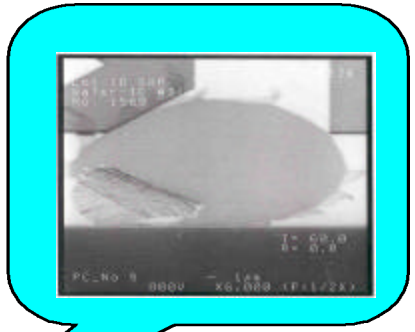
Issues of Conventional Ash Process for HDI

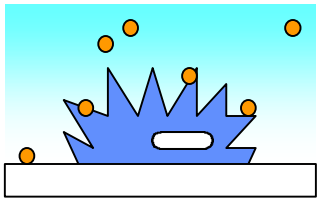


Wafer Heating by Hotplate or Lamp

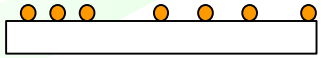


MW Plasma Ashing
Resist Blistering

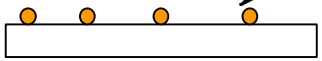




MW Plasma Ashing
Resist Popping

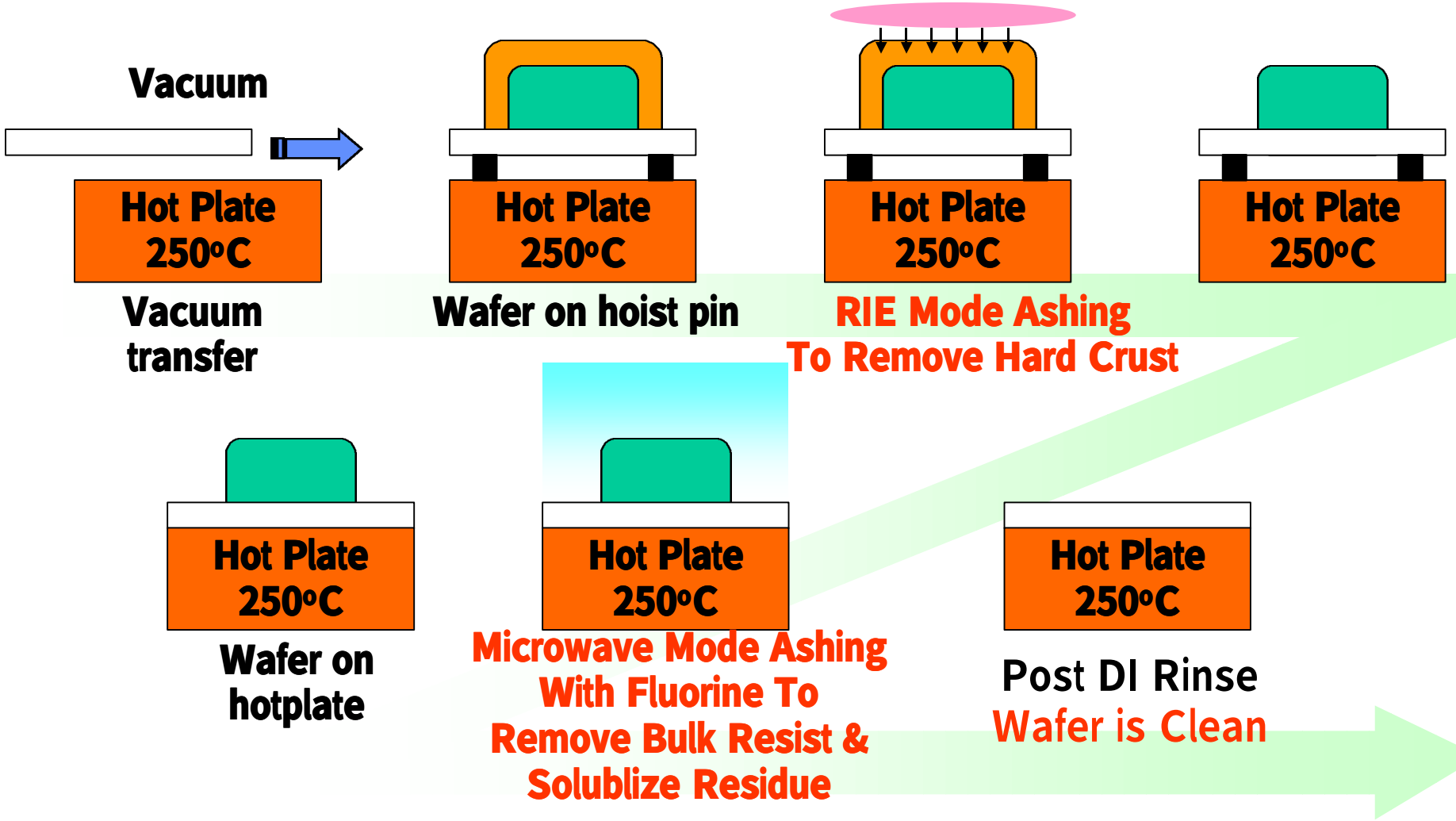


End of Ashing



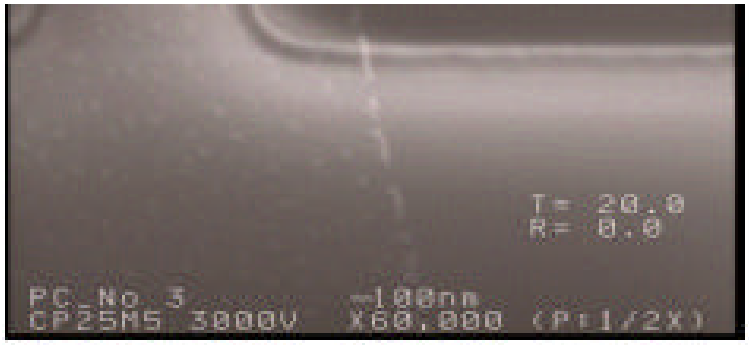
Post H_2SO_4/H_2O_2 Wet Clean
Resist Particles, Inorganic Residues Remain

Improved ENVIRO™ Process for HDI



Effect of Fluorine Addition to Ash Process

O_2 ash plus H_2SO_4:H_2O_2 wet clean



Ash with F addition plus DI rinse

- **Residue remains after O_2 ash plus H_2SO_4:H_2O_2 clean**
- **F addition removes all residues**
  - Si + F* → SiF_4 (gas)
  - As + F* → AsF_3 (water soluble)

SIMS Data of Surface Analysis

	Na	P	C
O2 ash +SRD	3.3E+10	1.6E+12	9.2E+13
O2 ash +H2SO4:H2O2	2.1E+10	1.4E+12	1.7E+13
F addition ash + SRD	1.3E+10	3.2E+11	4.0E+12

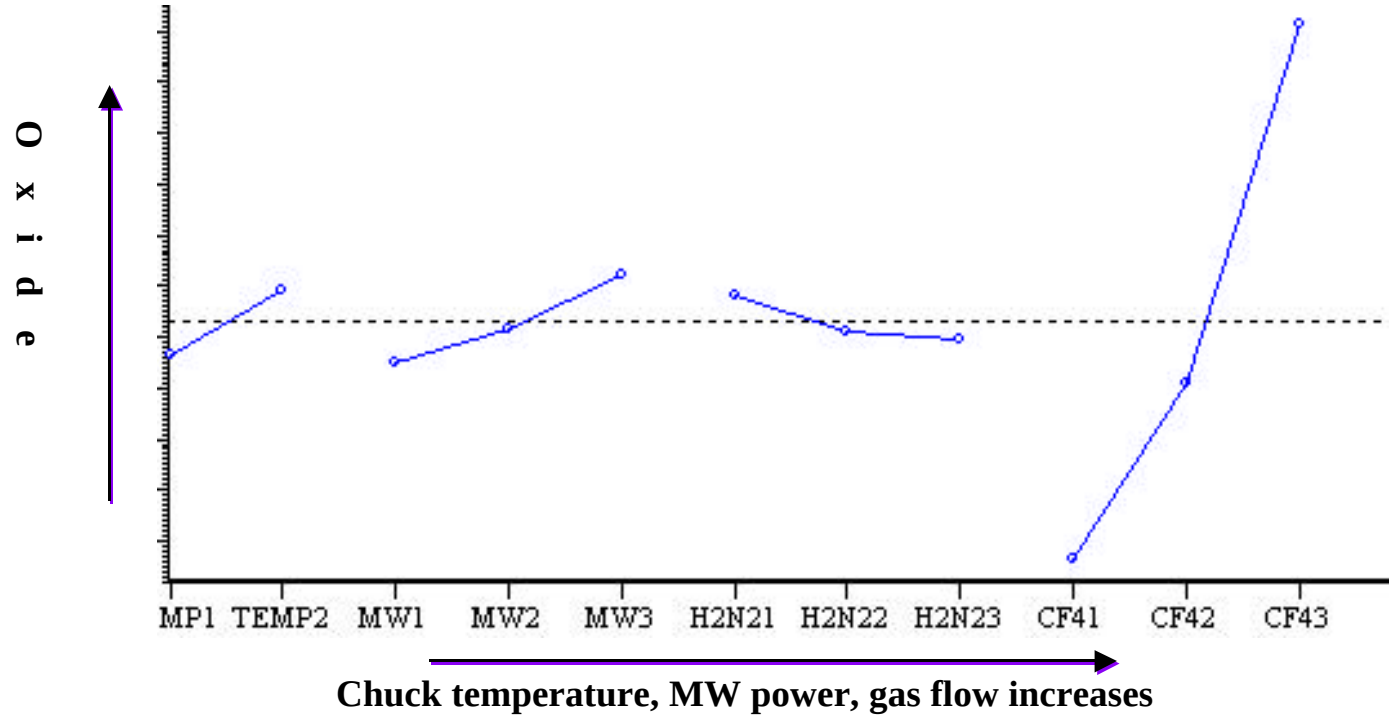
- Post ash H_2SO_4:H_2O_2 wet clean does not remove implant residue effectively
- F addition ash with a post DI rinse is an order of magnitude more effective

Surface Roughness Measured by AFM

Plasma treatments	Pre plasma treatment Height RMS Measured by AFM (A)	Post plasma treatment Height RMS Measured by AFM (A)	Post-Pre
O_2/ N_2:H_2 MW down stream	2.02	1.83	-0.19
O_2 RIE	2.13	1.76	-0.37
CF_4/ O_2/ N_2:H_2 MW plasma	2.14	1.83	-0.31

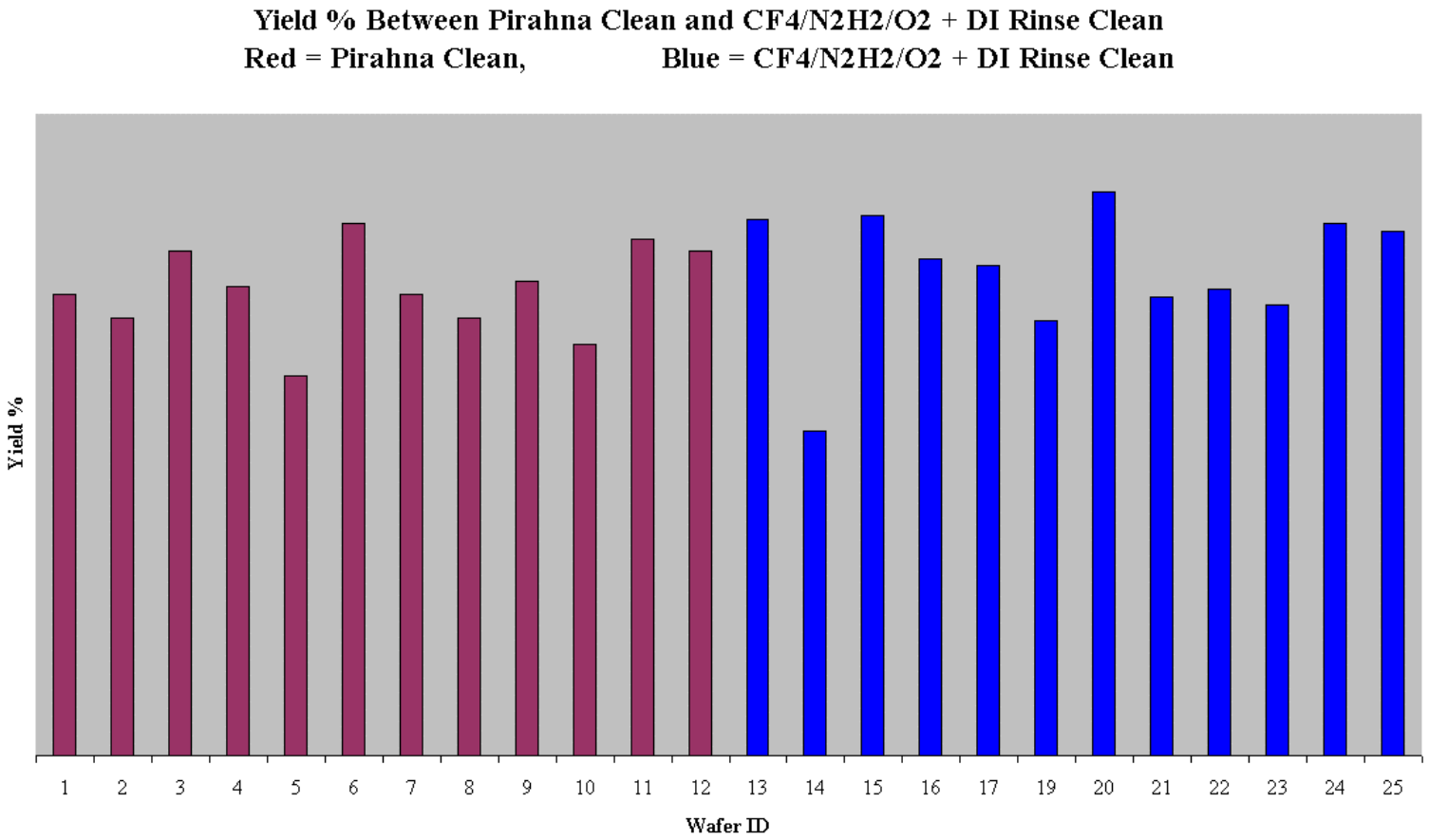
- F addition does not increase Si surface roughness

Impact of Process Parameters on Oxide Loss



- Main factor for increasing oxide loss is F concentration

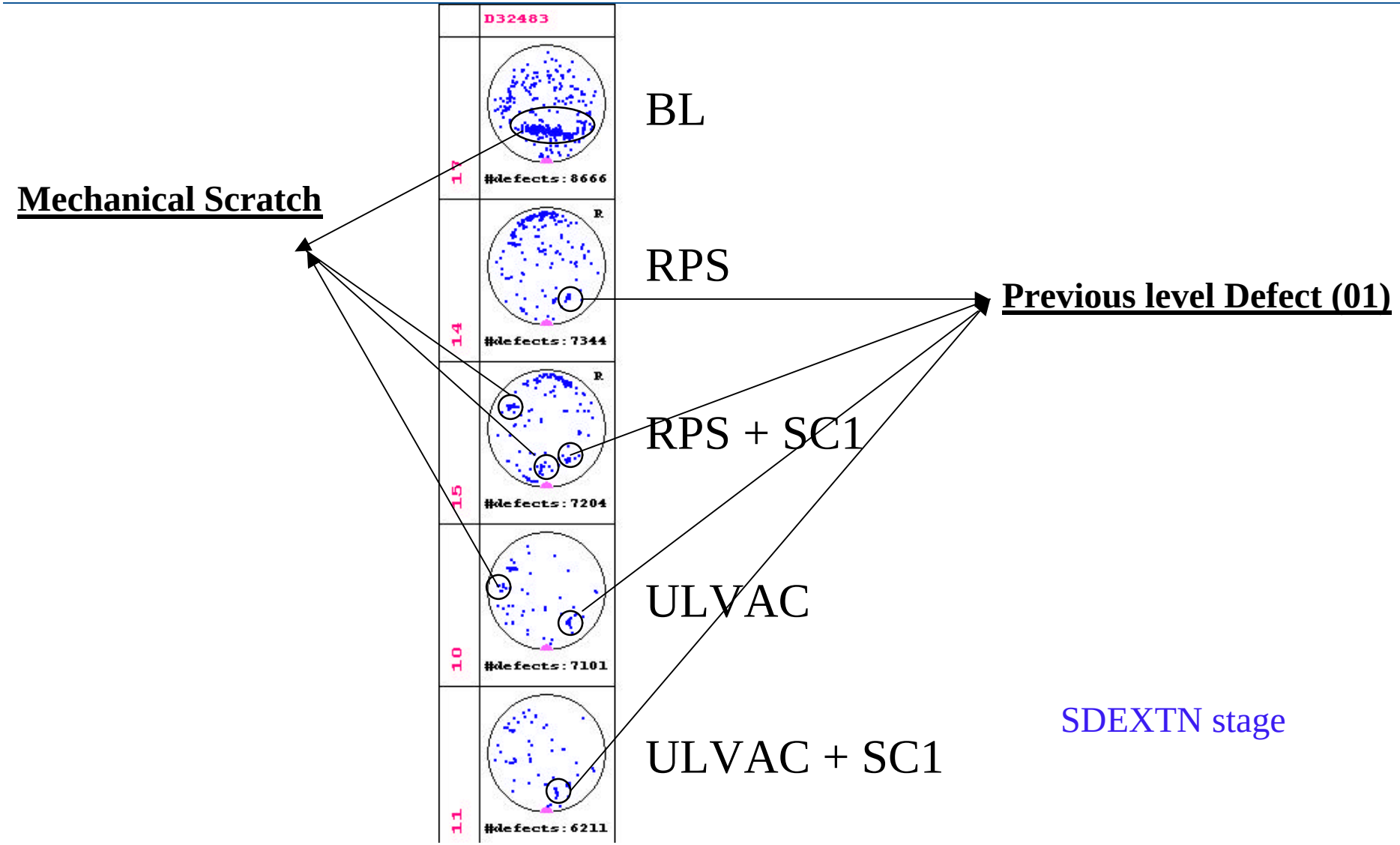
Yield Comparison between Wet & Dry Clean

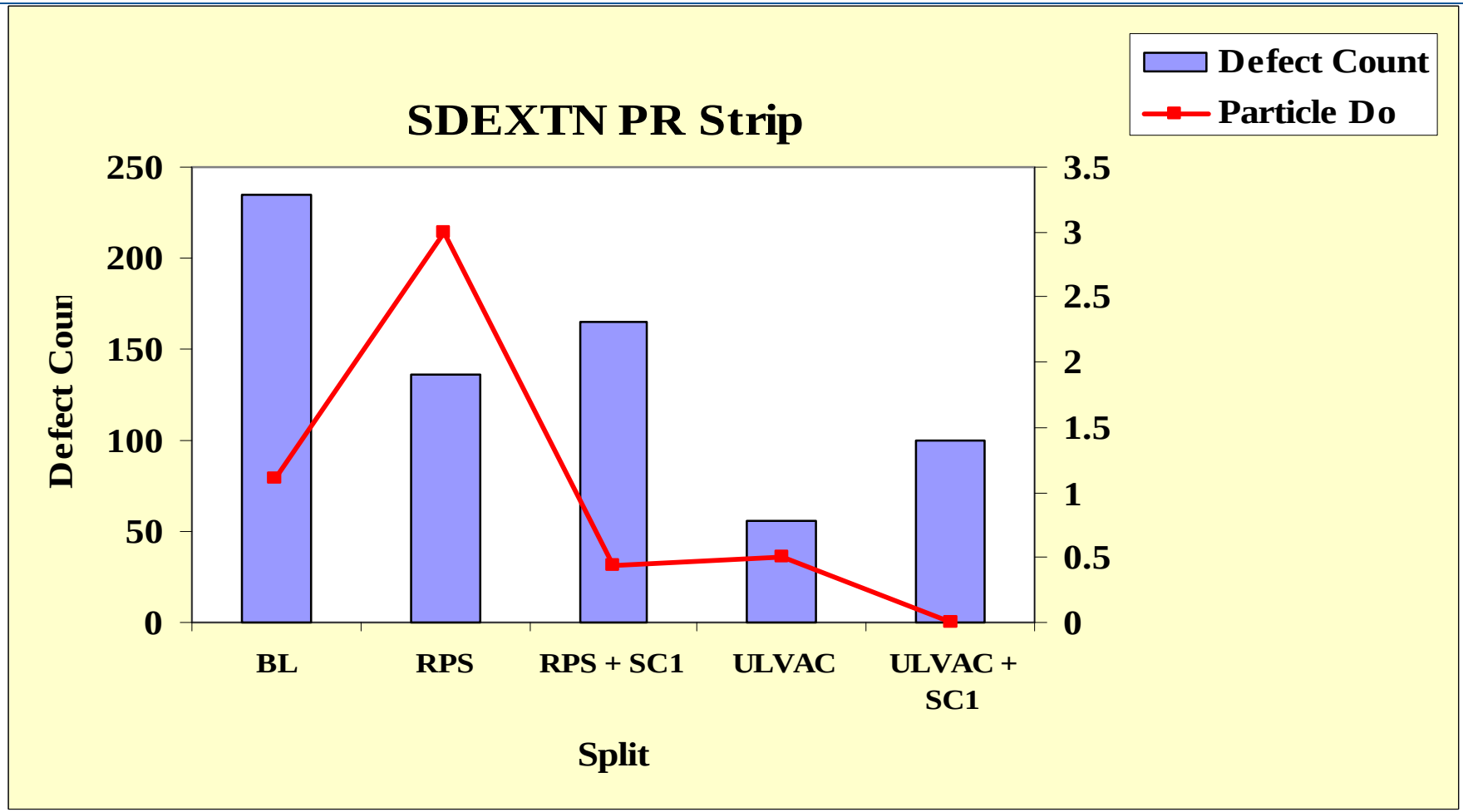


Defect Reduction from ENVIRO™ HDI Process

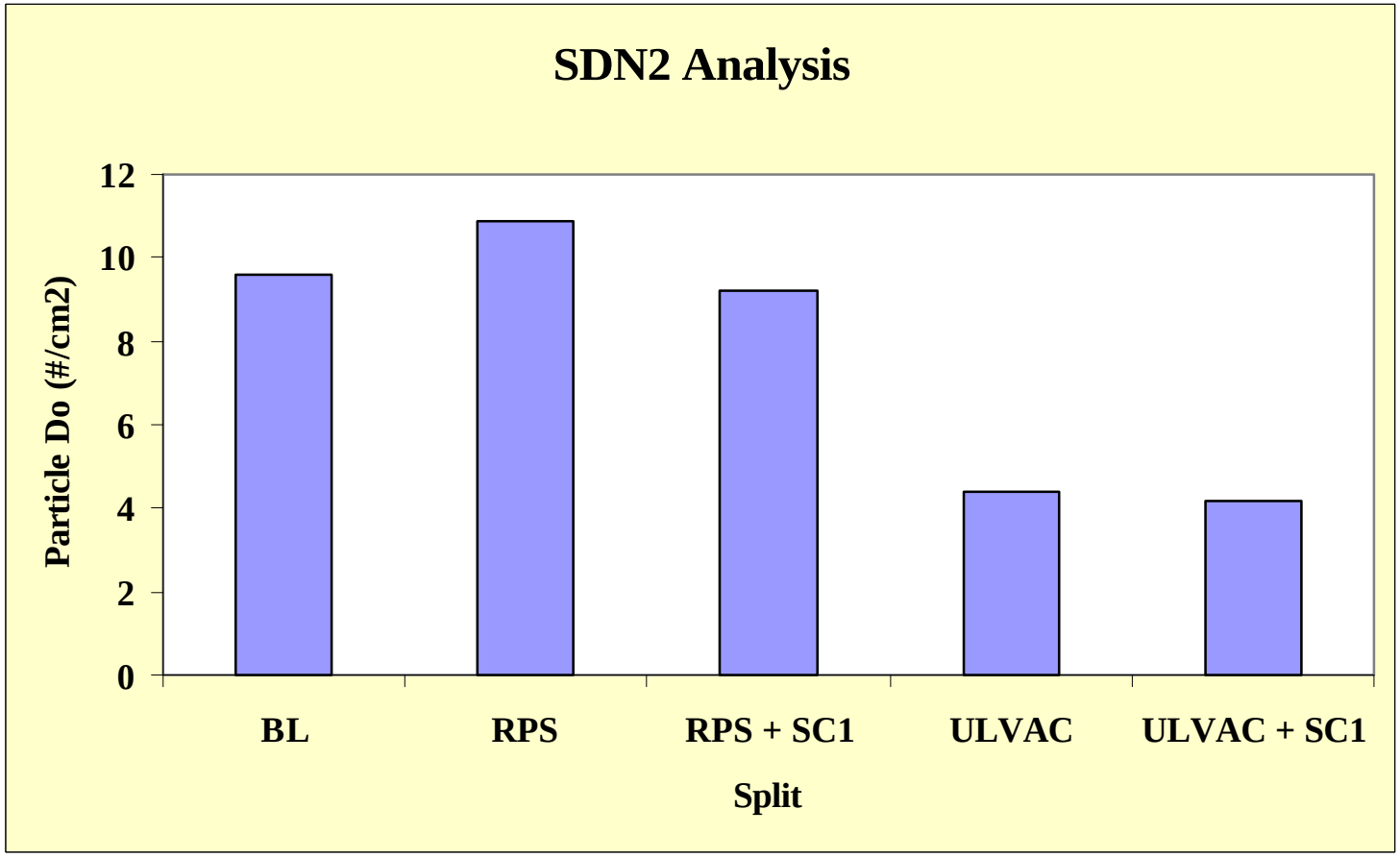
- 5-way split at 4 implant stages (SDEXTN, SDEXT2N, SDEXTP, SDN)
  - BL, RPS, ULVAC, RPS+SC1, ULVAC+SC1
- 2 wafers scanned on KLA2138 per split at multiple process steps

Typical Post PR Strip Defect Maps

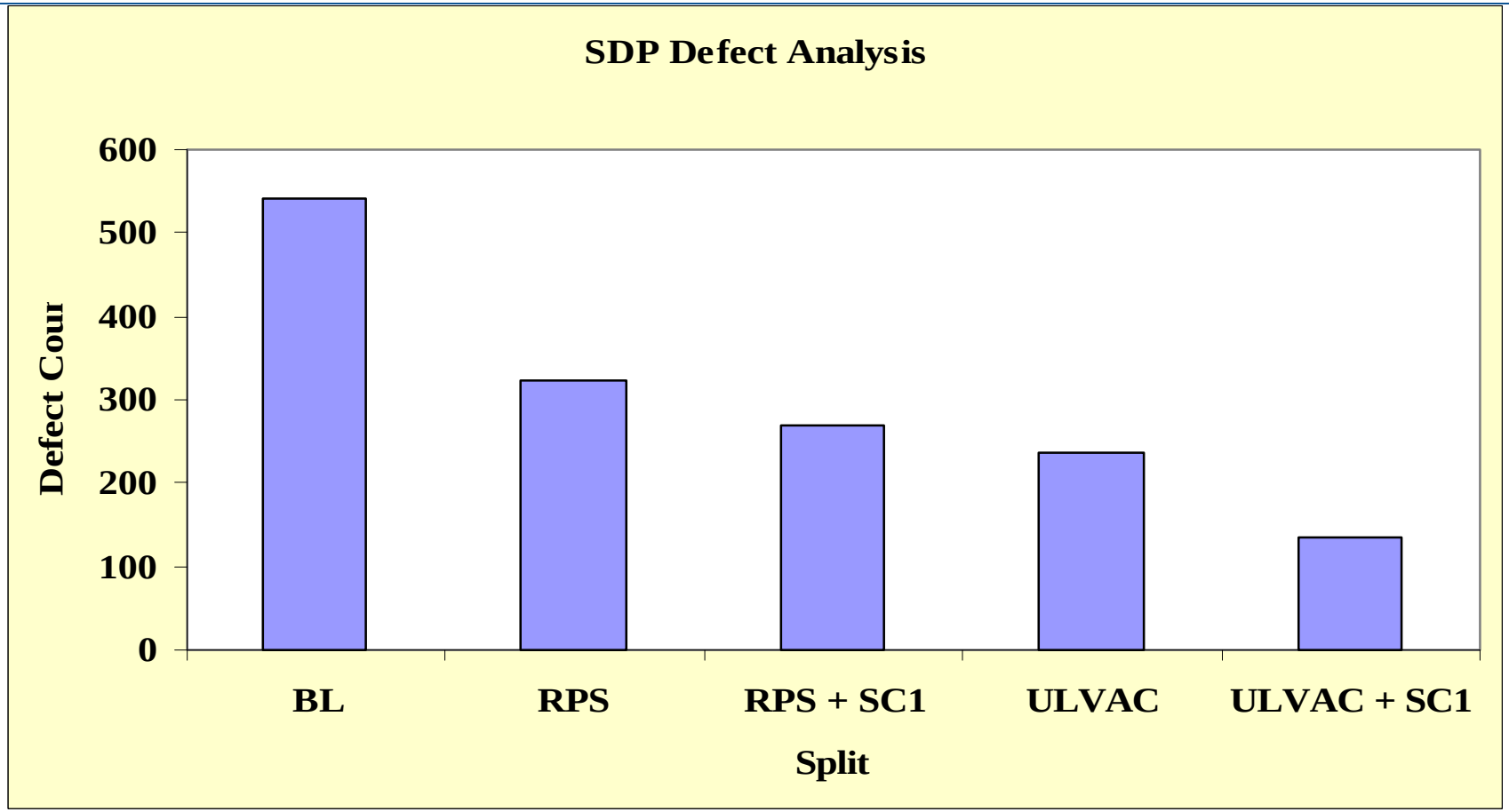




5X reduction with ULVAC



- 50% reduction with ULVAC
- Further 5% reduction with addition of SC1



- 50% reduction with ULVAC
- 75% reduction with ULVAC + SC1

Post HDI Clean Summary

- Dual plasma (O2 RIE and MW) can strip heavily implanted resist quickly without “popping”. Typical process time: 60sec.
  - Low per wafer cost for resist strip.
- Sulfuric acid/hydrogen peroxide clean can be eliminated from post ash wet clean sequence.
  - Cost savings from wet clean.
  - Cycle time reduction
- This approach can reduce defectivity.
  - Higher yield.

Resist Strip Challenge: Process without Damaging Porous Low-k Dielectric Materials

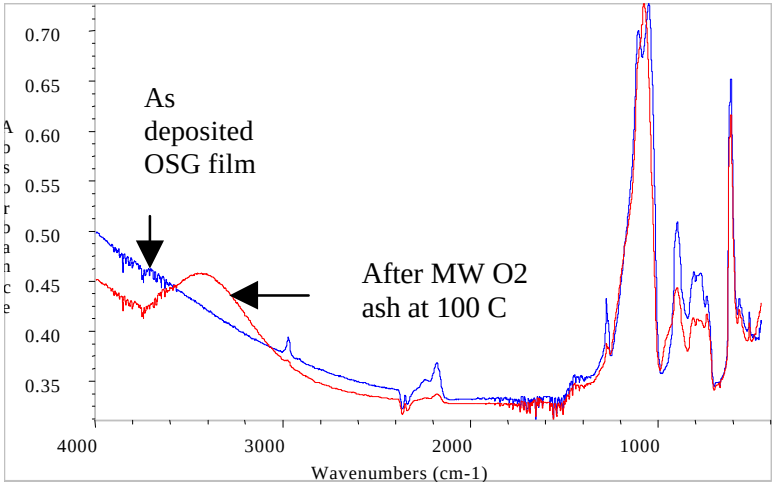
(Data Acquired in Collaboration with International Sematech)

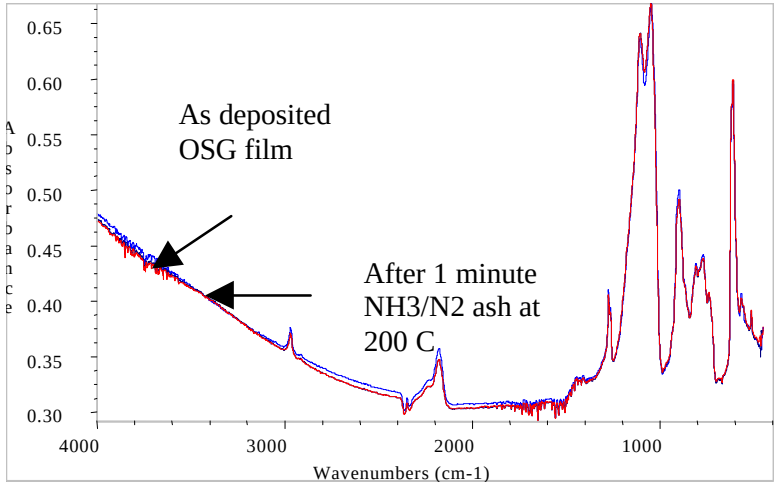
ITRS Interconnect roadmap (2002 update)

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Number of metal levels	8	8	8	9	10	10	10
Number of optional levels—ground planes/capacitors	2	2	4	4	4	4	4
Conductor effective ressitivit (μΩ-cm) Cu intermediate wiring	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (for Cu intermediate wiring) (nm)	16	14	12	10	9	8	7
Interlevel metal insulator (minimum expected)—effective dielectric constant (κ)	3.0-3.6	3.0–3.6	3.0–3.6	2.6–3.1	2.6–3.1	2.6–3.1	2.3–2.7
Interlevel metal insulator (minimum expected)—bulk dielectric constant (κ)	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4	<2.1

- Low k dielectric films are being used for the current generation devices, and porous low k will be used at 65nm node
- Resist strip without damaging porous low k is one of the integration challenges being pursued right now

Resist Strip Process vs. Low-k Damage





- Conventional O_2 based ashing causes C depletion and Si-OH formation (damage to low k film)
- One of the approaches to avoid damage to low k film is to switch to H_2 based chemistry, such as H_2/N_2, NH_3 or other H_2 containing gas or gas mixtures
- However, this approach does not automatically work for the porous low k film

* J. Hu, W. Uesato, P. Schoenborn, P. Clark, M. Boumerzoug, H. Xu, AVS First International Conference on Microelectronics and Interfaces (2000).

In this study, N_2/H_2 chemistry was used to compare different Enviro^{TM} process chambers for porous low k strip

Standard process chamber

- Dual plasma source, MW and RIE
- 6 process gases
- Endpoint detection
- Process pressure: 100 to 2000mT
- Wafer temperature: 100 to 260C

Low k process chamber with parallel plate RIE

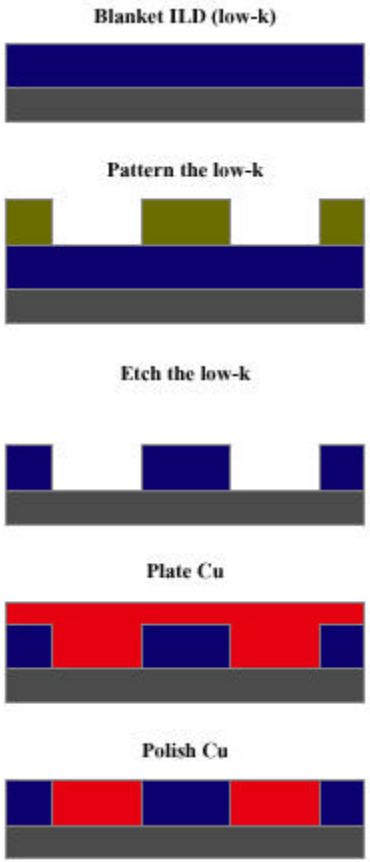
- Turbo molecular pump for process pressure control to 5mT
- Electrostatic chuck for wafer temperature control to 10^{o}C

Low k process chamber with WCP plasma source

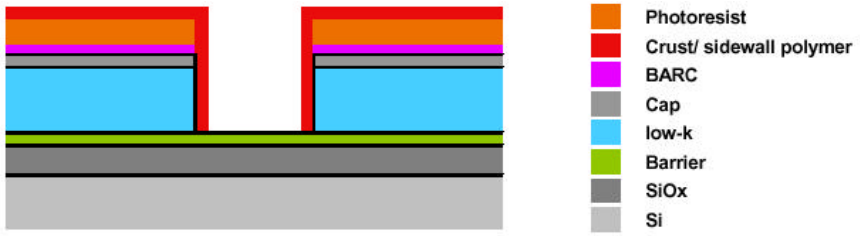
- Turbo molecular pump for process pressure control to 5mT
- Electrostatic chuck for wafer temperature control to 10^{o}C

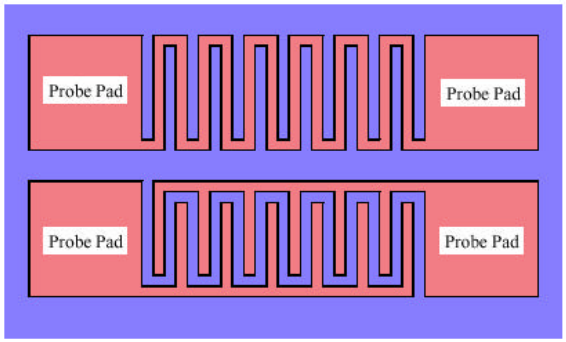
Single Damascene Electrical Test Structures

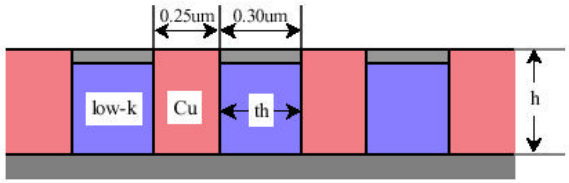
Process flow



Filmstack



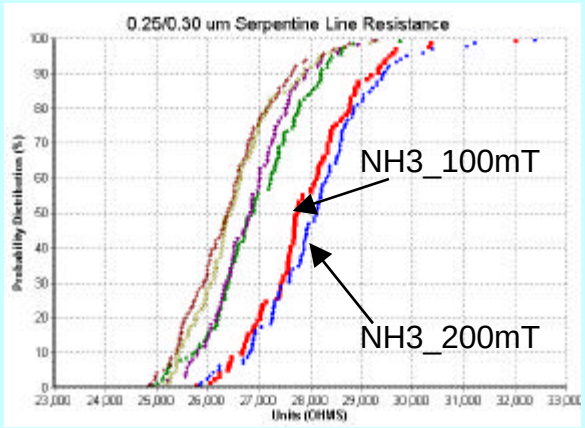


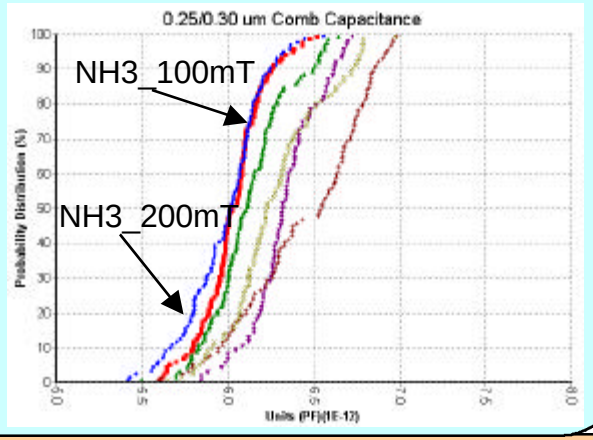


- Serpentines to measure line resistance and CD variation
- Combs to measure line to line capacitance and leakage resistance
- RC products to measure intrinsic low-k damage

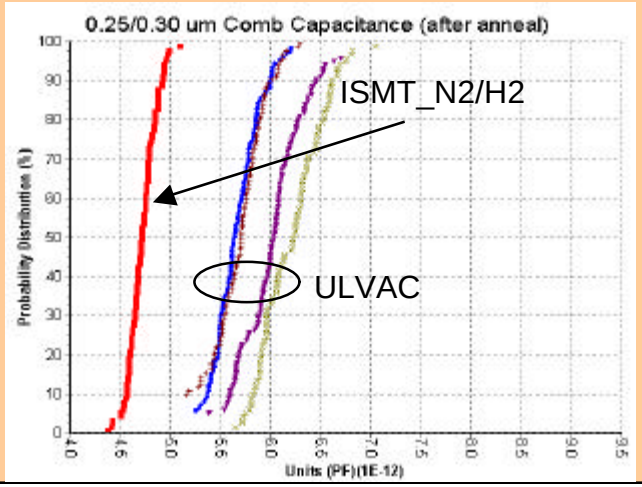
Porous MSQ More Prone to Damage By Resist Ash Process

CVD OSG





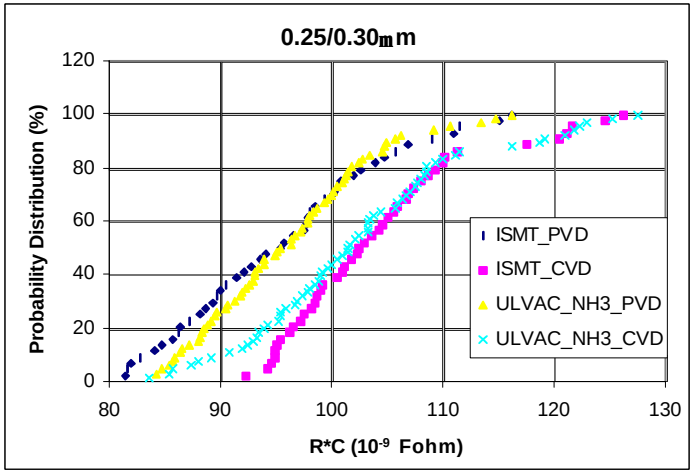
Porous MSQ

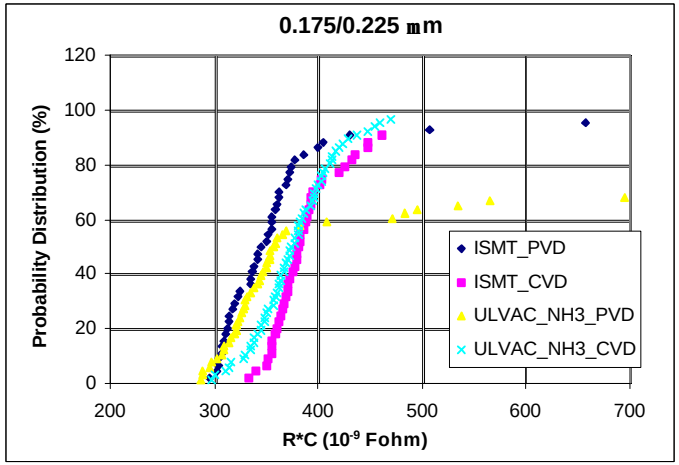


Condition	Post CMP and Anneal E-test Data			
	Rserp (kohm)	Comb cap (pF)	log Bridging I	RC (10^{-9} Fohm)
ISMT N2/H2	25.6	4.71	-13.2	120
ULVAC_NH3_A	22.5	5.64	-12.2	127
ULVAC_NH3_B	21.9	5.77	-12.3	126
ULVAC_NH3_C	21.2	6.03	-12.2	128
ULVAC_NH3_D	22.1	5.70	-12.3	126
ULVAC_NH3_E	20.4	6.22	-12.1	127

- 100mT NH_3 process in standard chamber is a good process for CVD OSG, but not for porous MSQ

Directional Ash & Better Wafer Temperature Control Needed for Porous MSQ



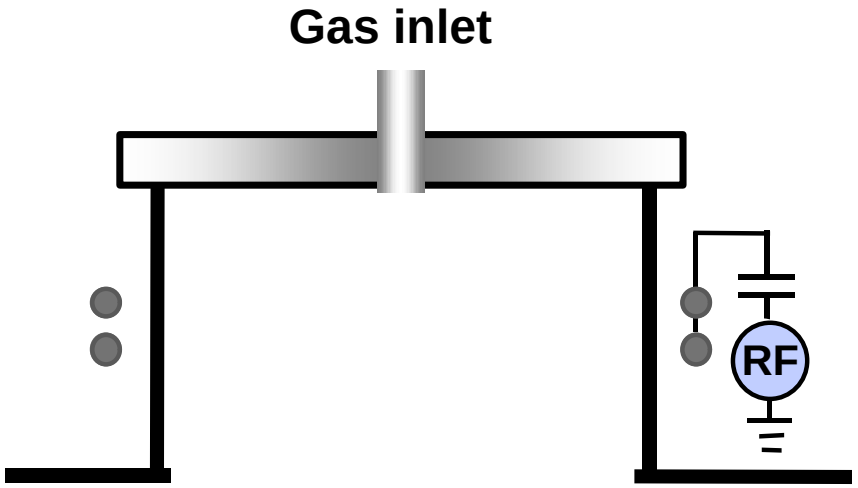


Condition		Post CMP + 400°C anneal e-test data				
Ash	Barrier	Rserp (kohm)	Comb Cap (pF)	log Briging l	R*C (*10^{-9} Fohm)	Est k
ISMT_PVD	PVD	17.0	5.6	-12.3	**96**	**2.5**
ISMT_CVD	CVD	13.2	7.8	-12.1	**103**	**2.7**
ULVAC_NH3	PVD	15.6	6.1	-12.1	**96**	**2.5**
ULVAC_NH3	CVD	13.4	7.6	-12.1	**102**	**2.7**

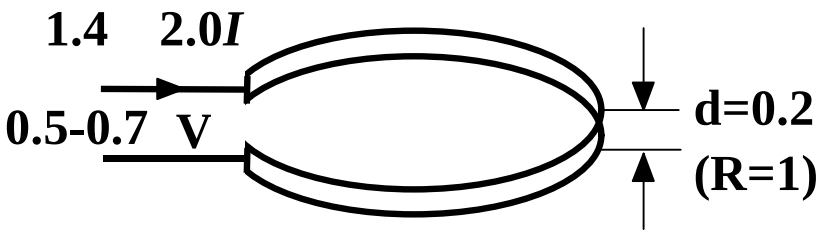
Condition		Post CMP + 400°C anneal e-test data				
Ash	Barrier	Rserp (kohm)	Comb Cap (pF)	log Briging l	R*C (*10^{-9} Fohm)	Est k
ISMT_PVD	PVD	35.1	9.9	-12.1	**348**	**2.5**
ISMT_CVD	CVD	27.3	14.0	-11.1	**382**	**2.7**
ULVAC_NH3	PVD	34.4	10.4	-11.8	**359**	**2.6**
ULVAC_NH3	CVD	27.8	13.5	-11.7	**375**	**2.7**

- Enviro^{TM} chamber modified with turbo molecular pump and electrostatic chuck for better low pressure and wafer temperature control allowed RIE processes with low damage to porous low k being developed
- Since ion density of RIE plasma decreases as pressure decreases, the ashrate is low

WCP (Widely Coupled Plasma) Source Characteristics

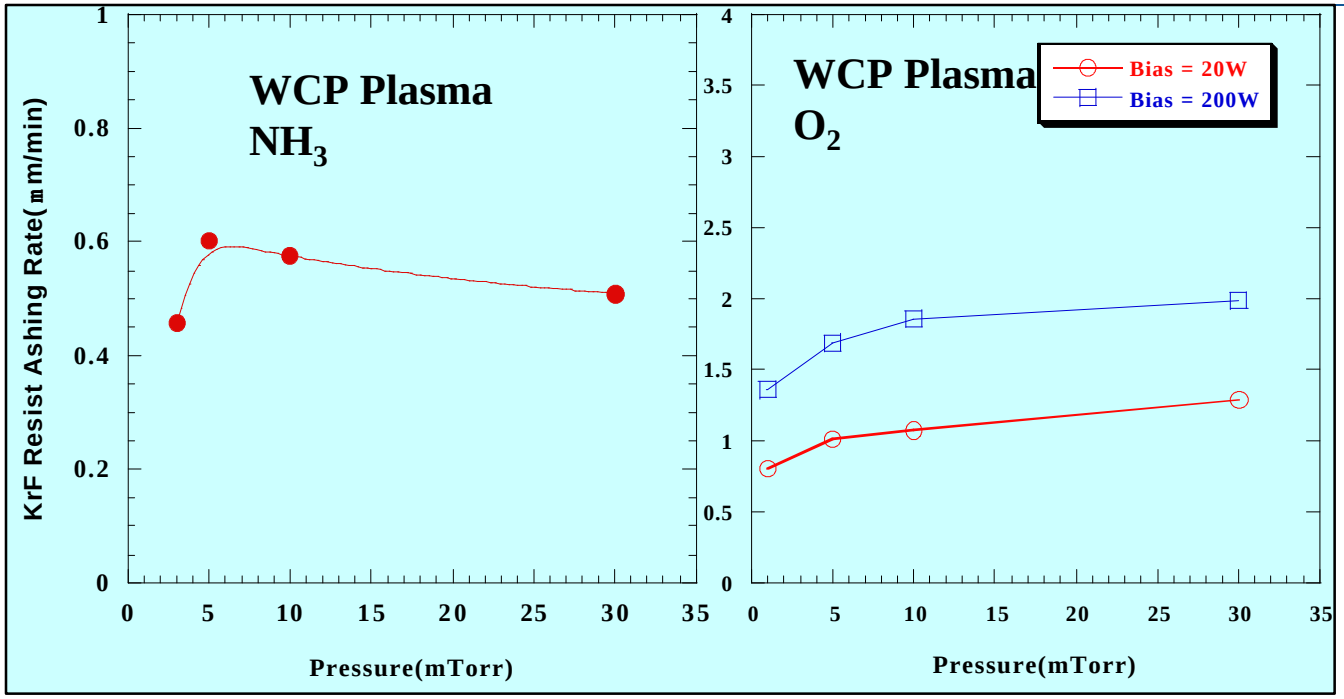


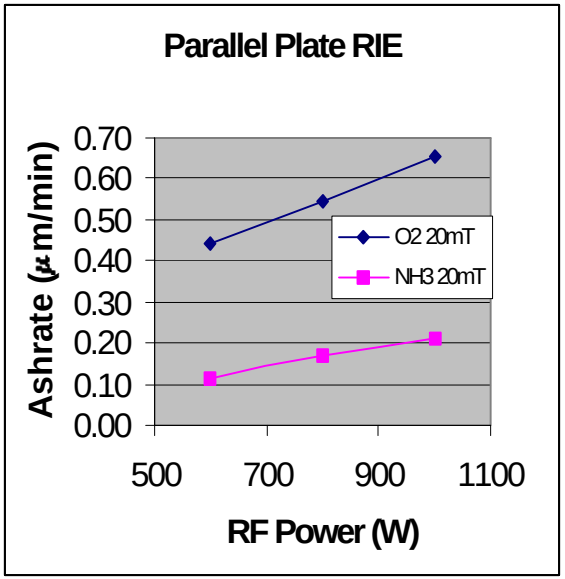
WCP antenna design



- High density and low electron temperature plasma generation in wide pressure range – high ashrate
- Low voltage on antenna coil – less sputtering on source wall

Ashrate Comparison Between WCP and Parallel Plate RIE Plasma





- Ashrate of WCP is more than 2 times of RIE for both NH_3 and O_2 chemistries

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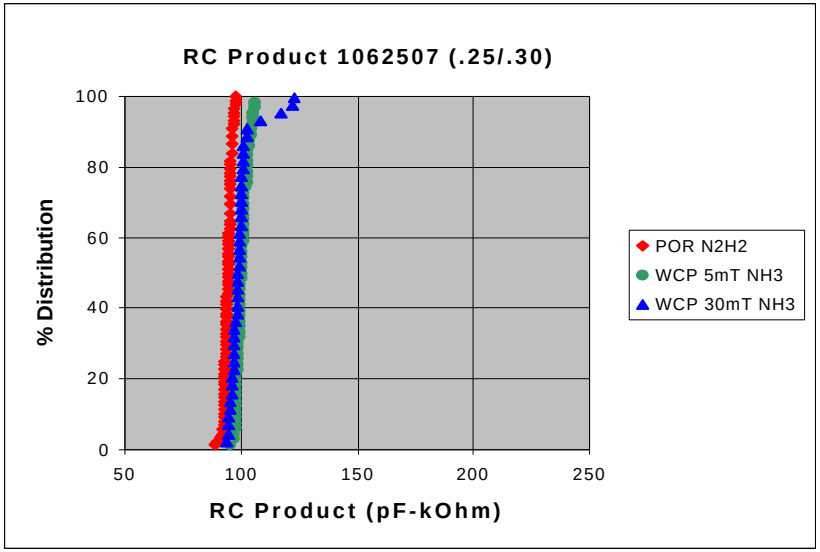
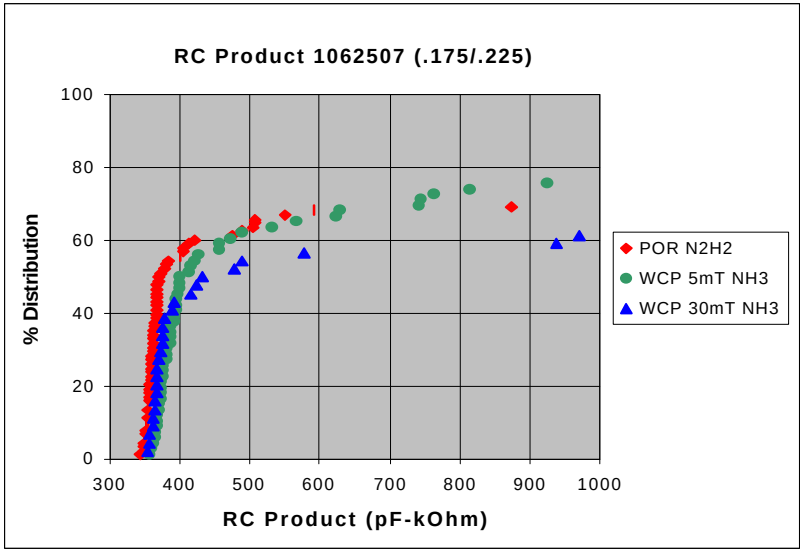
WCP Plasma Resist Ash for Porous MSQ – E-test Data





Condition		Post CMP + 400°C anneal e-test data				
Ash	Barrier	Rserp (kohm)	Comb Cap (pF)	log Briging I	R*C (*10^{-9} Fohm)	Est k
ISMT N2/H2	PVD	18.1	5.2	-12.1	**94**	**2.5**
WCP 5mT NH3	PVD	17.0	5.8	-12.0	**99**	**2.6**
WCP 30mT NH3	PVD	17.0	5.8	-12.1	**99**	**2.6**

Condition		Post CMP + 400°C anneal e-test data				
Ash	Barrier	Rserp (kohm)	Comb Cap (pF)	log Briging I	R*C (*10^{-9} Fohm)	Est k
ISMT N2/H2	PVD	40.2	8.6	-12.6	**346**	**2.5**
WCP 5mT NH3	PVD	37.6	9.8	-12.3	**368**	**2.7**
WCP 30mT NH3	PVD	36.7	9.4	-12.3	**345**	**2.5**

- WCP process does not damage porous MSQ.

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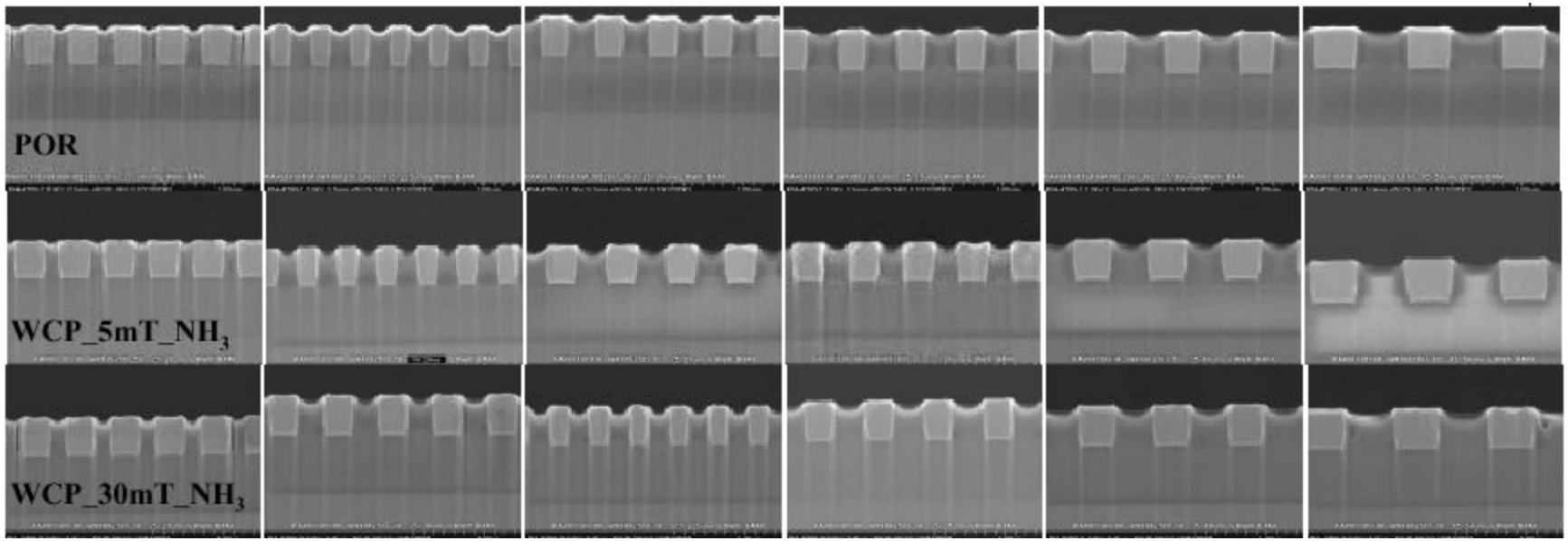
WCP Plasma Resist Ash for Porous MSQ – FIB/SEM Data

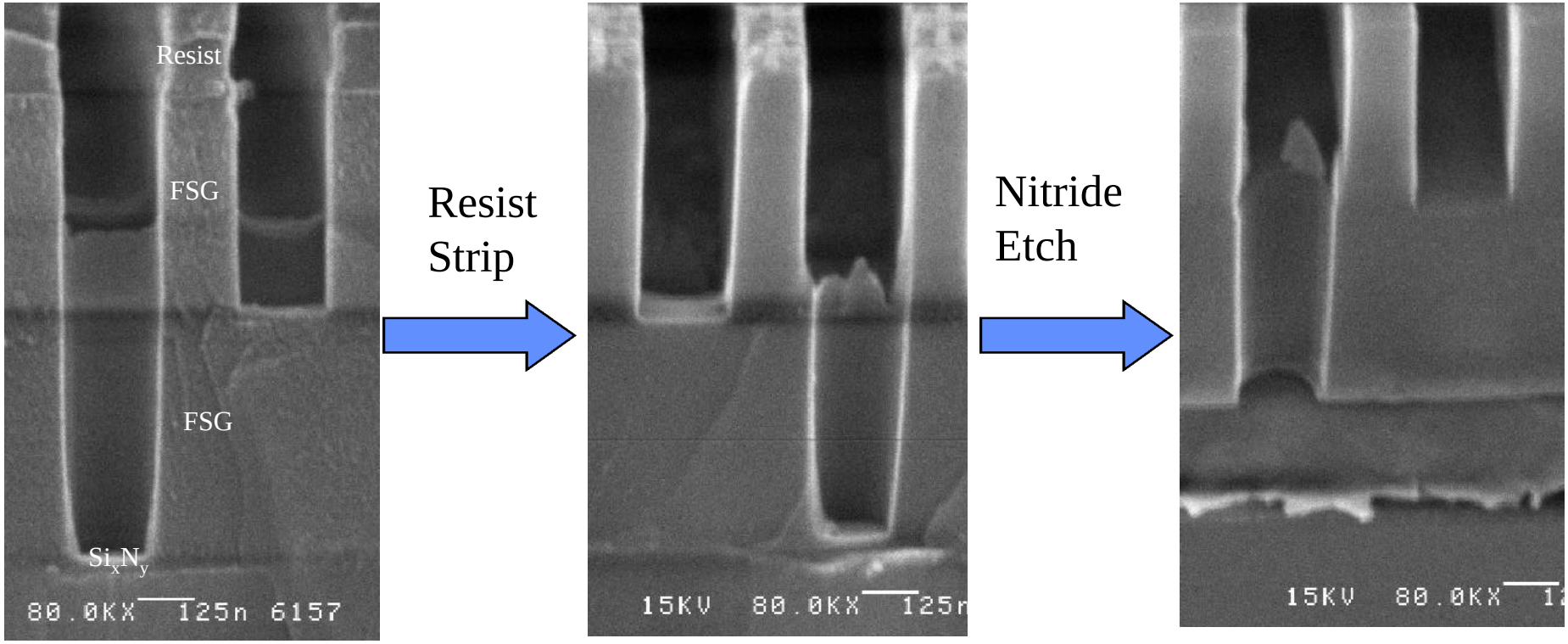


- WCP process dose not cause voids in low k film.

Summary/Conclusion

- Resist strip for porous low k is much more challenging than for non-porous low k
- Resist strip with minimum damage to porous MSQ low k can be achieved with directional ashing while maintaining low wafer temperature
- Higher density WCP plasma offers better ashrate than parallel plate RIE and more flexibility in process parameters – Important for handling many different types of porous low k materials.

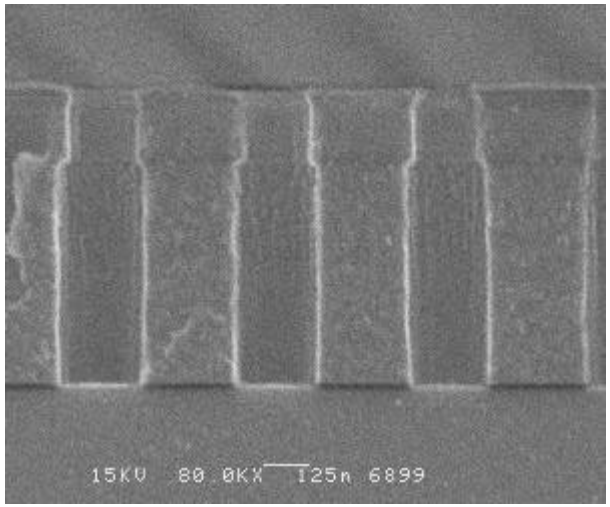
Other Applications of ENVIRO™ Low k Chamber



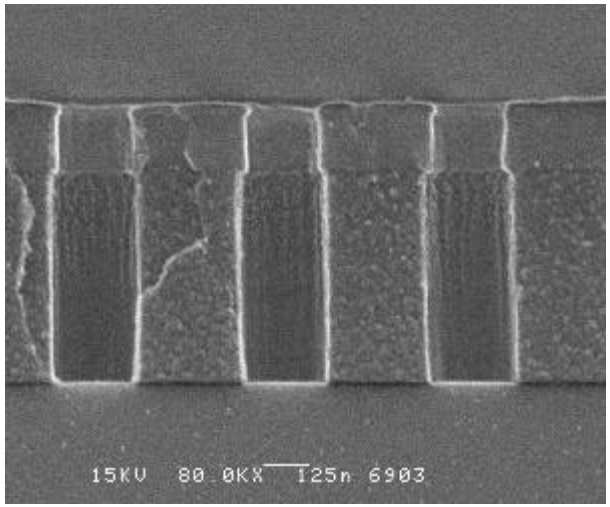
Integrated resist strip and stop layer etch process in same process chamber

Other Applications of ENVIRO™ Low k Chamber

Center



Edge



Bi-layer resist etch

Acknowledgement

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