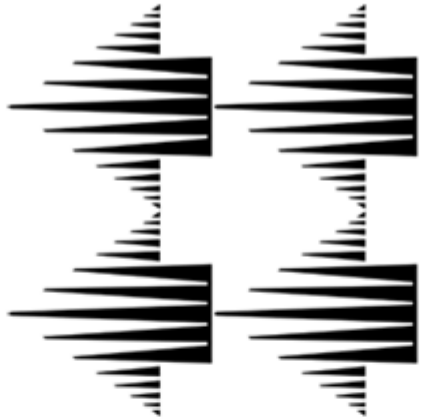


Photo resist Strip Capabilities at 90nm and below

J. Devrajan, Ph.D

Surface Integrity Group, Novellus

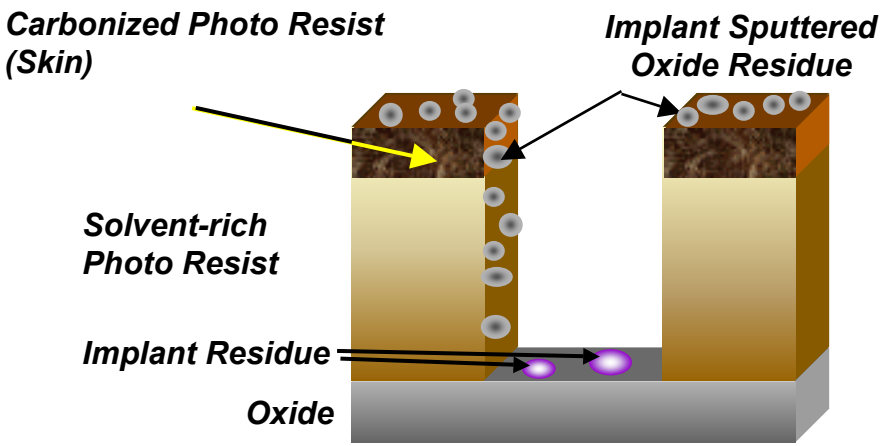
06-12-03

Presentation Outline

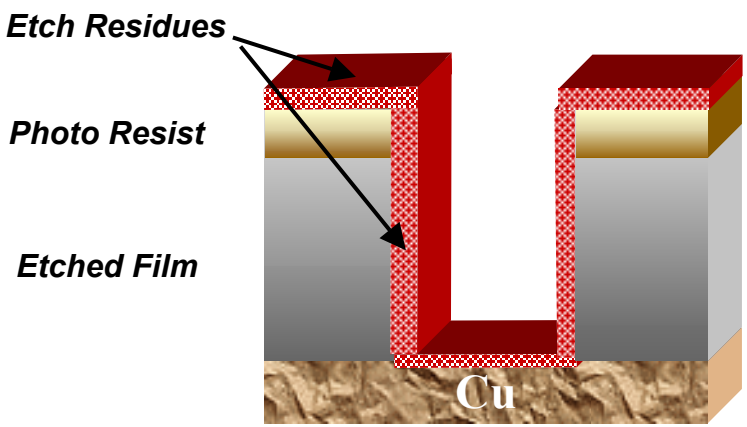
- **Photo resist Strip Requirements**
- **Gamma 2130 Architecture**
- **Applications Overview & Challenges**
  - Bulk Strip
  - High Dose Implant Strip (HDIS)
  - Recessed Resist Process (RRP)
  - Soft Silicon Etch (SSE)
- **Summary**

Requirements: Photo Resist Strip and Clean

- **Removal of photo resist after each mask level (etch and implant)**
  - No plasma-induced damage
  - Lowest COO (highest footprint and capital productivity)
- **Minimal post-strip residues to simplify subsequent wet cleans**
  - Implant: no resist flaking, no implant or sputtered oxide residues
  - Etch: reduce, eliminate or alter polymeric residues



Post-Implant (FEOL)



Post-Etch (BEOL)

90nm Low k Cu Dual Damascene

Strip/Clean Steps

M7 Via Strip & Trench
Strip/Barrier open

M6 Via Strip & Trench
Strip/Barrier open

M5 Via Strip & Trench
Strip/Barrier open

M4 Via Strip & Trench
Strip/Barrier open

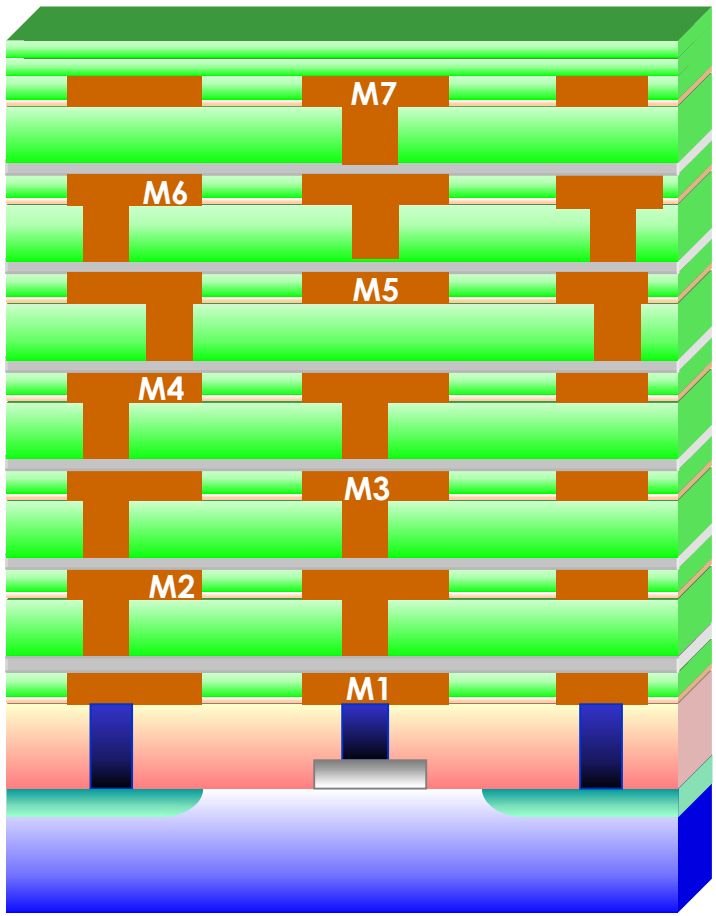
M3 Via Strip & Trench
Strip/Barrier open

M2 Via Strip & Trench
Strip/Barrier open

M1 Trench
Strip/Barrier Open

8 Bulk Strip Steps (includes contact)

4 HDI Strip Steps



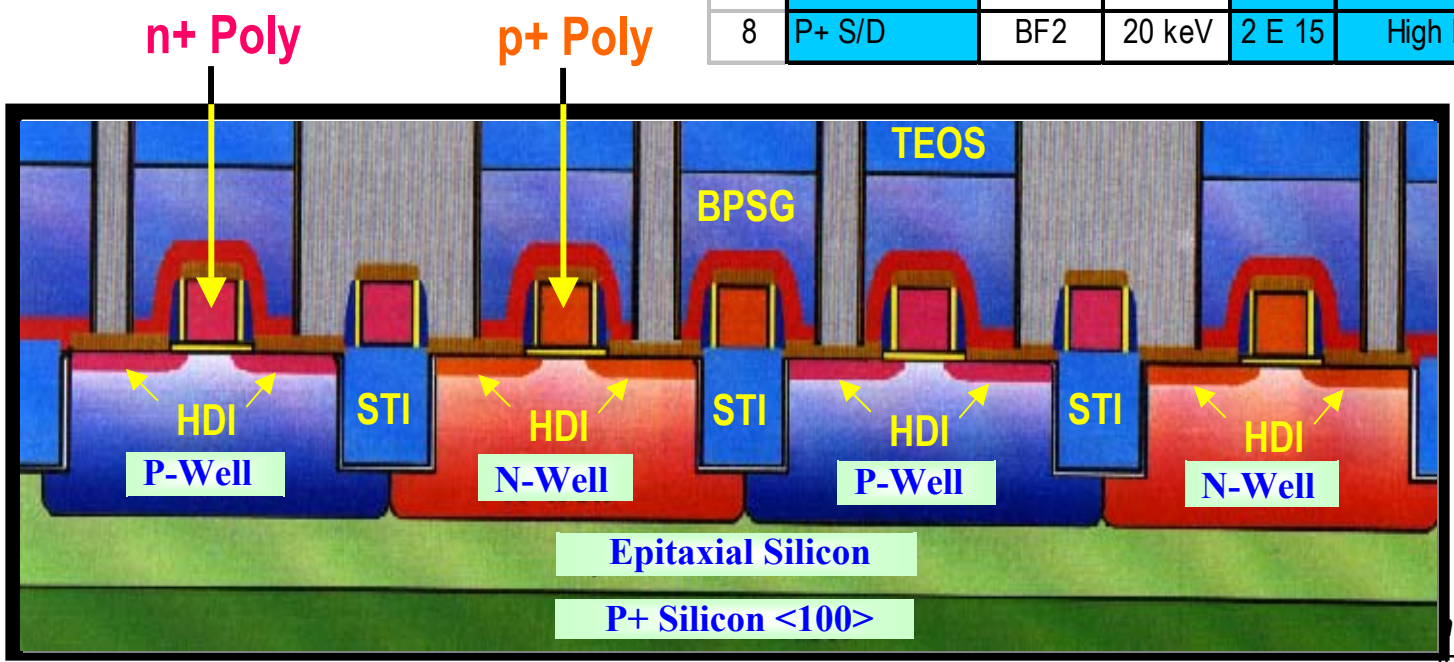
24+ levels of need for PR Strip/ Clean

Implanted Resist Conditions

- 2 High Energy Implants
- 4 High Dose Implants (HDI)
- 2 Low Dose/Energy Implants

Step	Process Step	Species	Energy	Dose	Implanted Resist
1	N Well	P	600 keV	1 E 13	High Energy
2	P Well	B	250 keV	2 E 13	High Enegy
3	N+ Poly	As	40 keV	3 E 15	High Dose
4	P+ Poly	BF2	20 keV	2 E 15	High Dose
5	N LDD	As	25 keV	3 E 13	
6	P LDD	B	5 keV	3 E 13	
7	N+ S/D	As	60 keV	3 E 15	High Dose
8	P+ S/D	BF2	20 keV	2 E 15	High Dose

LOGIC

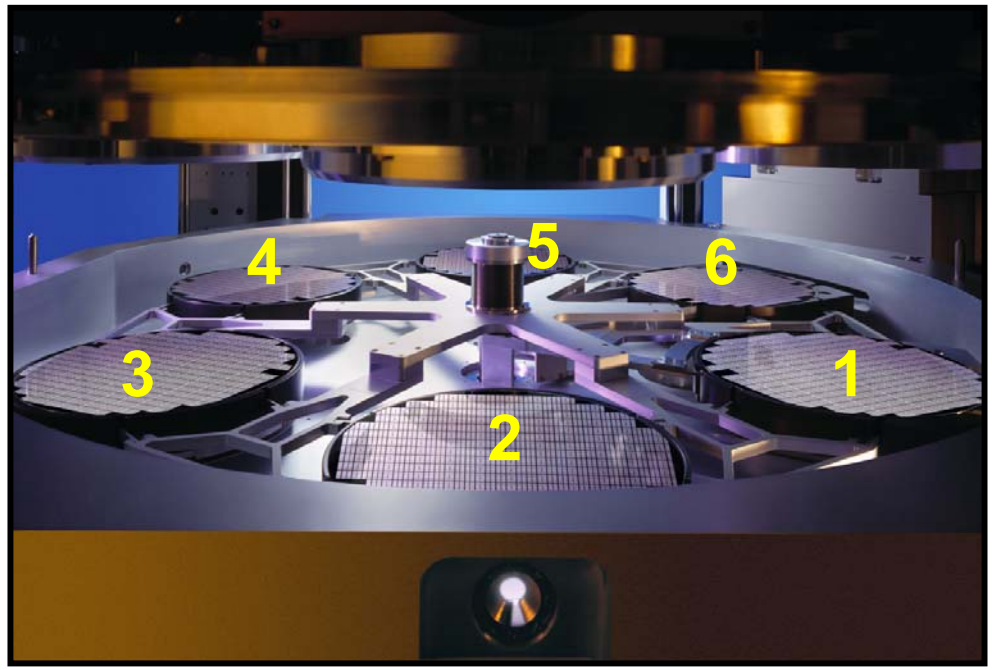


Gamma 2130 - A Simple 300mm solution

- Up to 5 strip stations
- 1 pre-heat station
- 2 load locks

From:

- One footprint
- One chamber
- One gas box

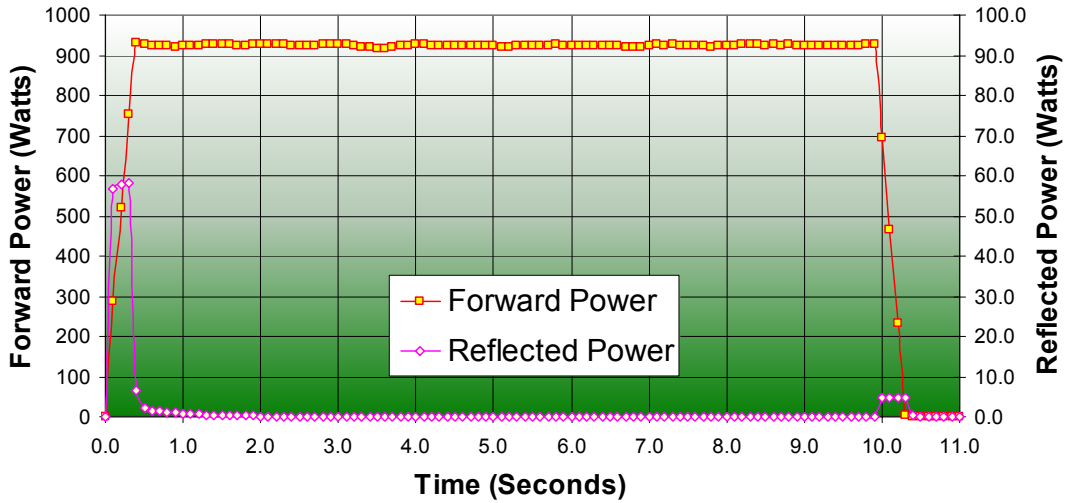


Simplicity
Reliability
Productivity

Gamma 2130 I²CP RF Source Efficiency

3 W / tube

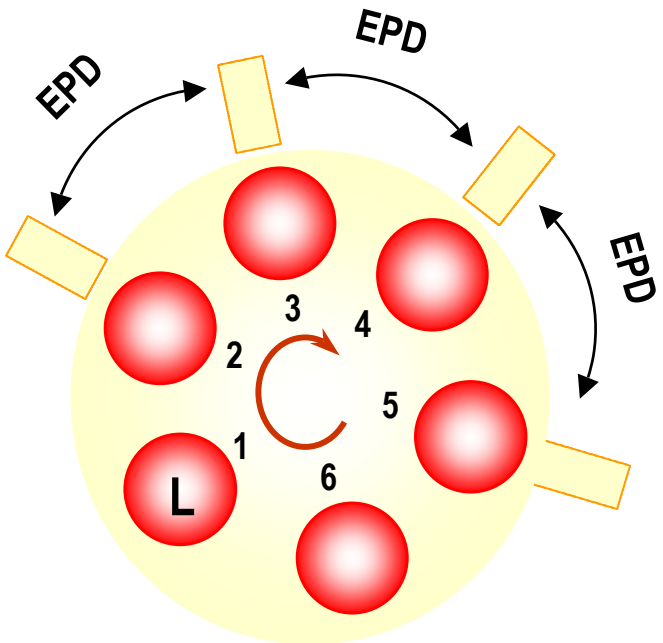
2 W / tube



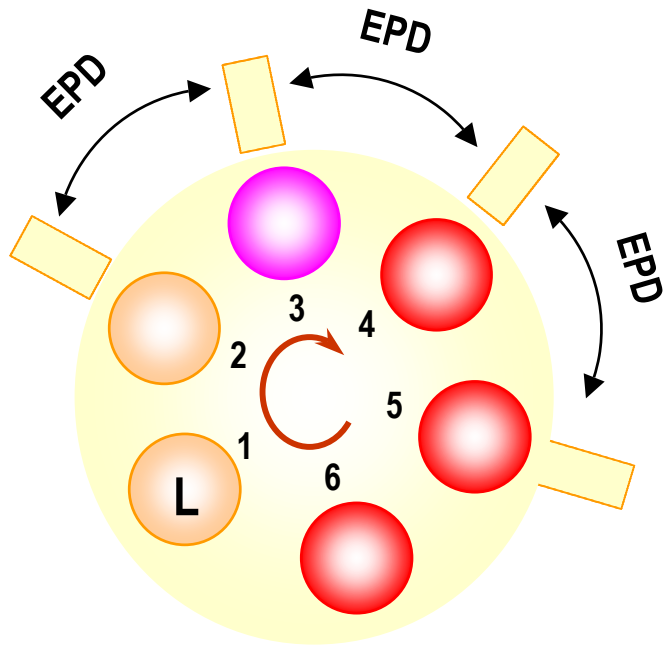
- **Easy ignition of plasma**
  - **Plasma ignites at 2W over wide pressure range**
    - Standard ICP sources need more than 100 to 500 W for ignition
  - **Efficient RF-match ensures low reflected power in 0.4 sec.**

G2130 Flexibility for All Strip Applications

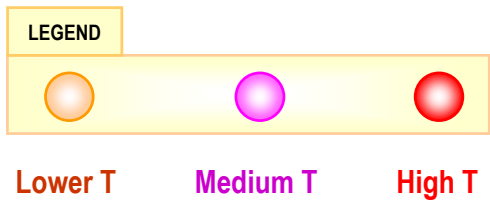
Process flexibility through independent control at each station



Bulk Strip Configuration

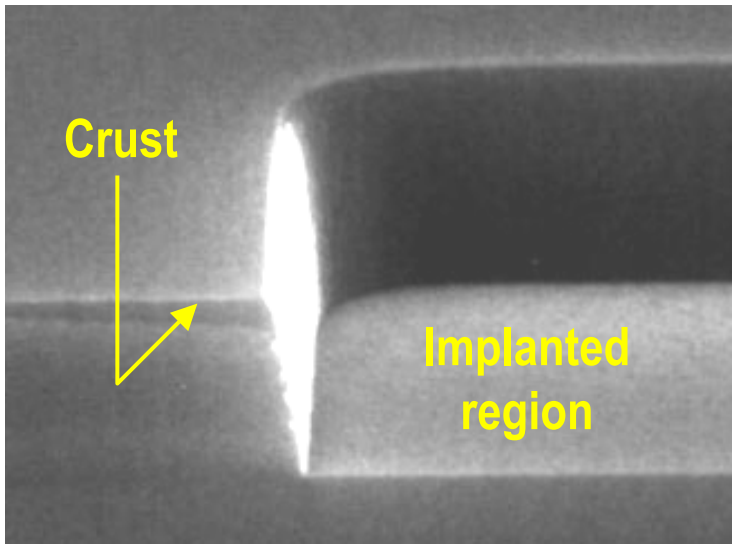


High Dose Implant Strip Configuration



Bulk Strip Throughputs >>200 wph

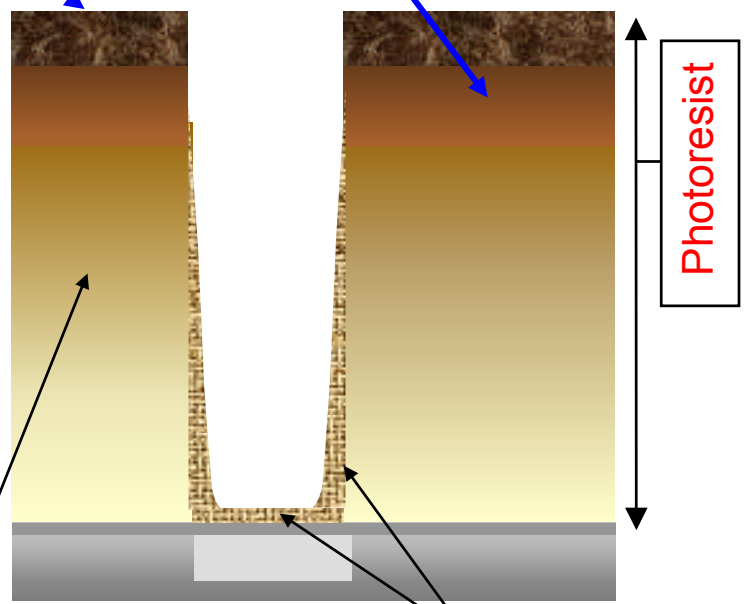
HDIS Challenges – Post-Implant Residues



Post-implantation wafer

Ion-induced carbonized layer in photo resist

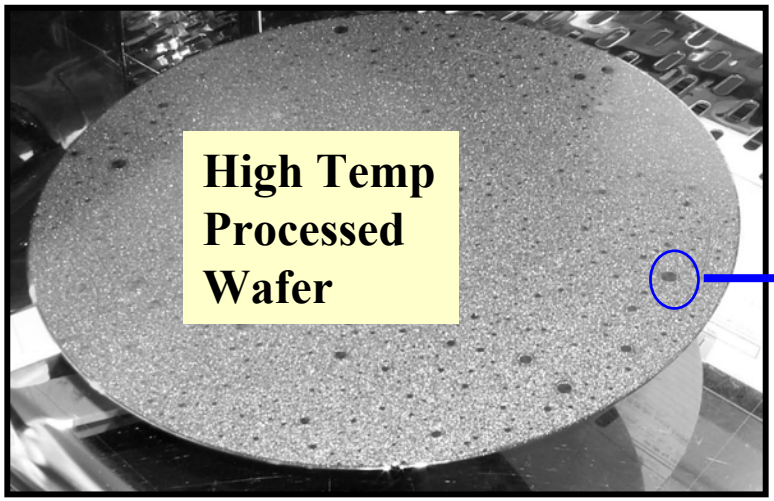
Ion-rich layer in photo resist

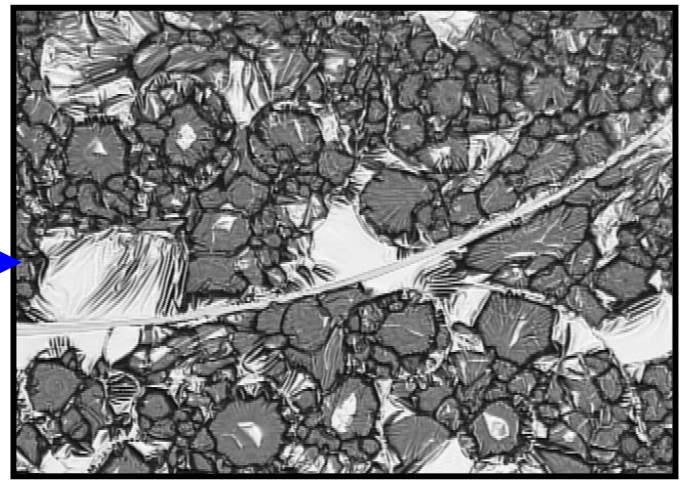


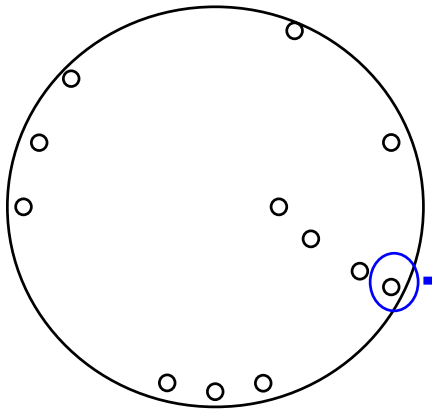
Solvent-rich photo resist layer

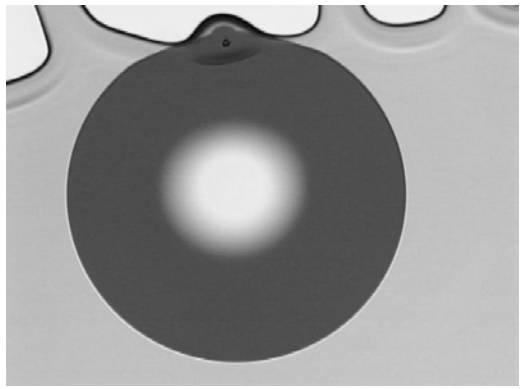
Implant sputter residues and implant species

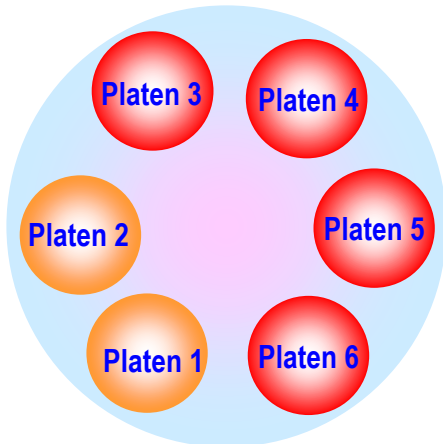
HDIS Challenges – Popping









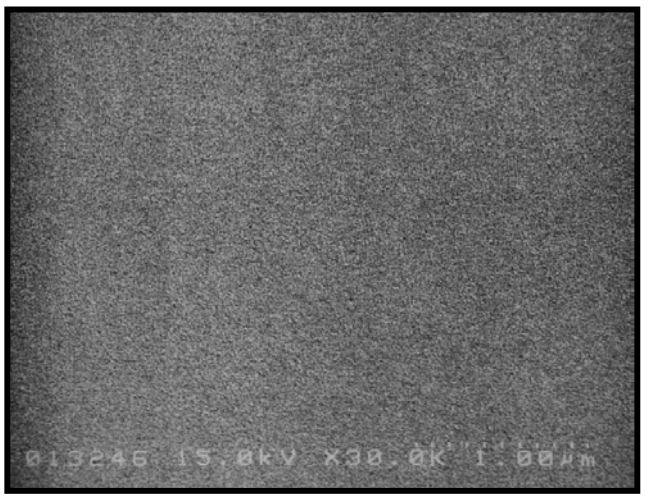


As-received wafer

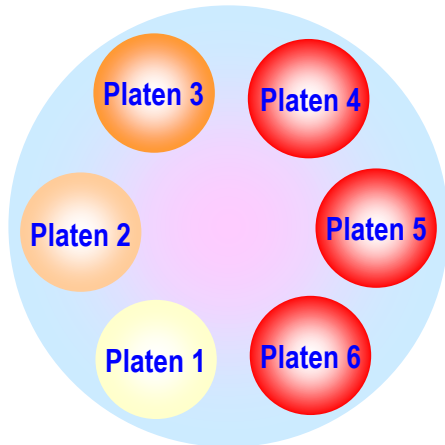
Pores that explode easily at high processing temperature

Gamma 2130 HDIS Solution

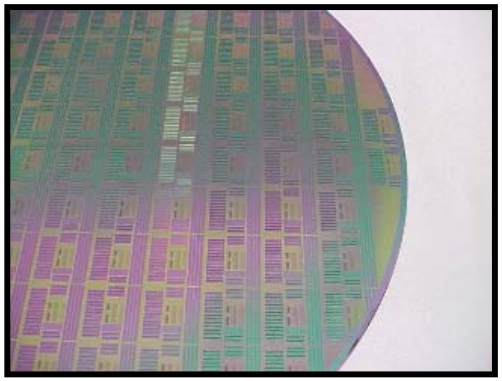
1. **Temperature Control –** Lower (ramped) temperature during crust removal. Much easier using the Gamma architecture
2. **Chemistry Control –** Different gases flow into stations performing crust removal



Popping-free results obtained using optimal temperature control

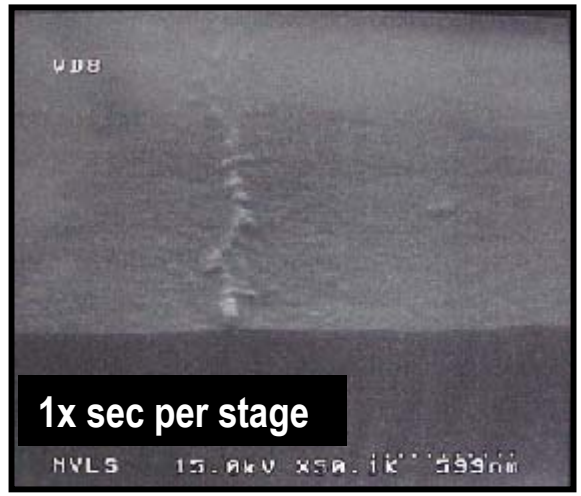


HDIS: Effect of Processing Time



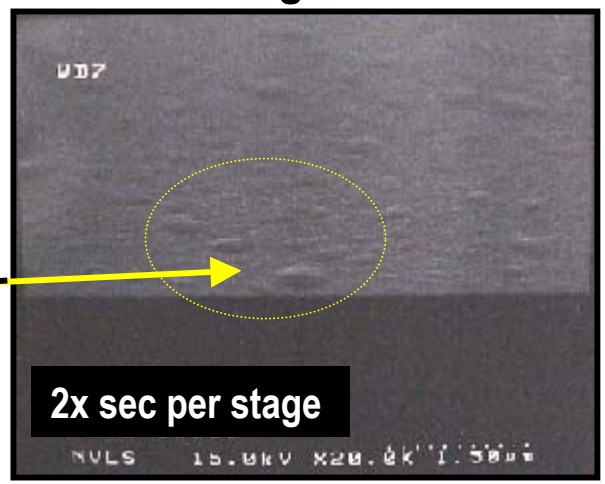
As Received
0.5 μm DUV resist

Edge



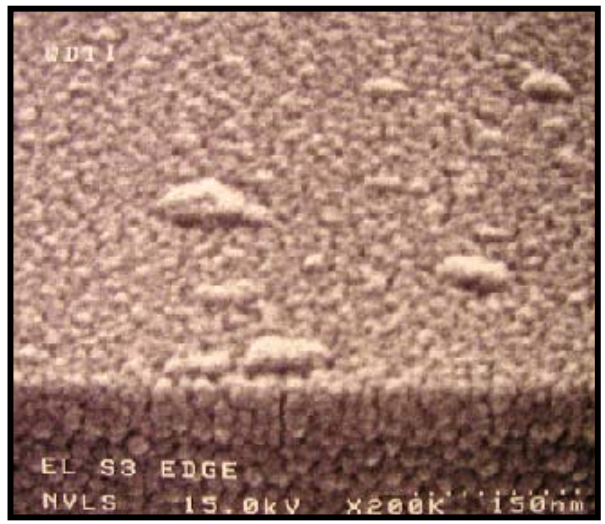
Center

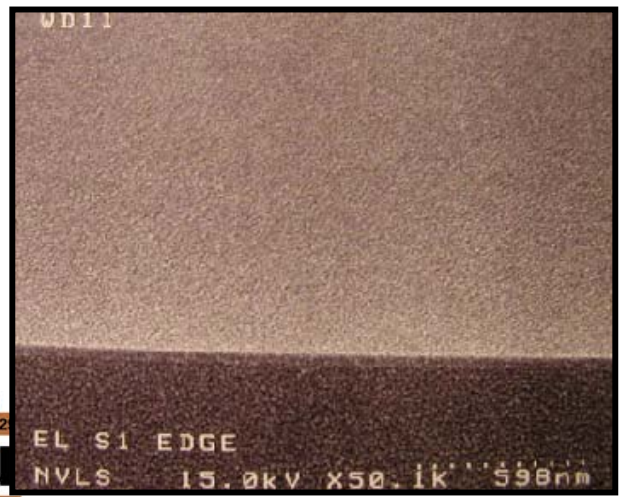
Small amount of residues



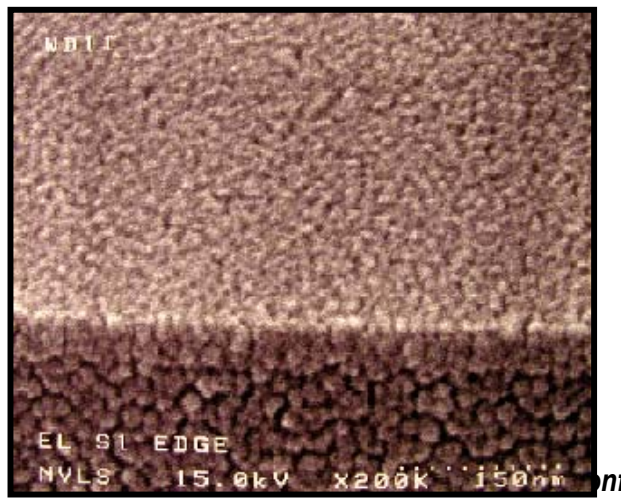
HDIS: Effectiveness of Forming Gas for Implant Residue Removal

Without Forming Gas



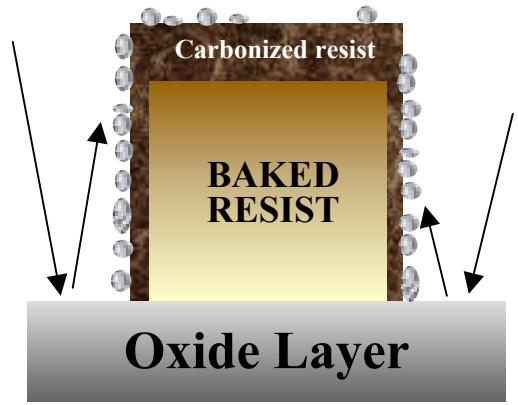


With Forming Gas

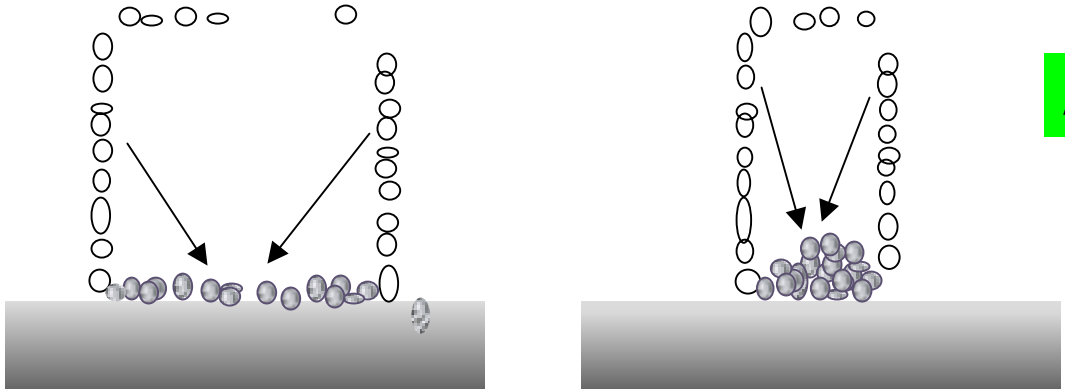


Post HDIS Residues: Sputtered Sidewalls

Underlying material sputtered to sidewalls during implantation

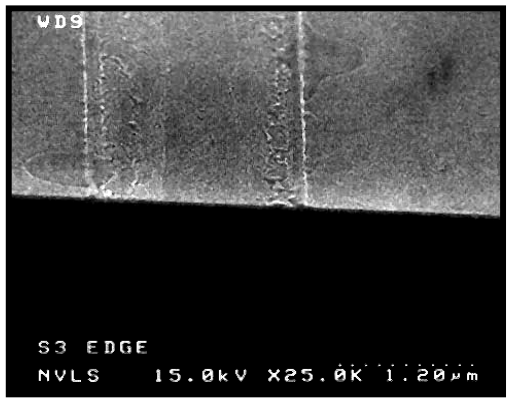
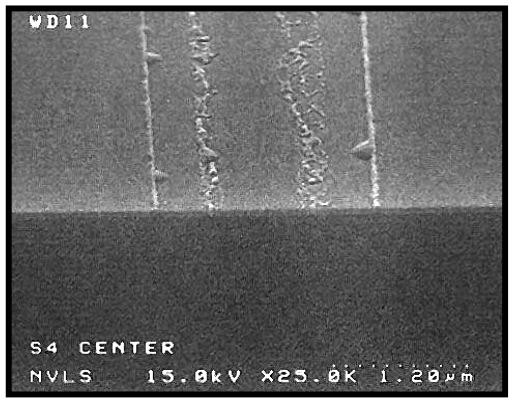
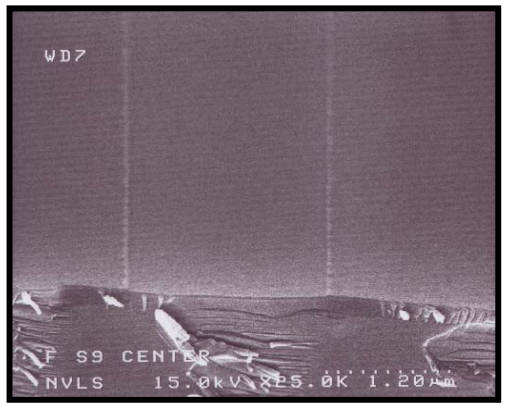
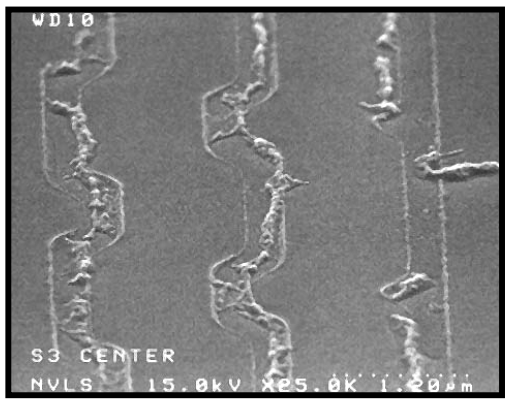
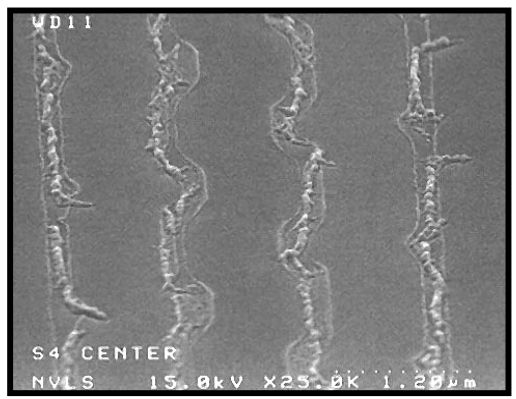
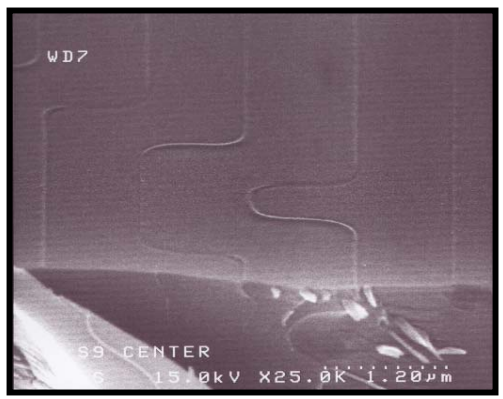


Before Strip



After Strip

HDIS: Removal of Sputtered Residues
Effect of Chemistry

	Without Forming Gas	With Forming Gas	With CF_4
1.0 μm Line Width			
0.2 μm Line Width			

- As line widths shrink, apparent amount of residues increases

HDIS - Silicon Loss Evaluation

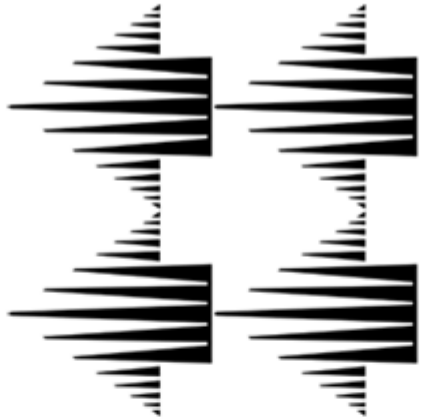
- G2130 HDIS process (with CF_4) shows 0 Å Si loss

TEMs removed

HDIS - Silicon Loss Evaluation

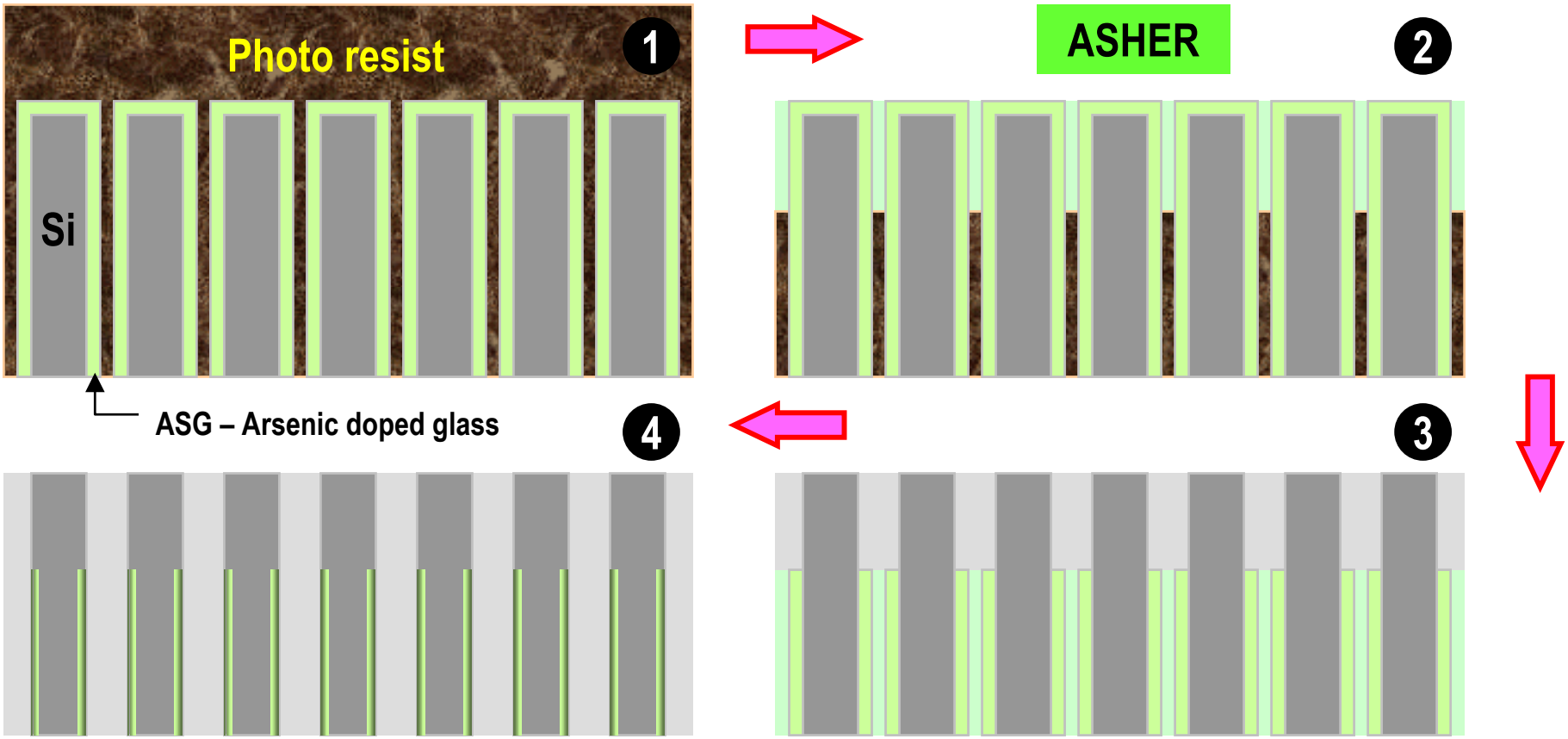
TEMs removed

- No Si loss for all recipes before and after wet clean



Recessed Resist Processing (RRP)
Soft Silicon Etch (SSE)
Backside Polymer Removal (BSP)

Recessed Resist Process - Overview (Trench Capacitor Application)



1. PR spun on Si trenches coated with ASG
2. Etch back PR

good w-i-w uniformity, w-t-w repeatability

3. Etch back ASG, strip PR
4. Drive in As into lower portions of the trenches

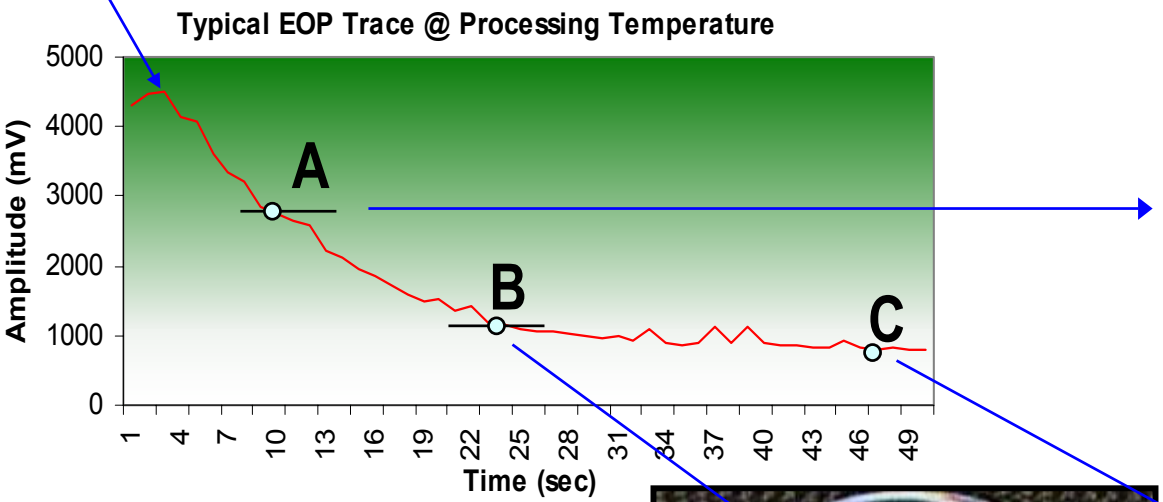
Reference: Lee, Kilho et al, Future Fab International, Issue 14, Feb. 11, 2003

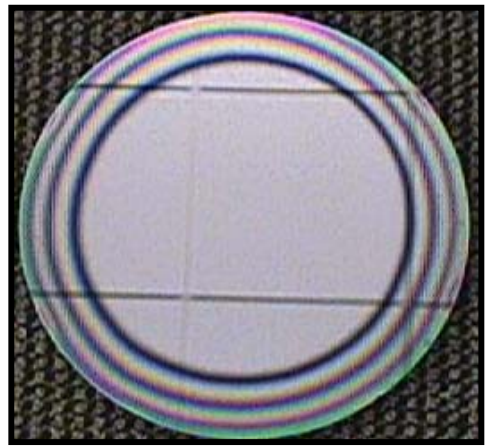
Recessed Resist Process – Challenges

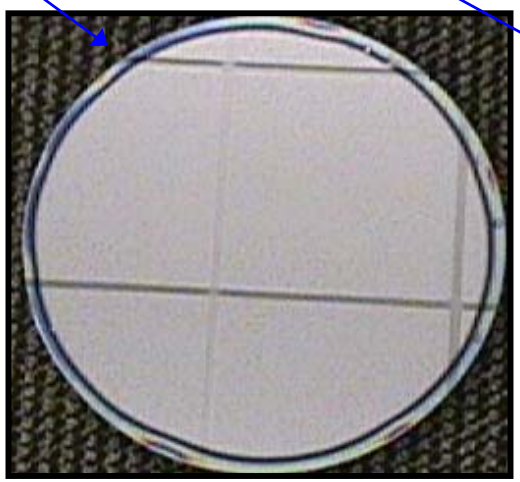
- **Incoming wafer differences**
  - **Photoresist thickness variations**
  - **Loading Effect due to differences in area density of trenches**
    - Timed etch is not an option. Process MUST be actively controlled using an Endpoint Detector (EPD)
    - Endpoint detection must be representative of process across wafer
      - Good process uniformity an absolute must (Max-min %U < 5%)
    - The EPD must show an accurate, repeatable performance
- **Processing temperature must be low to prevent capillary effect inside trenches**
- **Chemistry must be optimized for strip rate & hence throughput**

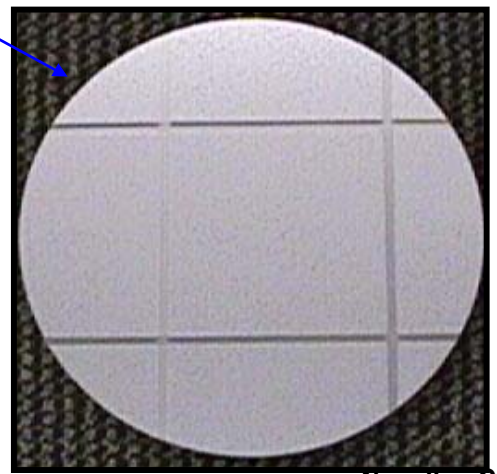
Recessed Resist Process – EOP Trace vs. Remaining Resist

Resist starts getting cleared



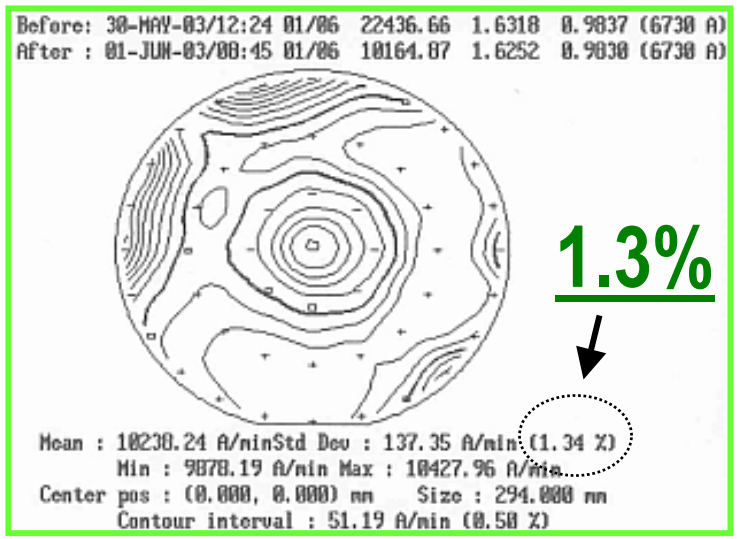






- Intensity of Signal trace clearly indicative of remaining resist
- Good process uniformity alone will guarantee trace representative of entire wafer

Recessed Resist Process – Uniformity



- Good w-i-w uniformity obtained through a combination of chemistry changes, recipe optimization, and hardware modifications

Recessed Resist Process – Patterned Wafer Results

Center

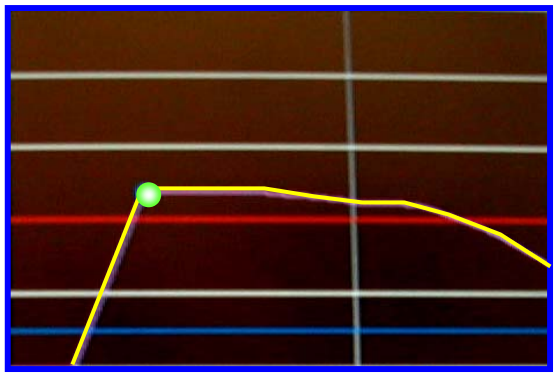
Edge (~11mm)

Edge (~6mm)

SEMs removed

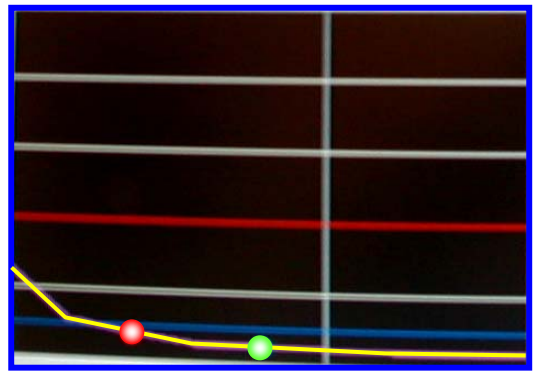
- Strip Rate inside the trenches approx. 4 – 5x that on the surface
- Actual depth of the recess may vary depending on process uniformity, strip rate, and incoming wafer variations
- Above performance (<4% max-min variation) deemed excellent by customer !

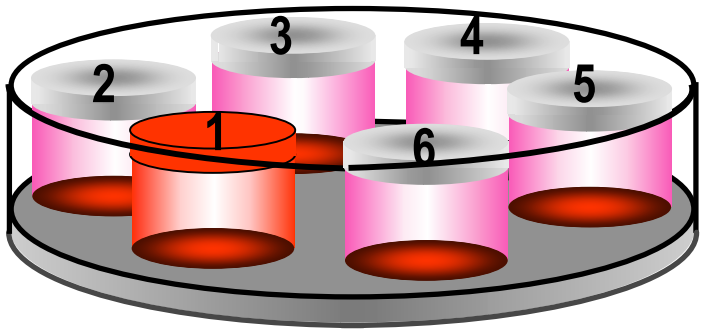
EOP Monitoring: Bulk Strip Patterned Resist with 100% Overstrip



EOP 1

EOP 2





- Pre-heat on
- All platens heated
- Standard plasma

Legend

Hot Platen

Plasma

High T Pre-heat

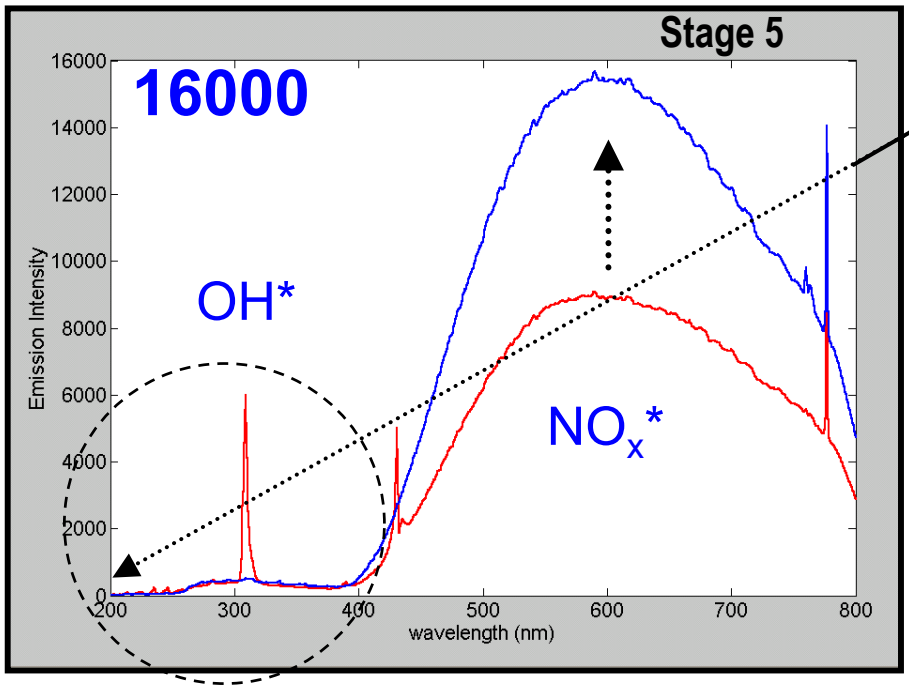
Spectral Analysis with O_2/N_2 process

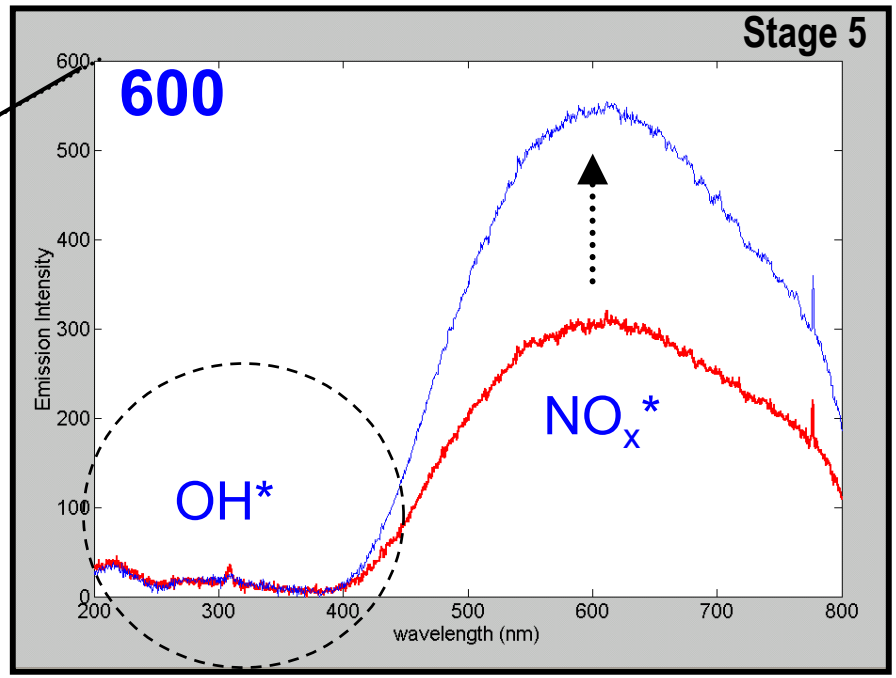
No cross talk between stations across the chamber

Monitoring at Stage 5

Before EndPoint

20% time after EP





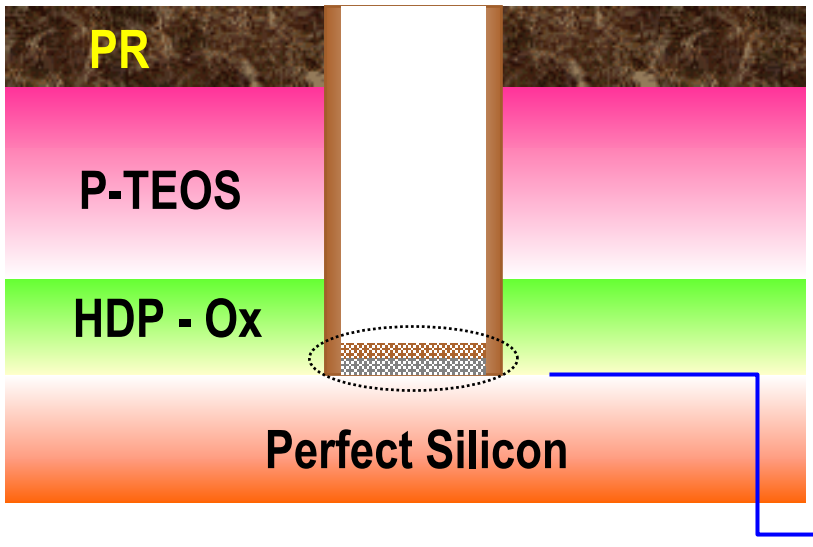
Wafer on Stage 5

(NO wafer on Stage 4)

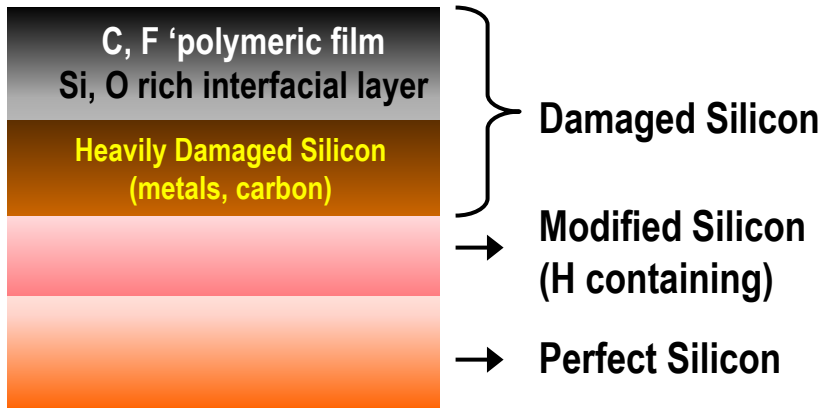
Wafer on Stage 4

(NO wafer on Stage 5)

Soft Silicon Etch – Overview



- Requirements
  - Remove 50-200 A of damaged Si prior to deposition steps
    - Si damaged during the previous etch process
    - Low contact resistance in HAR contacts required
  - Selectivity between films must be controlled

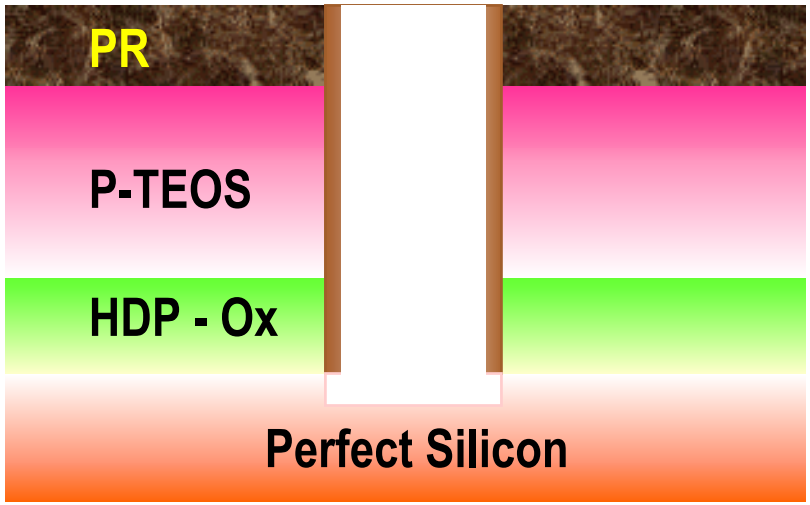


- 3 - 5 passes per wafer
- Photo resist may or may not be present at the time of Soft Si etch

Soft Silicon Etch – Challenges

- Extremely aggressive Aspect Ratios (14:1 AR in latest samples from customer)
- Process transfer from blanket films to the bottom of the HAR features
  - Presence of different AR features across wafer implies low etch rate process required
- Tight control on within-wafer and wafer-to-wafer repeatability (minimal loading effect)
- Wafer temperature control is a key requirement
  - Processes typically conducted at or near room temperature.
- Good control on selectivity between various layers
- The use of fluorine (> 1%) mandates the need for 'special' components

Soft Silicon Etch – Post Process SEMs



Post Soft Silicon Etch

SEMs removed

- **F chemistry (CF_4 or NF_3) used in the presence of O_2**
  - Damaged Si oxidized by O_2 and then etched off with F
- **A longer process time used to accentuate the isotropic nature of the etch, and to determine the etch rate**
  - Process time used = 180s, instead of typical 15-30s
  - Strip Rate was controlled at 150 A/min @ 5% max-min

Summary

- A typical product wafer will see approximately 12 wafer passes in a FEOL strip tool
  - Cost savings per wafer pass easily add up per product wafer
- The Gamma 2130 employs a unique architecture to provide throughputs in excess of 200 wph
- Challenges encountered in HDIS get dramatically magnified with technology shrinks
- The Gamma 2130 has production-proven, simple solutions for HDIS and other unique challenges posed by RRP and SSE

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