Measuring and Minimizing Line Edge Roughness in BEOL Damascene Dielectric Patterning

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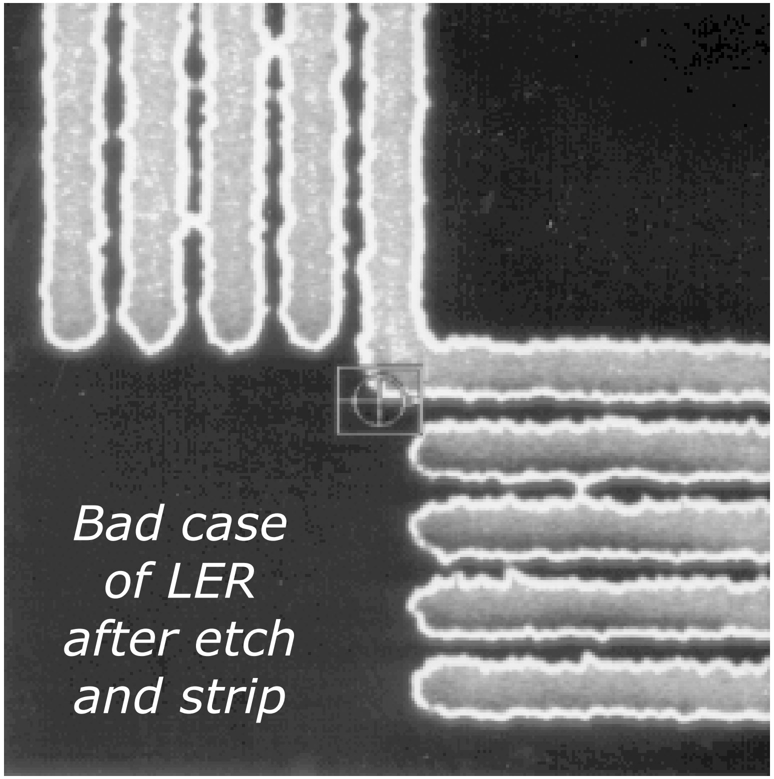
Outline

- What is line edge roughness (LER)?
- What mechanism causes it?
- How can it be quantified?
- What role is played by lithography?
- How can BEOL low-k dielectric film etching parameters be optimized to reduce it?

Introduction

- LER describes the sidewall jaggedness, striations, and rippling of photoresist and a subsequently etched feature
- Severity of LER ranges from cosmetically undesirable appearance in SEM micrographs to yield-degrading voids, line-to-line leakage, or shorts
- Although first seen during logic gate patterning, LER is a large concern *wherever* 193 nm (ArF) resists are used—including BEOL dielectric etching

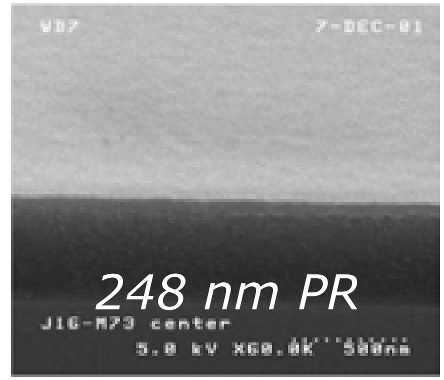


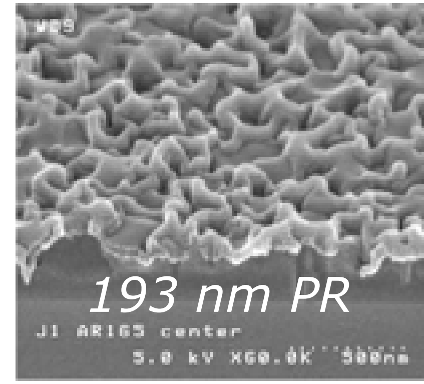
Experimental details

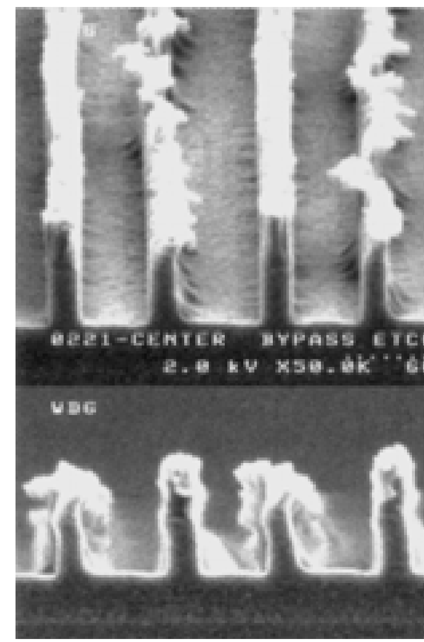
- Films: BEOL low-k inorganic CVD dielectric stack on 200 mm wafers
- Lithography: 193 nm photoresist mask with damascene trench patterns designed for 90 nm technology node
- Test structures: Isolated and dense lines/spaces with either 300 nm or 240 nm pitch measured on every die on the wafer
- Etching: Magnetically enhanced reactive ion etch (MERIE) tool
- Measurements: CD and LER measured before and after etching using Applied Materials VeraSEM and NanoSEM 3D in-line CD-SEM tools

What mechanism causes LER?

- Etch *resistance* comes from reducing the hydrogen content of resist (i.e. increasing C:H)
- 193 nm cannot use traditional phenolic groups to reduce hydrogen (too UV absorbing)
- Multiringed aliphatic groups are currently used to increase C:H in 193 nm resist, but the result is still not comparable to 248 nm resists
  - Old: poly methyl methacrylate platform (poor)
  - New: Cyclo olefin-maleic anhydride copolymer platform (less poor)
  - What's next?



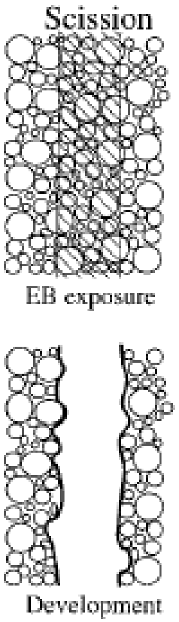


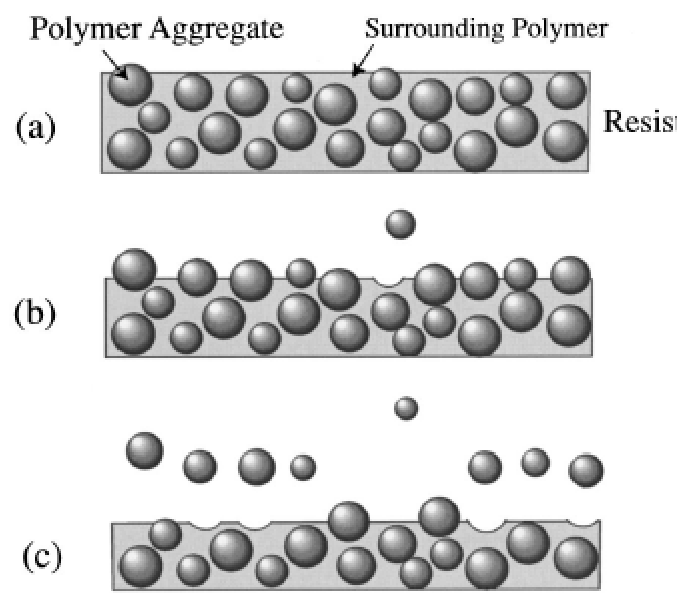


S. Lassig and E. Hudson, Sol. State Technol., **45** (10), Oct 2002, 47

What mechanism causes LER?

- Both 248 nm and 193 nm resists use chemical amplification to make up for the relatively low intensity of DUV light produced by the KrF and ArF lasers
- Chemically amplified resists form "spongy" walls—photoacid diffusion and catalytic reaction form coiled polymer chains or polymer aggregates, leading to a roughened sidewall when developed
- The developed resist is nonhomogeneous and likely to be further roughened by the physical and chemical action of plasma etching





H. Namatsu et al., J. Vac. Sci. Technol. B **16**, 6, 1998, 3315

Dealing with LER

- Although the origins of LER lie within the resist itself, how this gets translated to the final film pattern depends on:
  - Integration scheme (e.g. use of dielectric or metal hardmasks)
  - Plasma etch equipment and process
- Minimizing LER requires cooperation between lithography and etching engineers
- To study LER, a consistent and reliable technique first must be developed to measure it
- Once it can be quantified, reductions in LER can be achieved by optimization of both lithography and plasma etching parameters
  - Litho: Resist type/thickness, focus/exposure, temperatures, etc.
  - Etch: Wafer temperature, power levels, chemistry, pressure, etc.

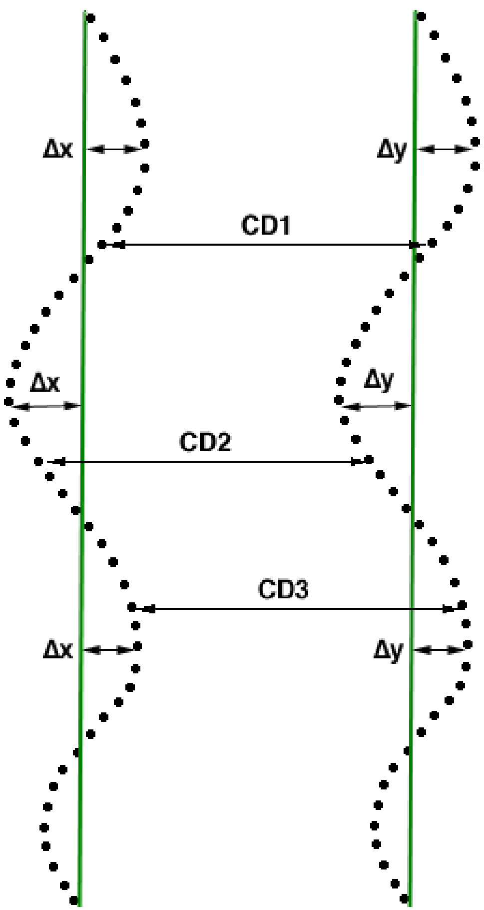
2002 ITRS roadmap

Year of Production	2001	2004	2007	2010	2013	2016
Technology Node (nm)	130	90	65	45	32	22
LER control (nm)	4.5	2.7	1.8	1.3	0.9	0.65

http://public.itrs.net/Files/2002Update/2002Update.pdf

- ITRS defines LER as "local line width variation (3σ total, all frequency components included, both edges) evaluated along a distance equal to four times the technology node"
- Does not specify the number of scans (degree of sampling), which can affect the measured LER depending on the frequency contributions
- Standardization is important to ensure consistent and comparable measurements

LER algorithm

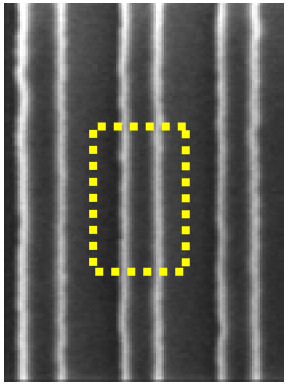


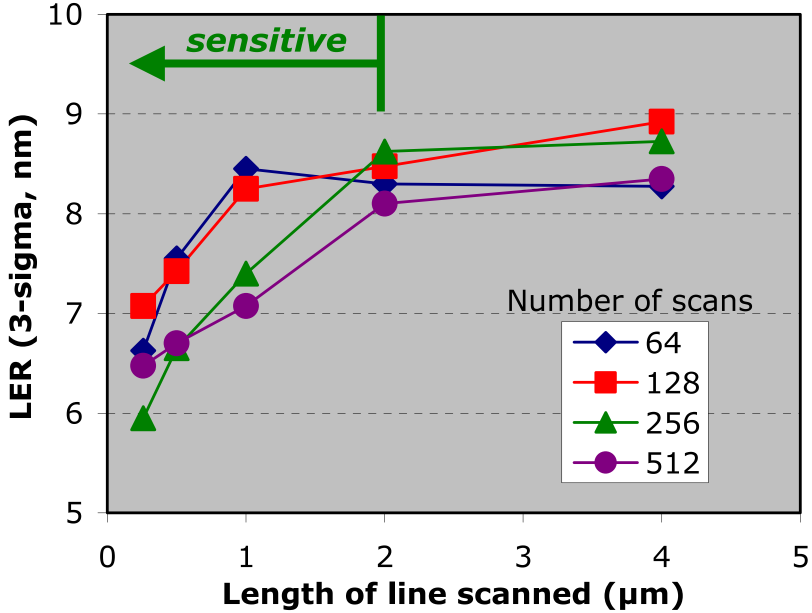
- The algorithm performs a linear fit (green line) to the edge points (black dots) of the signal for both edges
- Roughness is the standard deviation of the distances between the individual edge locations and the fitted line (Δx's)
  - $Roughness = 3\sqrt{\sigma^2_{left-edge} + \sigma^2_{right-edge}}$
  - Matches ITRS definition
- Many repetitions are performed along the length of the structure—64 is very typical, but some software allows as many as 1024 scan lines
- LER precision (3σ) is 1.0 nm on this tool

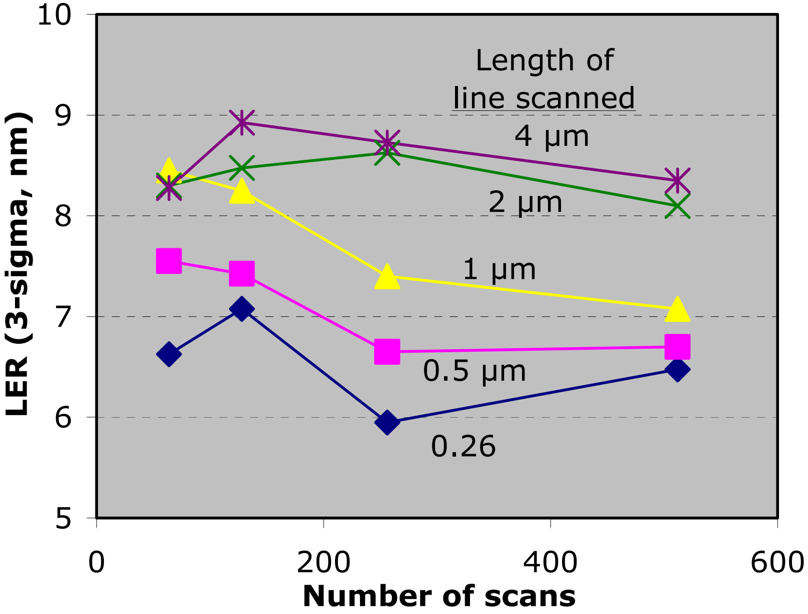
Dependence of LER on measurement technique

- LER is sensitive to the size of the box used to measure it
  - Too short and LER becomes a function of the box size—should be ≥ 2 μm tall, not 4x technology node
  - Not as sensitive to *number* of scans

Box height = 4 x 90 nm technology node (ITRS definition of LER)

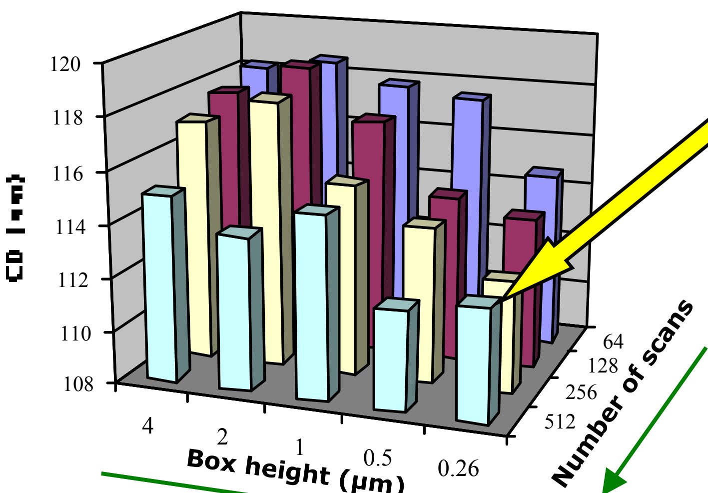






Sample rate

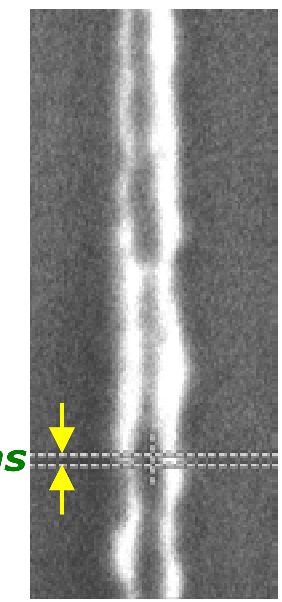
- More scans are needed to detect high frequency components of LER—but oversampling can be detrimental
- 2 µm measurement box with 256 scans gives ~ 8 nm between scans—good balance between sufficient sampling and avoiding charging



Watch out for charging effects—resist shrinkage can be significant for high degree of sampling

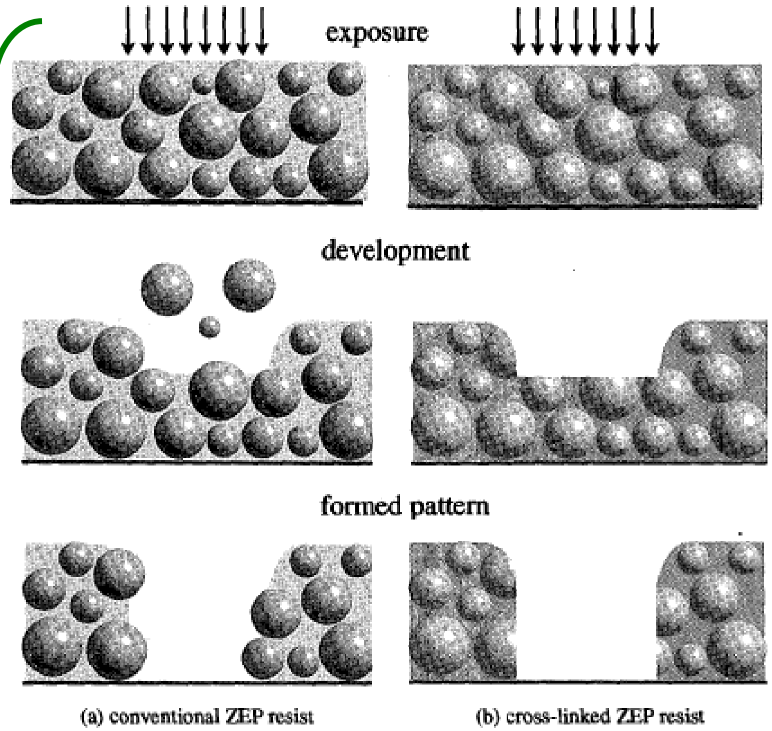
Increase in charging

8 nm between scans



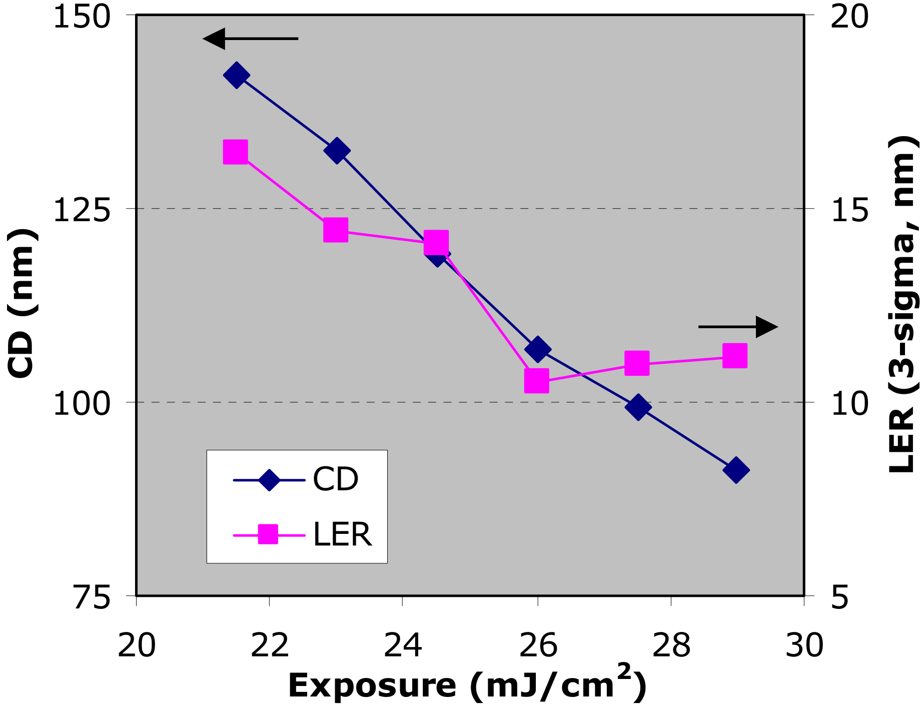
Reducing LER at litho

- To reduce LER (previous studies):
  - Improve quality of the aerial image
  - Use low molecular weight constituents in the photoresist
  - Suppress extraction of polymer aggregates from the resist sidewalls by cross-linking to reduce the difference in dissolution rate between the aggregates and their surroundings
  - Increase or decrease develop time (inconsistent results)

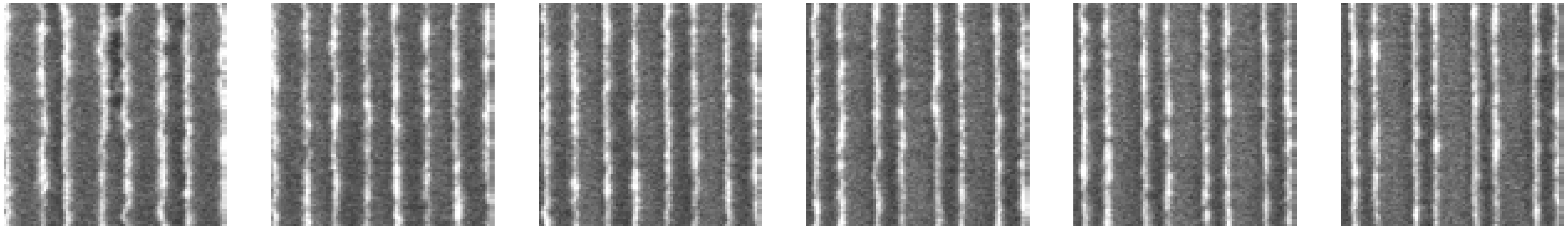


T. Yamaguchi et al., Intl. Microprocesses and Nanotechnology Conf., 1999, 158

Dense LER vs. exposure

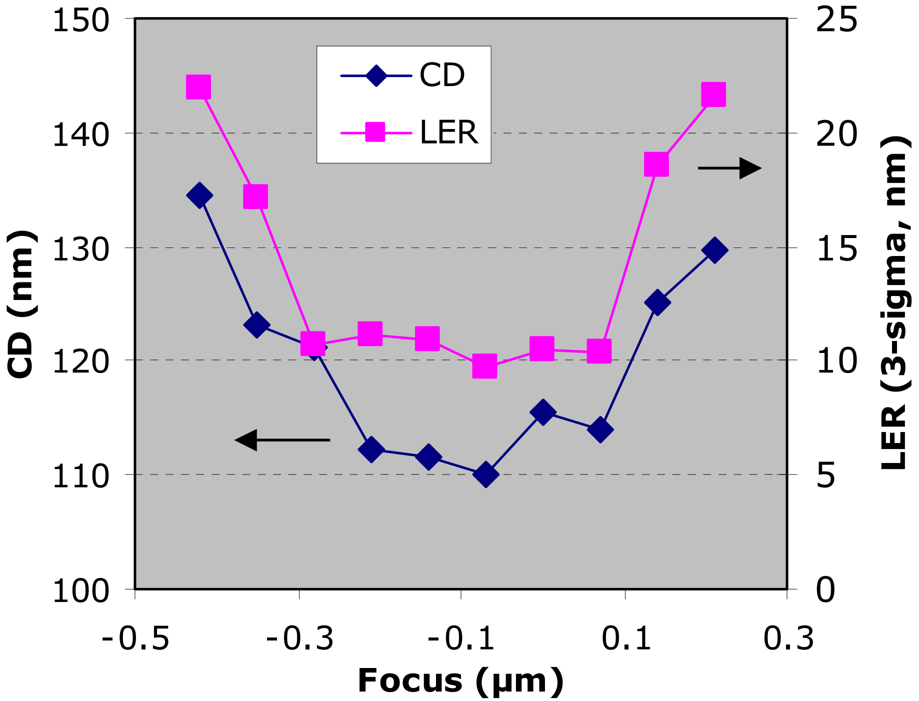


- LER and CD (before etching) both decrease with increasing exposure for dense lines
- Reducing LER may require a CD bias
- Improvement in LER may flatten out at higher exposure doses

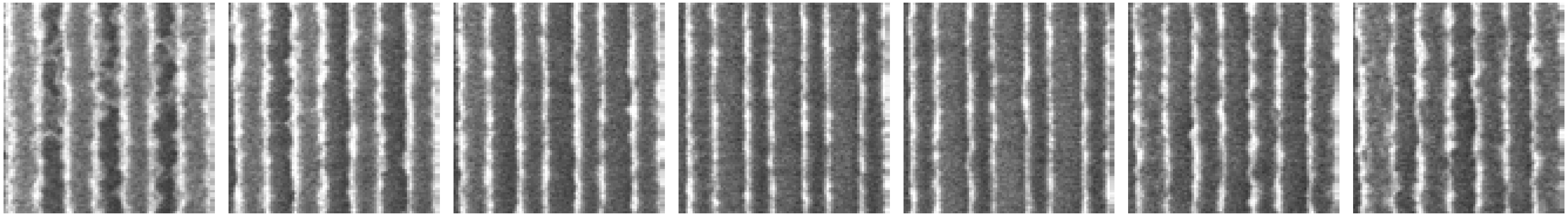


21.5 mJ/cm^2 | 23 mJ/cm^2 | 24.5 mJ/cm^2 | 26 mJ/cm^2 | 27.5 mJ/cm^2 | 29 mJ/cm^2

Dense LER vs. focus



- Both positive and negative defocus increase LER
- Optimum LER coincides with the minimum in the CD vs. focus curve
- CD and LER windows are closely related



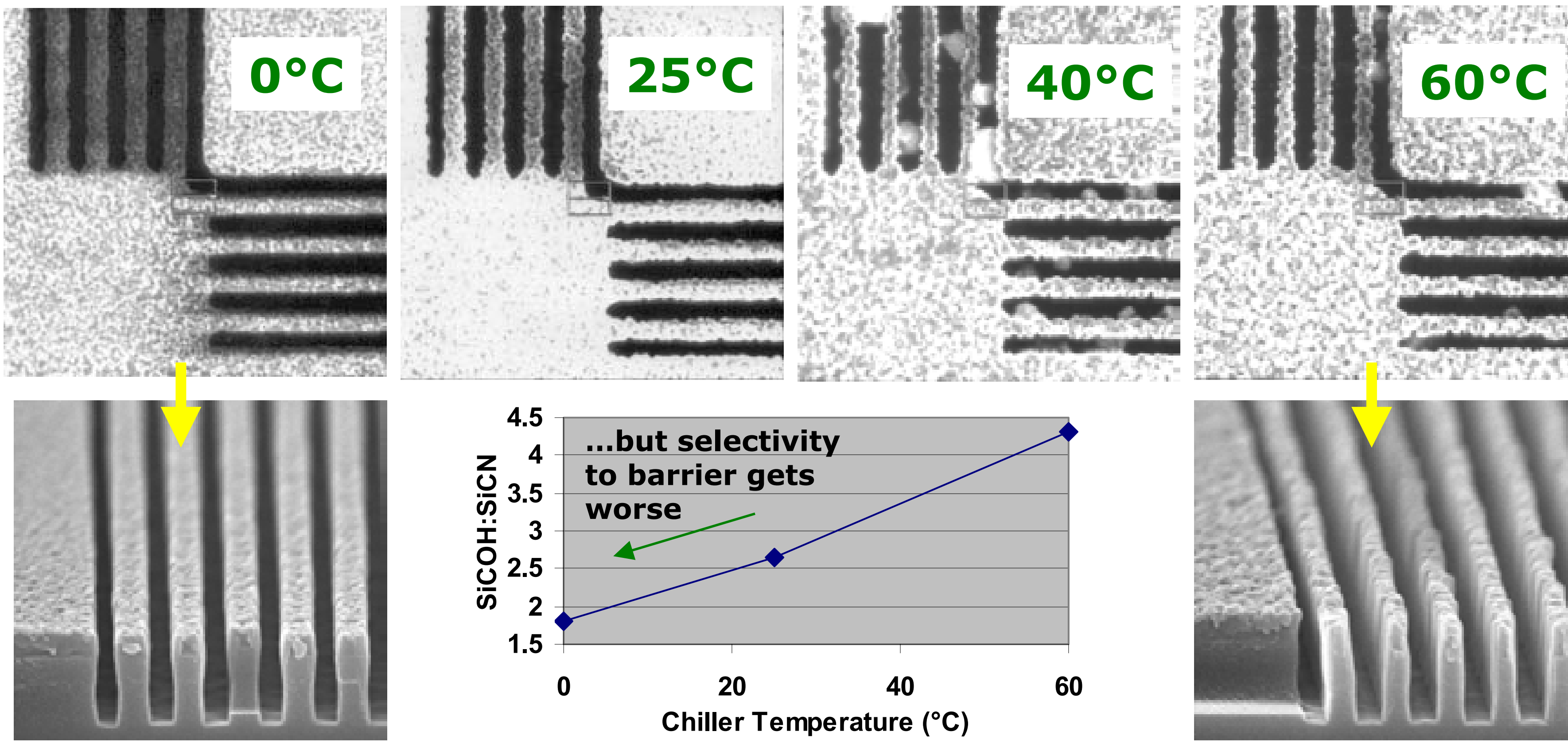
-0.42µm | -0.35µm | -0.28µm | -0.14µm | 0.00µm | 0.14µm | 0.21µm

Dielectric etching effects

- LER is clearly visible before etching, and unavoidable with 193 nm resist even when lithography is optimized
- Etching can slightly reduce LER or make it much worse, depending on the etch tool and process
- Magnetically enhanced reactive ion etch (MERIE) tool used here to etch trenches in low-k inorganic CVD dielectric stack
- Many etch process parameters were studied—the main factors affecting LER were found to be:
  - Chiller temperature
  - RF power (13.56 MHz connected to lower electrode)

Effect of chiller temperature

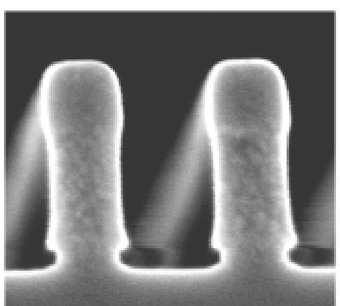
- Partial etch, leaving resist intact
- LER and resist pitting reduced at low temperature (0~25°C)

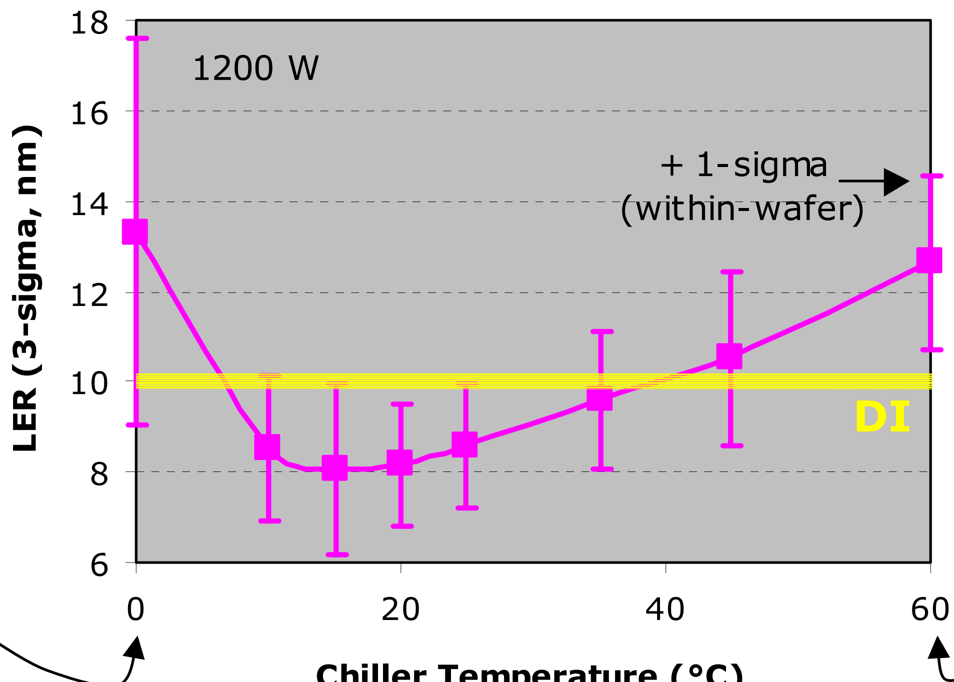


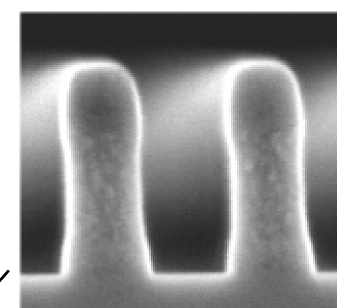
Effect of chiller temperature (normalized data from several lots)

- LER degrades at high *and* low temperatures (minimized at 15-20°C)—evidence of competing mechanisms
  - Resist roughening is reduced as temperature is lowered
  - More attack of cap and barrier films at low temperature

Lateral etching of barrier can occur on a cold wafer

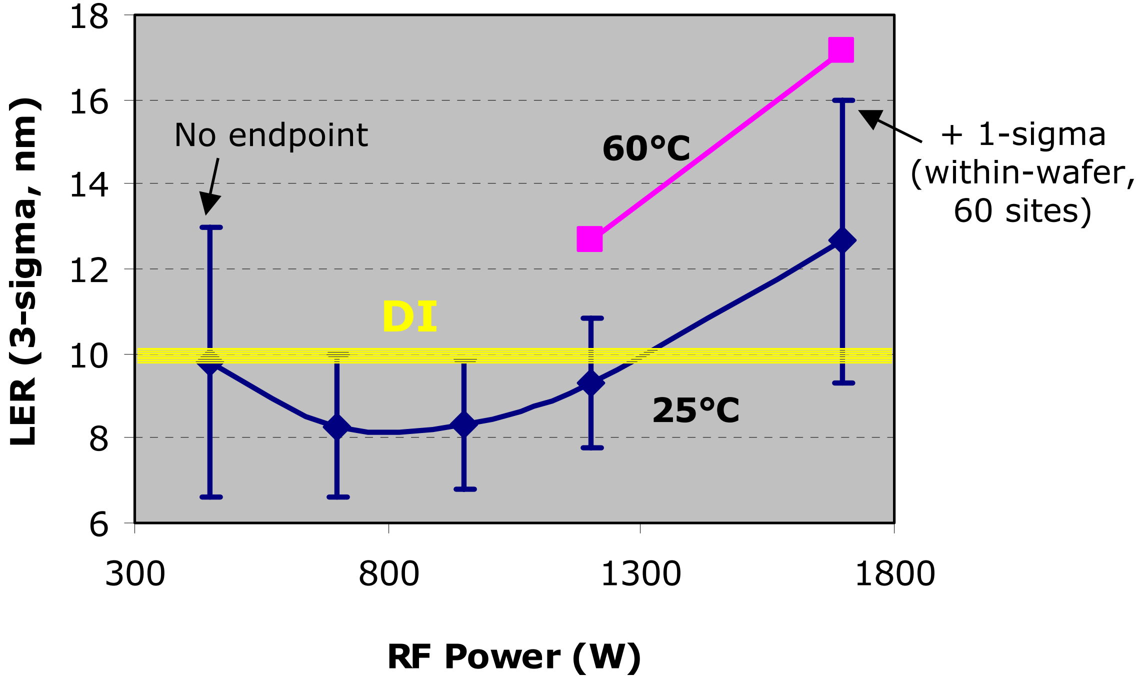






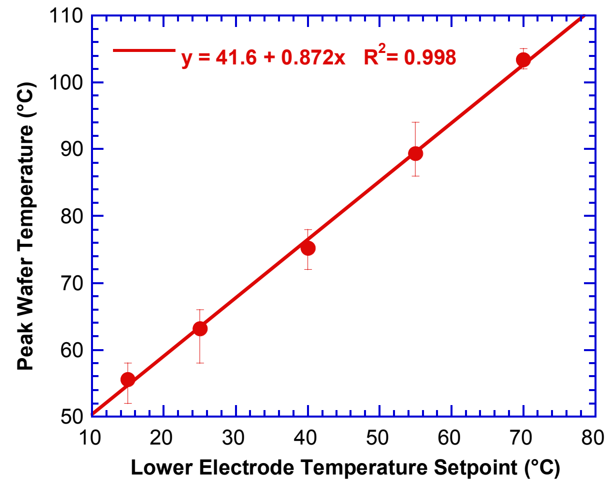
Effect of RF power
(normalized data from several lots)

- LER degrades at high power (especially when combined with high temperature) and appears to be minimized near 800 W
- Increase in LER at very low power may be caused by overetching from missed endpoint (slow etch rate, weak signal)

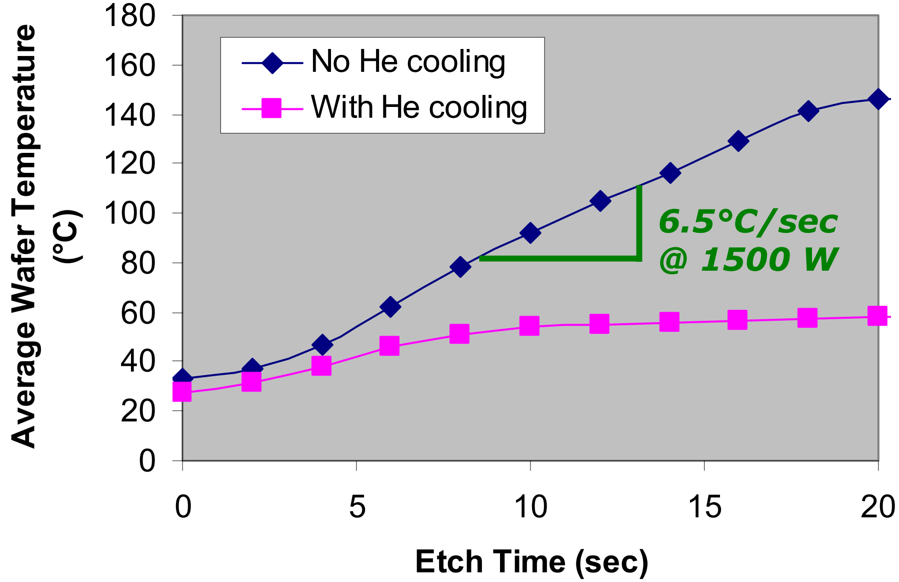


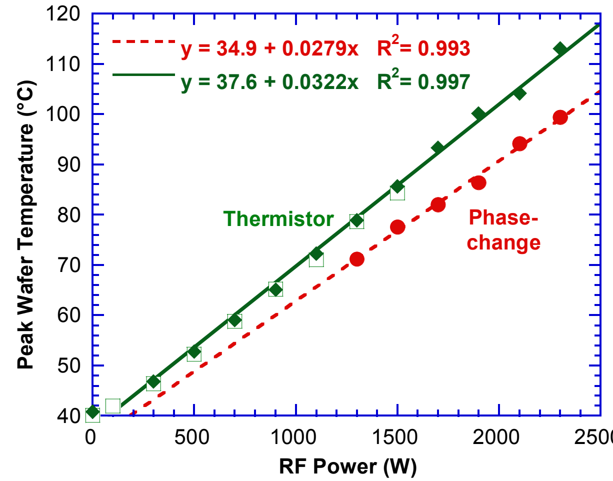
Correlation of power and temperature

- RF power and chiller temperature both strongly affect wafer temperature
  - ~ 17% of RF power is delivered as heat to wafer in this etcher
  - With He backside cooling, this heats the wafer ~ 3°C/100 W



C. Gabriel, J. Vac. Sci. Technol. B, **20** (4), Jul/Aug 2002, 1542

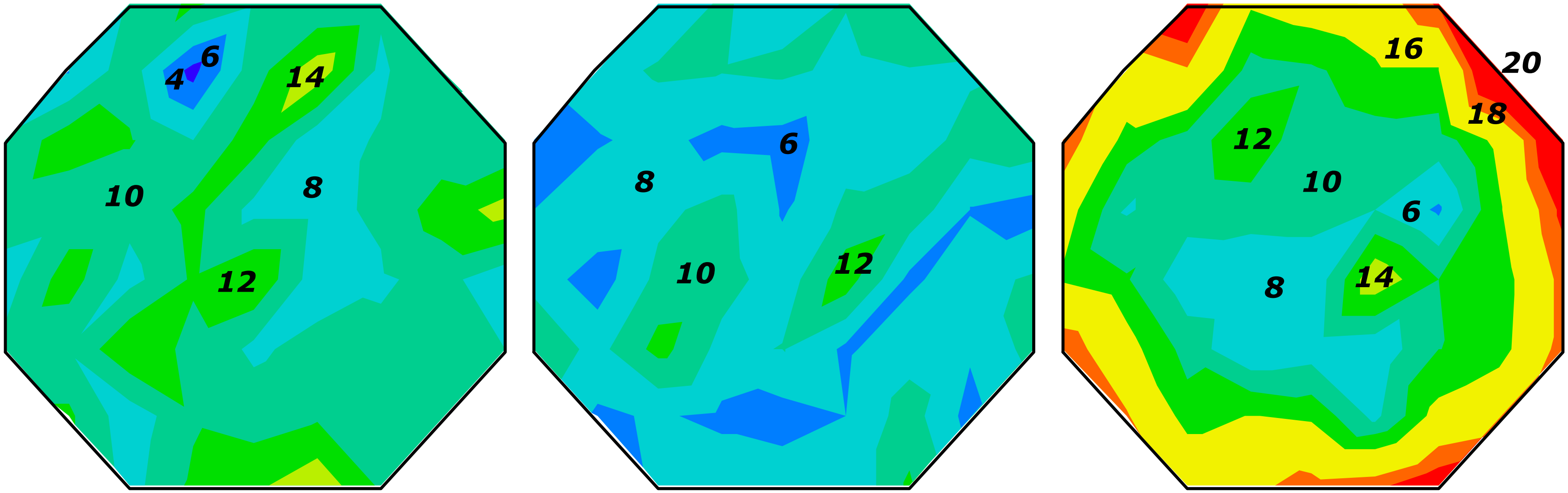




LER contour plots

- 60 LER measurement sites per wafer; 10 mm edge exclusion
- Before/after etch patterns look similar—diagonal contours
- No strong center-to-edge pattern except after etching at 0°C
- Contour plots (same scale, labels are LER in nm):

Before etch **After etch (25°C)** **After etch (0°C)**

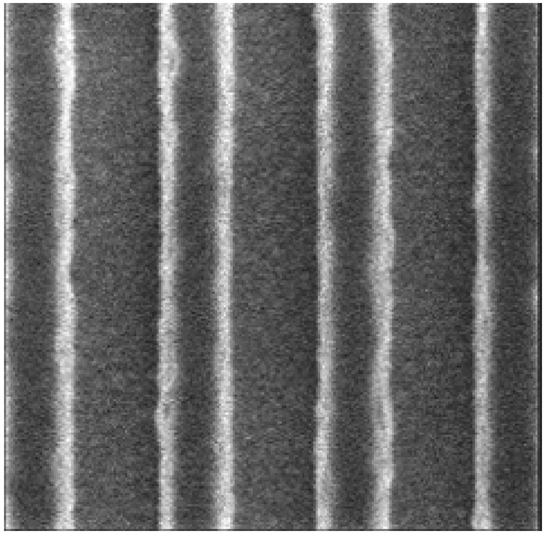


Improved damascene trenches

- Applying this understanding resulted in a 50% reduction in LER after damascene trench etching—with almost no impact on throughput and selectivity
- Further improvements are in progress to meet ITRS roadmap

Before etch

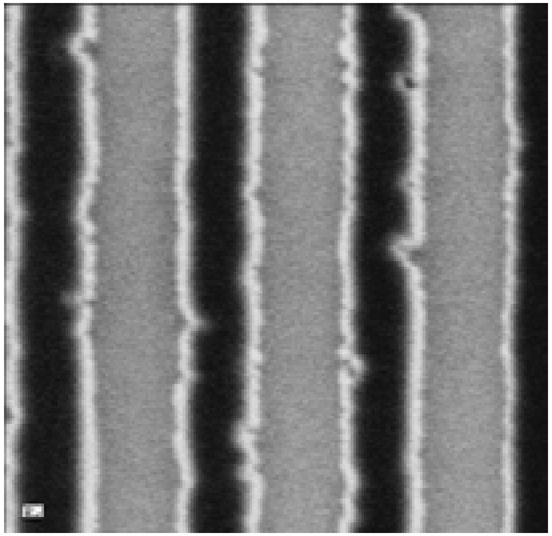
LER = 10.0 nm



Original etch

(optimized for 248 nm resist)

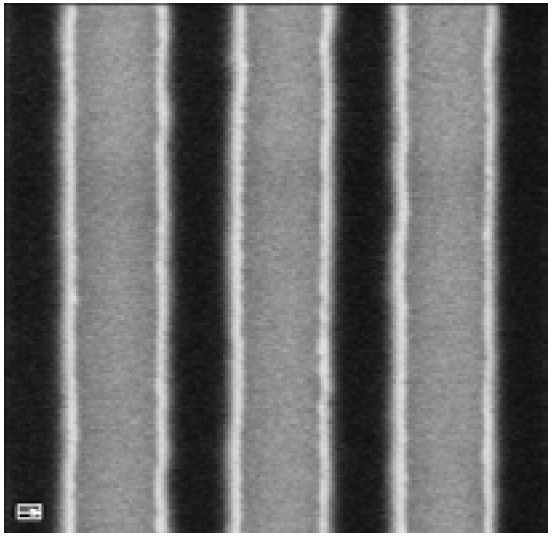
LER = 17.2 nm



Improved etch

(optimized for 193 nm resist)

LER = 8.3 nm



Conclusions

- Line edge roughness is a common and potentially serious problem when patterning 193 nm photoresist
- LER can be quantified using a CD-SEM tool—the section of line being scanned needs to be sufficiently long for consistent LER measurements
- Both lithography and plasma etching play a role in LER
  - Polymer aggregates in the resist cause it to be susceptible to roughening during both developing and etching
  - Both exposure and focus affect LER during lithography
  - During etching of a CVD low-k dielectric stack in an MERIE plasma etch system, the main parameters affecting LER are chiller temperature and rf power—LER is minimized at moderately low temperature and power

Acknowledgments

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