Line Edge Roughness Reduction for Advanced Metal Gate Etch with 193nm Lithography in a Silicon Decoupled Plasma Source Etcher (DPS II)

Tito Chowdhury, Harry Lee, Roni Khen, Hanna Bamnolker
Cypress Semiconductor, San Jose CA
Yan Du, Meihua Shen, Shashank Deshmukh, Jinhan Choi
Silicon Etch, Conductor Etch Division, Applied Materials, Santa Clara CA

Abstract

193nm lithography has become increasingly important as the critical dimensions of semiconductor devices continue to scale down towards sub 0.10um dimension. From dry etching perspective, however, 193nm resist brings new challenges due to its poorer plasma etch resistance, line edge roughness and lower thickness compared to 248nm DUV resist. Consequently, issues such as line edge roughness and poor profile control were observed after dry etch processing. This paper presents a successful development of advanced 0.1μm metal gate application using 193nm lithography on Applied Materials' decoupled plasma etcher DPSII system. The integrated process involves a hard mask open with ex-situ resist strip followed by metal/poly dual gate etching. Process chemistry and process parameters for nitride mask step were thoroughly explored and investigated. With CF4/CHF3 based chemistry, the process achieved a greater than 2:1 selectivity with straight nitride profile and smooth sidewall. Less than 7nm 3-sigma of CD bias uniformity was obtained across the wafer with edge exclusion up to 4mm on a 200mm substrate. Process parameters such as pressure, gas ratio and the total Fluorine-contained flow were proven to be the most influential on resist selectivity, profile and CD control. A careful balance needs to be maintained in order to deliver an overall process. The following W/WN/poly gate etch features a three-step approach that has produced straight profiles, excellent CD control and excellent gate oxide integrity. Post-etch measurement of line edge roughness shows an average of 5nm LER. It was observed LER is a strong function of etch chemistry, reaction regime etc. A detailed study showing methods to reduce LER is presented in this paper.