“Plasma Etching of Cobalt Silicide”

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High Temperature Plasma Etching of Cobalt Silicide

- Introduction
- Motivation: Etching versus Salidization
- Patents
- Dual Frequency HRe
- High Temperature Features:
  - High Temperature ESC
  - Wafer Temperature Control
- High Temperature Processing
- Conclusions
Why Cobalt Silicide?

- Used as Gate Electrode Material above the poly
- Low Resistivity - faster devices
- Ease of Post-Gate Integration
- Can handle high-power
- Most of this talk is on fairly large geometries for Wireless devices; end of talk shows results at 0.15 and 0.18 uM
Usual Process Flow is Salidization

- A thicker Poly is etched
- Process flow continues through spacer formation
- Co is sputtered
- A light RTA is performed
- This reacts the Co with the poly - but not Co above oxide
- A chemical wet etch washes away unreacted Co
- A final RTA is performed to form the final CoSi
Advantages of Plasma Etch over Salidization

- Salidization is conceptually easier - do not have to do a “difficult” plasma etch.

- Cobalt-Salidization has two main problems:
  1) Problem of unreacted material not being removed where it is desired (leads to yield/reliability defects)
  2) Problem of divots of reacted material being removed where it should stay (leads to variability in conductivity - device performance is decreased).
Literature Search/Prior Art

- There had only been academic studies of plasma etching of CoSi customized research tools.
- There was no established process/ prior art to plasma etching CoSi.
- Thus any discoveries are patentable.
High Temperature Plasma Etching of Cobalt Silicide: Tegal Patents

- Tegal has made a significant effort to enable and optimize this etch and has protected our investment.
- Also patents on dual frequency and “Wafer Temperature Control” (TM)
**Tegal HRe™ Plasma Technology**

**Very low bias power**
High selectivity to oxides
Controlled anisotropy

**Moderate bias power**
Minimized loading effects

**High bias power**
Chemically assisted physical etch
Improved volatility for metals oxides

<table>
<thead>
<tr>
<th>6510</th>
<th>6520</th>
<th>6540</th>
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</table>
| Shallow silicon trench etch  
Selective polysilicon gate etch  
Selective W or Co silicide etch  
Selective LOCOS nitride etch  
Selective nitride spacer etch | Compound semiconductors  
Aluminum interconnect  
Thick aluminum etch | Pt, Ir/IrO₂, Ru/RuO₂ electrode etch  
PZT and Y-1 (SBT) ferroelectric etch  
BST high-k dielectric etch  
Gold interconnect etch |
Why not Inductively Coupled?

- Tegal sells an ICP system - 6550 for MRAM and Thin Film Head Applications.
- We do not recommend this approach where the etch byproduct is not volatile at “standard” temperatures and that byproduct is conductive.
- When the conductive byproduct gets deposited on the window then it attenuates the RF power that gets coupled through the window.
- The deposit builds up thicker in the center typically, so there is a degradation of uniformity.
- *This effect can be significant after just 25 wafers.*
Research and Manufacturability Issues

• Process Stability
  – No Power Transfer Through Dielectric Window
    (Cobalt Conducting Film Attenuates Signal)
  – This is not an issue for volatile species like Al, Si.
  – This is an issue with involatile Cobalt.

• Process Capability
  – Low Pressures
  – High Densities
Temperature helps volatility

- Si Etching: SiCl$_4$ is volatile at 58°C (1 atm.)
- W Etching: WF$_6$ is volatile at 17°C (1 atm.)
- Ti Etching: TiCl$_4$ is volatile at 136°C (1 atm.)
- PbZrTi Etching: ZrCl$_4$ is volatile at ~ 350°C (plasma conditions)
- Co Etching: CoCl$_4$ is volatile at ~ 200°C (plasma conditions)
High Temperature ESC Features

- Jonsen-Rahbek ESC Design Accommodates Any Material or Wafer Backside
- Tegal Patented Auto-Clamp Assures Each Wafer is Optimally Clamped
- Wide Operating Range: 200 °C -> 500 °C
- Self-Calibrating Backside Wafer Temperature Sensing in addition to Chuck Temperature Sensing.
- Tegal patented *Wafer Temperature Control (TM)* Assures Controlled Wafer Temperature.
- Wafer Temperature is a Process Recipe parameter.
- We get good results for CoSi with a water cooled chuck using wafer temperature control.
Wafer Temperature Control: FeRAM Example
JDP with STMicroelectronics

- We are just concluding a 15 month Joint Development Project with STM in Italy.
- This development occurred on Tegal etchers installed at STM.
- A Tegal process engineer participated in the JDP on “hard-to-etch” materials. These included:
  - Ni
  - Ferroelectric Materials
  - SiC
  - CoSi
- Joint publications are a part of this JDP.
Plasma Etching of *Hard-to-Etch Materials*

G. Arena, C. Tringali, P. Vasquez (STMicroelectronics)
G. Beique, S. Marks (TEGAL Corp.)
In the Int.l Technology Roadmap of Semiconductors is reported that new materials for gate conductors, interconnect, DRAM capacitors and dielectrics play a key role to advancing beyond the future technology nodes. 

*The Roadmap states that etching of these materials requires entirely new technologies and approaches, better controls of deposition in the etch chamber and optimum of chamber cleaning procedures.*

**Main Etch Requirements:**
The etching gases are chosen in order to produce species that chemically react with the material to be etched to form volatile reaction products (by-products). These spontaneously desorb from the surface into the plasma phase, where it is removed by the vacuum system.

**Key Requirement is the etch by-products volatility**
ITRS - Front End Processes

Thin Films Potential Solutions

**CoSi**

DRAM Stacked capacitor potential solution

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<td>Technology Node</td>
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<td>100nm</td>
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<td>45nm</td>
<td>40nm</td>
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<td>40nm</td>
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<td>PVD, CSD, MOCVD</td>
<td>PVD, CSD, MOCVD</td>
<td>MOCVD, New Methods</td>
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FeRAM Potential Solutions

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<th>Technology Node</th>
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<th>65 nm</th>
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<th>32 nm</th>
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<td>Upper Electrode</td>
<td>metal</td>
<td>metal</td>
<td>metal</td>
<td>metal</td>
<td>metal</td>
<td>metal</td>
<td>metal</td>
</tr>
<tr>
<td>High x dielectric</td>
<td>ON</td>
<td>TiOx, Al2Ox</td>
<td>TiOx, Al2Ox</td>
<td>BST, STO</td>
<td>BST, STO</td>
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<tr>
<td>Bottom Electrode</td>
<td>poly-Si</td>
<td>metal</td>
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<td>metal</td>
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</table>

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(page 35, figure 32)

(page 26, figure 29)
Cobalt Silicide / Poly Etch
Cobalt Silicide Etching Issues

- Cobalt Silicide is a very promising material for the gate electrode formation. However, one of the main issues in the integration of CoSi$_2$ is the dry etching process of this material.

- Typically plasma RIE etchers do not allow to completely etch this material, due to the inherent low volatility of the cobalt etch by-products (i.e. CoCl$_x$), that causes increasing of cobalt concentration in the silicide layer during the etch (F. Fracassi et al - J. Electrochem. Soc. Vol. 143 No. 2 Feb 1996) and leads to metal residuals on the wafer surface (micromasking effects).

- This requires a different etching approach.
Cobalt Silicide Etching Chemistry

<table>
<thead>
<tr>
<th>Plasma Chemistry</th>
<th>CoSi$_2$ Etch Rate [Å/min]</th>
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<tbody>
<tr>
<td>CF$_4$ (100%)</td>
<td>22</td>
</tr>
<tr>
<td>Cl$_2$ (100%)</td>
<td>750</td>
</tr>
<tr>
<td>Br$_2$ (100%)</td>
<td>0</td>
</tr>
<tr>
<td>I$_2$ (100%)</td>
<td>0</td>
</tr>
<tr>
<td>CO(100%)</td>
<td>6</td>
</tr>
<tr>
<td>CO/CF$_4$ (20%/80%)</td>
<td>20</td>
</tr>
<tr>
<td>CO / Cl$_2$ (20%/80%)</td>
<td>40</td>
</tr>
<tr>
<td>CF$_4$ / O$_2$ (10% / 90%)</td>
<td>20</td>
</tr>
<tr>
<td>Ar (100%)</td>
<td>11</td>
</tr>
</tbody>
</table>

- Using a 100% Cl$_2$ plasma an appreciable ER has been achieved
- Using other plasma compositions ER values were very poor
- Using the Cl$_2$ plasma and reducing the bias from -500V to -100V the CoSi2 ER was negligible.

(BIAS Value -500V)
No.2 Feb 1996

**Approach:**
To use the TEGAL reactor with a 100% chlorine chemistry

G. Arena  
DSG - Catania R&D Photo & Etch Development Group
Cobalt Silicide Etch Process Trends: RF Power & Pressure

- Increasing Source Power a linear ER increase was observed.
- Increasing the bias power the etch rate is increased too.
- Increasing pressure CoSi$_2$ etch rate decreases and etch non-uniformity increases up to 10%
Cobalt Silicide Etch Process Trends: Wafer Temperature

Etching temperature Vs. CoSi2 etch profile

Best result

Temperature [°C]

Etch profile [degree]
## Cobalt Silicide Final Etch Process

### Process Parameters

<table>
<thead>
<tr>
<th>ITEM</th>
<th>VALUE</th>
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</thead>
<tbody>
<tr>
<td>Etch rate [A/min]</td>
<td>2070</td>
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<tr>
<td>Etch Non-Uniformity</td>
<td>4.8%</td>
</tr>
<tr>
<td>Etch Profile</td>
<td>87°</td>
</tr>
<tr>
<td>CD variation [µm]</td>
<td>+0.02</td>
</tr>
<tr>
<td>HM loss [Å]</td>
<td>800</td>
</tr>
<tr>
<td>CoSi2 : poly selectivity</td>
<td>0.5 :1</td>
</tr>
</tbody>
</table>

**CoSi₂**

<table>
<thead>
<tr>
<th>ITEM</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etch rate [A/min]</td>
<td>1448</td>
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<tr>
<td>Etch Non-Uniformity</td>
<td>2.3%</td>
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<tr>
<td>Etch Profile</td>
<td>87°</td>
</tr>
<tr>
<td>CD variation [µm]</td>
<td>+0.01</td>
</tr>
<tr>
<td>Substrate (oxide) loss [Å]</td>
<td>50</td>
</tr>
<tr>
<td>poly : oxide selectivity</td>
<td>130 :1</td>
</tr>
<tr>
<td>Total etch profile</td>
<td>87° Continuous, no bowing or undercut</td>
</tr>
</tbody>
</table>

**Poly**

### X-TEM of the APCVD oxide/CoSi2/Poly stack

- APCVD oxide
- CoSi₂
- Poly

0.5 µm
Cobalt Silicide Final Etch Process

- Good etch profile
- CD variation < 0.05 µm
- Low substrate loss (<30 Å)
Other samples

- Customer(s) provided wafers.
- Customer(s) opened hard mask.
- At 0.18 uM, there was a polymeric residue on top before etch and after etch - but no microloading at all was observed.
- At 0.15 uM, there was a very sloped mask, but steep CoSi profile.
Another Customer 0.15μM - No u-loading
Customer 3 - sloped oxide mask
86 degree Profile 0.18 μM features
Conclusions

- Combining the successful Dual Frequency HRe-Approach with High Temperature (patented) results in enhanced CoSi etch capability at least to the 0.15 Micron regime.
- Agile Temperature Control allows separate processing temperatures for Silicide and Poly.
- Process is stable because the issue of a conducting non-volatile film obstructing the RF power transmission is not an issue.