"Plasma Etching of Cobalt Silicide"

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High Temperature Plasma Etching of Cobalt Silicide

- Introduction
- Motivation: Etching versus Salidization
- Patents
- Dual Frequency HRe^{-}
- High Temperature Features:
  - High Temperature ESC
  - Wafer Temperature Control
- High Temperature Processing
- Conclusions

Why Cobalt Silicide?

- Used as Gate Electrode Material above the poly
- Low Resistivity - faster devices
- Ease of Post-Gate Integration
- Can handle high-power
- Most of this talk is on fairly large geometries for Wireless devices; end of talk shows results at 0.15 and 0.18 uM

Usual Process Flow is Salidization

- A thicker Poly is etched
- Process flow continues through spacer formation
- Co is sputtered
- A light RTA is performed
- This reacts the Co with the poly - but not Co above oxide
- A chemical wet etch washes away unreacted Co
- A final RTA is performed to form the final CoSi

Advantages of Plasma Etch over Salidization

- Salidization is conceptually easier - do not have to do a "difficult" plasma etch.
- Cobalt-Salidization has two main problems:

  1) Problem of unreacted material not being removed where it is desired (leads to yield/reliability defects)

  2) Problem of divots of reacted material being removed where it should stay (leads to variability in conductivity - device performance is decreased).

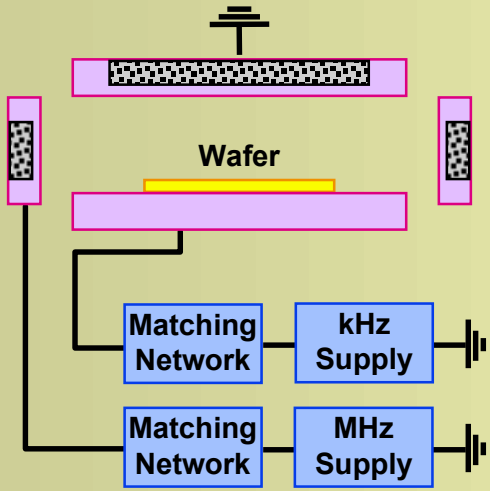
Literature Search/Prior Art

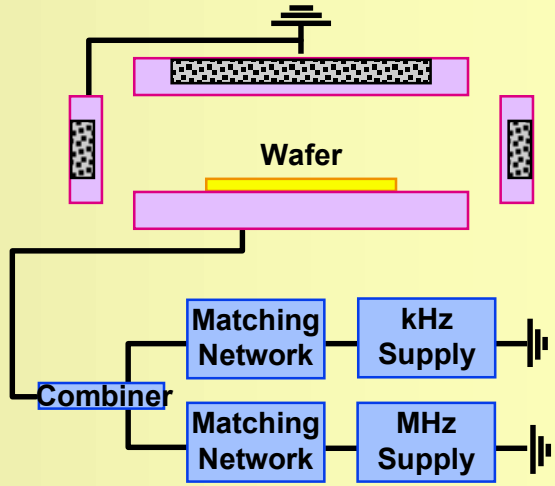
- There had only been academic studies of plasma etching of CoSi customized research tools.
- There was no established process/ prior art to plasma etching CoSi.
- Thus any discoveries are patentable.

High Temperature Plasma Etching of Cobalt Silicide: Tegal Patents

- Tegal has made a significant effort to enable and optimize this etch and has protected our investment.
- US Patent 6,391,148 B2: "Cobalt Silicide Etch Process and Apparatus" (2002) Marks, Jerde, DeOrnellas (assigned to Tegal).
- World Patent WO 01/41189 A2: "Cobalt Silicide Etch Process and Apparatus" (2001) Marks, Jerde, DeOrnellas (assigned to Tegal).
- US Patent: "Silicide etching process and apparatus for etching silicide and other materials" (2001) Marks, Jerde, DeOrnellas (assigned to Tegal).
- Also patents on dual frequency and "Wafer Temperature Control" (TM)

Tegal HRe™ Plasma Technology





Very low bias power High selectivity to oxides Controlled anisotropy	Moderate bias power Minimized loading effects	High bias power Chemically assisted physical etch Improved volatility for metals oxides
6510	6520	6540
Shallow silicon trench etch Selective polysilicon gate etch Selective W or Co silicide etch Selective LOCOS nitride etch Selective nitride spacer etch	Compound semiconductors Aluminum interconnect Thick aluminum etch	Pt, Ir/IrO_2 , Ru/RuO_2 electrode etch PZT and Y-1 (SBT) ferroelectric etch BST high-k dielectric etch Gold interconnect etch

Why not Inductively Coupled?

- Tegal sells an ICP system - 6550 for MRAM and Thin Film Head Applications.
- We do not recommend this approach where the etch byproduct is not volatile at "standard" temperatures and that byproduct is conductive.
- When the conductive byproduct gets deposited on the window then it attenuates the RF power that gets coupled through the window.
- The deposit builds up thicker in the center typically, so there is a degradation of uniformity.
- *This effect can be significant after just 25 wafers.*

Research and Manufacturability Issues

- Process Stability
  - No Power Transfer Through Dielectric Window (Cobalt Conducting Film Attenuates Signal)
  - This is not an issue for volatile species like Al, Si.
  - This is an issue with involatile Cobalt.
- Process Capability
  - Low Pressures
  - High Densities

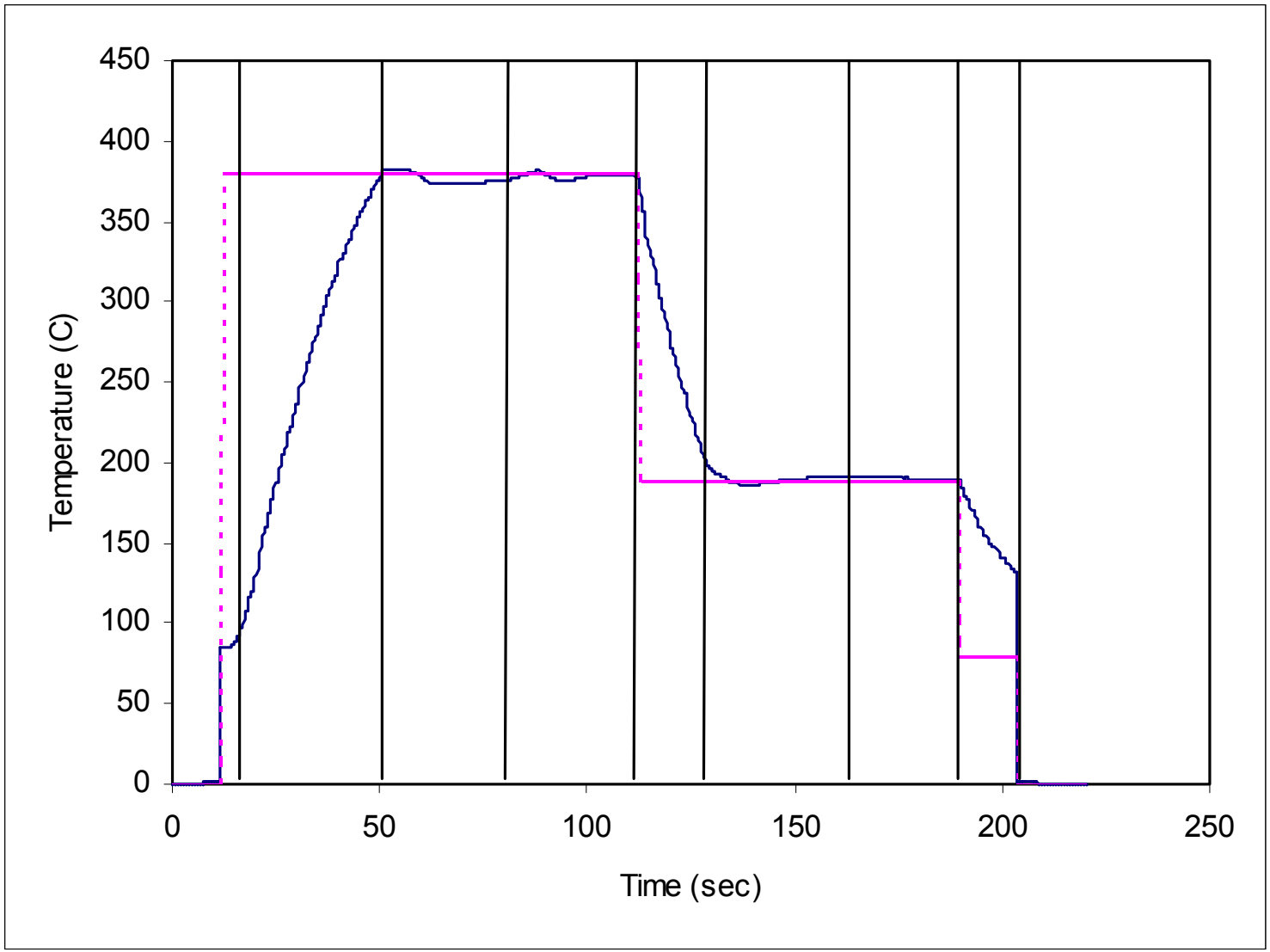
Temperature helps volatility

- Si Etching : $SiCl_4$ is volatile at 58°C (1 atm.)
- W Etching : WF_6 is volatile at 17°C (1 atm.)
- Ti Etching: $TiCl_4$ is volatile at 136°C (1 atm.)
- PbZrTi Etching : $ZrCl_4$ is volatile at ~ 350°C (plasma conditions)
- Co Etching : $CoCl_4$ is volatile at ~ 200°C (plasma conditions)

High Temperature ESC Features

- Jonsen-Rahbek ESC Design Accommodates Any Material or Wafer Backside
- Tegal Patented Auto-Clamp Assures Each Wafer is Optimally Clamped
- Wide Operating Range: 200 ^{o}C ->500 ^{o}C
- Self-Calibrating Backside Wafer Temperature Sensing in addition to Chuck Temperature Sensing.
- Tegal patented ***Wafer Temperature Control (TM)*** Assures Controlled Wafer Temperature.
- Wafer Temperature is a Process Recipe parameter.
- We get good results for CoSi with a water cooled chuck using wafer temperature control.

Wafer Temperature Control:FeRAM Example



JDP with STMicroelectronics

- We are just concluding a 15 month Joint Development Project with STM in Italy.
- This development occurred on Tegal etchers installed at STM.
- A Tegal process engineer participated in the JDP on "hard-to-etch" materials. These included:
  - Ni
  - Ferroelectric Materials
  - SiC
  - CoSi
- Joint publications are a part of this JDP.

DSG Catania R&D

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Plasma Etching of *Hard-to-Etch Materials*

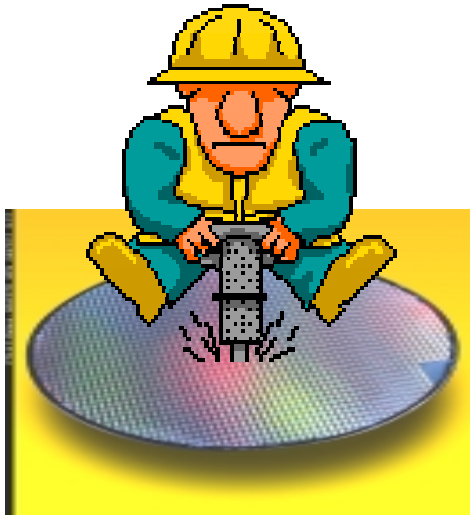
***G.Arena* ,C.Tringali , P.Vasquez (STMicroelectronics)**
G. Beique, S.Marks (TEGAL Corp.)

STMicroelectronics

Hard-to-etch Materials

In the Int.l Technology Roadmap of Semiconductors is reported that new materials for gate conductors, interconnect, DRAM capacitors and dielectrics play a key role to advancing beyond the future technology nodes

The Roadmap states that etching of these materials requires entirely new technologies and approaches, better controls of deposition in the etch chamber and optimum of chamber cleaning procedures



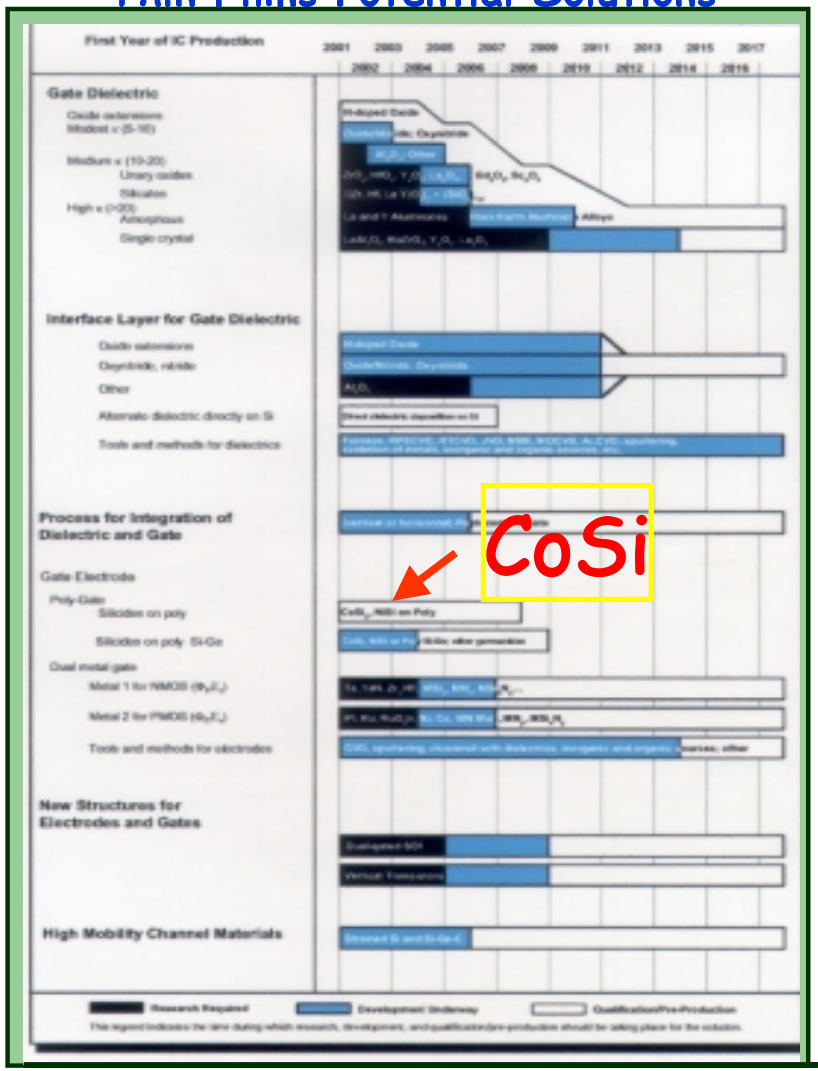
Main Etch Requirements:

The etching gases are chosen in order to produce species that chemically react with the material to be etched to form volatile reaction products (by-products). These spontaneously desorb from the surface into the plasma phase , where it is removed by the vacuum system.

Key Requirement is the etch by-products volatility

ITRS - Front End Processes

Thin Films Potential Solutions



(page 26 , figure 29)

DRAM Stacked capacitor potential solution

Year of First Product Shipment	2001	2002	2003			2007	2010	2013	2016
Technology Node	130nm	115nm	100nm	9 m	m	65nm	45nm	32nm	22nm
Ferroelectric Materials		PZT*, SBT				PZT, SBT, New Materials (BLT, etc.)			
Deposition Methods		PVD, CSD#		PVD, CSD, MOCVD		MOCVD, New Methods			

PZT

(page 32 , figure 31)

FeRAM Potential Solutions

Technology Node	130 nm	2002	2003	90 nm	2005	2006	65 nm	45 nm	2 nm	22 nm
Upper Electrode	metal									
High κ dielectric	ON	Ta_2O_5, Al_2O_3			BST, STO		Epi-BST			
Bottom Electrode	poly-Si	metal					perovskite			

BST

(page 35 , figure 32)

Cobalt Silicide / Poly Etch

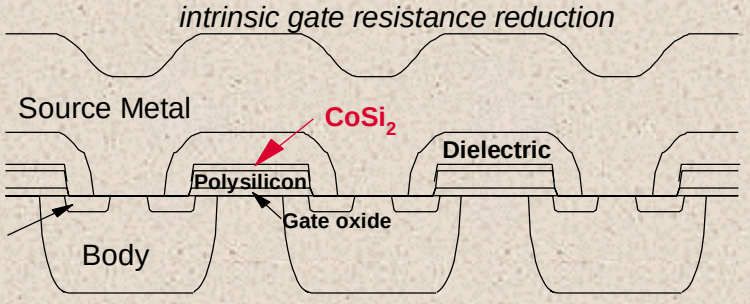
Cobalt Silicide Etching Issues

- Cobalt Silicide is a very promising material for the gate electrode formation. However, one of the main issues in the integration of $CoSi_2$ is the dry etching process of this material.

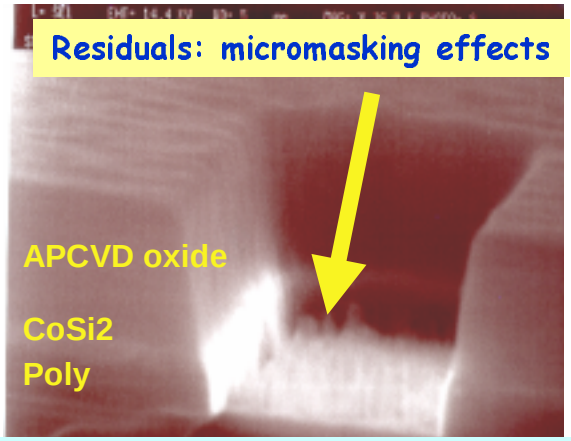
- Typically plasma RIE etchers do not allow to completely etch this material, due to the inherent low volatility of the cobalt etch by-products (i.e. CoClx), that causes increasing of cobalt concentration in the silicide layer during the etch (*F.Fracassi et al – J. Electrochem. Soc. Vol.143 No.2 Feb 1996*) and leads to metal residuals on the wafer surface (micromasking effects).

- This requires a different etching approach.

PowerMOSFETs structure with $CoSi_2$ Silicide.



US Patent 5,933,734



Standard Plasma RIE is not able to etch $CoSi_2$

Cobalt Silicide Etching Chemistry

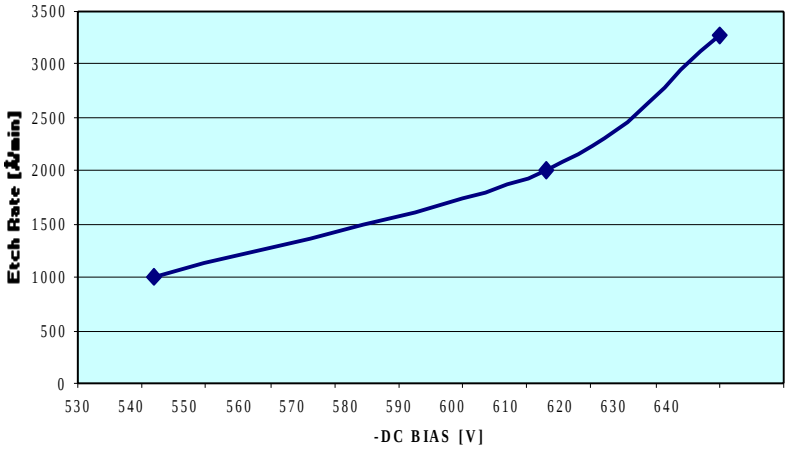
Plasma Chemistry	$CoSi_2$ Etche Rate [Å/min]
CF_4 (100%)	22
Cl_2 (100%)	750
Br_2 (100%)	0
I_2 (100%)	0
CO(100%)	6
CO/CF_4 (20%/80%)	20
CO / Cl_2 (20%/80%)	40
CF_4 / O_2 (10% / 90%)	20
Ar (100%)	11

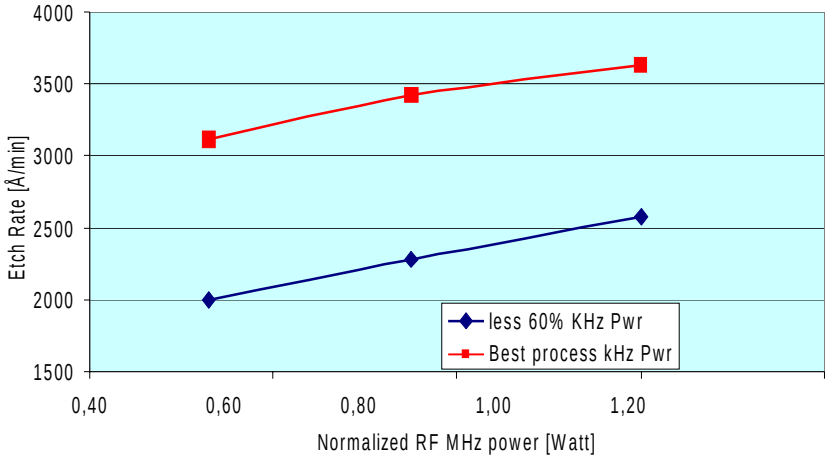
(BIAS Value -500V)
From : F.Fracassi et al – J. Electrochem. Soc. Vol.143 No.2 Feb 1996

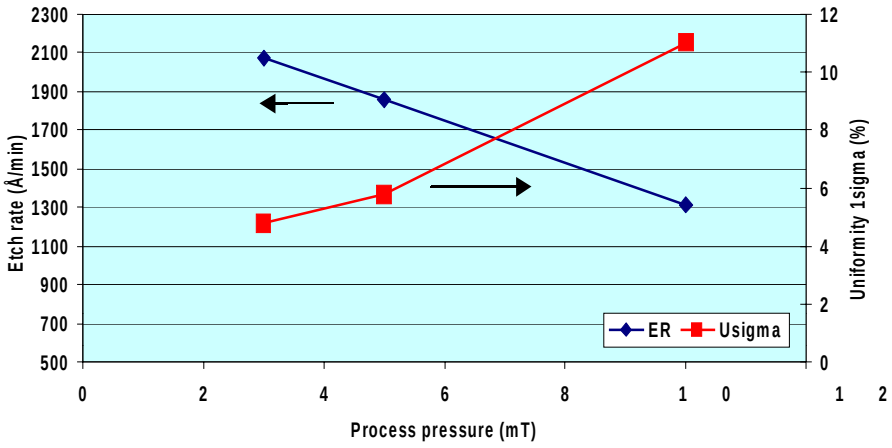
- Using a 100% Cl_2 plasma an appreciable ER has been achieved
- Using other plasma compositions ER values were very poor
- Using the Cl_2 plasma and reducing the bias from -500V to -100V the CoSi2 ER was negligible.

Approach:
To use the TEGAL reactor with a 100% chlorine chemistry

Cobalt Silicide Etch Process Trends: RF Power & Pressure

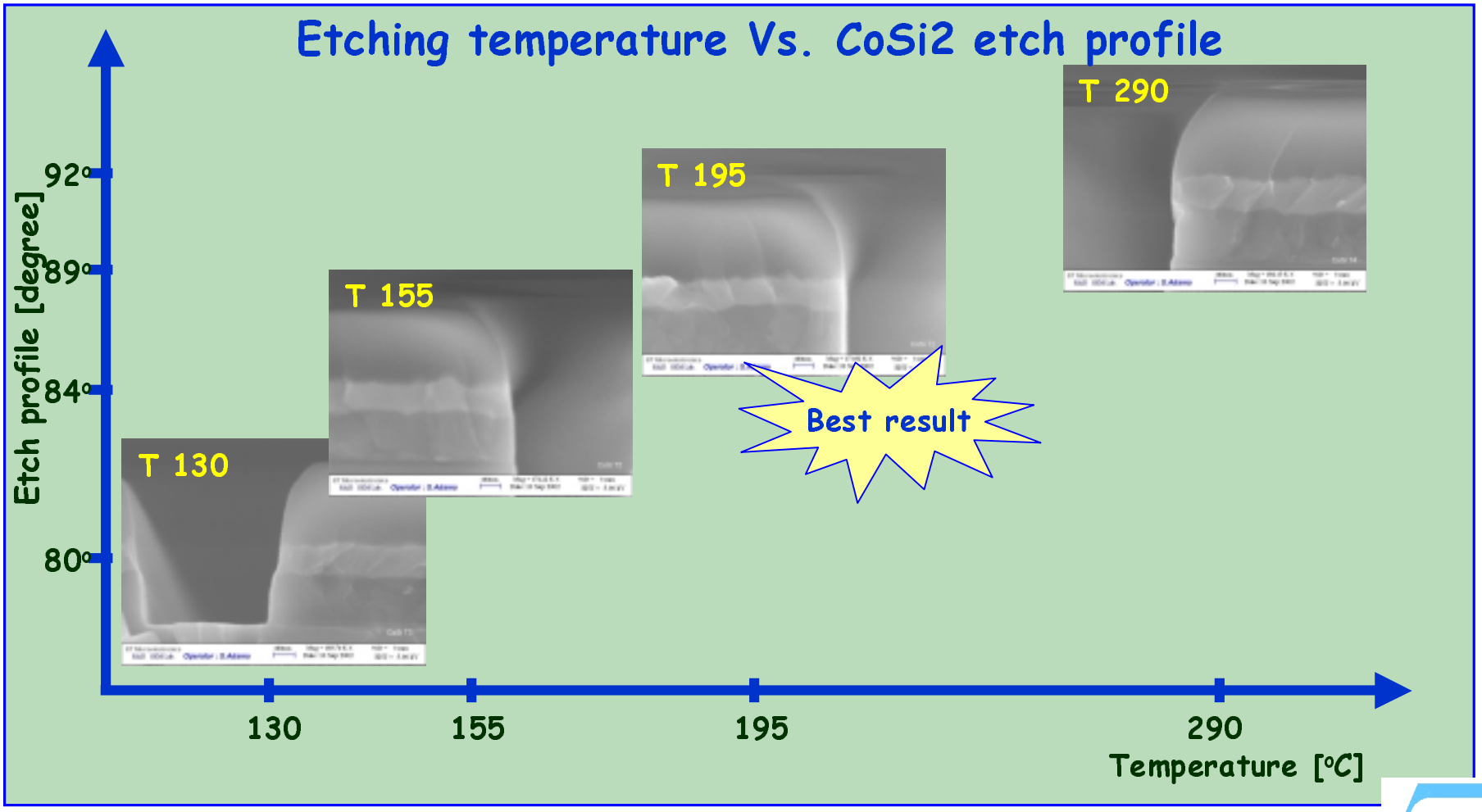






- Increasing Source Power a linear ER increase was observed.
- Increasing the bias power the etch rate is increased too
- Increasing pressure $CoSi_2$ etch rate decreases and etch non-uniformity increases up to 10%

Cobalt Silicide Etch Process Trends: Wafer Temperature

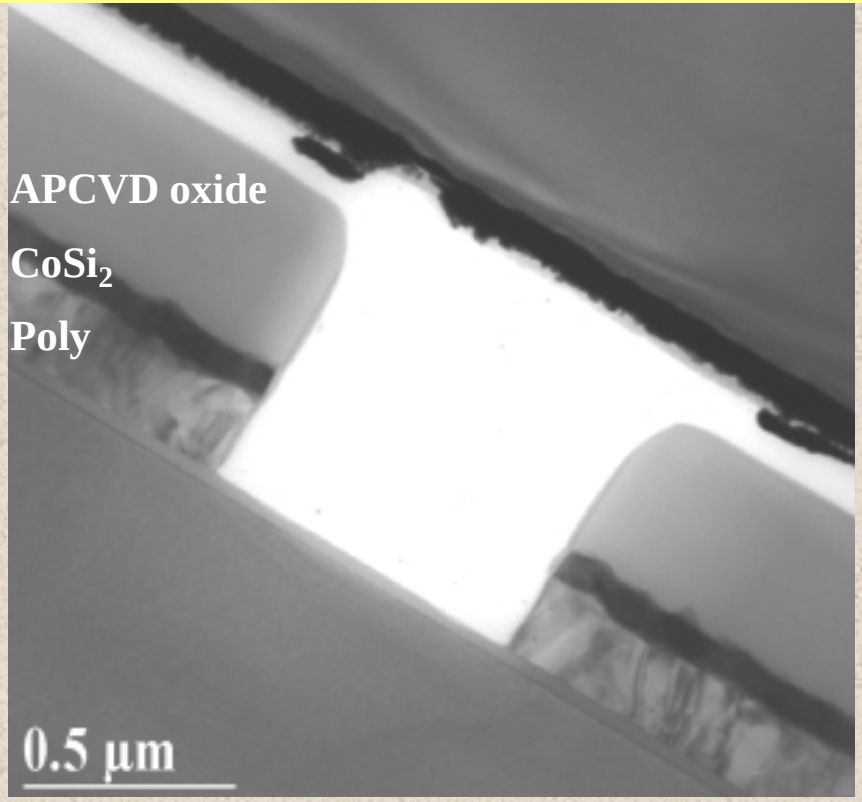


Cobalt Silicide Final Etch Process

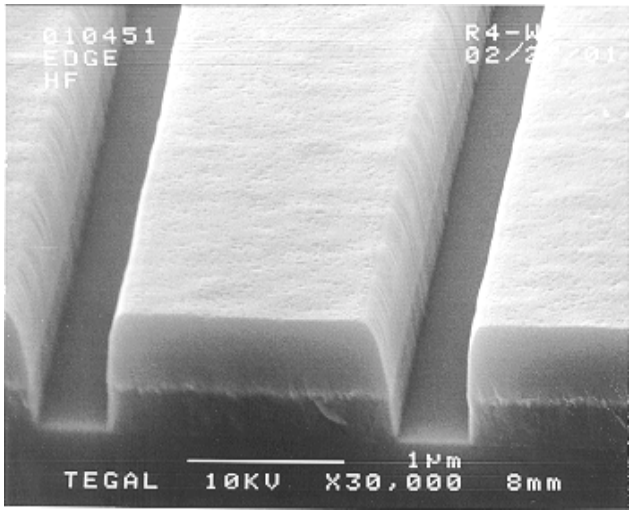
Process Parameters

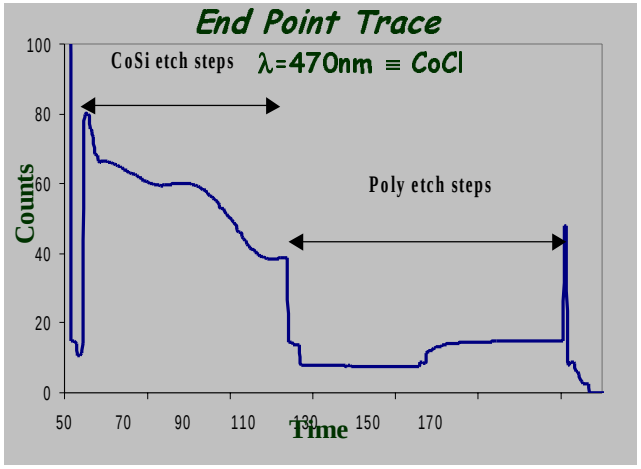
	ITEM	VALUE
$CoSi_2$	Etch rate [A/min]	2070
	Etch Non-Uniformity	4.8%
	Etch Profile	87°
	CD variation [µm]	+0.02
	HM loss [A]	800
	CoSi2 : poly selectivity	0.5 :1
Poly	Etch rate [A/min]	1448
	Etch Non-Uniformity	2.3%
	Etch Profile	87°
	CD variatio [µm]	+0.01
	Substrate (oxide) loss [A]	50
	poly : oxide selectivity	130 :1
Total etch	profile	87° Continuos , no bowing or undercut

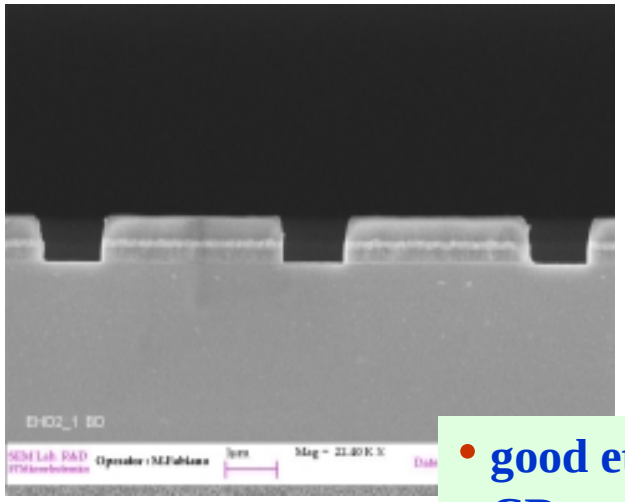
X-TEM of the APCVD oxide/CoSi2/Poly stack

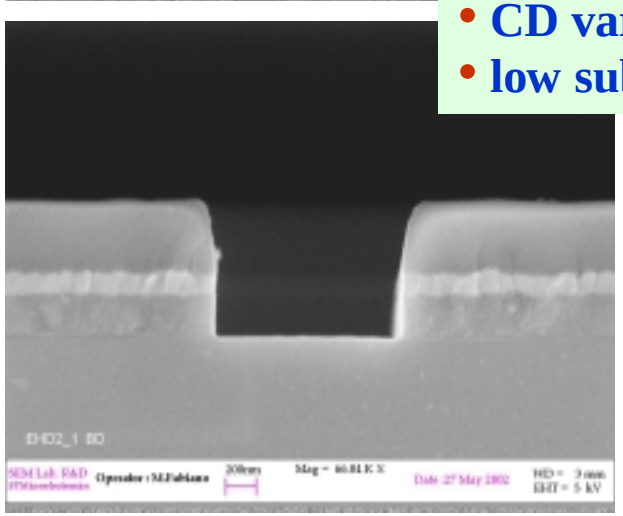


Cobalt Silicide Final Etch Process







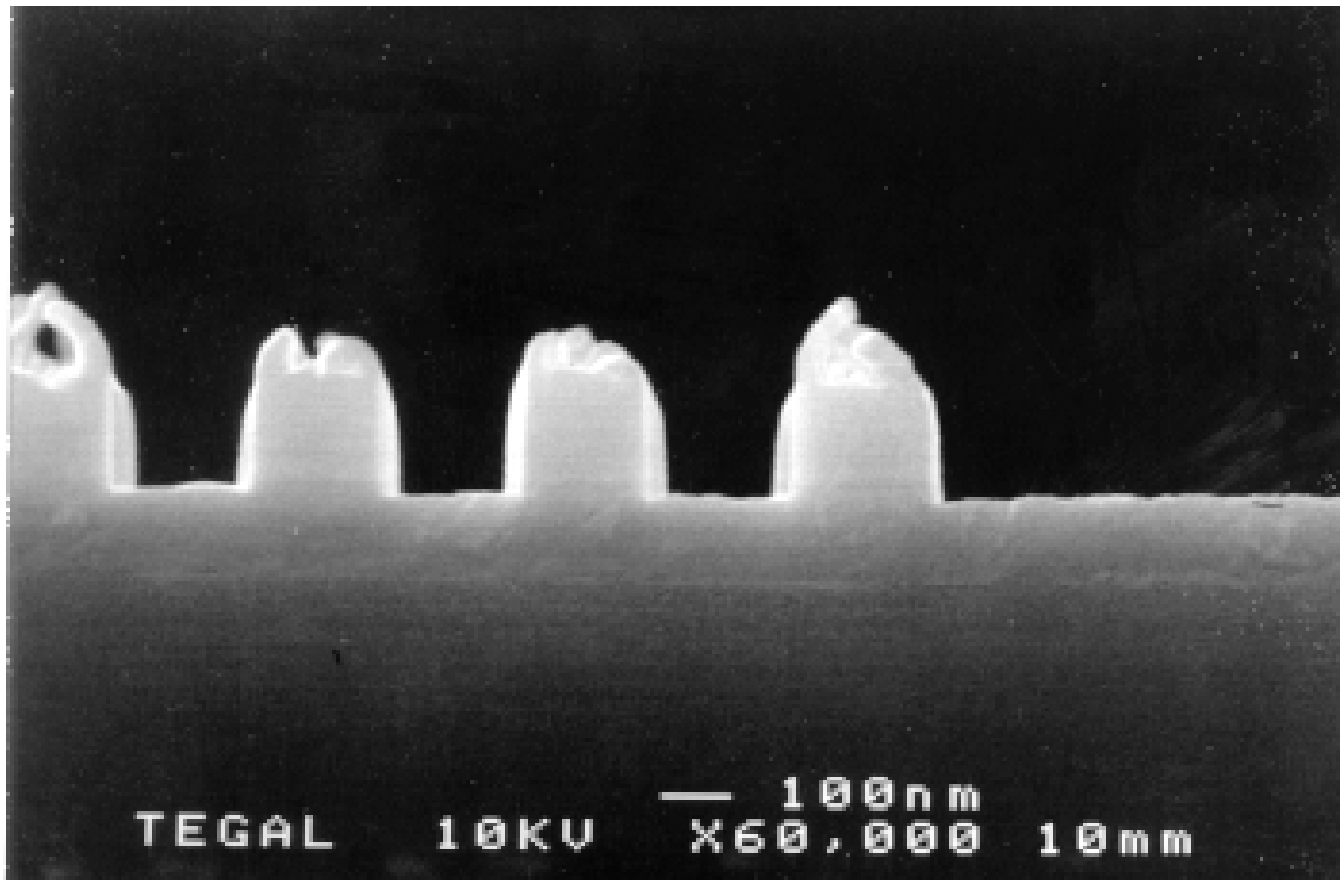


- good etch profile
- CD variation < 0.05µm
- low substrate loss (<30Å)

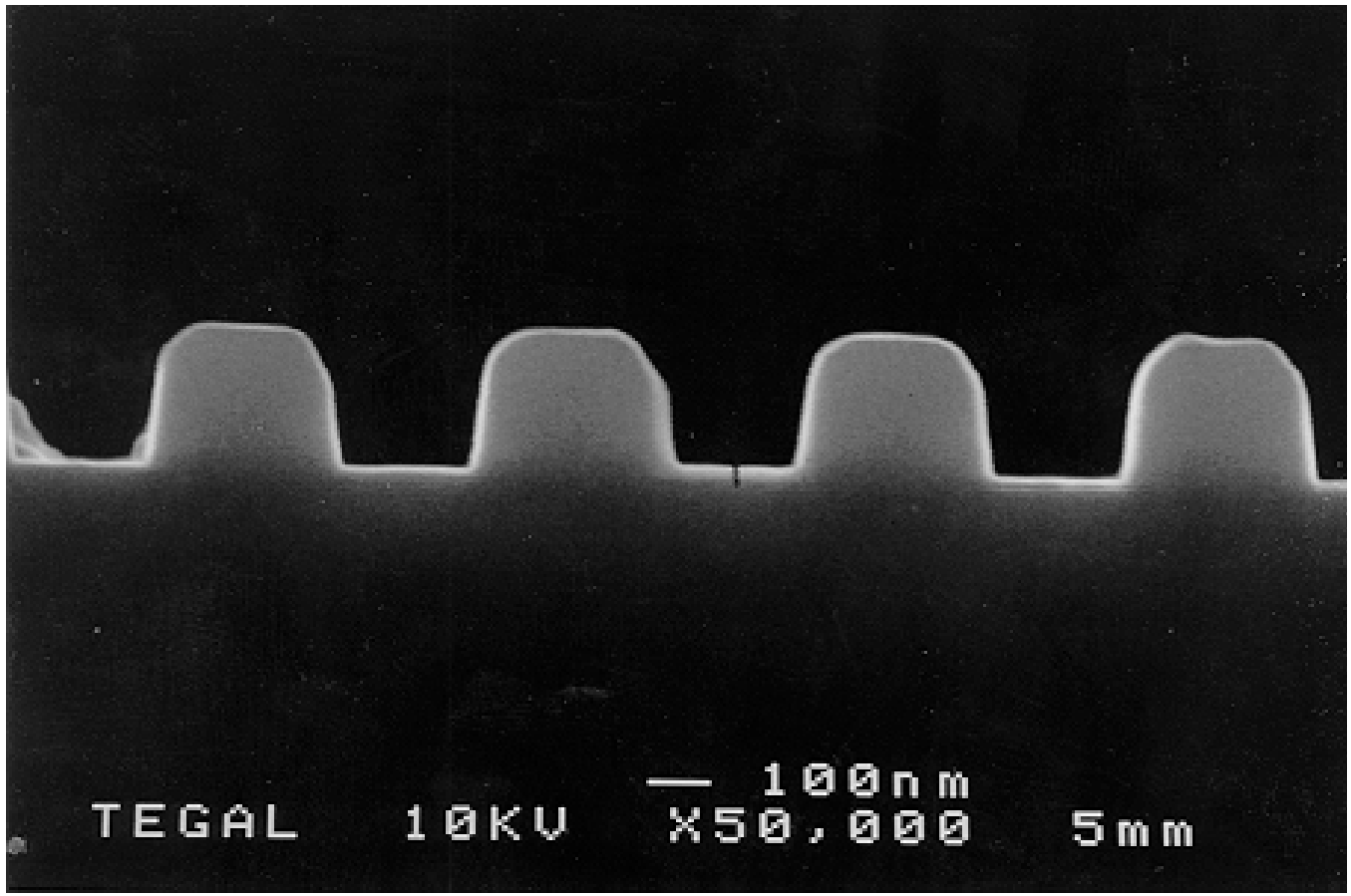
Other samples

- Customer(s) provided wafers.
- Customer(s) opened hard mask.
- At 0.18 uM, there was a polymeric residue on top before etch and after etch -but no microloading at all was observed.
- At 0.15 uM, there was a very sloped mask, but steep CoSi profile.

Another Customer 0.15uM - No u-loading



Customer 3 - sloped oxide mask
86 degree Profile 0.18 uM features



Conclusions

- Combining the successful Dual Frequency HRe-Approach with High Temperature (patented) results in enhanced CoSi etch capability at least to the 0.15 Micron regime.
- Agile Temperature Control allows separate processing temperatures for Silicide and Poly.
- Process is stable because the issue of a conducting non-volatile film obstructing the RF power transmission is not an issue.