MATERIAL ISSUES AND IMPACT ON RELIABILITY OF Cu/LOW k INTERCONNECTS

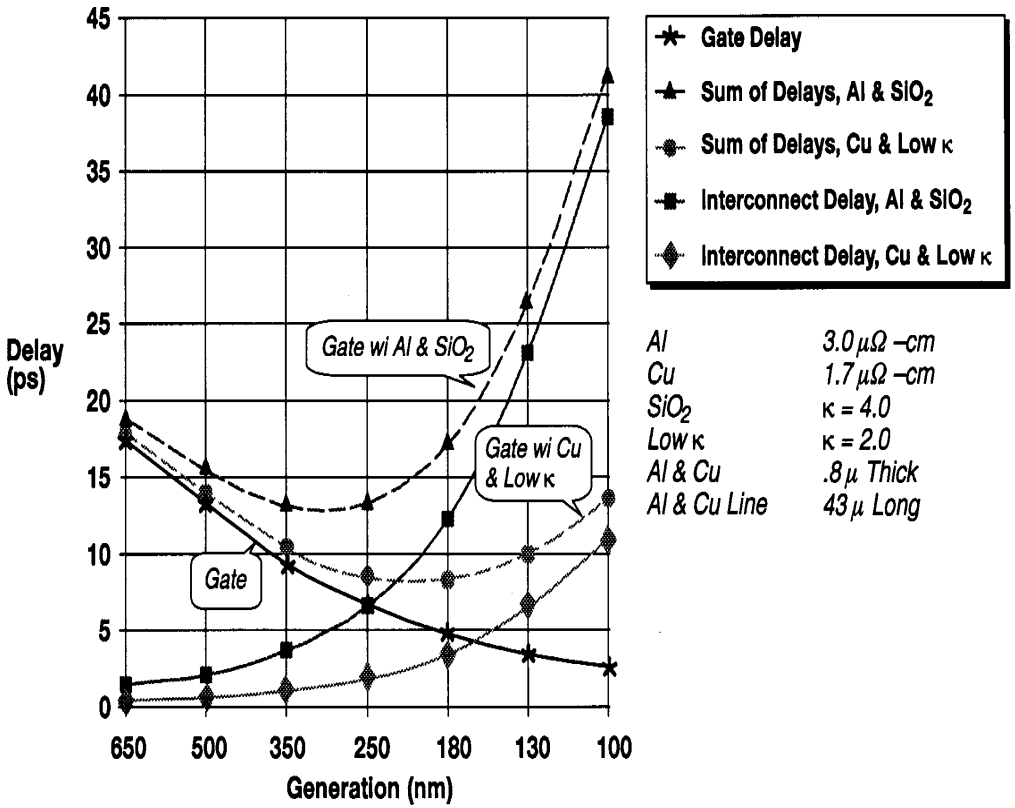
Paul S. Ho
Microelectronics Research Center
University of Texas at Austin

AVS Chapter 10/2002

- Technology challenges for low k dielectrics
- Chemical bond and polarizability
- Reliability of Cu/lowk interconnects
  - Thermal stresses
  - Electromigration
- Recent advance on reliability
- Summary

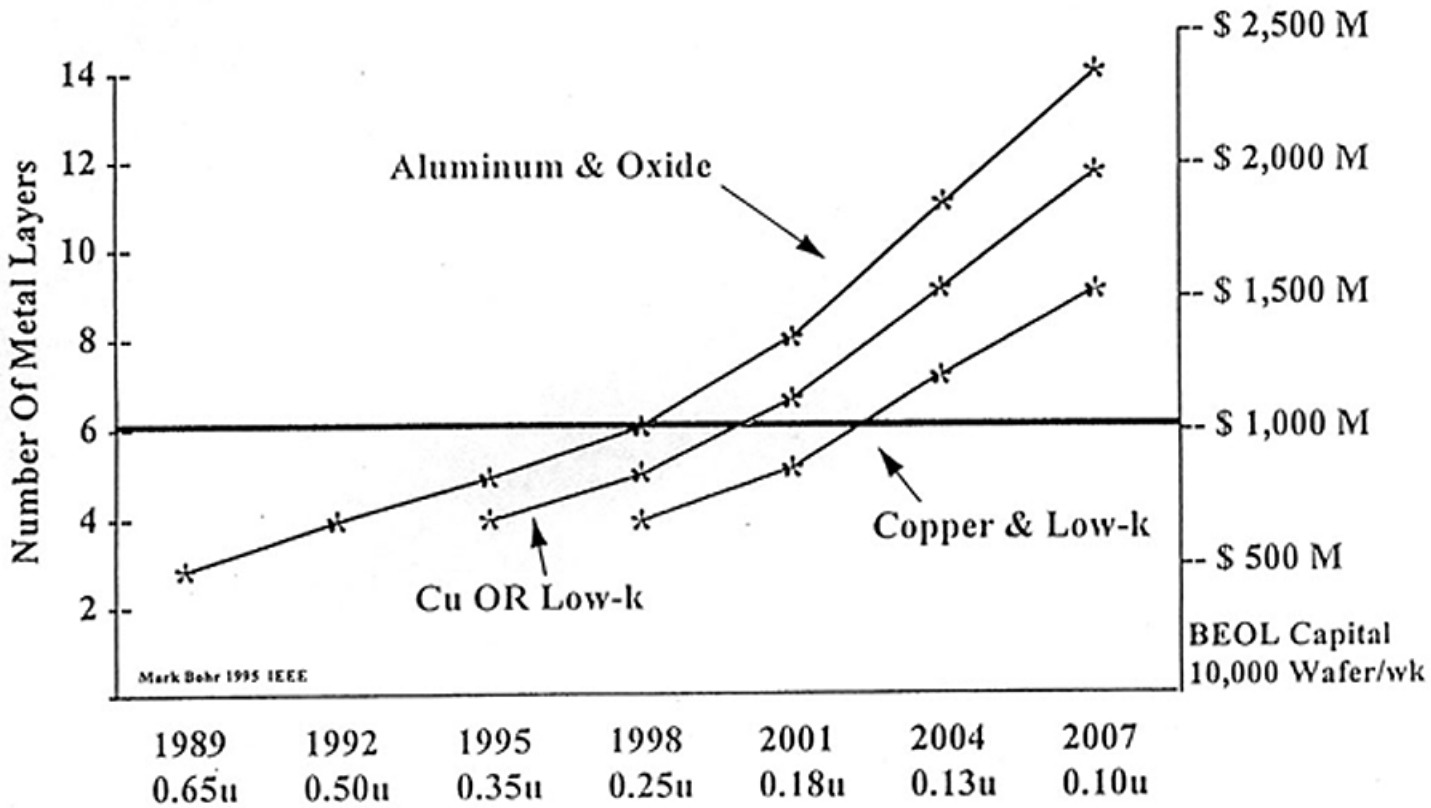
Effect of Scaling on Gate and Interconnect Delays

- Interconnect delay dominates IC speed
- Implementation of low k dielectrics reduces
  - RC delay
  - Power dissipation
  - Crosstalk noise
  - Number of metal level



Mark Bohr, IEEE IEDM Proc. 1995

Cost and Manufacturability Issue



Sematech 1998

Table 1: Technology Trends and the Need for Low-Dielectric Constant Materials

Year	1995	1998	2001	2004	2007
Feature Size (μm)	0.35	0.25	0.18	0.13	0.10
Metal Levels	4 - 5	5	5 - 6	6 - 7	7 - 8
Device Frequency (MHz)	200	350	500	750	1,000
Interconnect Length (m/chip)	380	840	2,100	4,100	6,300
Capacitance (fF/mm)	0.17	0.19	0.21	0.24	0.27
Resistance (metal1)(ohm/μm)	0.15	0.19	0.29	0.82	1.34
Dielectric Constant (*k*)	4.0	2.9	2.3	<2	2 - 1

- Based on the National Technology Roadmap for Semiconductors, 1994

Interconnect Technology Requirements for MPU

Year of introduction "Technology Node"	1999 180nm	2000	2001	2002 130nm	2003	2004	2005 100nm
MPU ½ pitch	230	210	180	160	145	130	115
Minimum metal effective resistivity (μΩ-cm) Al wiring*	3.3	3.3	3.3	3.3	3.3		
Minimum metal effective resistivity (μΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (conformal) (nm)	17	16	14	13	12	**11**	**10**
Interlevel metal insulator- effective dielectric constant (κ)	3.5-4.0	3.5-4.0	2.7-3.5	**2.7-3.5**	**2.2-2.7**	**2.2-2.7**	**1.6-2.2**

Solutions Exist
Solutions Being Pursued
No Known Solutions

International Technology Roadmap for Semiconductors, 1999

Interconnects Technology Requirements for MPU

Year of introduction "Technology Node"	2001 130nm	2002	2003	2004 130nm	2005	2006	2007 65nm
MPU ½ pitch	150	130	107	90	80	70	65
Minimum metal effective resistivity (μΩ-cm) Al wiring*	3.3	3.3					
Minimum metal effective resistivity (μΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (conformal) (nm)	16	14	12				
Interlevel metal insulator- effective dielectric constant (κ)	3.0-3.6	3.0-3.6	3.0-3.6				

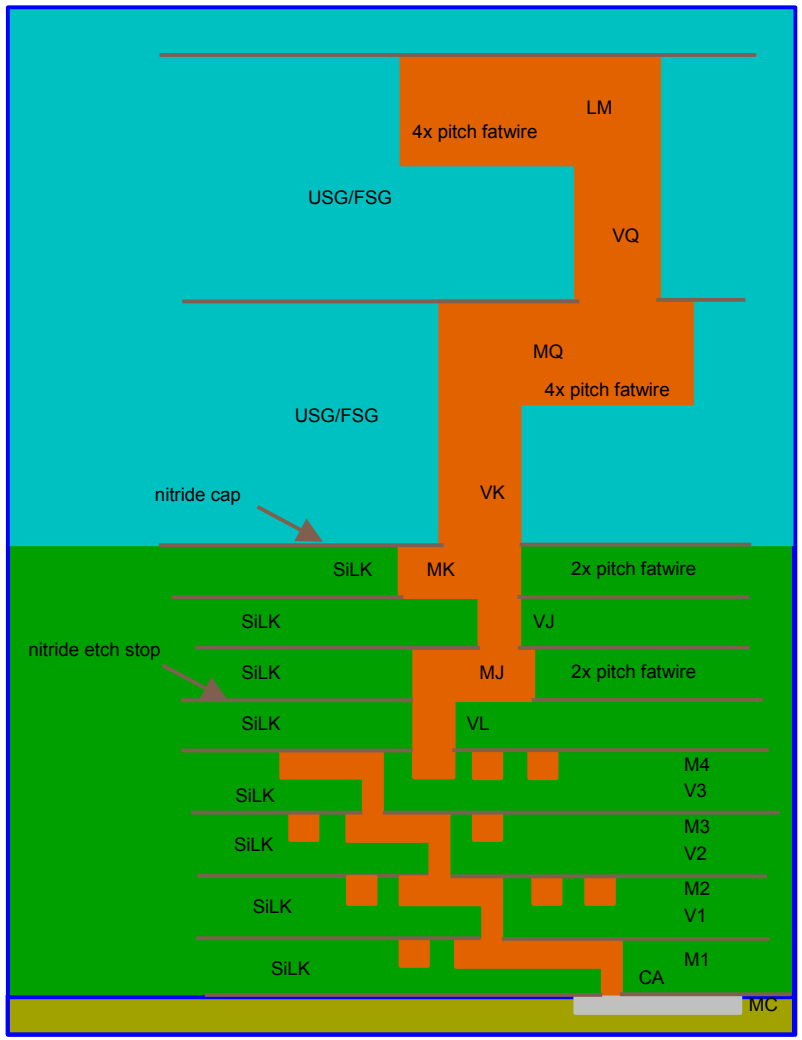
Solutions Exist
Manufacturing Solutions known
No Known Solutions

International Technology Roadmap for Semiconductors, 2001

IBM CMOS9S0 Technology

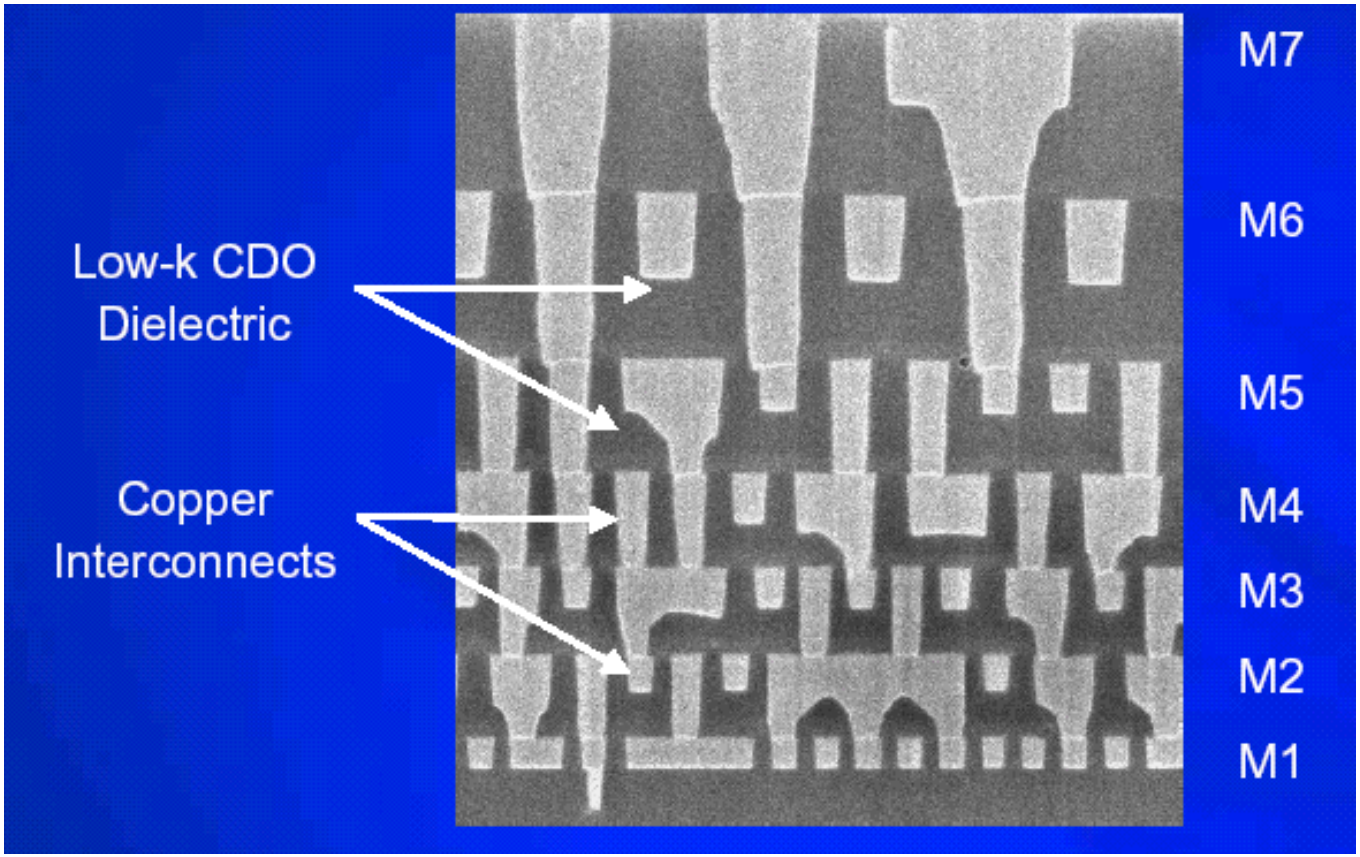
9S BEOL Stack
8 Level Metal
(4@1x, 2@2x, 2@4x)

	0.13 µm	0.18 µm
MDR shrink	0.25x	0.35x
Supply Voltage	1.2V	1.5V
Gate Length (drawn)	0.125 µm	0.175 µm
M1 pitch	0.35 µm	0.49 µm
M2 pitch	0.40 µm	0.63 µm
Mx pitch	0.45 µm	0.63 µm
2x pitch FW	0.90 µm	1.26 µm
4x pitch FW	1.80 µm	NA
Metal Levels	8	7
ILD	SiLK	USG/FSG
K_{eff}	3.0	4.0



R. Goldblatt et al., IITC 2000

Intel 90nm Interconnect Technology



7 metal levels on 300mm wafer
Low k CDO, capacitance by 18%
M. Bohr, Intel Developer Forum 9/2002

Contributions to Dielectric Constant

$$\varepsilon = 1 + 4\pi P/E$$

- Electronic polarizability

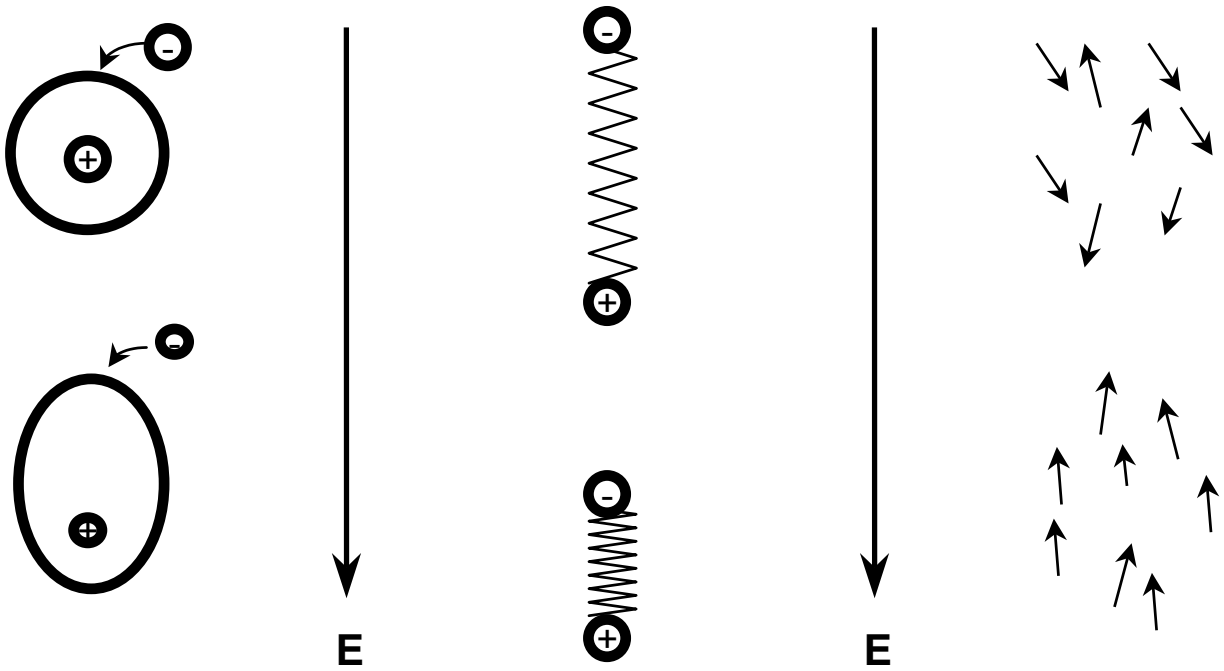
  optical frequency ($10^{14\text{-}15}$ S^{-1})
- Vibrational (atomic)

  IR ($10^{12\text{-}13}$ S^{-1})
- Rotational (orientation of permanent dipoles)

  microwave (10^{9} S^{-1})

Microscopic Origins of Polarization

3 Sources of Polarization



Electronic (Induced)

Visible -UV

Atomic (Induced)

Infrared

Orientational (Permanent)

μw - infrared

K. Taylor, IRPS Tutorial 2000

Basic Approaches to Reduce Dielectric Constant

- Optimization of molecular structure
  - Minimize configurational and dipole polarizability, e.g. use of C-C and C-F bonds
- Reduce density and incorporation of porosity
  - Add uniform and microscopic pores with k of 1
- Limitation: both approaches degrade the thermomechanical properties
  - Proper tradeoff of dielectric constant and thermomechanical properties important

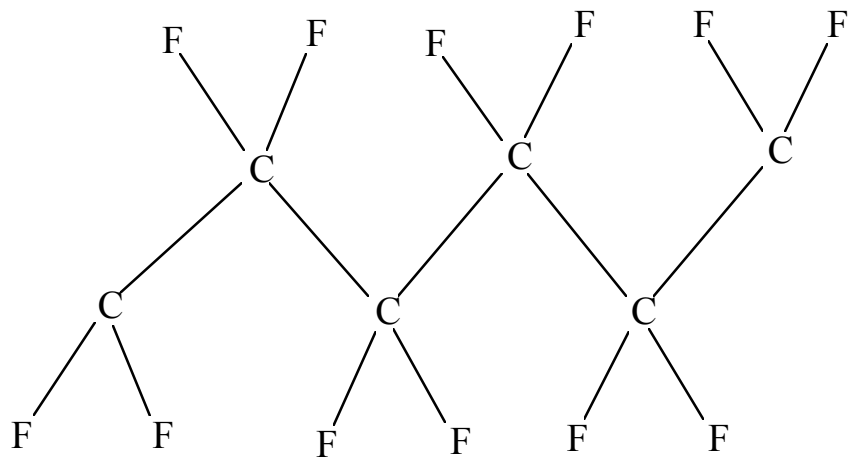
Electronic Polarizability vs. Strength of Chemical Bonds

Bond	*Polarizability* (angstrom^3)*	*Ave. Bond Energy# (Kcal/mole)*
C-C	0.531	83
C-F	0.555	116
C-O	0.584	84
C-H	0.652	99
O-H	0.706	102
C=O	1.020	176
C=C	1.643	146
C≡C	2.036	200
C≡N	2.239	213

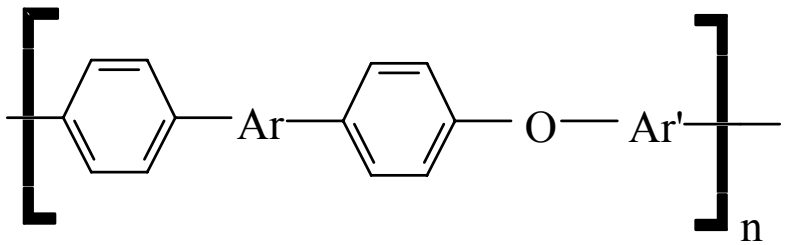
* J. Am. Chem. Soc. 1990, 112, p.8533.
# S. Pine, Organic Chemistry 5th ed.(1987).

PTFE: use of bonds with low polarizability

- very low k (~1.9)
- flexible chains limit thermomechanical stability:
  - small modulus
  - low tensile strength
  - low Tg
  - high CTE



Rigid-Polymer-Chain Dielectrics
Poly (aryl ether) -- more flexible than PI

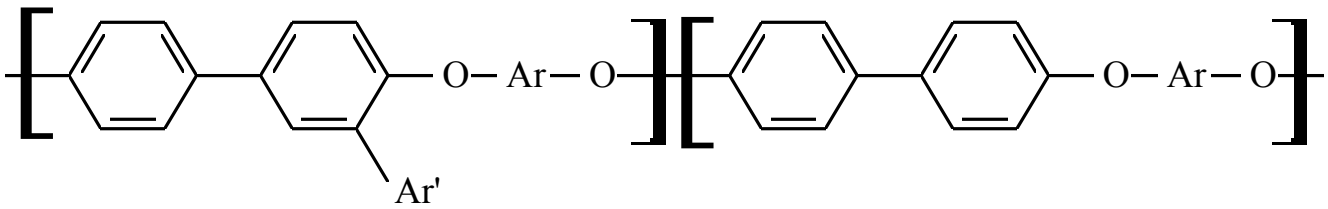


Compared to Polyimide:

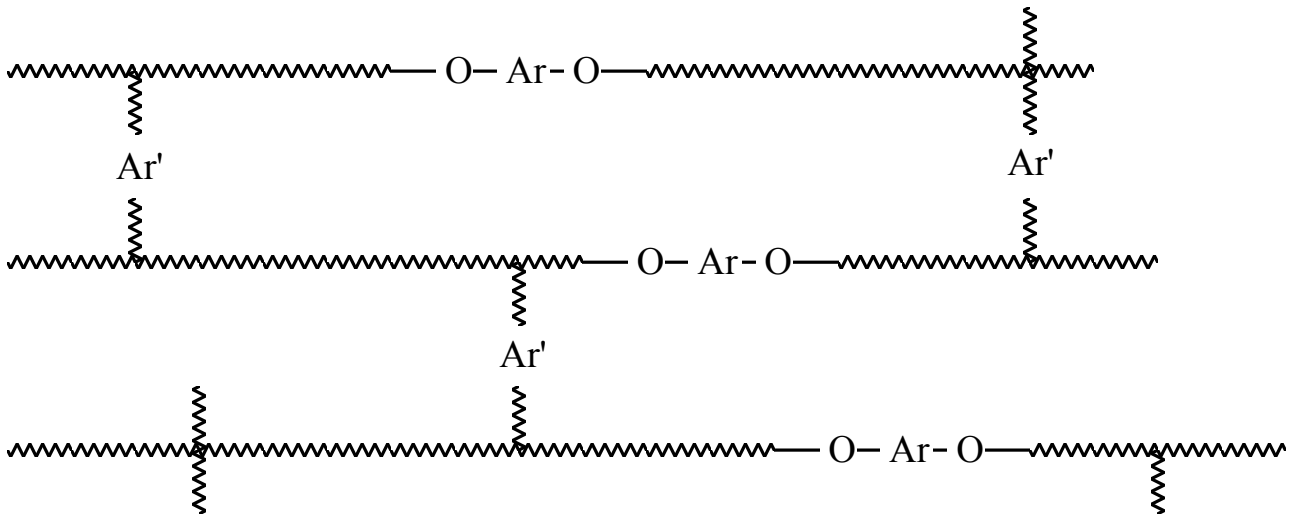
- lower k (~2.8, isotropic)
- $\Delta n \sim 0$
- lower modulus

  E ~ 2 GPa
- Higher CTE 50-70 ppm/deg.
- Lower Tg < 300°C

Crosslinked Poly(aryl ether):



Crosslinking of chains provides thermo-mechanical stability:



Optical Index and Dielectric Constant: Electronic vs. Nuclear Polarization

(n measured @ 632 nm)

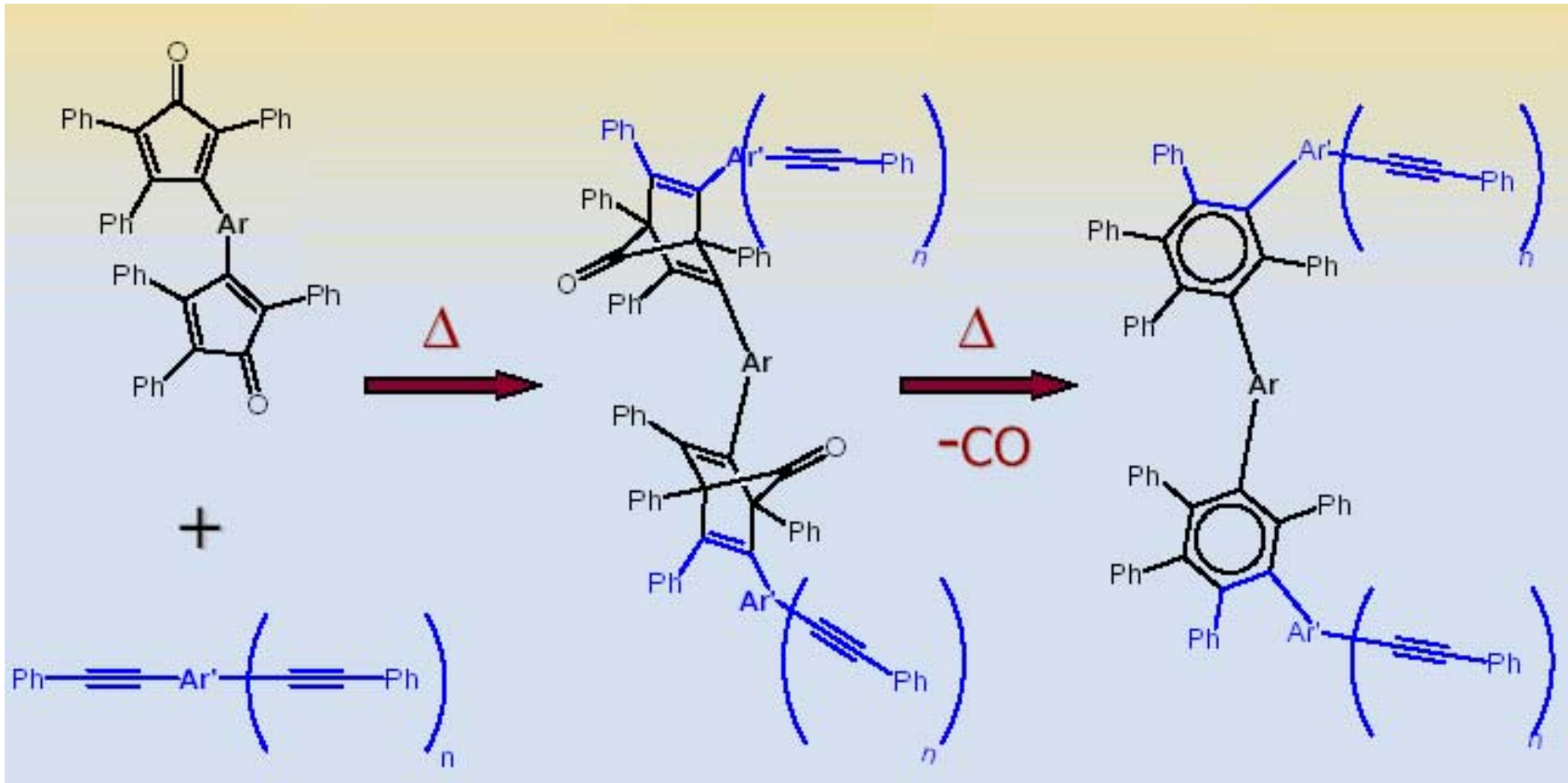
Material	n_{in}	n_{out}	n_{out}^2	$k_{out}(1MHz)$	$\Delta = k - n_{out}^2$
PTFE	1.350	1.340	1.796	1.92	0.12
BPDA-PDA	1.839	1.617	2.615	3.12	0.50
FPI	1.670	1.518	2.304	2.65	0.35
PAE #1	1.676	1.669	2.787	3.00	0.11
PAE #2	1.671	1.672	2.796	2.80	0.00
BCB	1.554	1.554	2.415	2.65	0.24
SOG	1.374	1.373	1.886	2.52	0.63
SiO_2	1.47	1.47	2.16	~4	1.8

Recent Low k Dielectric Materials

Material	Type	Manufact.	k
SiLk	Organic themoset	Dow Chemical	2.65
FLARE 2.0	Poly aryl ether	Allied Signal	2.8-2.9
Black Diam. Corel	MSQ type CVD	Applied Mat. Novellus	2.7
P SiLK Orion LKD 5109 XPX	Porous spin on material	Dow Trikon JSR Asahi	2.0-2.3

Molecular Structure of SiLK

(S.J. Martin et al. Adv. Mat. 12, 1769, 2000)



Formation of polyphenylene polymer structure

H. C. Silvis, Am. Chem. Soc., Boston, 2002

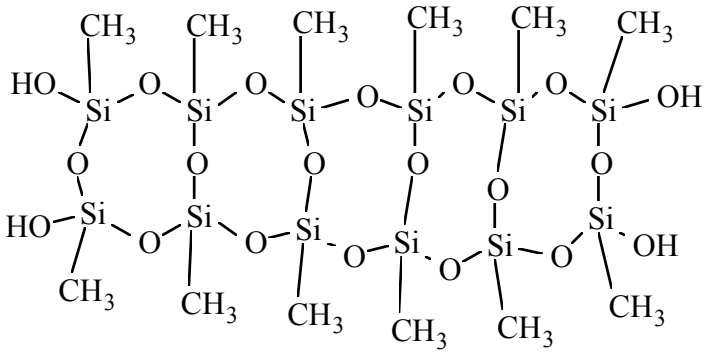
Crosslinked Silica-Based Materials

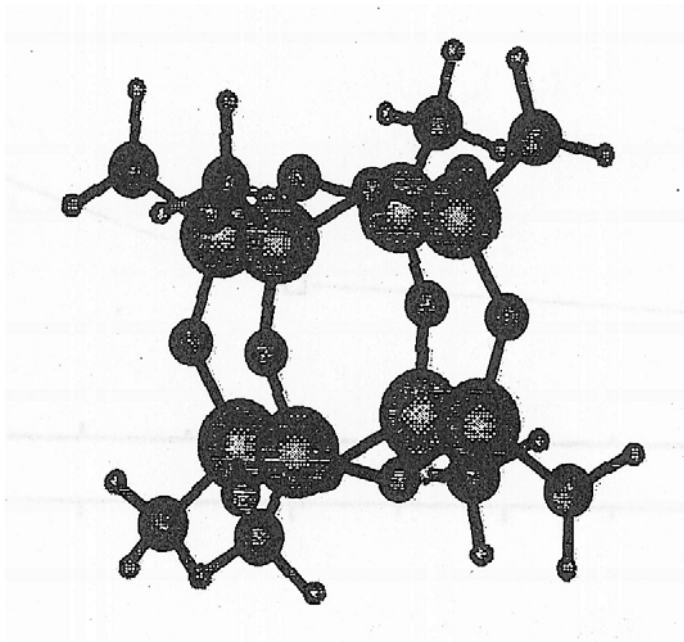
- Si-O network provides rigidity
- Organic groups lower k to 2.5-3.3

silsesquioxane $RSiO_{1.5}$

HSQ
k = 2.9-3.0

MSQ
k = 2.7-2.8





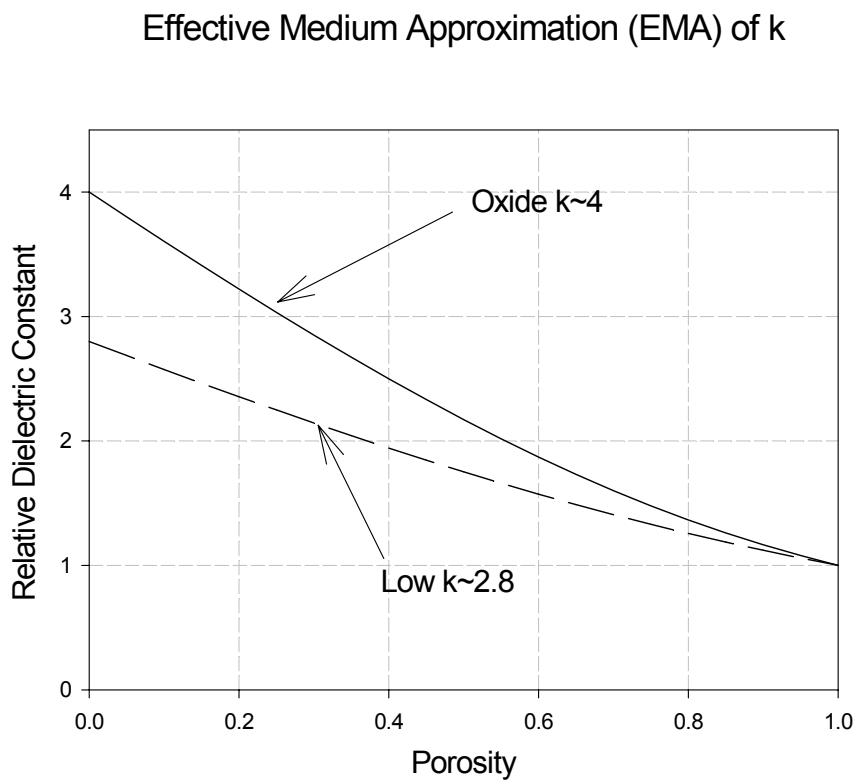
Selected dielectric and thermomechanical properties of low k films

Material	k	Young's Modulus (GPa)	Lateral TEC 25-225 °C (ppm/°C)	Tg (°C)	TGA % weight loss (425 °C, 8 hrs.)
PTFE	1.92	0.5	135	250	0.6
BPDA-PDA	3.12	8.3	3.8	360	0.4
crosslinked PAE	2.8-3.0	2.7	52	350	2.5
Fluorinated PAE	2.64	1.9	52	>400	x
BCB	2.65	2.2	62	-	30
SiLK	2.65	2.3	54	-	2.1
Parylene-N	2.58	2.9	55-100+	425 (melt)	30
Parylene-F	2.18	4.9	33	-	0.8
HSQ	2.8-3.0	7.1*	20.5	-	x

* Biaxial modulus
x Not measured
- None observed

M. Kiene et al., Handbook of Si Semicond. Metrology, Marcel Dekker Inc. 2001

Effect of Porosity on Dielectric Constant

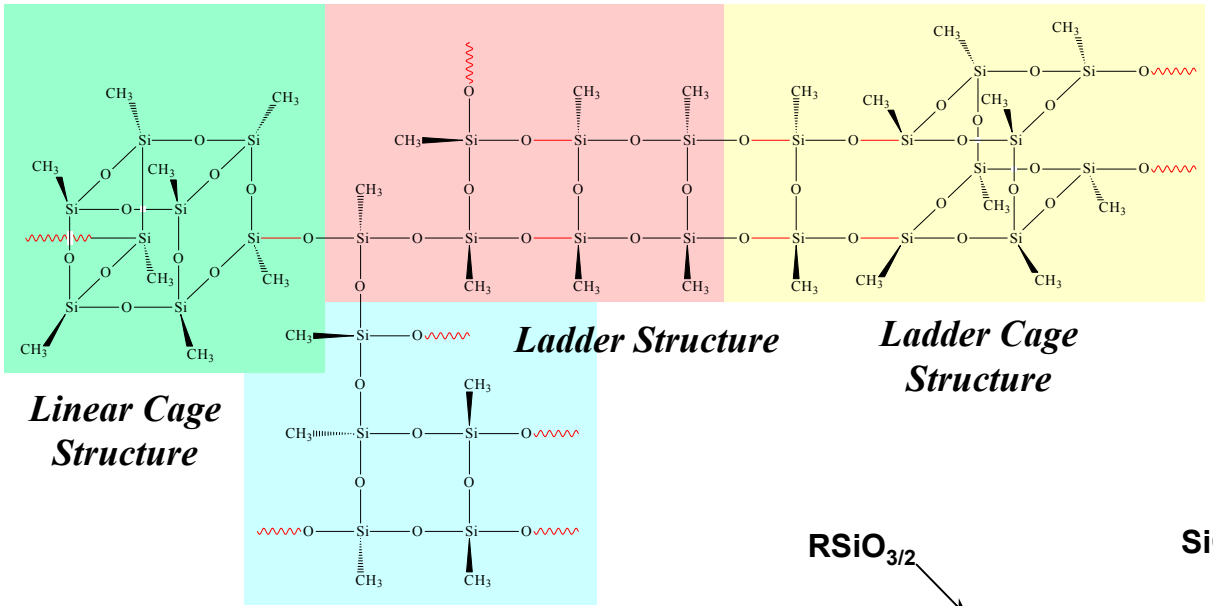


Bruggeman's EMA:

$$f_1 \frac{k_1 - k_e}{k_1 + 2k_e} + f_2 \frac{k_2 - k_e}{k_2 + 2k_e} = 0$$

- k scales ~ linearly with porosity
- Lower porosity needed if the fully dense material is low k <3.0

ORGANOSILICATES (W. Volksen et al, MRS April, 2001)



Linear Cage Structure

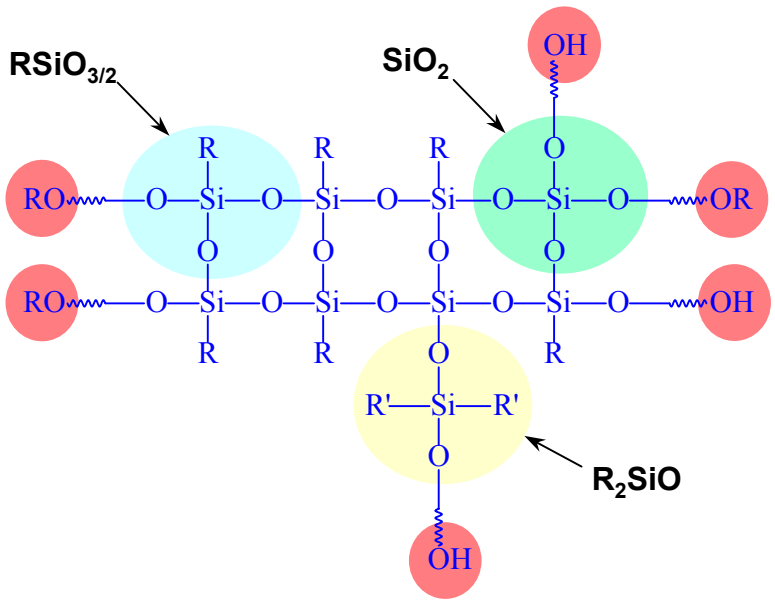
Ladder Structure

Ladder Cage Structure

Random Structure

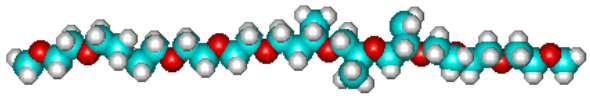
R or R' = { —CH_3, —H ; —alkyl, —C_6H_5 }

R" = alkyl

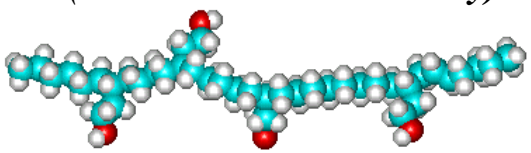


- *Hydrophobic*
- *Planarizing*
- *O_2 Resistant*
- *$k \sim 2.8$*

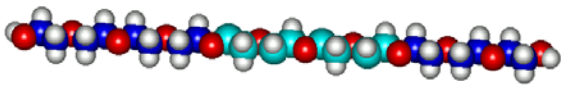
POROGENS FOR ORGANOSILICATES (W. Volksen MRS 2001)



Homopolymers & Random Copolymers (Main Chain Functionality)

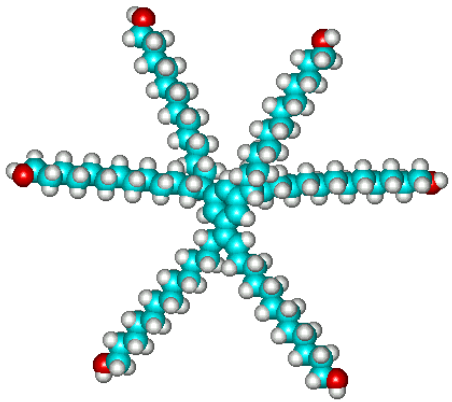


Homopolymers & Random Copolymers (Pendant Functionality)

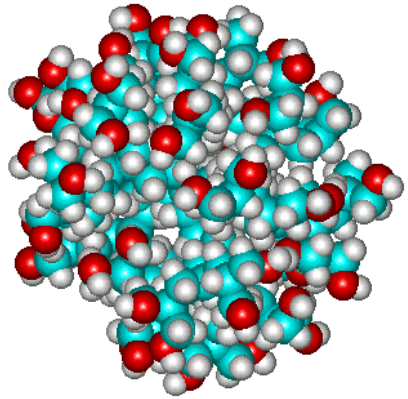


Block Copolymers (Micelles)

Linear Polymers



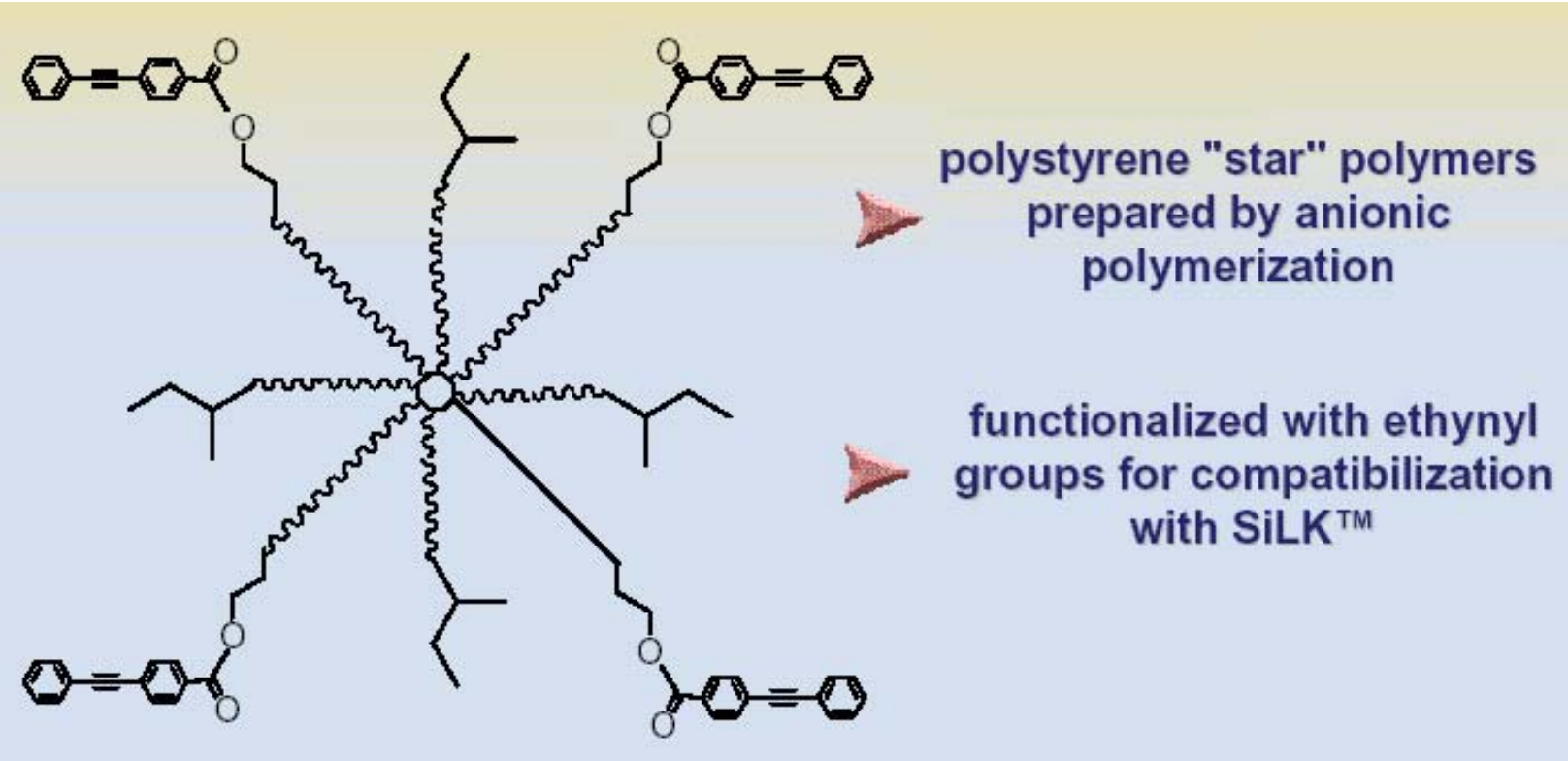
Nanospheres/Xlinked Nanoparticles



Branched/Starburst Polymers and Copolymers

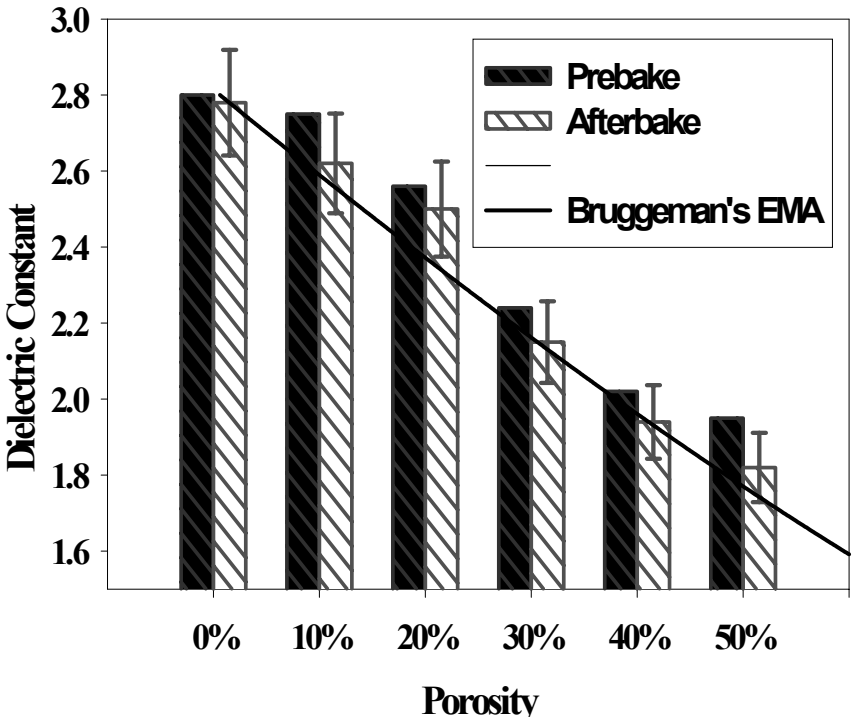
Poly(propylene oxide), poly(ethylene oxide), poly(methyl methacrylate) aliphatic polycarbonates, aliphatic polysulfones, poly(lactones), poly(lactides), poly(ether-lactones), poly(lactone-lactides), poly(ethylene oxide-co- propylene oxide), poly(caprolactone-co-valerolactone), nitrogenous methacrylate copolymers

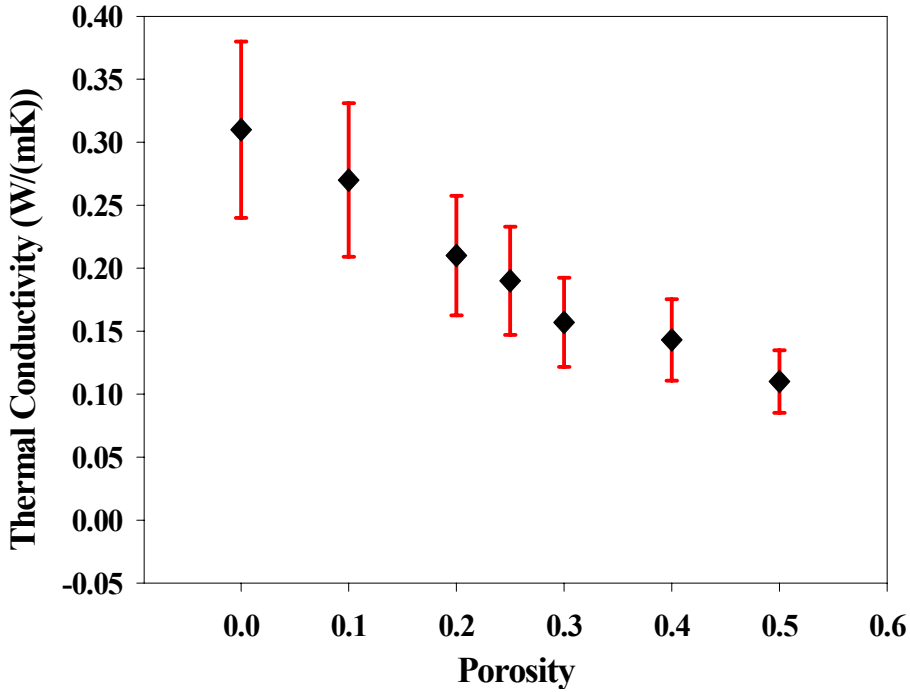
Synthesis of Porous SiLK by Porogen Method



Joint project of Dow and IBM
H.C. Silvis, ACS Boston 8/2002

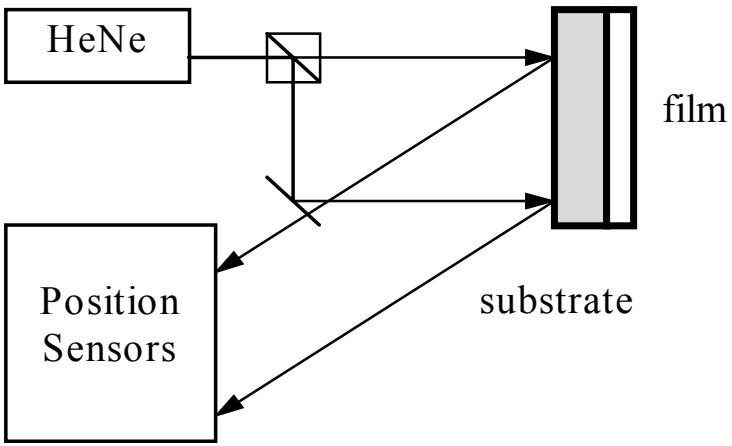
Porosity Effect on Dielectric Constant and Thermal Conductivity

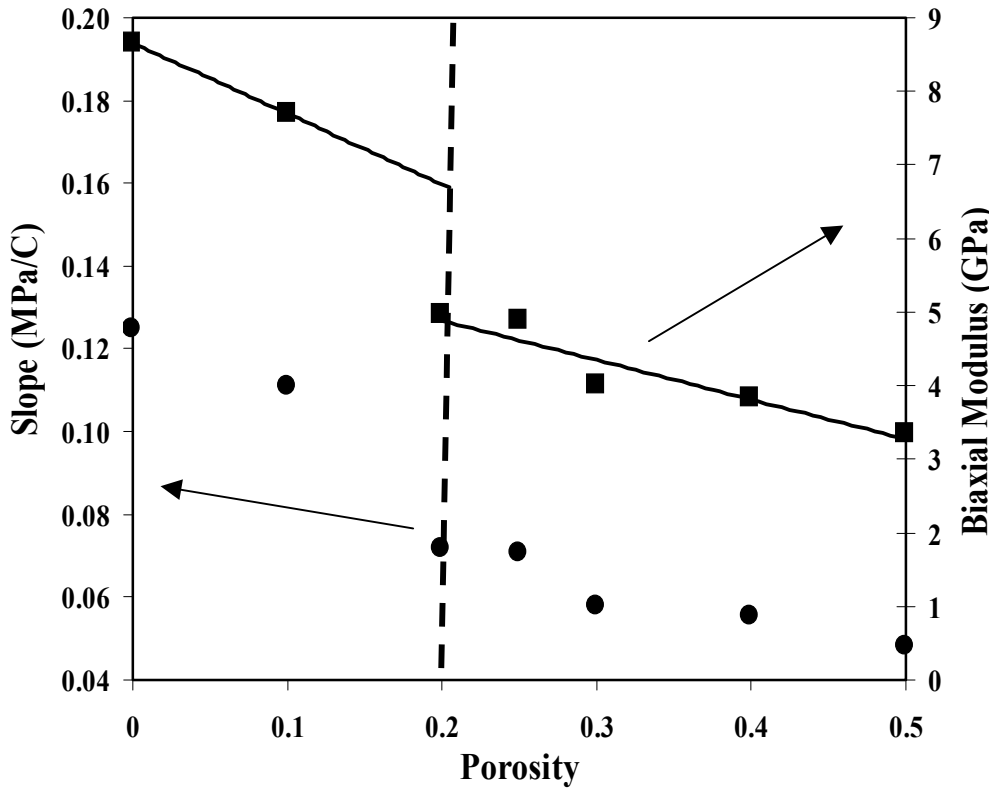




Both dielectric constant and thermal conductivity decrease with porosity but not affected by percolation

Porosity Effect on Thermomechanical Properties





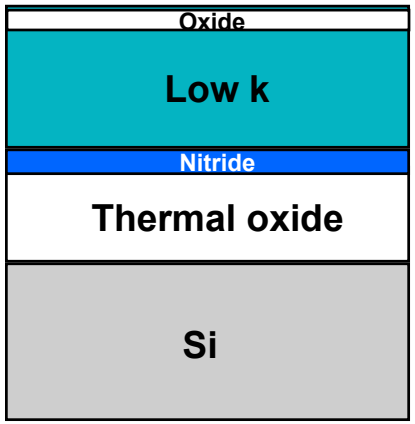
The slope of the thermal stress curve

$$d\sigma_{th} = dT(\alpha_{sub} - \alpha_{film})\frac{E_f}{1-\nu_f}$$

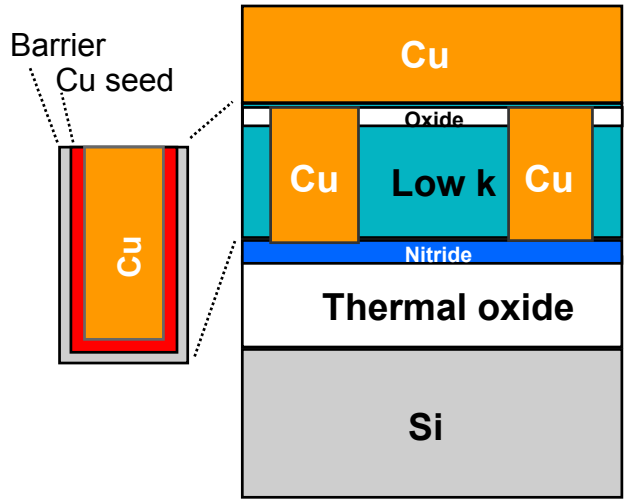
Assuming CTE does not change with porosity, the elastic modulus decreases by about 30% at percolation

Integration of Cu Damascene Structure

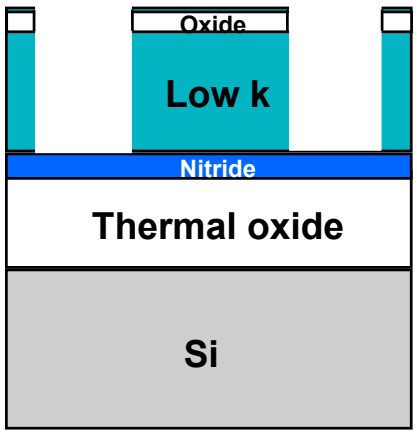
1. Deposit Low κ
2. Deposit Cap (350 - 400°C)



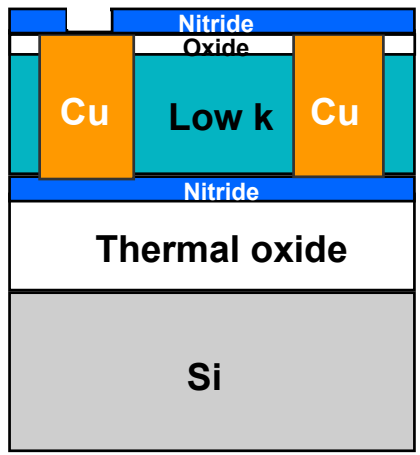
4. Deposit barrier (< 200°C)
5. Deposit Cu seed (< 200°C)
6. Electroplated Cu fills trench
7. Cu anneal (250 - 350°C)



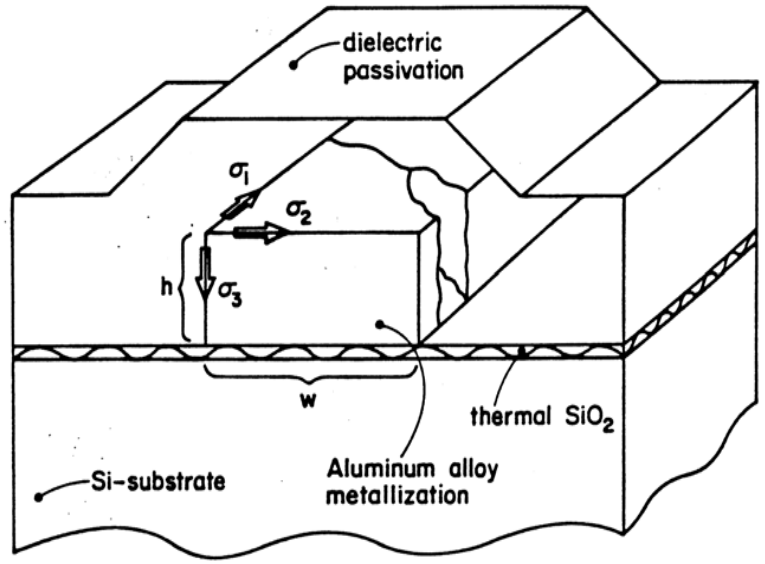
3. Pattern and etch Low κ



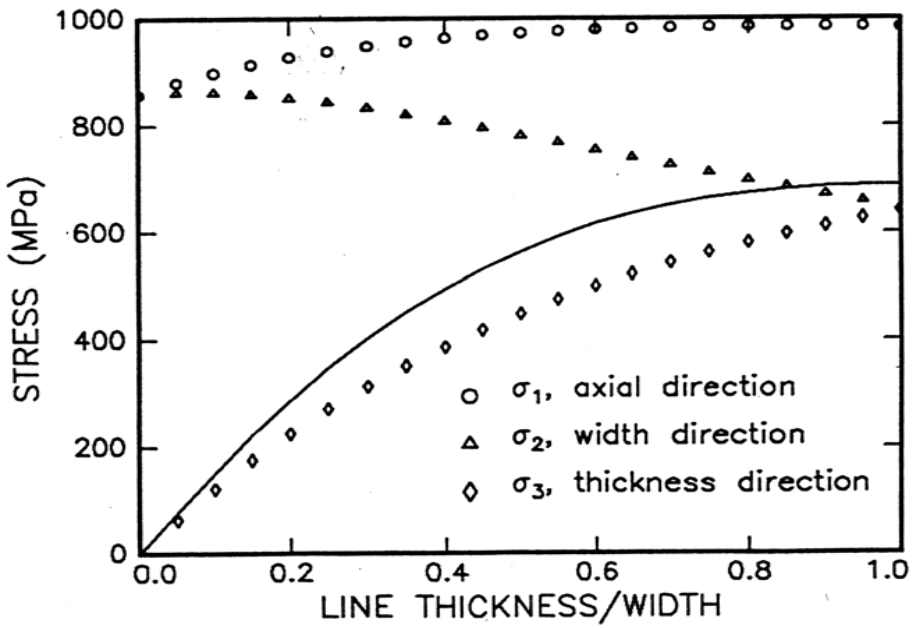
8. CMP Cu
9. Deposit cap (350 - 400°C)



EFFECT OF QUARTZ CONFINEMENT ON THERMAL STRESS OF AL LINE STRUCTURES



ESHELBY'S MODEL OF ELASTIC INCLUSIONS
M. Korhonen et al., MRS Bulletin, 1992)



Von Mises Yield Stress

$$\sigma_Y = \frac{1}{\sqrt{2}}\left[(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2\right]^{\frac{1}{2}}$$

σ_x, σ_y, and σ_z are principal stresses

For thin films, $\sigma_x = \sigma_y$, $\sigma_z = 0$, so $\sigma_Y = \sigma_x$ or σ_y and plastic yield can readily occur.

For passivated lines, $\sigma_x \neq \sigma_y \neq \sigma_z \neq 0$. σ_Y , the driving force for plastic yield is significantly reduced. For low k structures, σ_Y becomes material dependent.

Hydrostatic Stress

$$\sigma_H = (\sigma_x + \sigma_y + \sigma_z)/3$$

Driving force for stress voiding. Void formation requires vacancy source coming from Cu grain growth and stress concentration at via-line interface. (E. Ogawa et al., IRPS, '02)

X-ray Measurements of Thermal Stresses in Al and Cu Lines

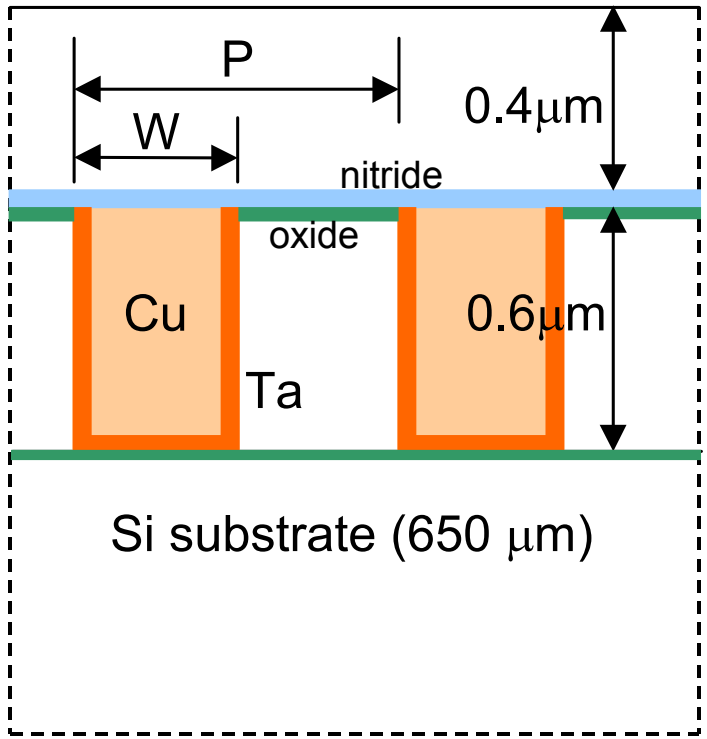
- Single-level Al and Cu lines passivated with TEOS or low k dielectric
- Line dimensions

	W(μm)	P(μm)
Al	0.5	1.0
Cu	0.6	1.2

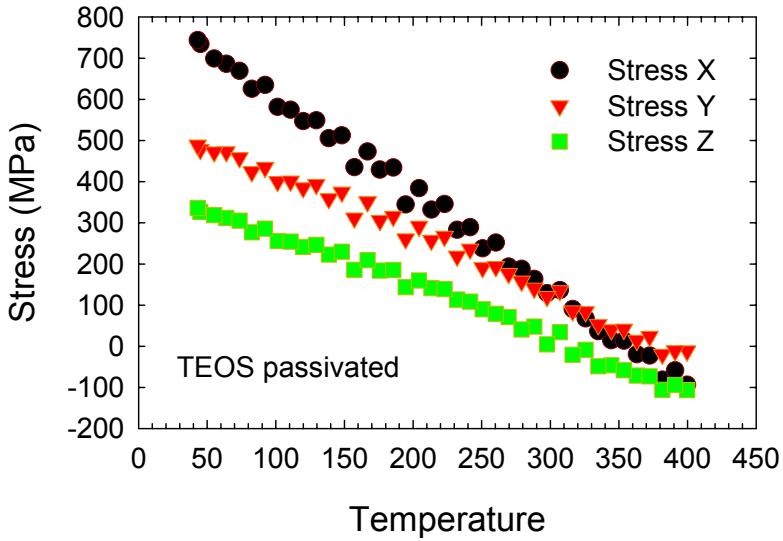
Ta barrier ~ 250Å

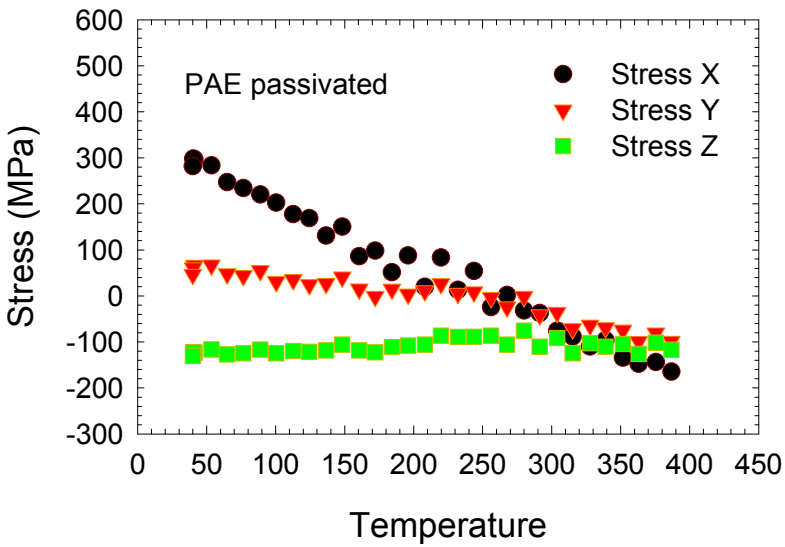
- X-ray diffraction measures strains ε, then

$$\sigma = C_{ij} \bullet \varepsilon$$



Thermal Stresses in Al Lines





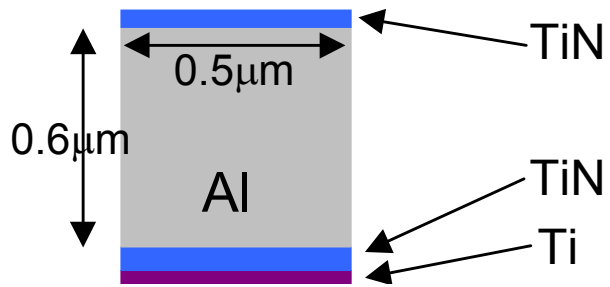
- TEOS passivated lines

→ large tensile stresses are found in all three directions

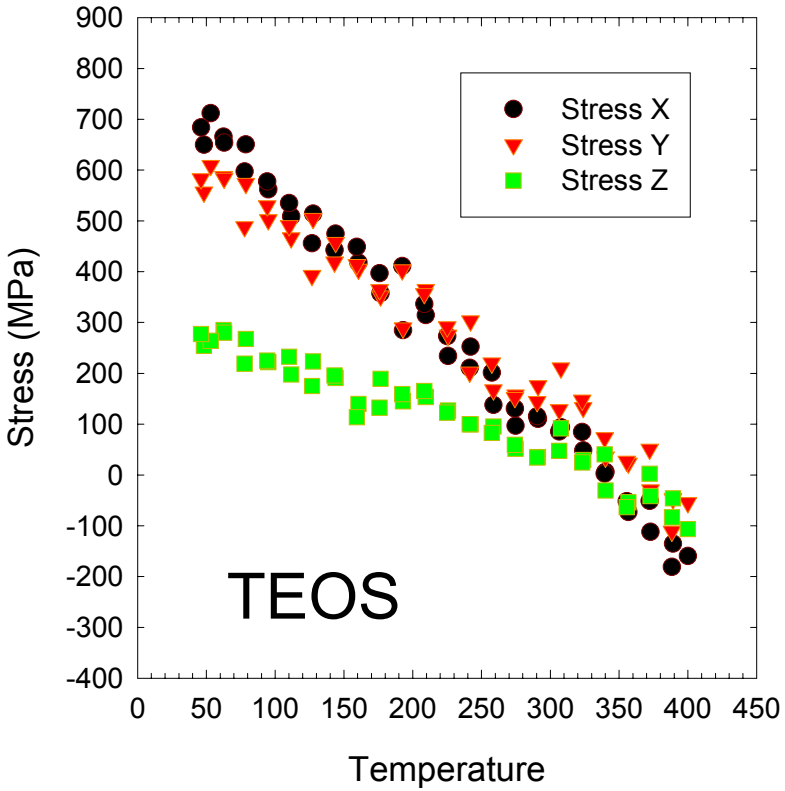
- Low k (PAE) passivated lines

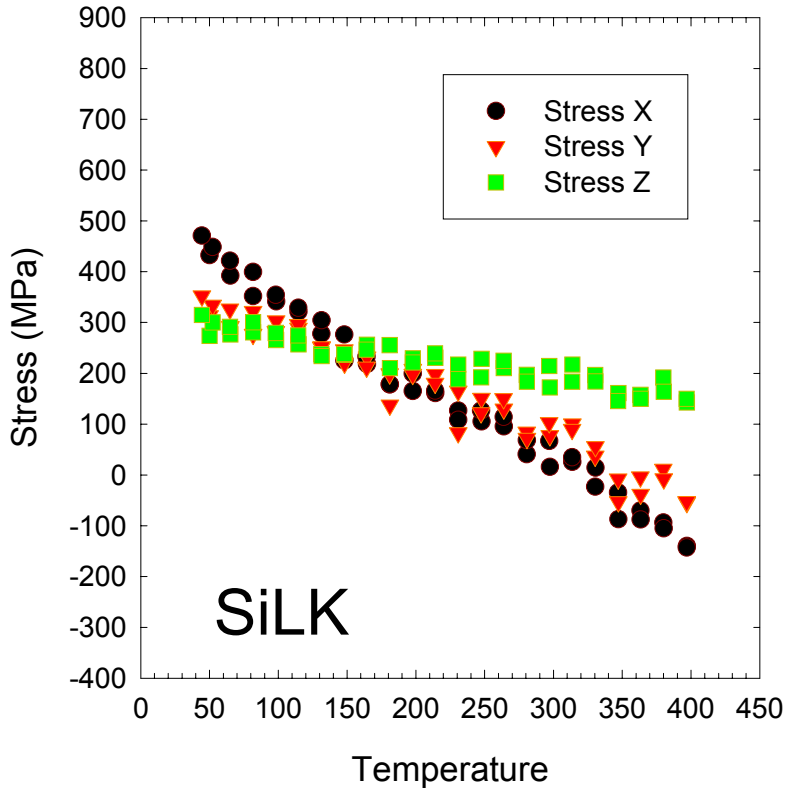
→ σ_x is dominated by substrate

→ compressive σ_z due to high CTE of PAE



Thermal Stresses in Cu Damascene Lines





- The stress state of Cu lines with SiLK is very different from Al lines with PAE passivation; both σ_y and σ_z are positive.

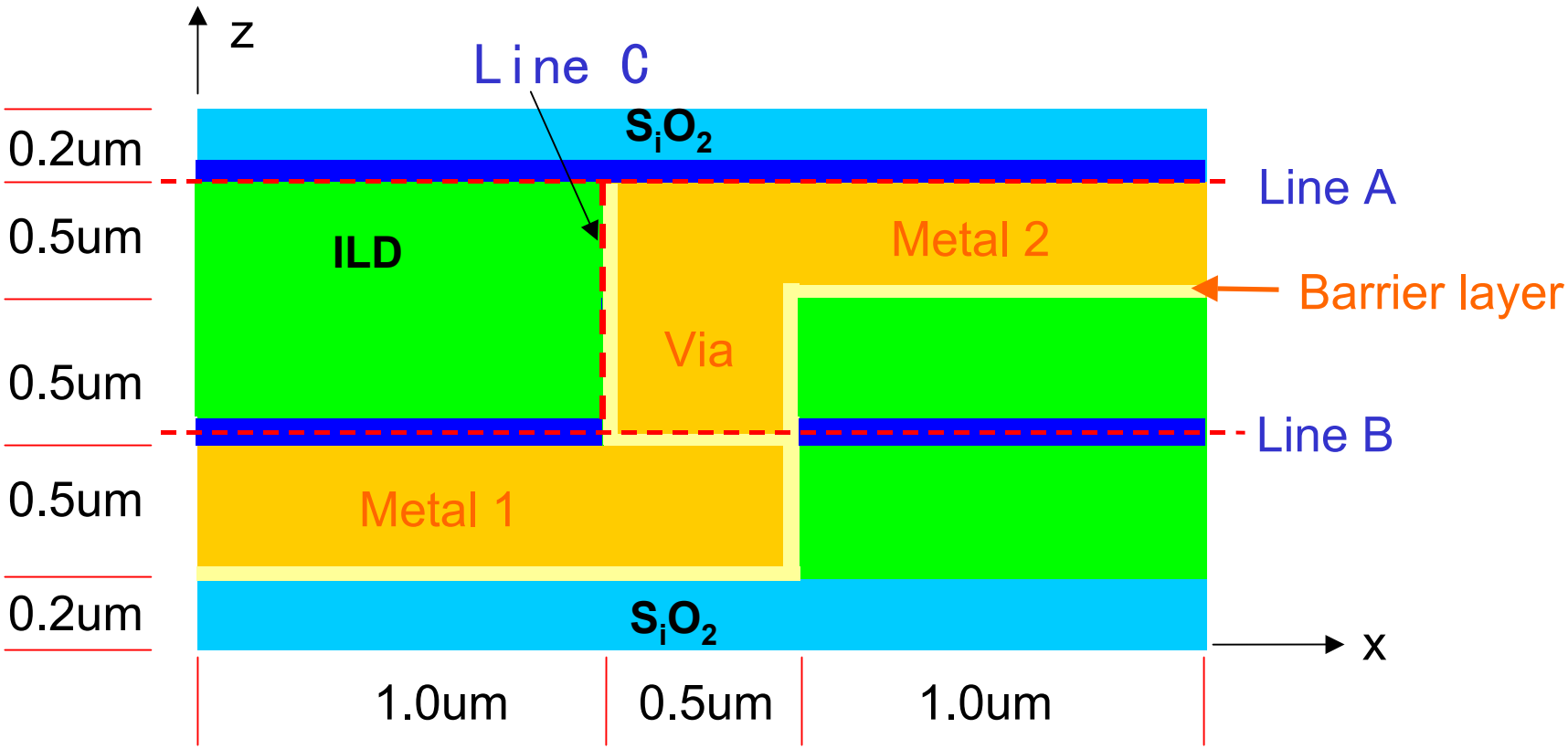
Stress Behavior of Low k Passivated Lines

- CTE and modulus of low k ILD reduce s_y and s_z in Cu compared with TEOS.
- Ta barrier is important in sustaining tensile stresses in Cu lines
- Barrier will significantly affect the stress state as its thickness decreases with line scaling

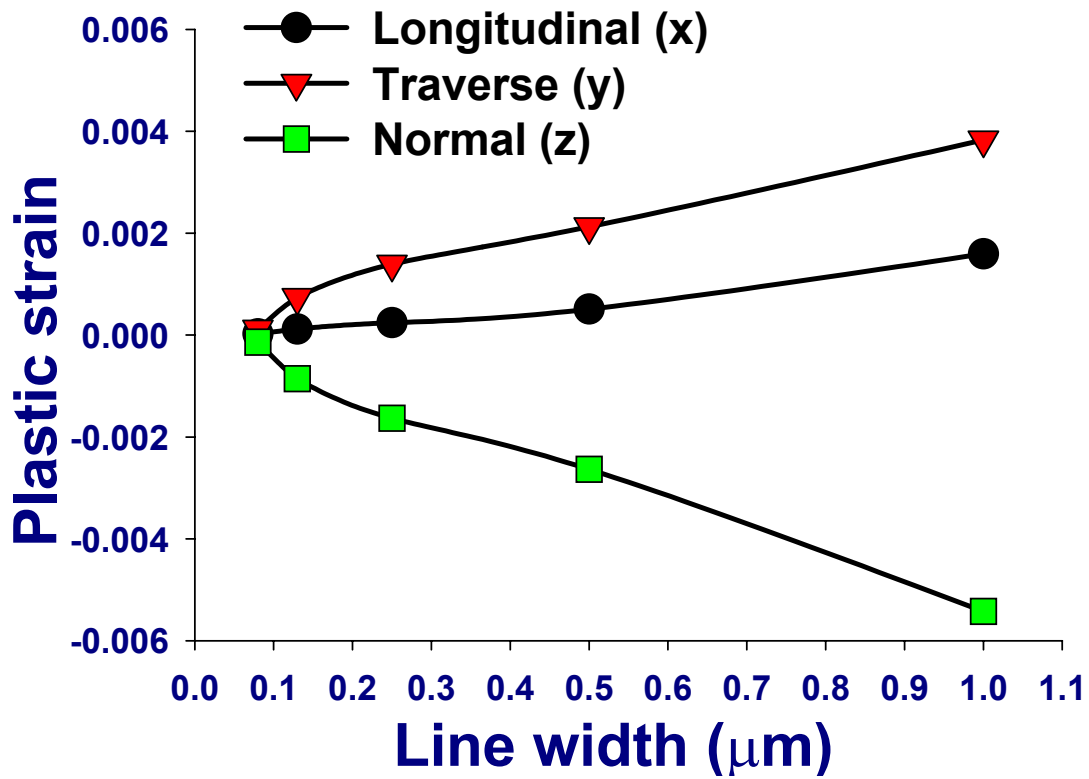
	E (GPa)	ν	α (ppm/°C)
Copper	129.8*	0.34	17.0
Silicon	130.2	0.28	2.3
SiOF	71.7	0.16	0.94
MSQ	6.2	0.30	17.0
SiLK™	2.45	0.35	66.0
Ta	185.0	0.34	6.5

Thermal Stress Analysis for Cu/low k Dual Damascene Structure

Position of Line A and B

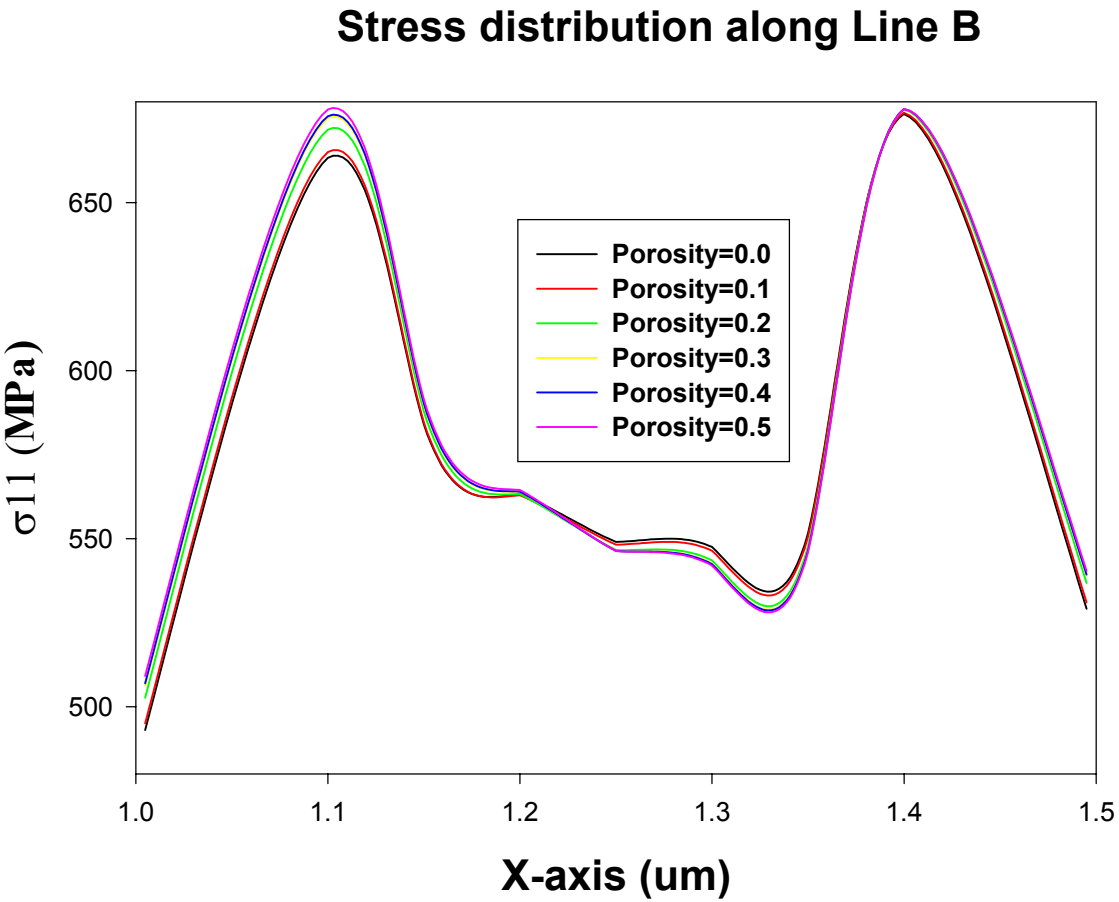


Average plastic strain in SiLK dielectric in single damascene lines



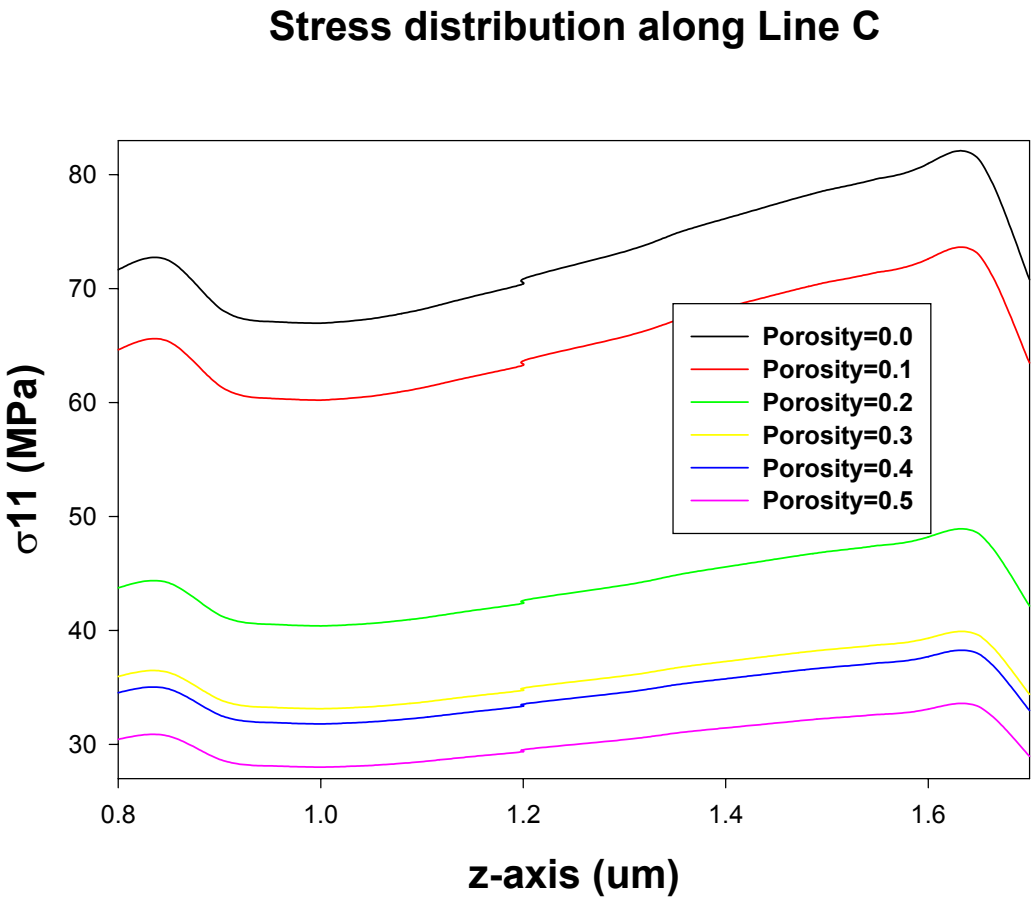
Low k dielectric sustains only small plastic strain which will reduce further with scaling in line dimension

The σ_{11} stress in Cu along the bottom barrier-via interface



High tensile stress at the via bottom interface but a small porosity effect.

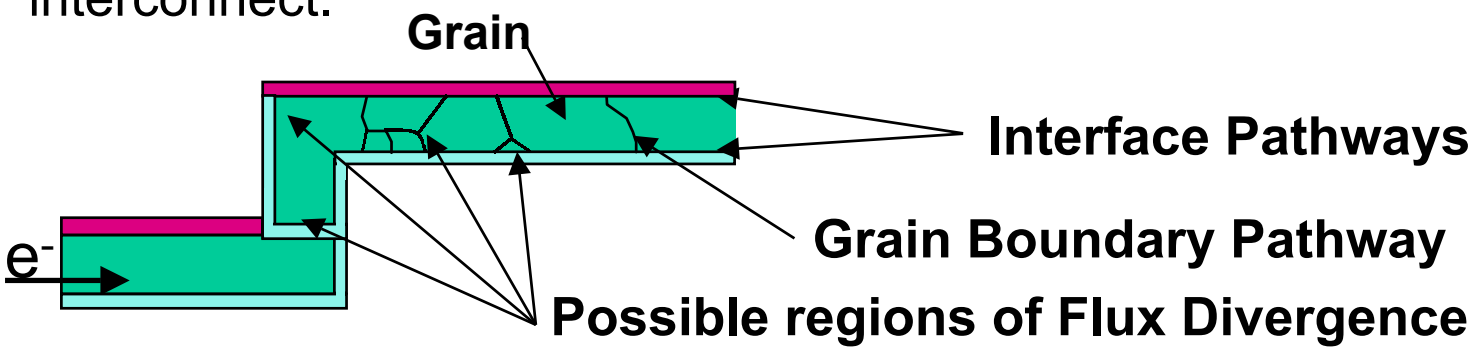
The σ_{11} stress in low k ILD along the vertical barrier-via interface

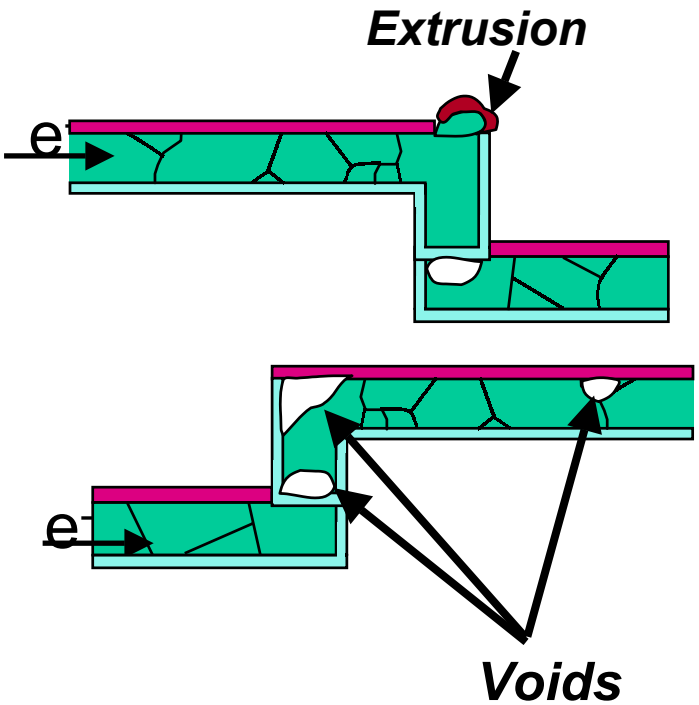


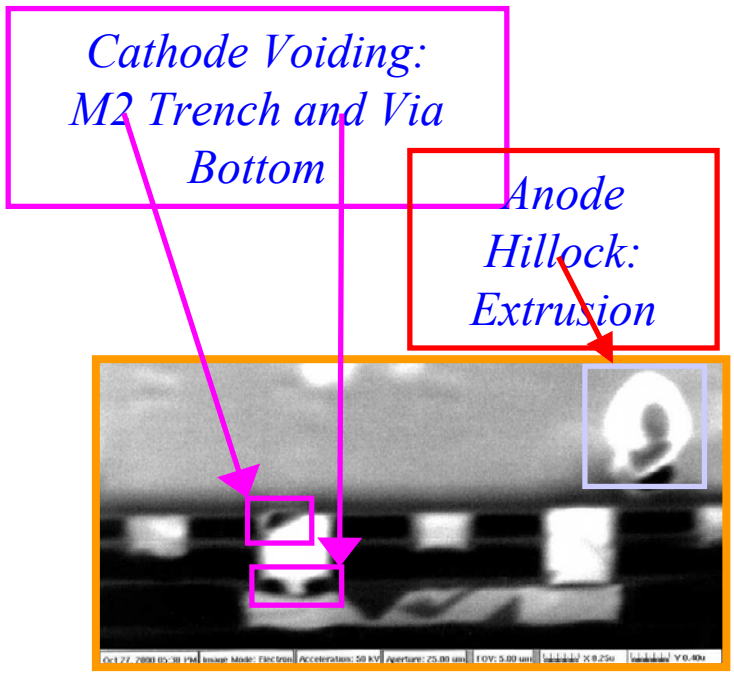
Significant porosity effect due to change in elastic modulus. This affects the driving force for delamination

EM Damage Formation in Damascene Structure

Damage formation due to flux divergence in dual-damascene interconnect.



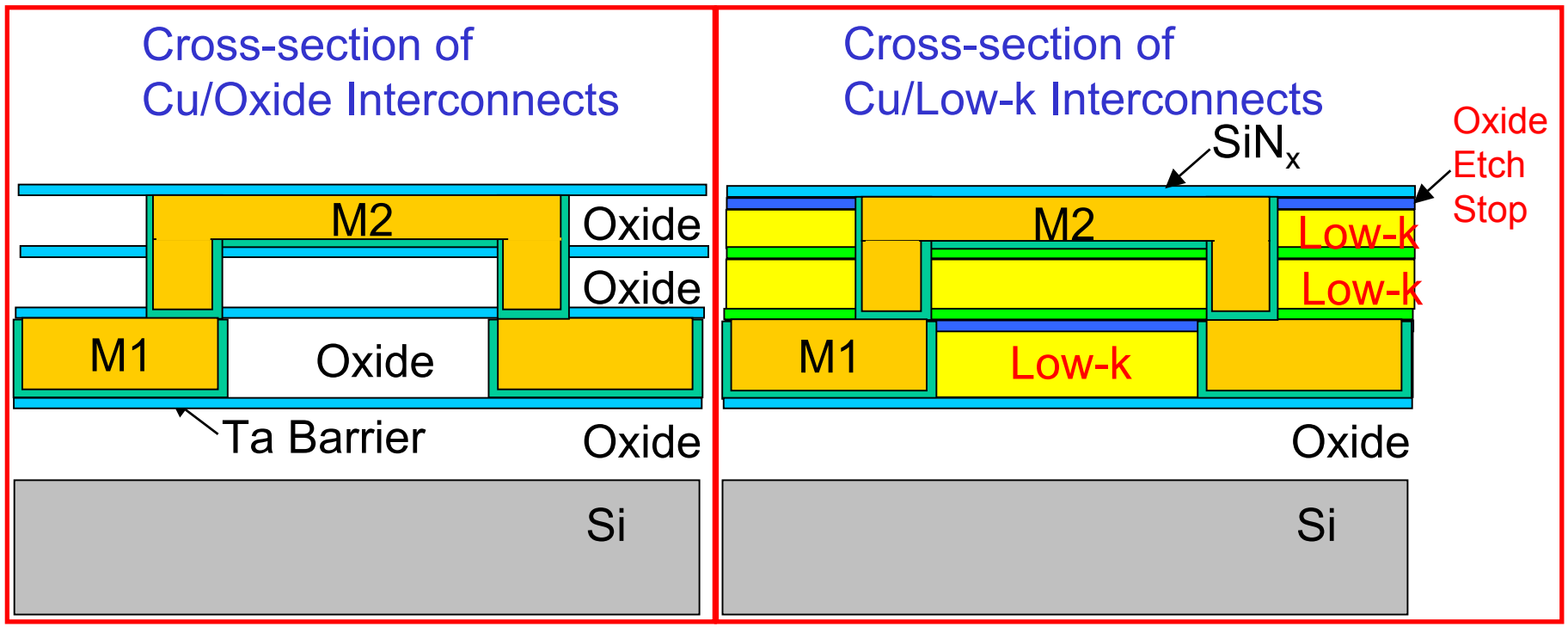




E. T. Ogawa et al., *2001 IEEE Int. Reliability Physics Symposium Proc.* 2001, pp. 341-349.

EM Cu/low k test structure

- Low-k dielectric materials are implemented in all levels
- Oxide etch stop layer is deposited on low-k material.
- The low k ILD and CMP etch stop layer introduce new interfaces in Cu/low k interconnects.



The Blech Effect and the Role of Stress for EM

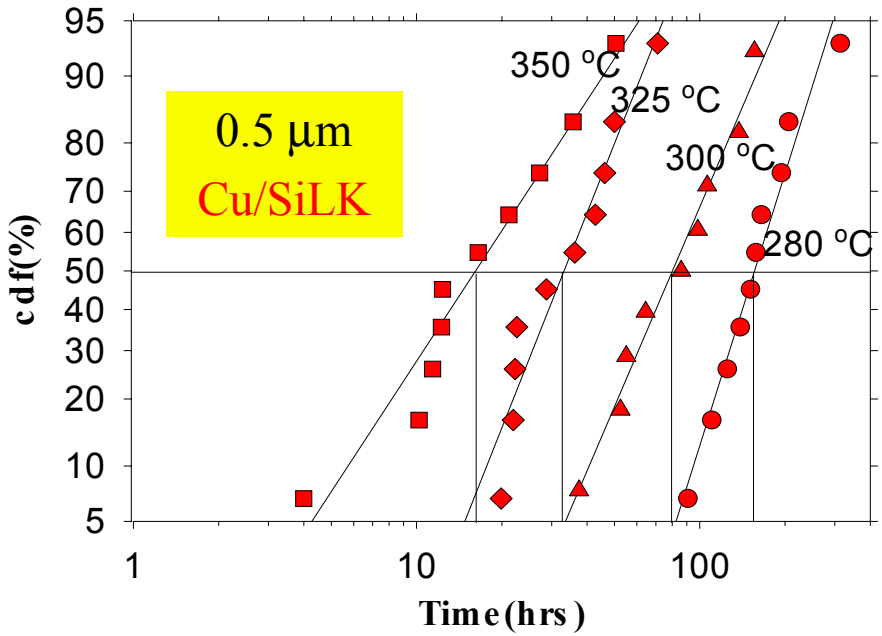
- The average drift of Cu ions under EM driving force compensated by a back flow stress:

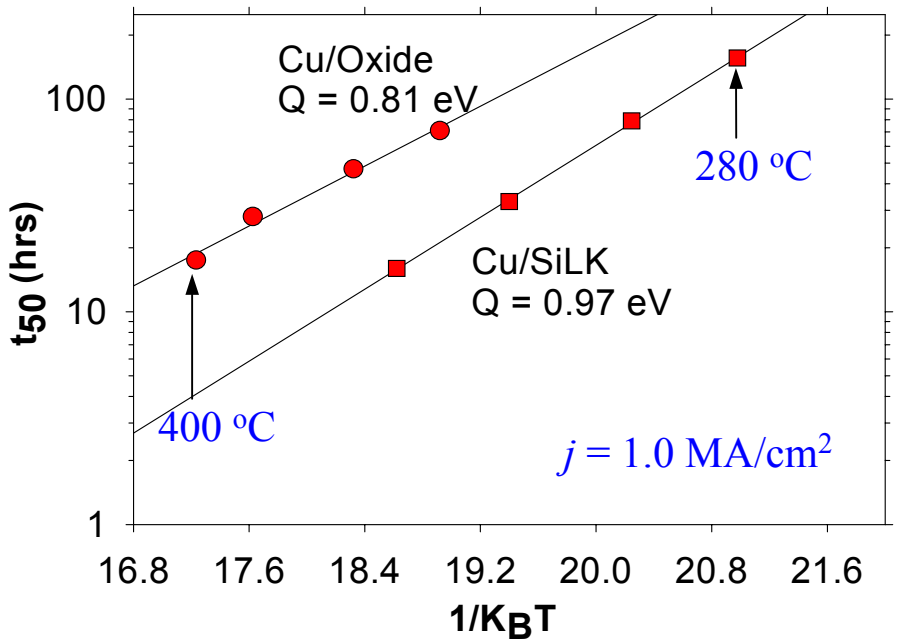
$$v_d = v_{EM} + v_{BF}$$
$$= \mu (Z^* e \rho j - \Delta\sigma / L)$$

- The weak mechanical property of low k dielectrics cannot sustain a high back flow stress, causing the drift rate to increase and EM lifetime to reduce.
- Back flow stress can induce interfacial delamination and cause EM failure. Adhesion and structural integrity are important in controlling EM reliability.

EM Characteristics of Cu Interconnects

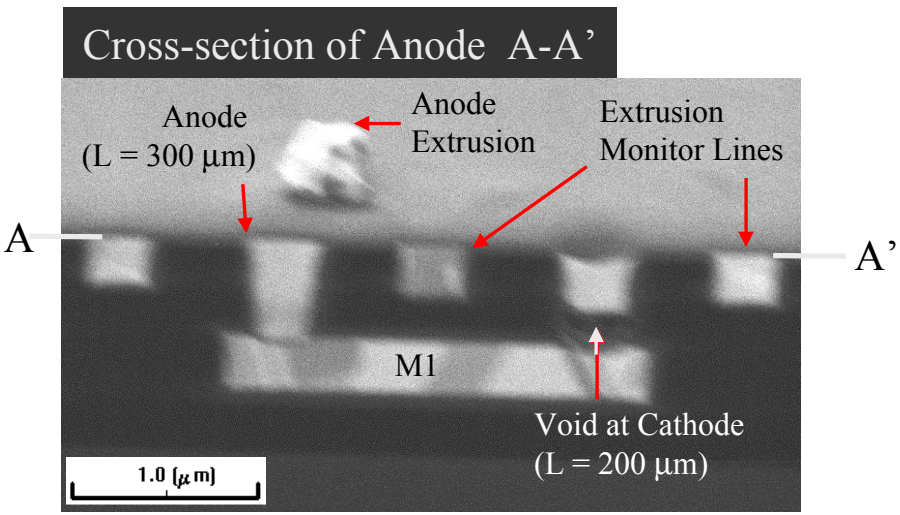
- Similar activation energy, Q, between 0.8 ~ 1.0 eV for Cu/oxide and Cu/low-k interconnects, suggesting interfacial diffusion as dominant mechanism.
- The weak mechanical property of low k dielectric reduces the back-stress, increasing mass transport and reducing EM lifetime.

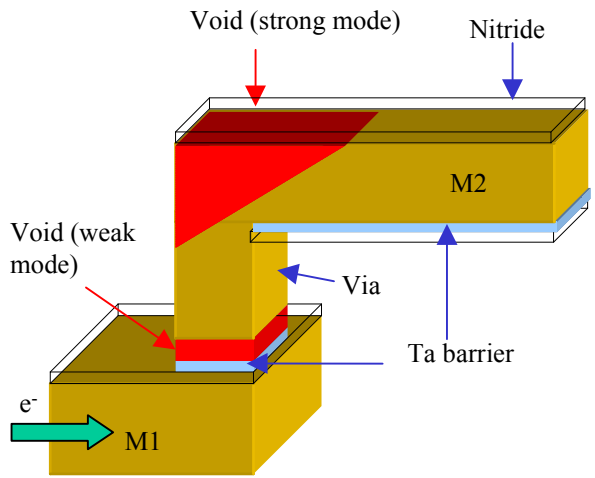




EM Failure Analysis in Cu/Oxide Structure

- At the anode end, extrusion occurs through the SiNx cap layer due to EM induced Cu mass transport . (Anode Extrusion)
- After extrusion, back stress in the line will decrease to enhance void formation at the cathode.

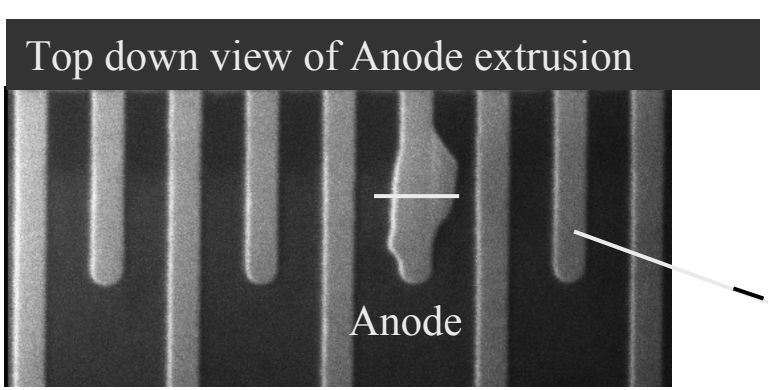


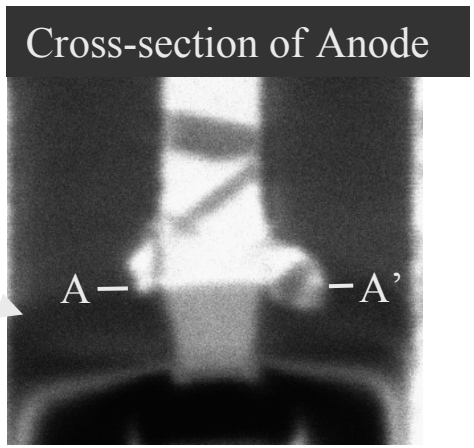


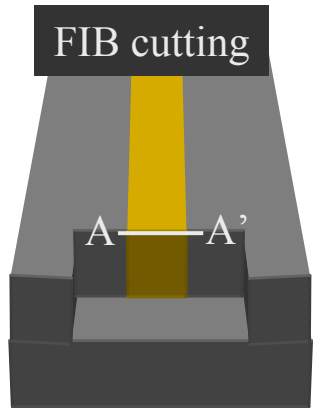
Cathode

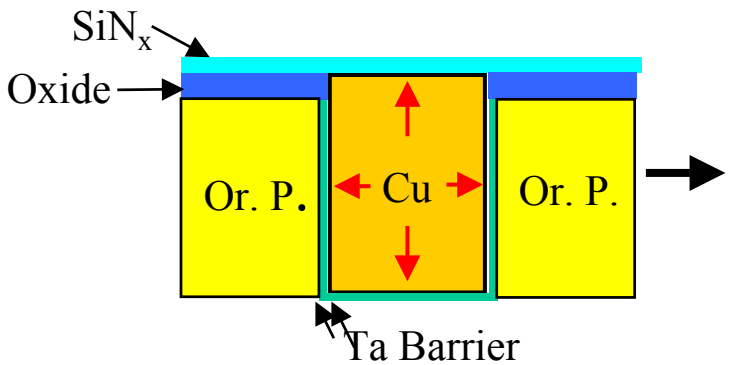
EM Failure in Cu/Low k Interconnect

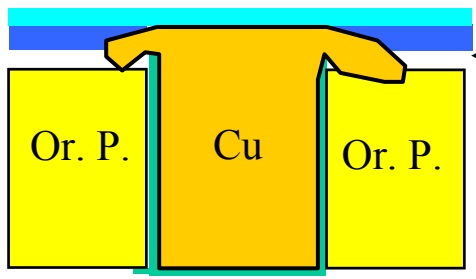
- A hydrostatic compressive stress at anode breaks the interface of organic polymer and cap layer.
- Cu extrudes through interface between organic polymer and cap layer; failure due to interfacial delamination.









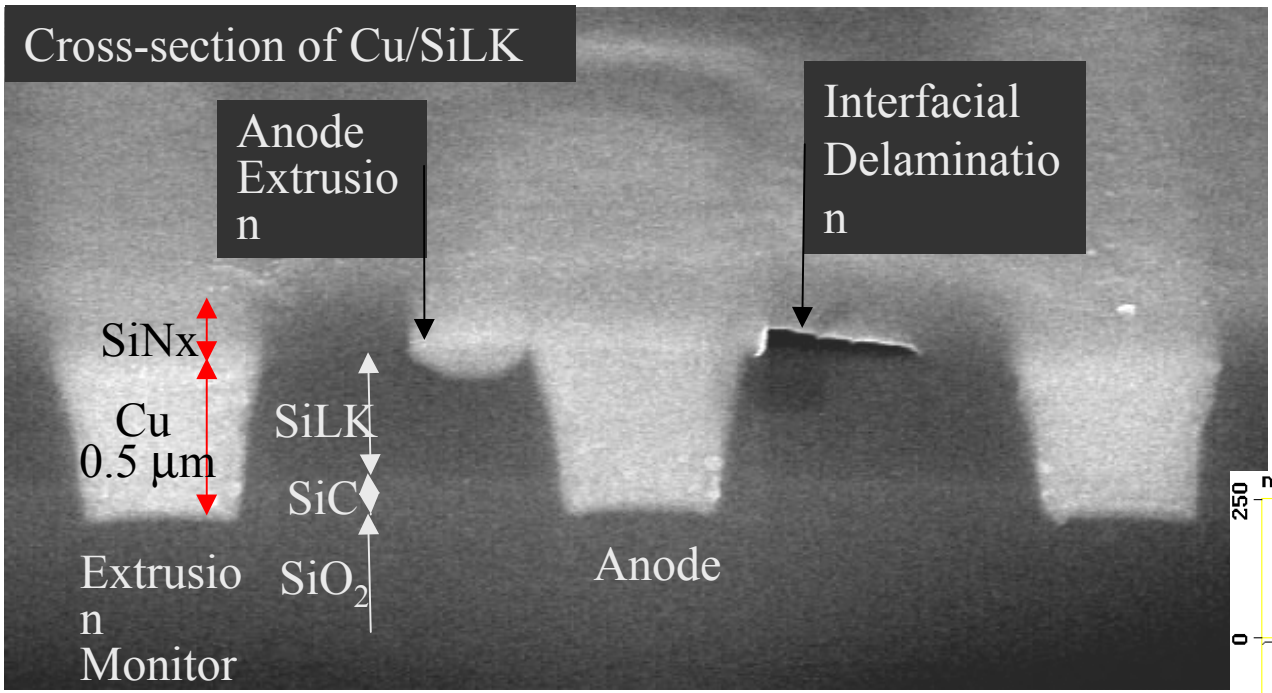


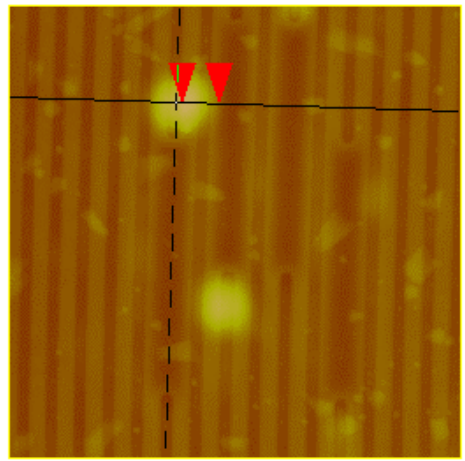
Interfacial adhesion can be an EM reliability issue

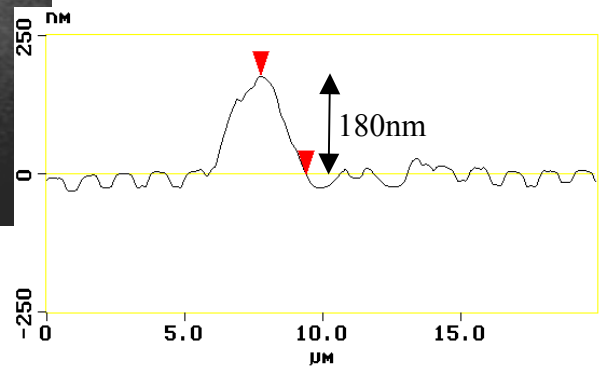
(K.D. Lee, UT Austin, 2001)

Failure Analysis - Cu/SiLK:

- A high compressive stress at anode caused interfacial delamination as well as anode extrusion.

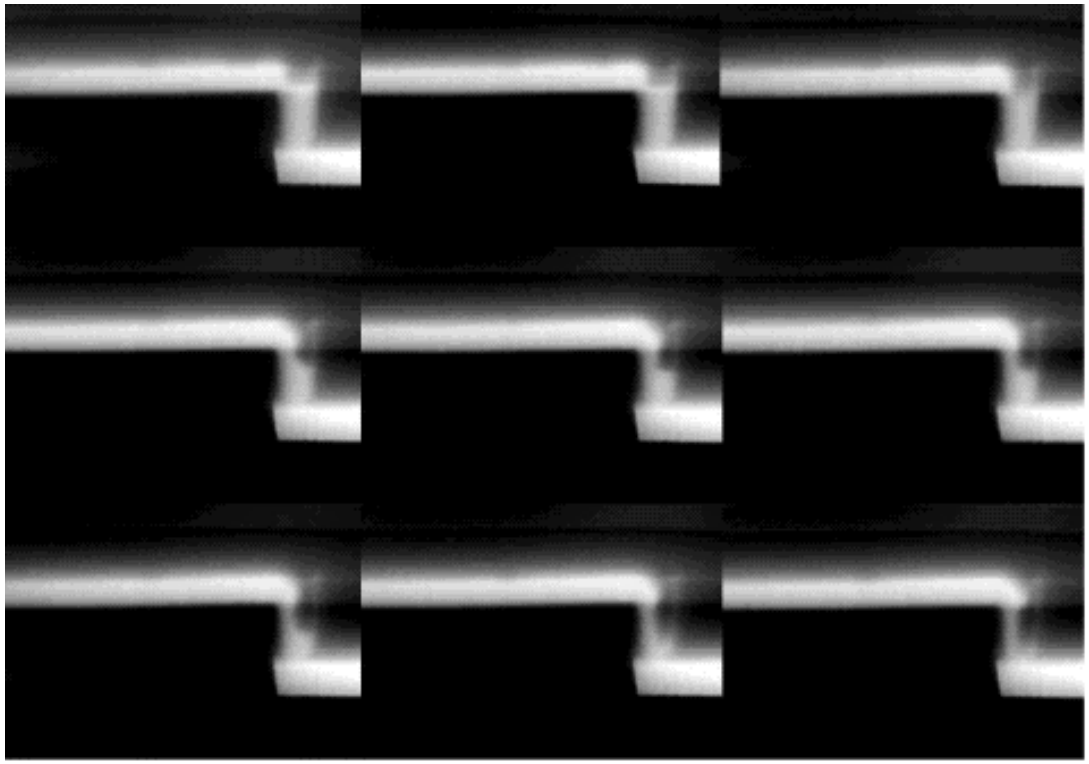




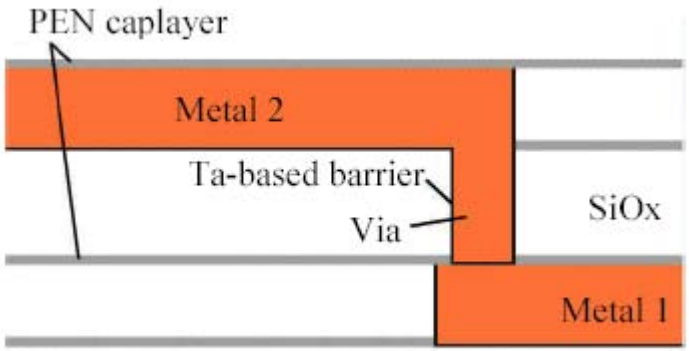


In-situ SEM study of EM in Cu damascene structure

Void formation initiated at the cathode, then extended along the line into the via bottom, causing the structure to fail.



M.A. Meyer et al., AMD Germany, MAM 2002



250ºC, 20MA/cm^2

Images in 2 hr sequence

Effect of surface coating on EM lifetime for Cu lines

(C.K. Hu et al., APL **81**, 1782, Sept. 02)

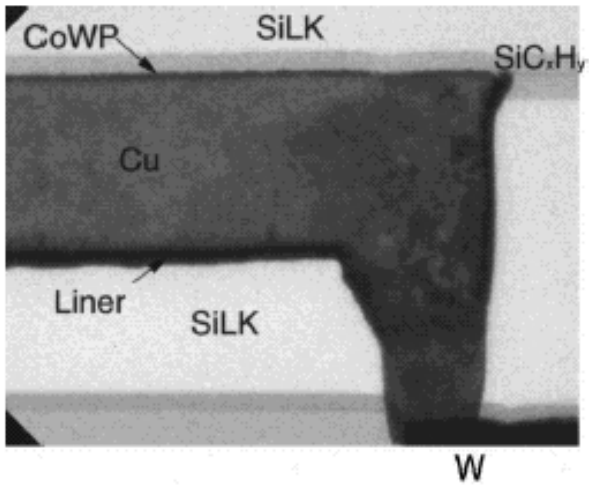


FIG. 2. TEM cross-sectional image of a Cu interconnect coated with CoWP using the test structure in Fig. 1(b).

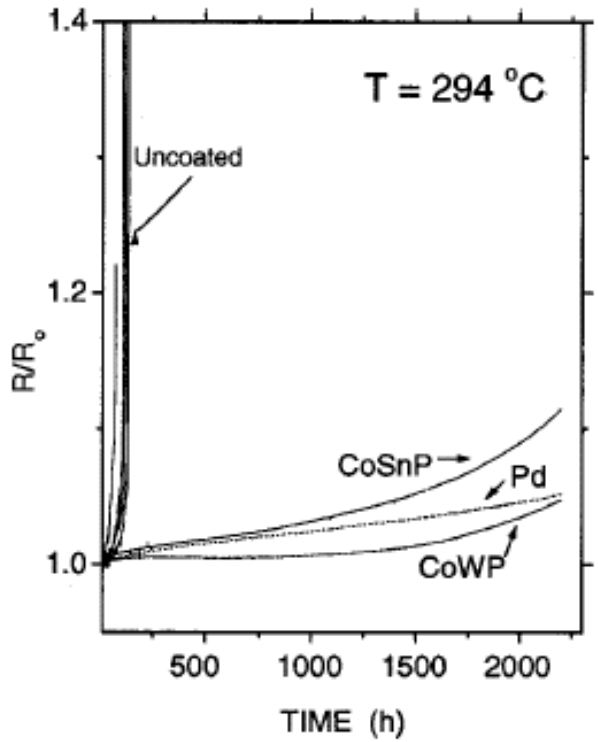
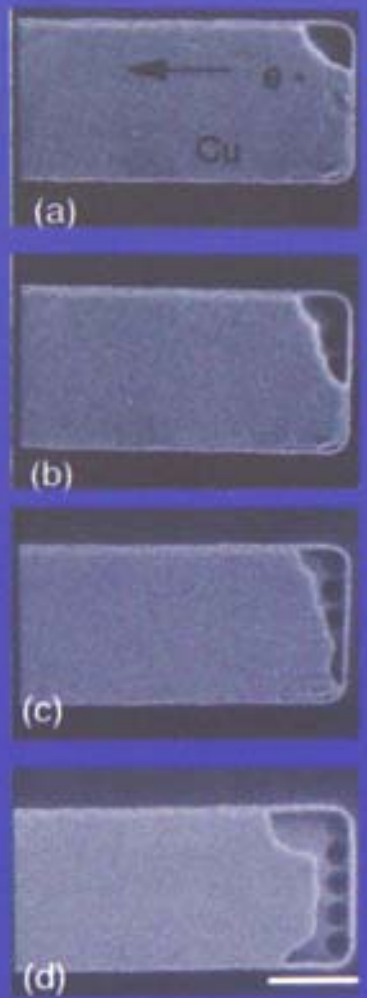


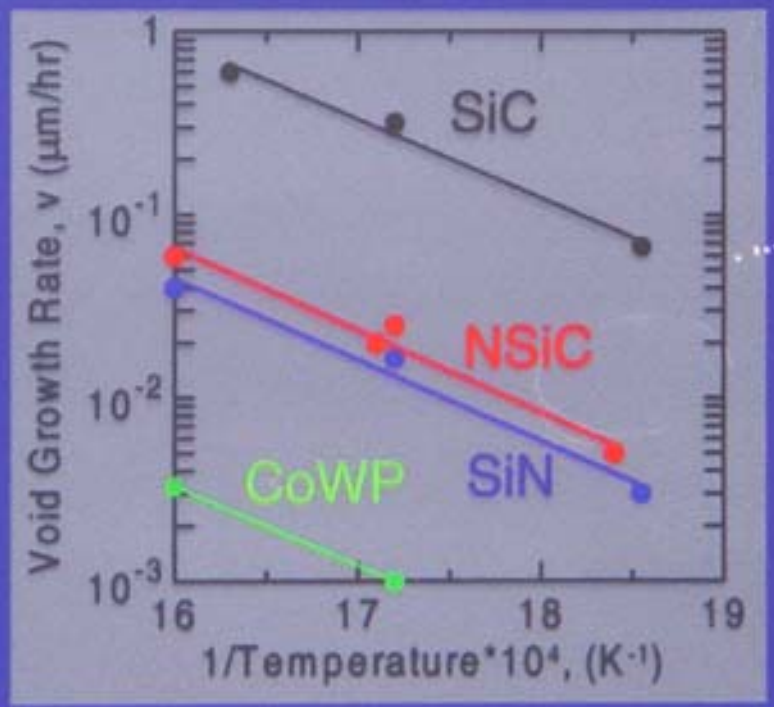
FIG. 4. Graph showing the resistance of a damascene Cu conductor, with and without a thin metal film on the top surface, vs time.

EM lifetime improved by more than 10x with failure occurs only at the via bottom

In-situ Void Growth Measurements in SEM



$$v = \alpha e^{\frac{-\Delta H}{kT}}$$



M. Lane et al., Nat. Cong. on Th. & Appl. Mechanics, Blacksburg, VA, 6/02

Summary

- Low k dielectrics are required for development of Cu interconnects for 130 nm technology node and beyond.
- Thermal stress behavior indicates that barrier and cap layers are important in sustaining structural integrity of low k interconnects. Local stress concentration can lead to delamination and failure of structure.
- EM results show mechanical properties can significantly affect lifetime and distinct failure modes are observed due to interfacial delamination in low k structures.
- Implementation of surface coating to reduce the interfacial mass transport and enhance adhesion is important for reliability improvement for Cu/low k interconnects

Acknowledgement

- Low k material characterization
  M. Morgen (Lucent), M. Kiene (AMD), C. Hu (Intel), J. Zhao (Motorola), J. Liu
- Electromigration
  E. Ogawa (TI), K. D. Lee, X. Lu
- Thermal Stress
  Y. Du (AMD), S. H. Rhee (AMD), D. Gan, G. Wang
- Financial Support
  Semiconductor Research Corp (SRC, H. Hosack)
  International Sematech (J. Wetzel, J. Iacoponi)
  Texas Advanced Research and Technology Program