ETCH CHALLENGES IN LOW K INTEGRATION

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PEUG
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OUTLINE

- Process Integration Challenges
  - Via First-No middle Etch Stop Dual Damascene Process Flow
  - AMAT 3LM Test Structures
  - Photoresist Poisoning
  - BARC Etch Back
  - Via Etch
  - Trench Etch

- Process Module Process Control
  - Thickness Feedforward to widen process window
  - Excursion Detection
  - iRM provides Trench Depth Endpoint

- Summary
PROCESS MODULE™ INTEGRATION SCHEME

Via First Dual Damascene Scheme Offers Simplest, Lowest Cost Solution
3-LM E-TEST STRUCTURE

- BKM process flow
  - Process and inspections steps
  - Complete tool set in house
  - Based on process window characterization and parametric performance

- Multiple lots establish baseline
  - Continuous improvement to increase yield

- Complete characterization
  - Physical properties
  - Defect performance
  - Electrical performance
  - 18 electrical parameters tracked for each lot
  - Success criteria consistent with world class manufacturing
PHOTORESIST POISONING

Resist Foot Due to Poisoning

Poisoning is more severe on edge of structure

FIB showing broken links due to poisoning

Resist Poisoning Manifests Through N Out gassing of Films During Processing
ELECTRICAL YIELD SIGNATURE FOR PR POISONING

Defect density test structure

• Edge of the structures showed more serious PR poisoning and thus lower yield compared to that in the center of the structure

• Possibly due to the concentration variation of NHx at center and edge of the dense via array.
VIA CHAIN YIELD AT VARIOUS M1 OLAP

• AMAT test structures allow us to differentiate PR poisoning issue from general etch issues. This is helpful in identifying the problem in the case of minor poisoning.

Note:
In general, large via to trench olap reduces the probability of misalignment and thus has higher yield.
CURRENT TRENCH OVER VIA LITHOGRAPHY PERFORMANCE

Improvement In Resist Poisoning Obtained Through: Film, Resist and Integration Optimization
T2 LITHOGRAPHY/ETCH CHALLENGES

Conformal BARC

Partial Trench etch

Non-Conformal BARC - Loading

Conformal and non-Conformal BARC have Limitations
0.12µm Via – No Fill Issues

No issue with scribe seal at via level

No fencing after T2 etch (No Etch Stop)
No Residue after BARC etch-back
DARC as ARC for T2 Lithography

0.13 µm Node T2 Scheme Was Moved to Full Fill BARC and Etch-back to Improve Etch / Litho Interactions at M2
VIA OPEN CORROSION

Cu corroded below via

Optimized Process

>95% Yield, Long Via chain

No Cu Corrosion

Interaction between film, etch chemistry and Wet Clean optimized for high yielding Via Chains
LOW κ DEP/ETCH PROCESS CONTROL

Control Capability

- BD thickness feedback
- Etch Feed Fwd/Fdback
- Real Time, WTW
- Real Time Excursion Detection
PROCESS CONTROL

Black Diamond\textsuperscript{TM} (Open Loop)

- Ave: 9959 Å, Stdev: 0.6%

Timed Via Etch (No Feedforward)

- Ave: 5327 Å, Stdev: 1.43%

Via Etch w/ Feedforward Control

- Ave: 5359 Å, Stdev: 0.80%

- Blanket Partial Etch

Black Diamond Dep
VIA ETCH CONTROL

Open Loop

Closed Loop

Experimental BD Thickness

FF to Adjust BD Etch Time

Closed Loop Control with Feed Forward
Minimizes Variations in Barrier Loss
TRENCH DEPTH CONTROL WITH IRM

Dielectric Etch
eMax™ EnTek™ Centura®

Endpoint

iRM detector
Plasma
Reflected light

wafer

Signal Processing Control

Module Marathon Data

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Trench Depth</th>
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<tbody>
<tr>
<td>150</td>
<td>4250Å</td>
</tr>
<tr>
<td>625</td>
<td>4200Å</td>
</tr>
<tr>
<td>1060</td>
<td>4350Å</td>
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<tr>
<td>1600</td>
<td>4400Å</td>
</tr>
<tr>
<td>2100</td>
<td>4400Å</td>
</tr>
<tr>
<td>Post Wet clean</td>
<td>4400Å</td>
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</tbody>
</table>

200Å Trench Depth Variation Across >2000 Wafers
CLOSED LOOP VS OPEN LOOP

Wafer Thickness Induced Variation Due to Process Perturbation

Tight Distribution Using iAPC and FF Control

Parallel Plate Capacitance

Bi-Modal Distribution Caused by Thickness Variations
SUMMARY

- Low-k materials have posted significant challenges to the integration and particularly to the etching/patterning of the structures.

- Characterization and understanding the nature of various issues are critical for the success in low-k integration.

- Combination of Integration Knowledge with Device Characterization Capability help reduce Device Qualification cycle time.

- Troubleshooting methodology and systematic approach in addressing the issues are crucial to the yield management.

- Process control brings great values in minimizing the variability and eliminating excursions.