Impact of SiOC Low K Materials on Dual Damascene Patterning

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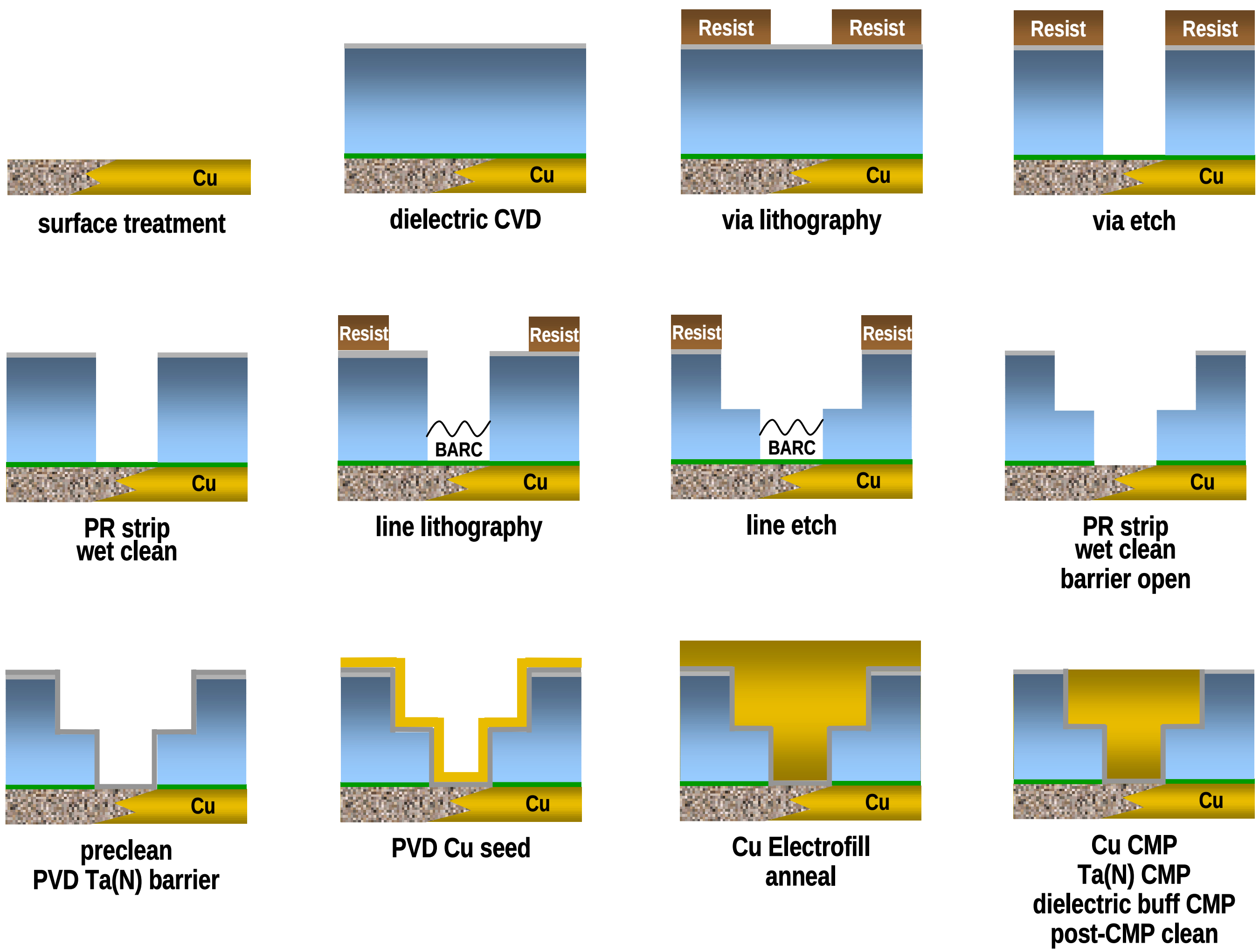
Presentation Outline

- Dual damascene process flow.
- Dual damascene etch challenges.
- Photoresist poisoning.
- Trench etch.
- Via etch.
- Trench-over-via etch.
- Barrier open etch.
- Summary

Dual Damascene Process Flow
Via First



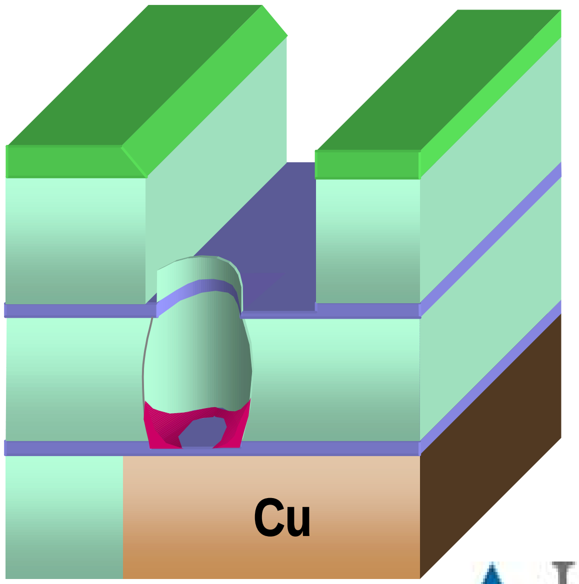
Dual Damascene Etch Challenges

General Dual Damascene Etch Challenges

- Profile control
- Trench bottom profile
- Striations
- Etch selectivity
- Microloading
- No endpoint
- Uniformity
- Veils
- Strips selective to dielectrics
- k increase

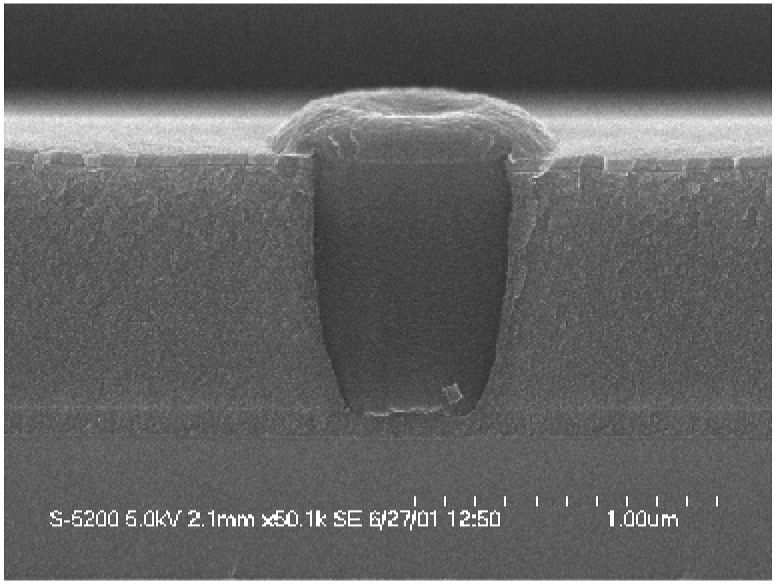
CVD SiOC Low k Film Issues

- Carbon content
- Chemical reactivity
- Reduced density

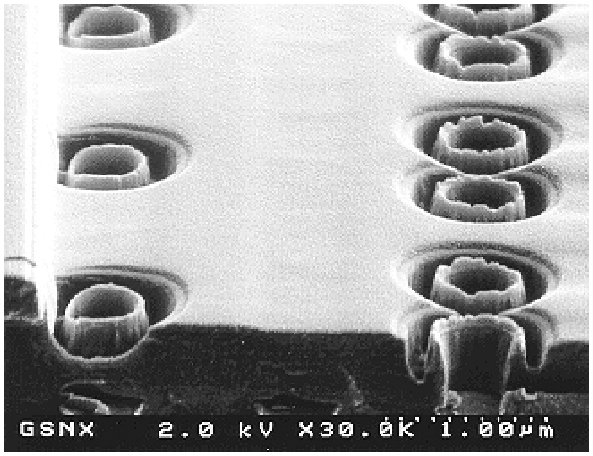


DUV Resist Poisoning

- Amines poison DUV photoresist, preventing development.
- Amines enter dielectric stacks from a number of sources.
- The phenomenon has been reported for most classes of low k films.
- Amines diffuse rapidly in low density low k films.



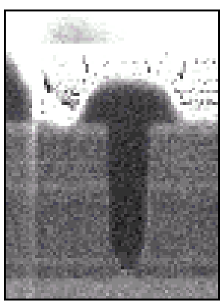
X-section view



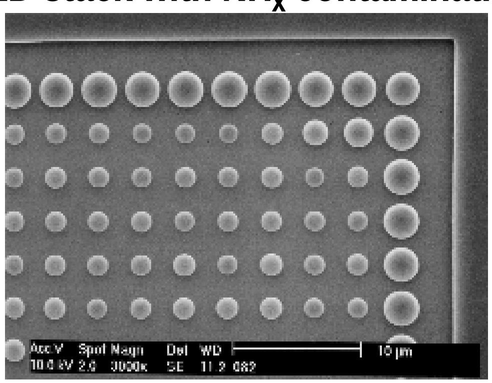
After trench etch.

DUV Resist Poisoning

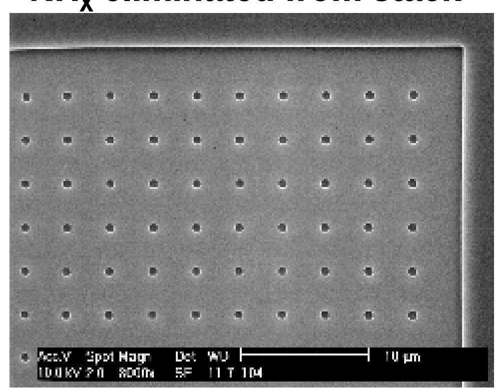
- Nitrogen in dielectric deposition processes (N_2O, NH_3) is the primary cause of DUV resist poisoning.
- Nitrogen can enter SiOC layers during barrier film pre-deposition set-up steps and during the actual depositions.
- Etch and strip steps are of secondary importance at best.
- The source material, as well as the reactor must not inject N_2 into the process chamber.

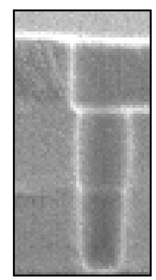


ILD stack with NH_x contamination



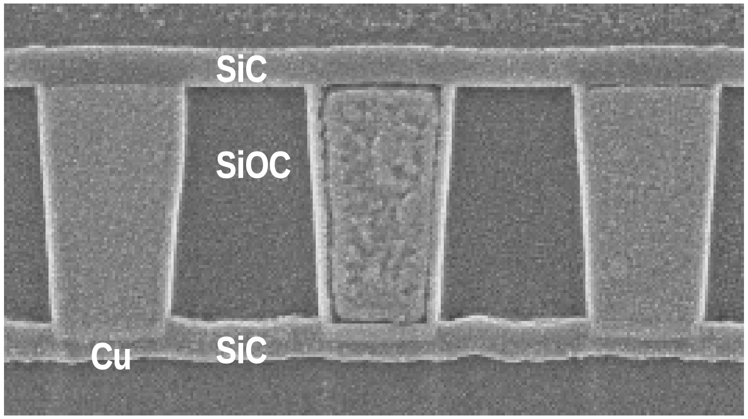
NH_x eliminated from stack





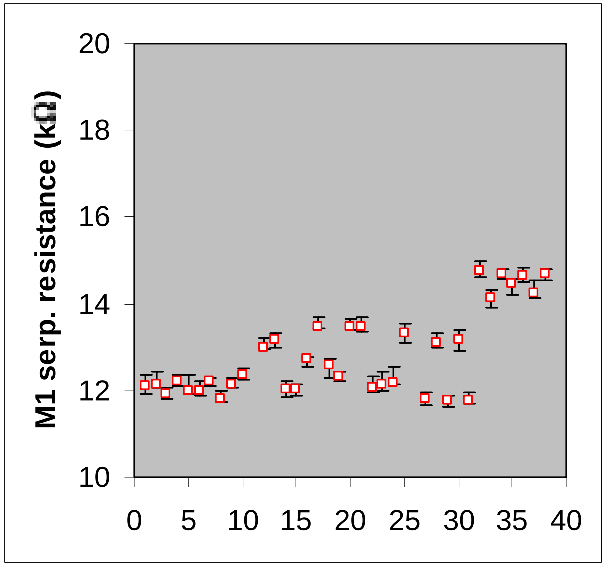
Trench Etch - Metal 1

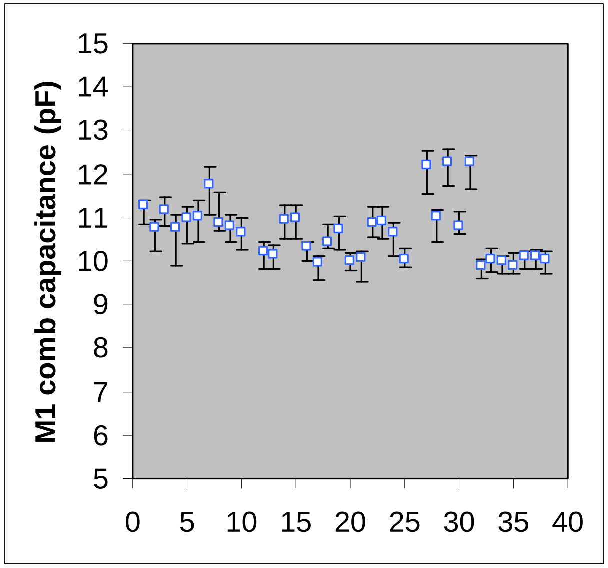
- Metal 1 trench etch is the least demanding process.
  - Low aspect ratios.
  - Etch stops used.
- M1 Etch Issues
  - CD control.
  - Profile control.
  - Microloading.
  - Uniformity.
  - Selectivity to barrier film.
- Followed by barrier open step to expose W plugs.

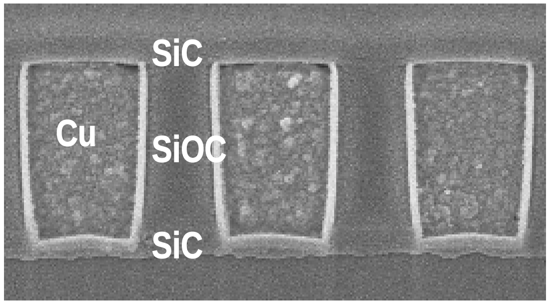


M1 Lines in SiOC low k film.

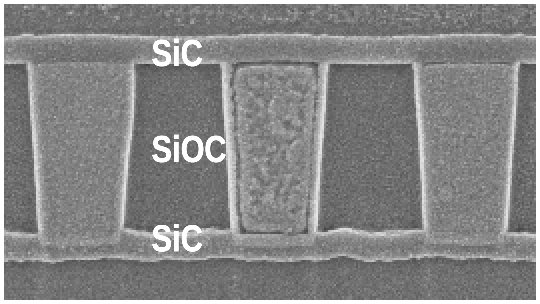
Trench Etch - Metal 1
Electrical Data versus Process Performance







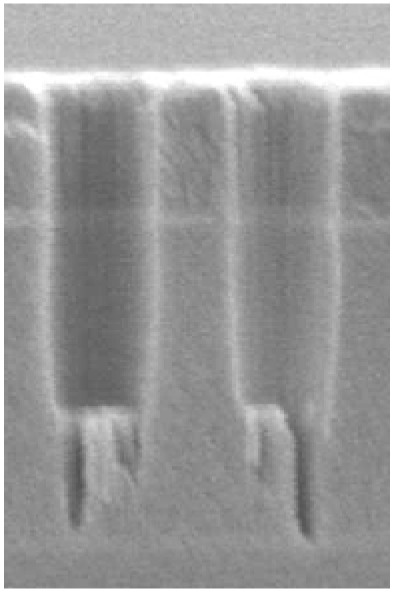
M1 lines in SiOC low k film.
Bowing and cusping.



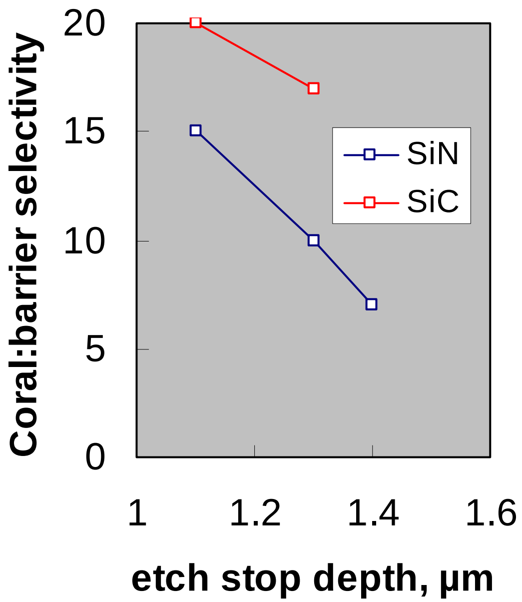
M1 lines in SiOC low k film.
Optimized process.

Via Etch Challenges
Etch Stop

NOVELLUS



0.25 Via "etch-stopped" at a depth of ~0.6µm



- The carbon content of CVD SiOC films can cause "etch stop."
  - Attainable etch depth is dependent on etch selectivity.
  - Multi-step via etches are often employed.
  - Independent control of plasma density and ion energy is desirable.

Cu 29 novellus

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Via Etch Challenges
Chemical Reactivity

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- The Si-CH_3 groups in CVD SiOC films are susceptible to attack by fluorine and oxygen atoms.
- Protective polymer thickens toward the via bottoms.
- Overetch process must be optimized for minimal bowing.

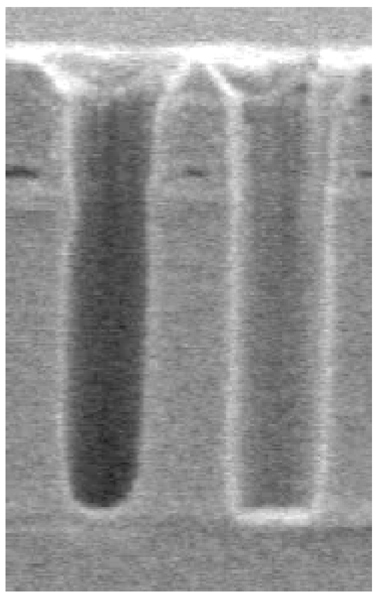
0.25 Via etched to a depth of 1.0µm

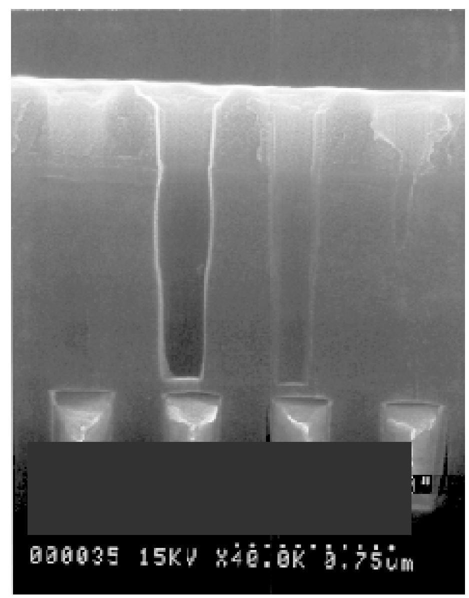
Resist

ARL

Coral

SiC:H





Via bowing caused by overetch step.

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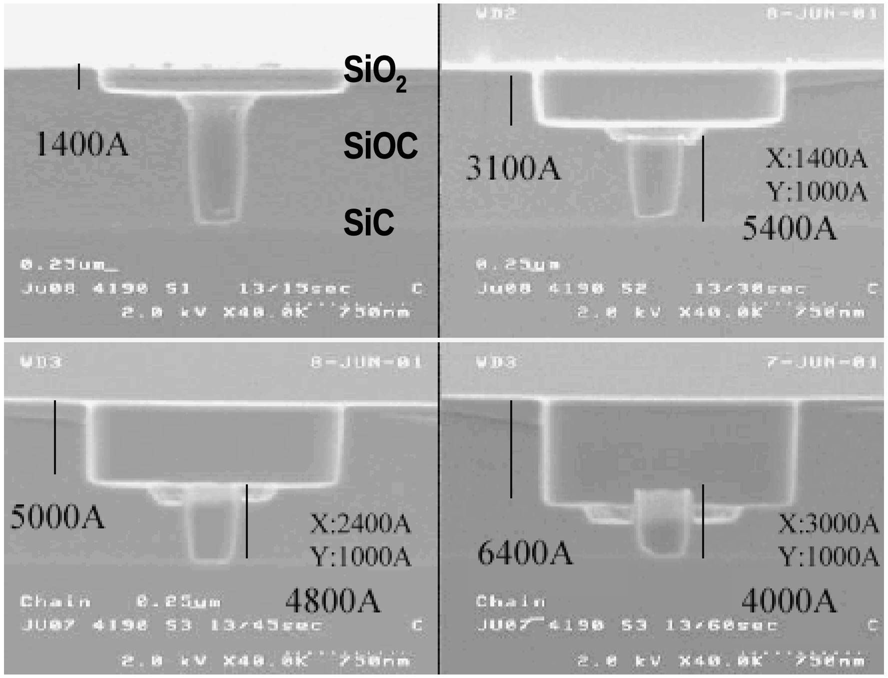
Trench-over-Via Etch: The most demanding process.

Many demands must be met simultaneously.

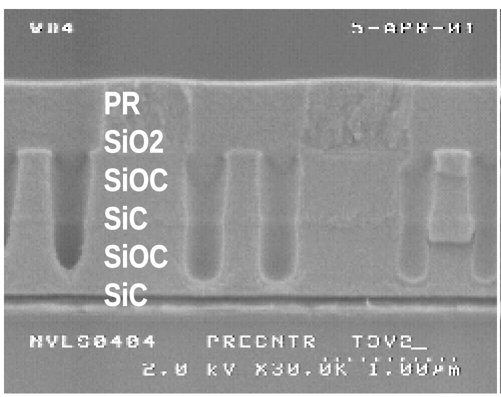
- Trench profile and CD control.
- Smooth trench bottom.
- Protection of barriers in vias.
- Via profile maintenance.
- Control of "terracing" and veil formation.



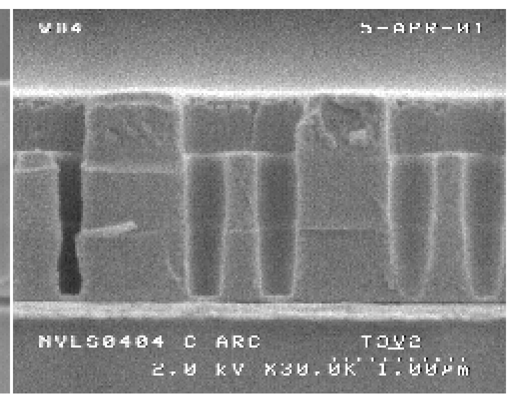
Progression of T/V etch in 0.25µm via chain feature, Resist and I-line plugs have been stripped in-situ.

Trench-over-Via Etch: Barrier Protection

- **Dual damascene processes with oxide or FSG ILDs often rely on spin-on “BARCs” to protect etch stop/diffusion barriers.**
- **SiOC:barrier selectivity is too low for this scheme to work.**



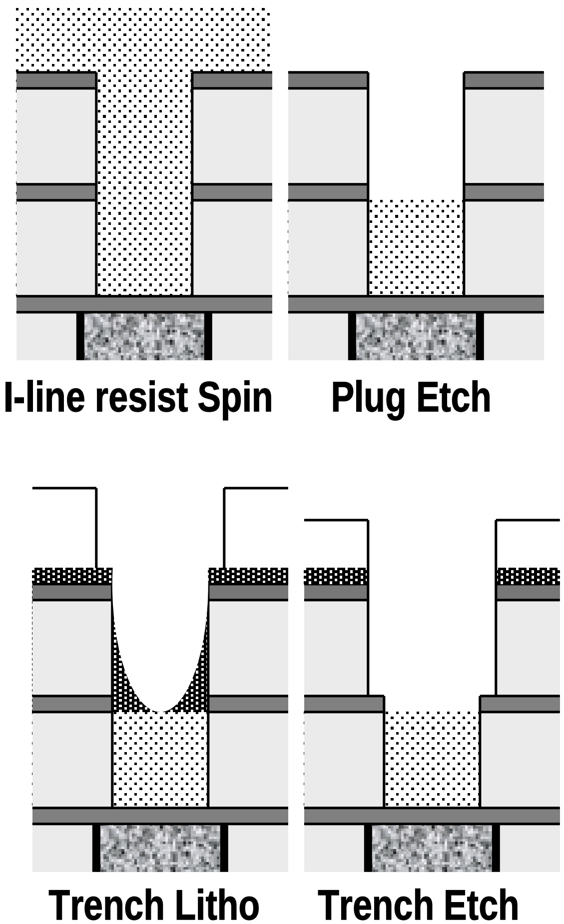
After M2 Lithography



After BARC etch

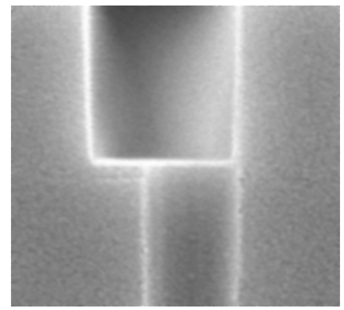
Trench-over-Via Etch: Barrier Protection

- An alternative is to form thick plugs of organic material in the vias.
  - Trench etch may be optimized for trench properties rather than selectivity to barrier.
  - Via profile can be maintained without etch stop layer.
  - Veils and terraces may also be controlled.
- Control of plug height is important.

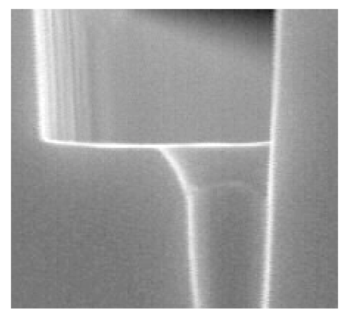


Trench-over-Via Etch: No trench etch stop layer.

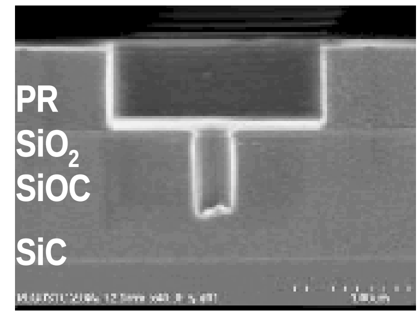
- Advanced dual damascene processes do not use etch stop layers.
  - Reduced cost.
  - Reduced effective k.
- Trench bottom profile and depth control challenging.
- Via profile protection challenging.
  - Low density SiOC films sputter more easily.

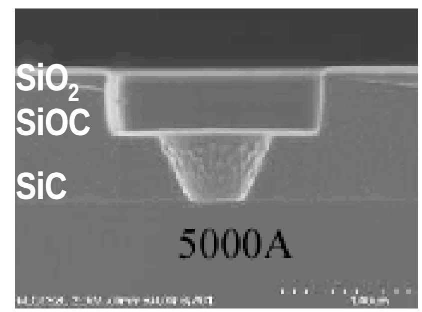


FSG DD with SiN trench stop layer.



FSG DD without trench stop layer.

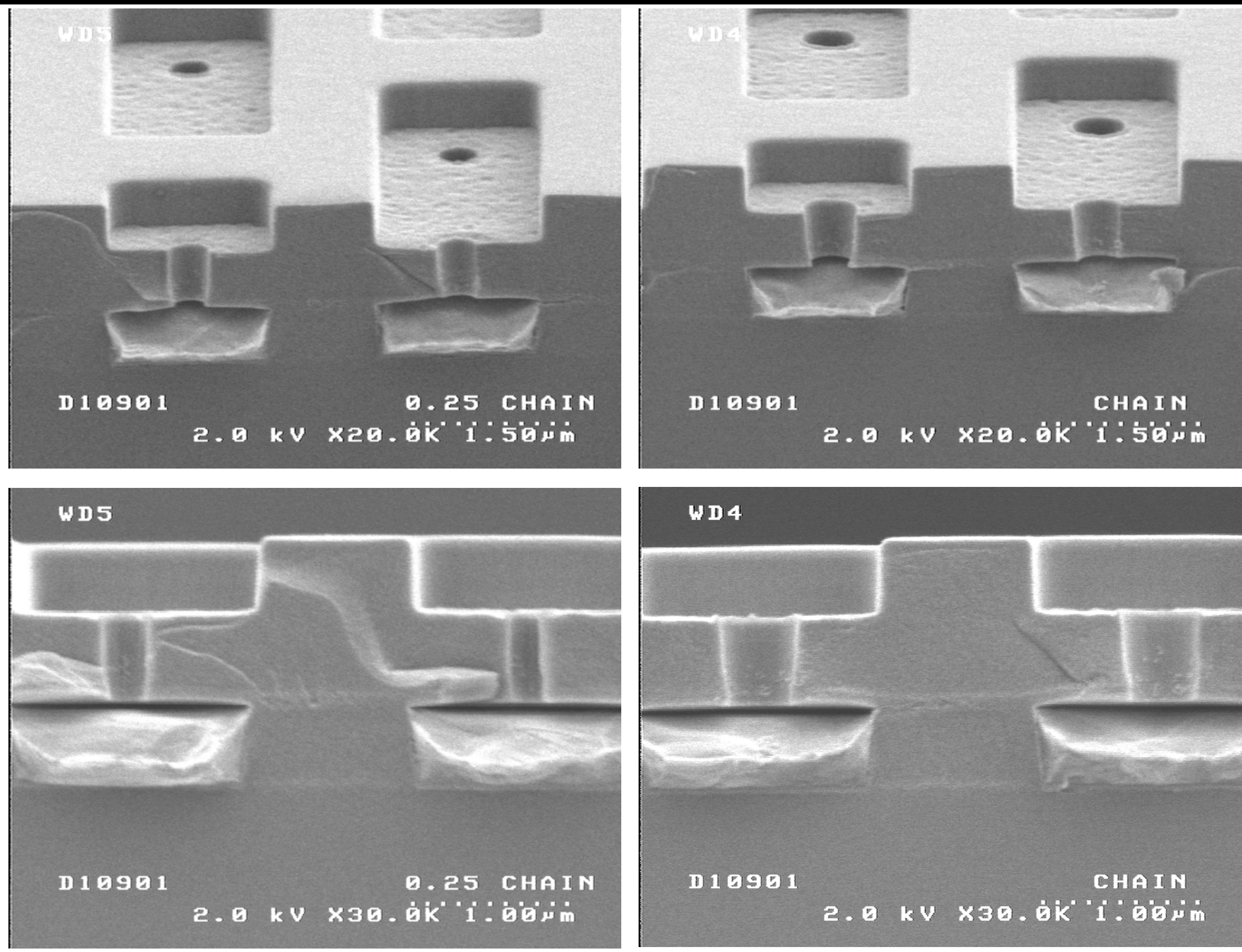




Vias in SiOC films taper rapidly during trench etch.

An Optimized Process Flow

Trench etch, deveil, resist strip, barrier open in-situ.

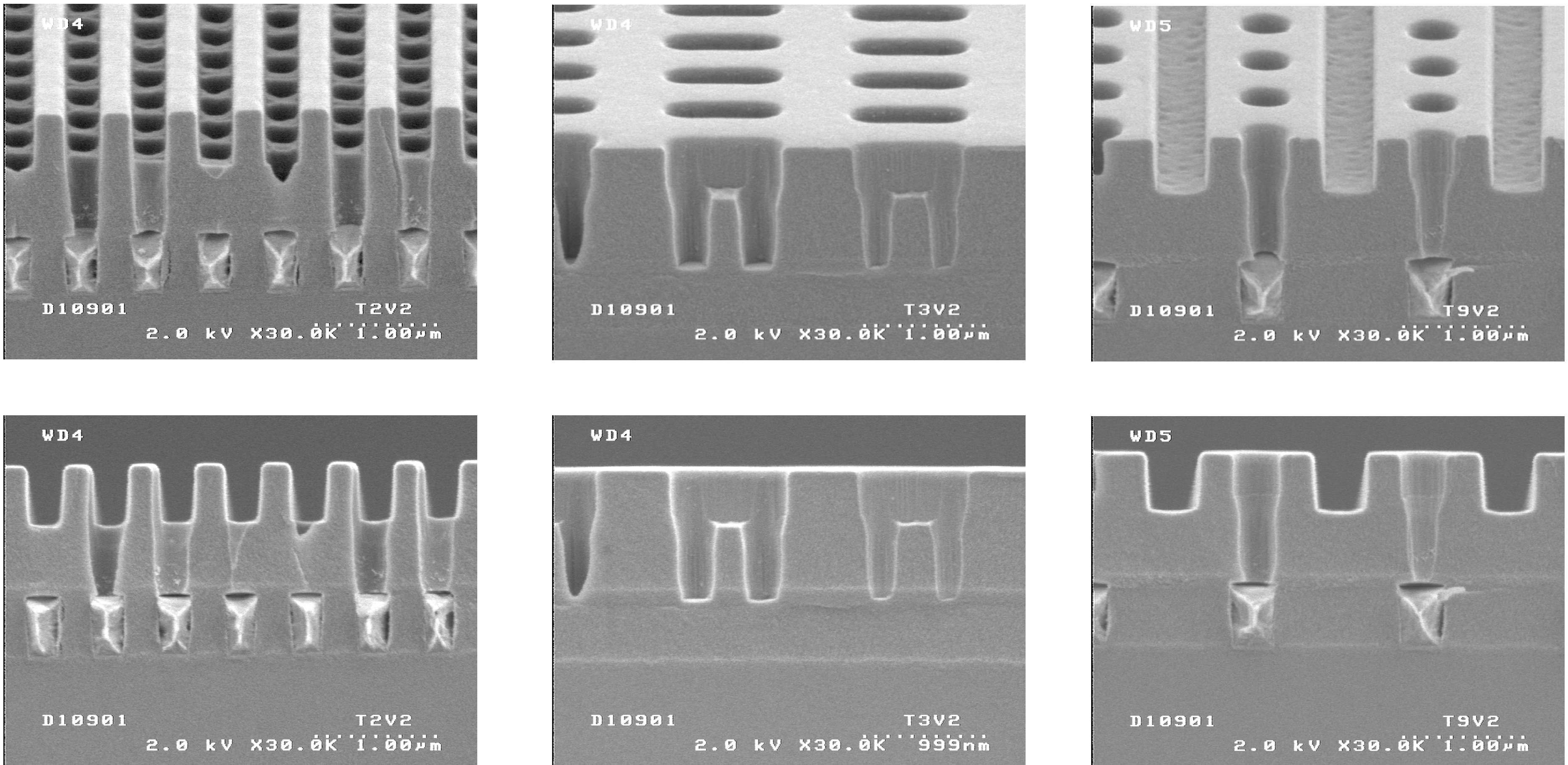


0.25µ **0.50µ**

Via chains

An Optimized Process Flow

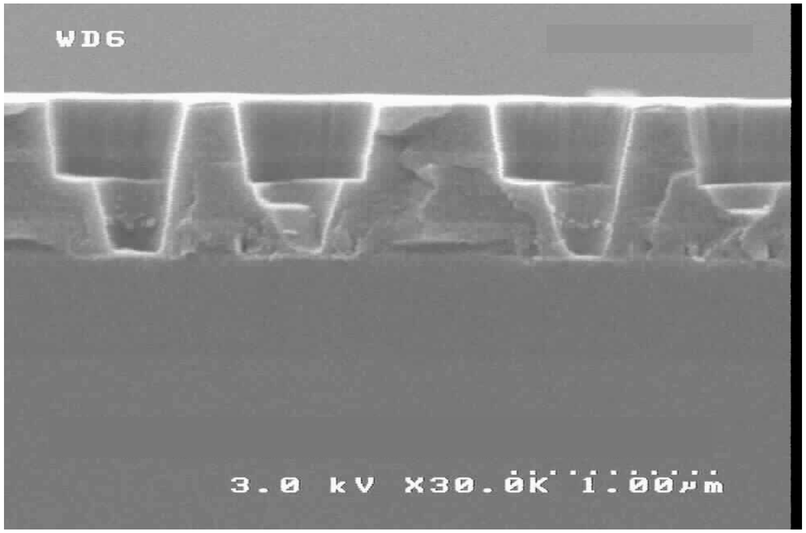
Trench etch, deveil, resist strip, barrier open in-situ.



Various trench dimensions over 0.25µ vias

Barrier Open Etch: Profile Alteration

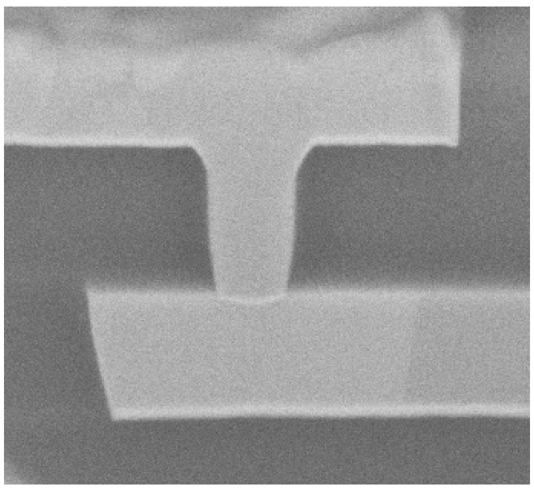
- **Seemingly simple etch, however excessive sputter enhanced feature tapering can**
  - **Alter CDs**
  - **Reduce yield**



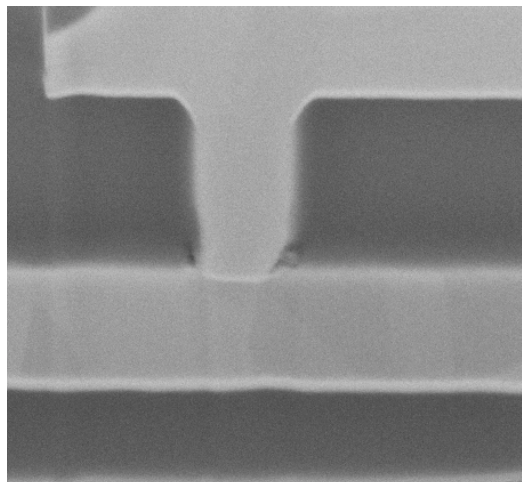
SiC barrier etch with excessive SiOC tapering.

Barrier Open Etch: Undercut

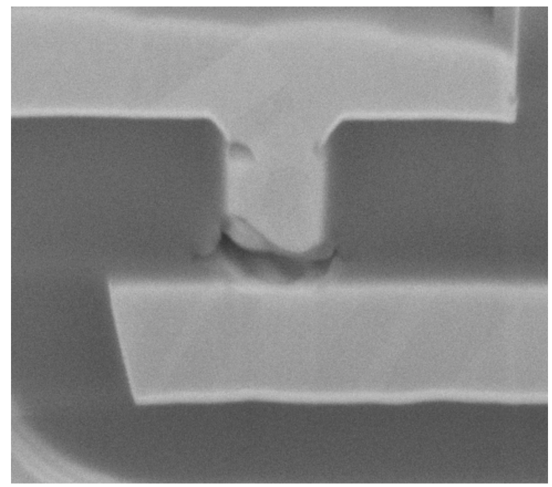
- **Isotropic barrier open processes compromise**
  - **Barrier and seed step coverage.**
  - **ECD copper fill.**



Directional barrier etch allows good via fill by ECD Cu.

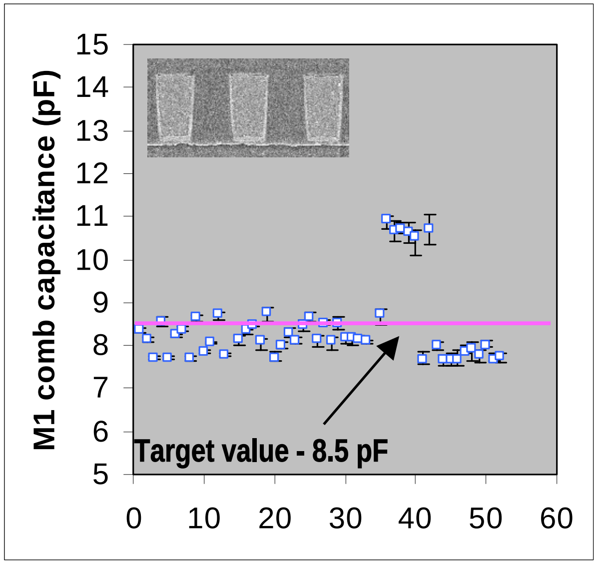


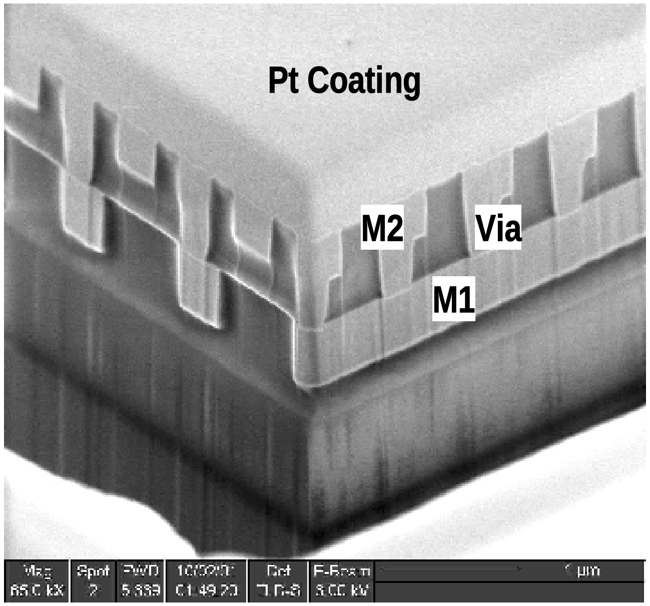
Isotropic barrier etch causes poor barrier/seed step coverage and voids in ECD Cu.



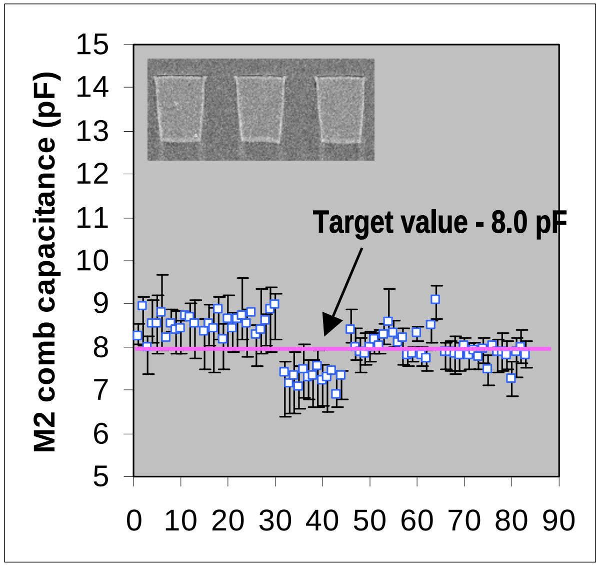
Vias with Cu voids fail during normal thermal cycling.

Dual Damascene Electrical Data





0.25 µm 2-level Metal Structures



Summary

- The introduction of the dual damascene architecture eliminated old challenges,
  - Aluminum etch
  - Dielectric gap fill
- And replaced them with the new dielectric etch challenges that were discussed here.
- New challenges are here,
  - 193nm photoresist
  - Thinner barriers
  - Porous dielectrics