Sub 0.1um Gate Etch Challenges for Memory Applications

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Outline

- New Gate Oxide
  - Why?
- New Gate Stack
  - Why?
  - Options
  - Etch requirements
  - Current Performance on preferred Option
  - Challenges
- Other Risks

Advanced Gate dielectric

- **Challenge**
  - **13 and 18 A EOT**
  - **1 σ < 1.5 % at 13 A and 18 A**
  - **Device to perform at 1.32 Volts Max.**
  - **Leakage of 1E-4 at EOT of 13 A**
  - **Block boron from P+ poly silicon**
  - **No negative impact on mobility compared to exisiting technology.**
  - **TDDB**
  - **Dit < 1E11**

- **Problems with current Furnace Oxide**
- Cannot scale below 16.78 A (optical) which is around 22 A EOT
- Can optimize for boron blocking and mobility within very narrow window..

- **Solution**

  - **Nitridated Gate Oxide < 20 A**

Big Challenge for Etch , Cleans and metrology!!

GATE Roadmap

- **Requirements:**
  - N+, P+ type gate to optimize NMOS & PMOS performances
  - Low resistivity material
  - Minimized depletion on N/PMOS transistor
  - Compatible with SAC. Need SAC for Cell size.
- **Options:**
  - N+/P+ Poly /Wsix : Rs too high (25 Ω/) and process too complex
  - N+ and P+ type metal gate : too early ; definition phase
  - N+/P+ Poly / Barrier/Metal gate
  - Logic process N+/P+ Poly / CoSi2 is the simplest approach but incompatible with SAC
- **Proposed Roadmap**:
  - N+/P+ Poly / Barrier/Metal gate

Poly/Barrier/Metal GATE

- **Scope of Work**

  - To develop Dual Poly/ Barrier/ Metal /Hard mask Gate stack based on previous Wsix process.

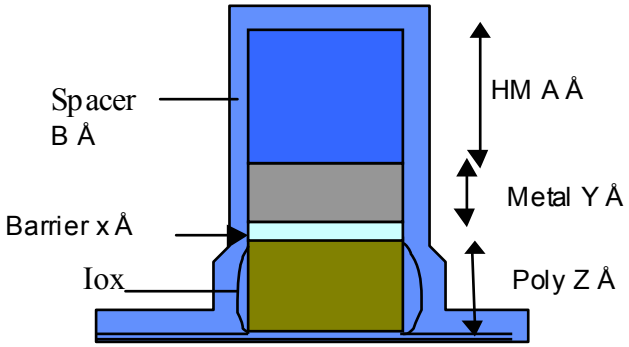
- **Hypothesis**
  - **Replacing WSix by Metal will give Gate Rs = 5 ohm/[]**
  - **No dopant diffusion through metal strap with barrier**
- **Steps**
  - **Metal deposition : CVD /PVD**
  - **Barrier Layer: reactive sputtering**
  - **Hardmask gate capping (Compatible with Metal Gate)**
  - **Gate stack etch**
  - **New cleans compatible with Metal Gate**

Poly/Barrier/Metal GATE

193 nm PR for 0.1 um CD.

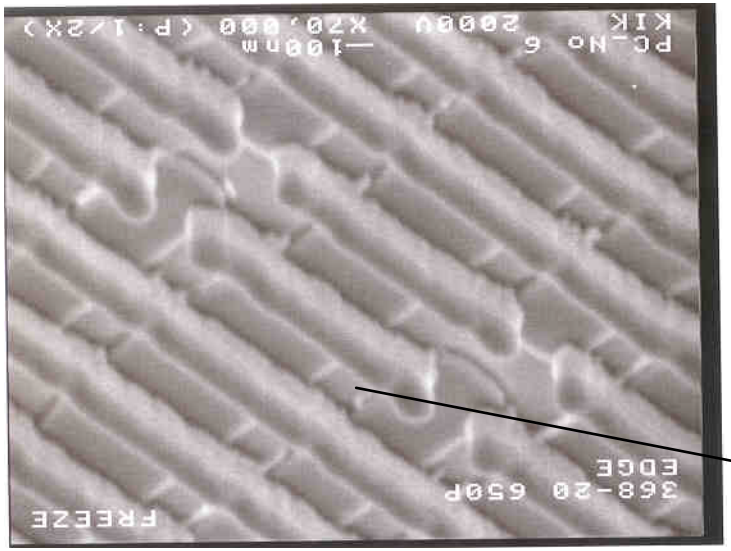
- **Requirements:**

Physical cross-section

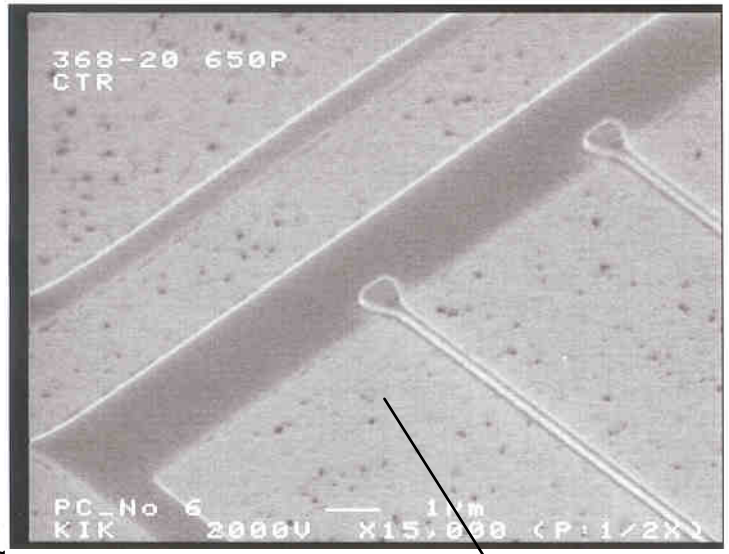


- HM:PR Sel > 2-3:1
- Metal: HM Sel > 3-4:1
- Metal:PR >2:1
- Metal: Poly >3:1 since Poly is Thin
- Endpoint for OX <20 A
- CD Range within wafer <7 nm
- Iso -Dense < 5 nm
- Gate Trimming upto 20 nm

Stringers and Pitting



Stringers



Pitting

- Stringers and Pitting on same wafer with SF6/N2 Metal Gate.

Rev 1 with 248 nm PR

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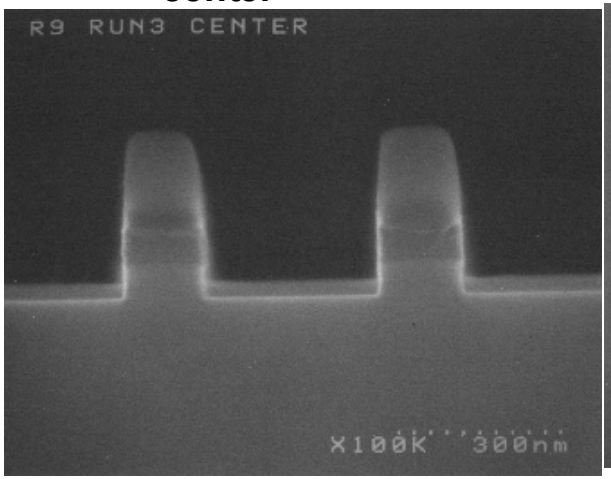
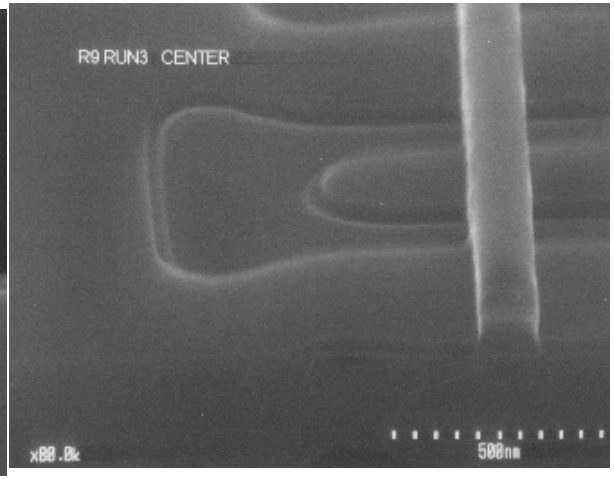
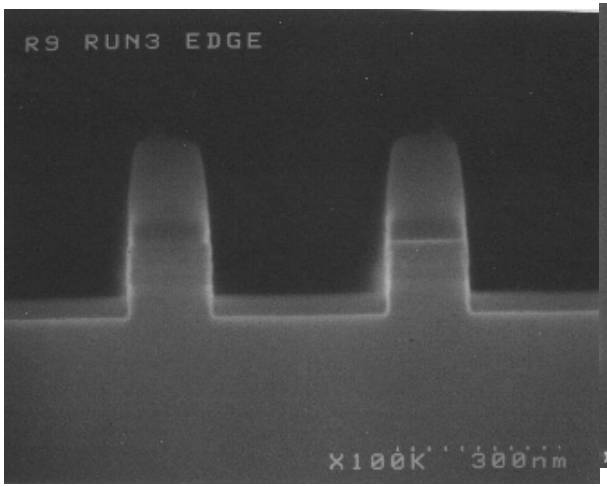
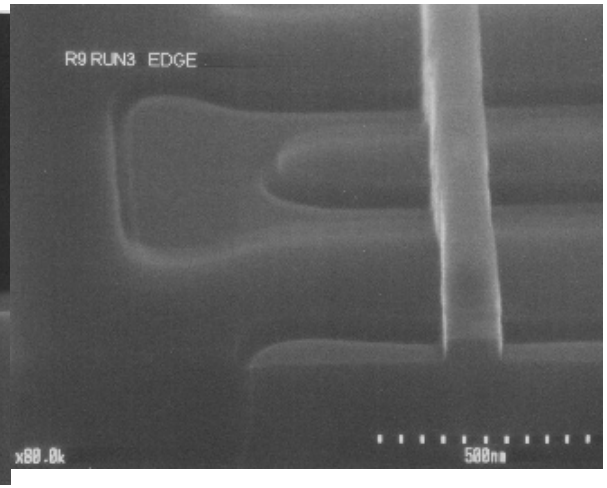
center









edge

Dist	FICCD	FI MOD	FI ISO
78.74839226	0.1643	0.1581	0.168
92.23617874	0.1731	0.172	0.1854
58.83407919	0.1685	0.1571	0.167
78.90923136	0.167	0.1549	0.1776
40.83137744	0.1698	0.1611	0.1704
43.27996605	0.1701	0.1572	0.1803
13.56461817	0.1686	0.1623	0.1723
42.86483932	0.1627	0.1559	0.1755
59.47856754	0.1732	0.1537	0.1858
13.44716108	0.1693	0.1618	0.1815
75.5255594	0.1639	0.1546	0.171
32.65008449	0.1697	0.1618	0.1774
58.57713244	0.1696	0.1621	0.1607
58.39369838	0.167	0.1637	0.166
94.46089853	0.1702	0.1599	0.1752
84.92485632	0.1666	0.1572	0.1661
Average	0.16835	0.159588	0.173763
Range	0.0105	0.0183	0.0251
3*STDEV	0.008963	0.013676	0.021985

What This Means:

- **ISO Range needs improvement**
- **Over 800 A of HM loss during Metal Gate etch**

N+/P+ Profile Differences

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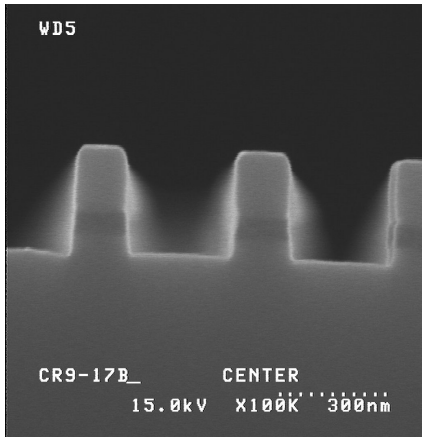
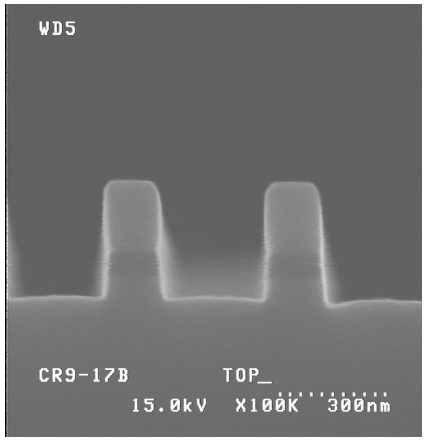
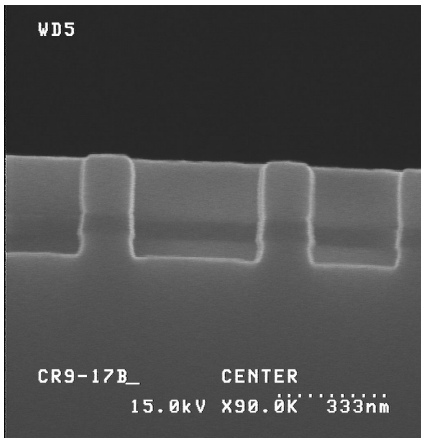
Center **TOP**

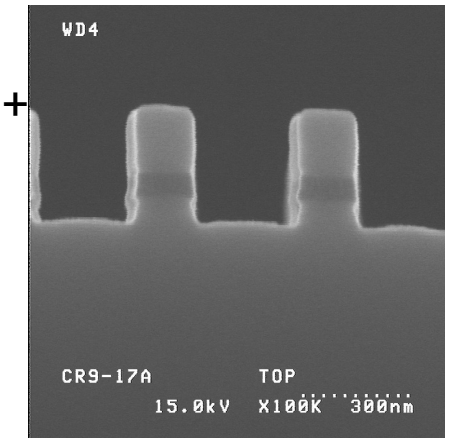
P+





N+

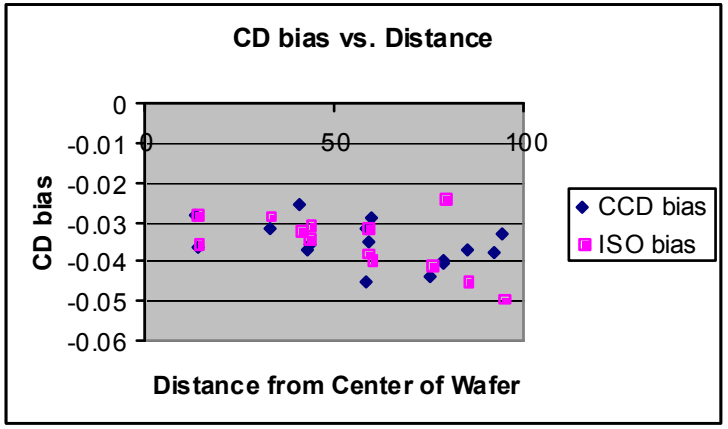




-40 nm Etch bias

Post	CCD bias	Pre
0.1266	-0.04	
0.134	-0.0377	
0.1274	-0.0352	
0.1261	-0.0405	
0.1309	-0.0258	
0.1272	-0.0359	
0.1262	-0.0366	
0.1269	-0.037	
0.1332	-0.0288	
0.1277	-0.0285	
0.1194	-0.0438	
0.1279	-0.0317	
0.1327	-0.0314	
0.1209	-0.0454	
0.1313	-0.033	
0.1271	-0.0373	
0.127844	-0.03554	Average
0.0146	0.0196	Range
0.012008	0.016421	3*STDEV

Post	ISO bias	
0.1289	-0.0238	
0.1161	-0.0318	
0.1115	-0.0305	
0.111	-0.0352	
0.1188	-0.0339	
0.1101	-0.0391	
0.12	-0.0279	
0.1142	-0.0405	
0.1166	-0.0281	
0.1192	-0.0313	
0.1179	-0.0375	
0.1197	-0.0491	
0.1095	-0.0445	
0.116423	-0.03486	Average
0.0194	0.0253	Range
0.016001	0.021407	3*STDEV



What This means:

- Edge CD bias larger for R9 as well.
- R9 also has poor iso CD Range issue

PR Selectivity-193 nm with Sumitomo *Advanced Technology*

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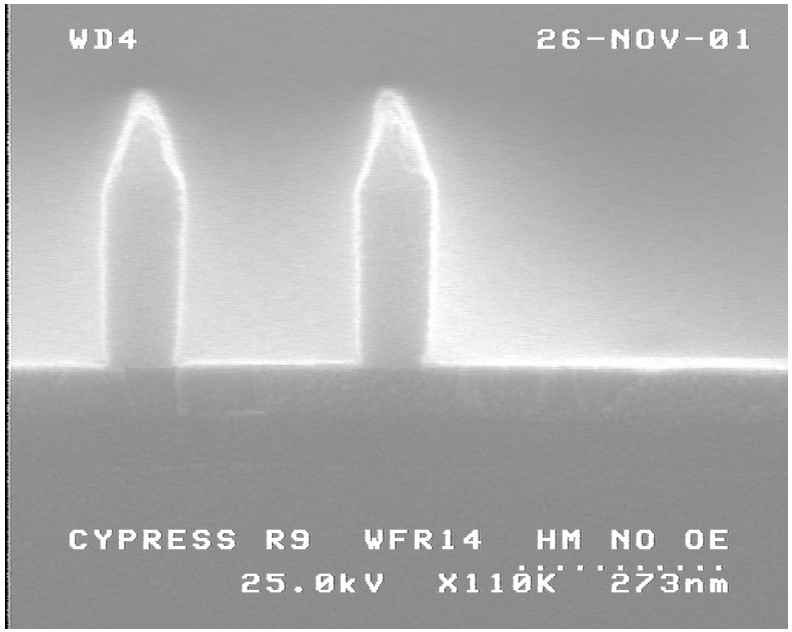
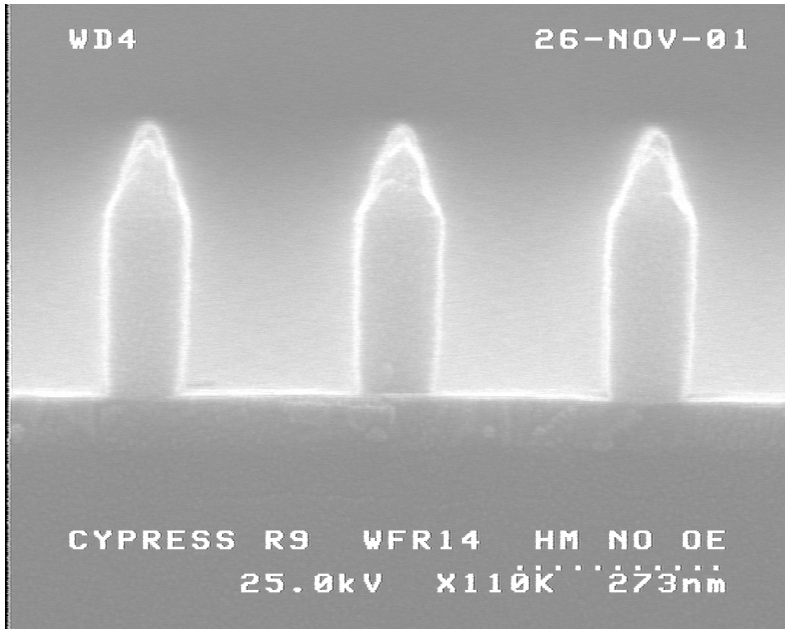


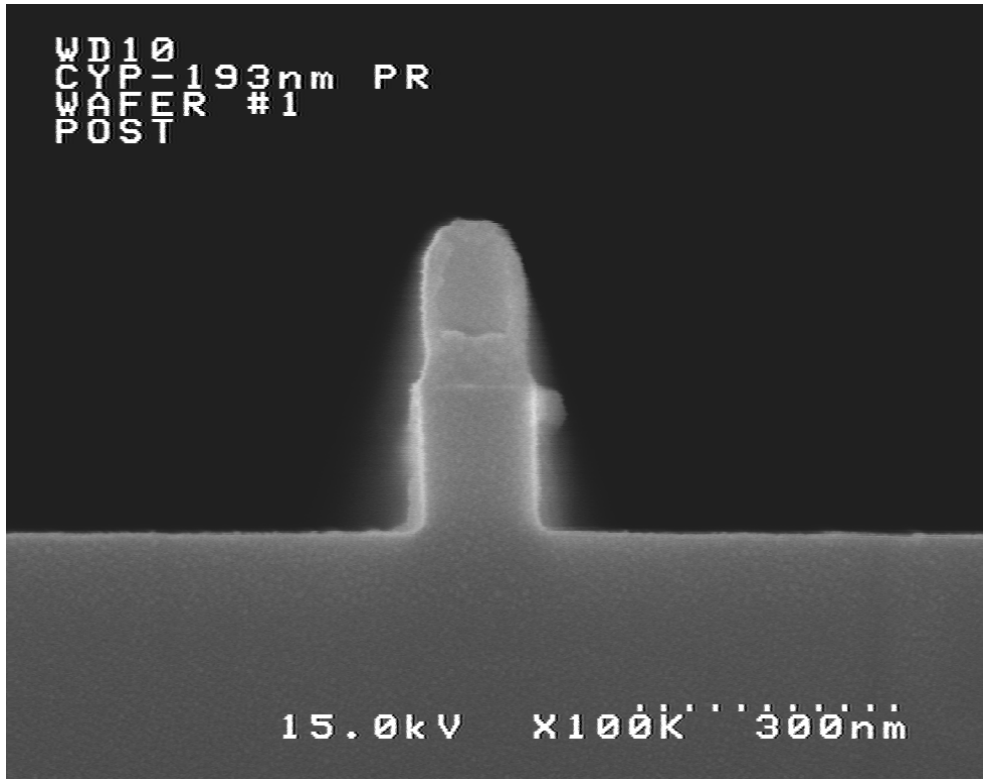


PR+BARC≈ 1080Å

SiN:PR ≈ 1.25:1 at the top

≈ 1:1 at the facet

PR Selectivity-193 nm with JSR



SEM Image - CF4 BARC Open + CF4/CHF3 SiN Main Etch
Selectivity ~ 1.5:1

193 nm Mask open SEM (JSR)

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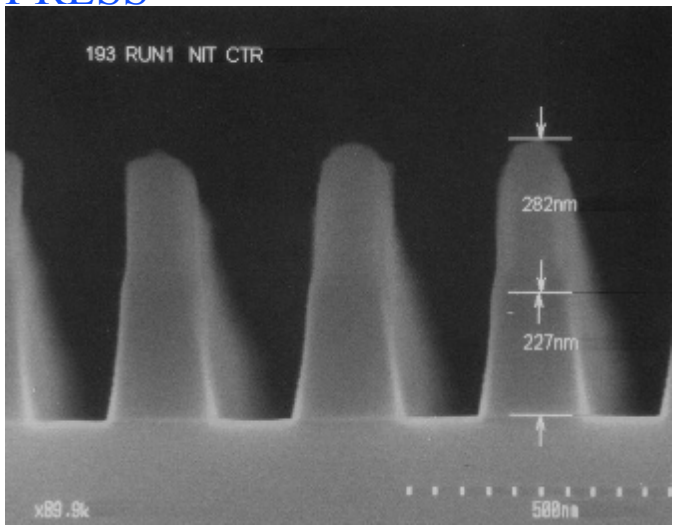
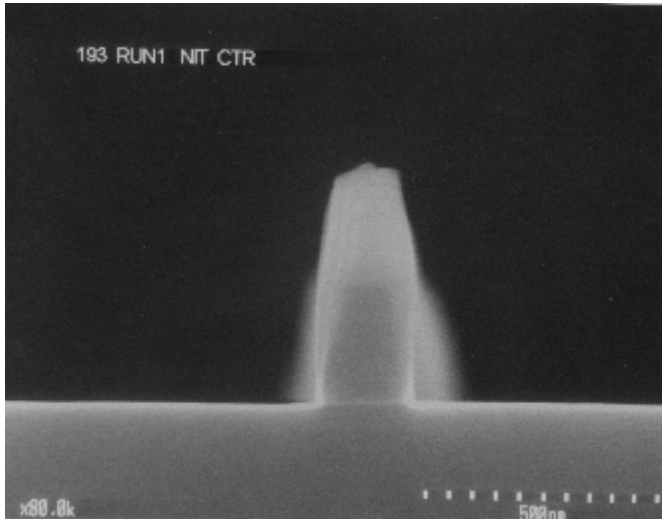
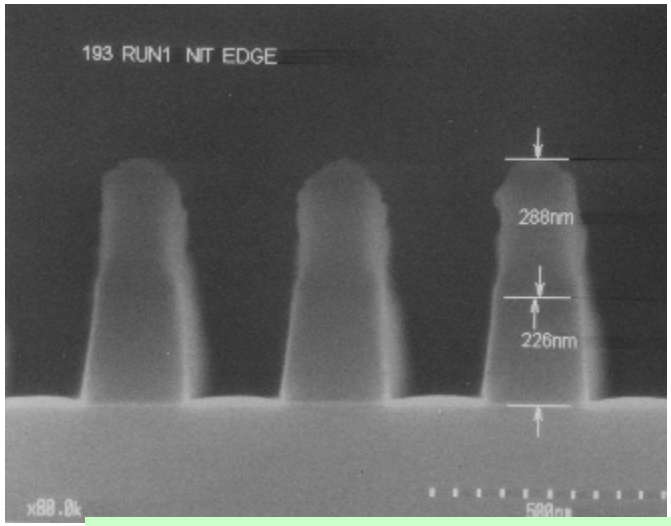
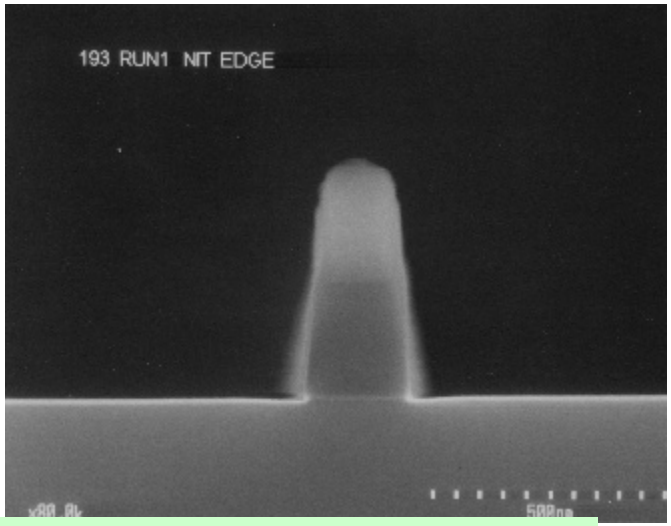
Wafer center





Wafer edge





280nm PR+BARC remaining after Nitride etch.

0.1 Poly Gate with Trimming

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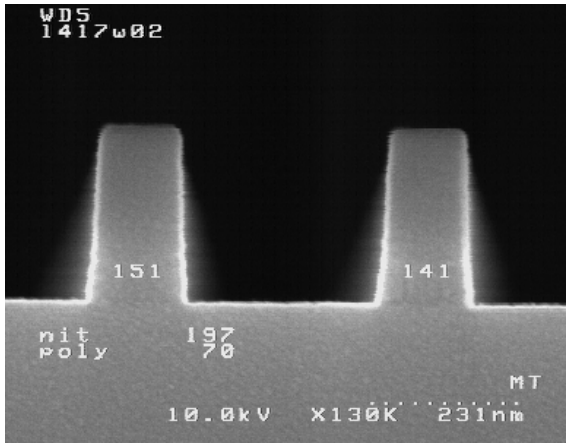
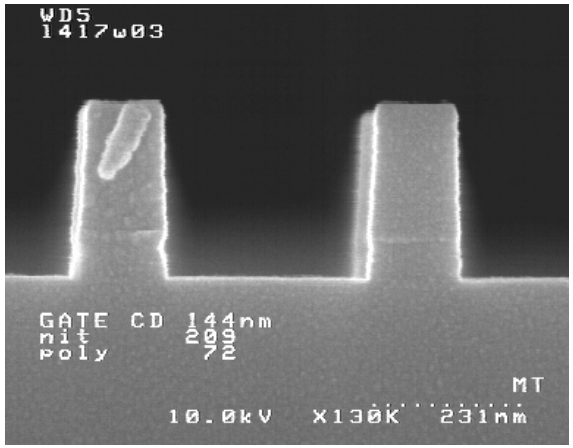
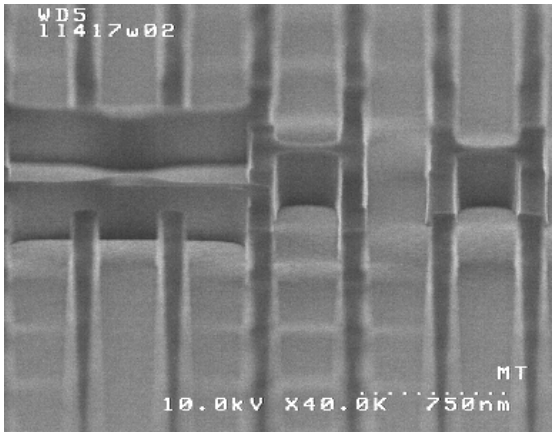
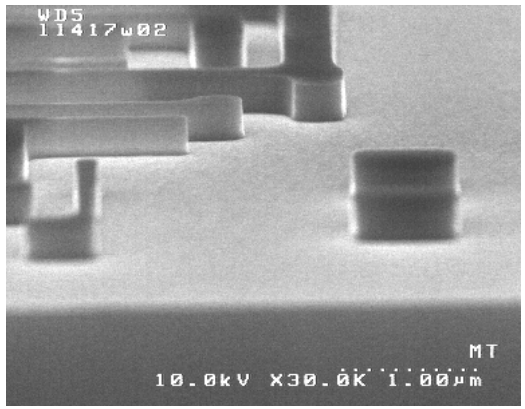
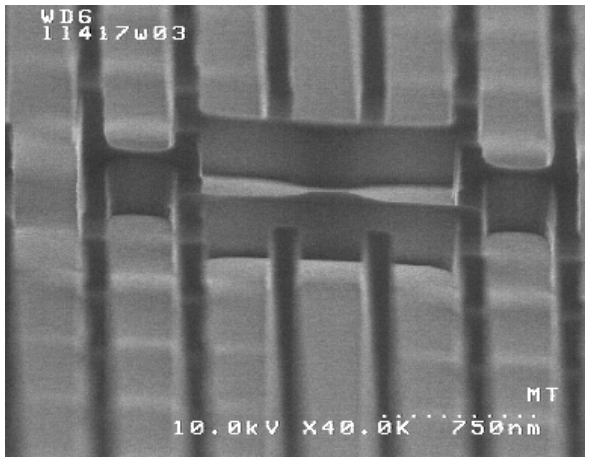
DICD = 0.175 um



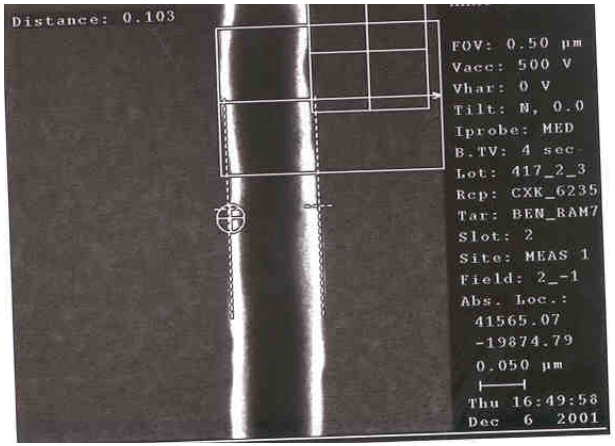








Field 2 (Exp= 32 mJ) = FICD 0.135 um as per Verasem
MOD 111 = 0.105 um



Gate Etch Line Trimming

Hypothesis

Lower ARC BP and more O2 in ARC etch encourages more isotropic etch, trimming lines

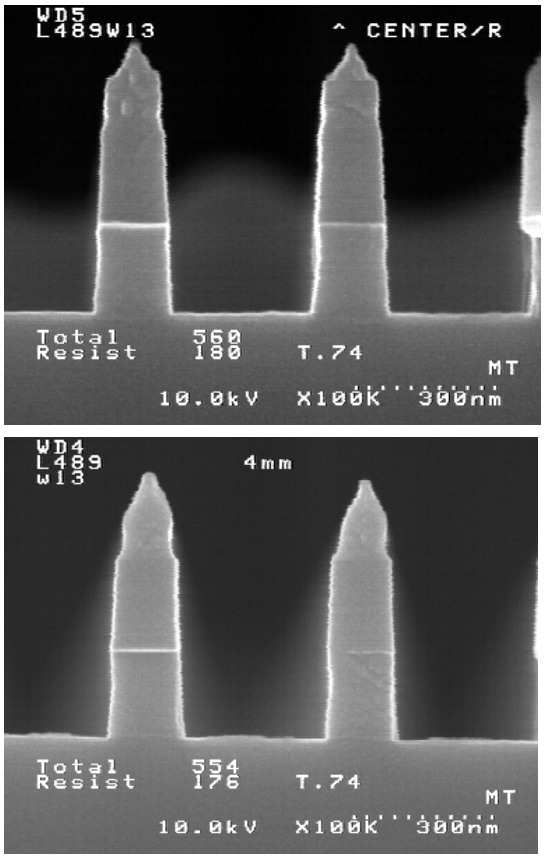
Experiments

Monitor CD bias for all features over various ARC BP and HeO2 flow. Check for the resist budget. Wafers with R7 process flow were used.

Results

- 35nm bias with trimming achieved
- no change in CD uniformity seen
- 248 nm Resist budget issues!!
- trimming >35nm requires trimming in HM step as well

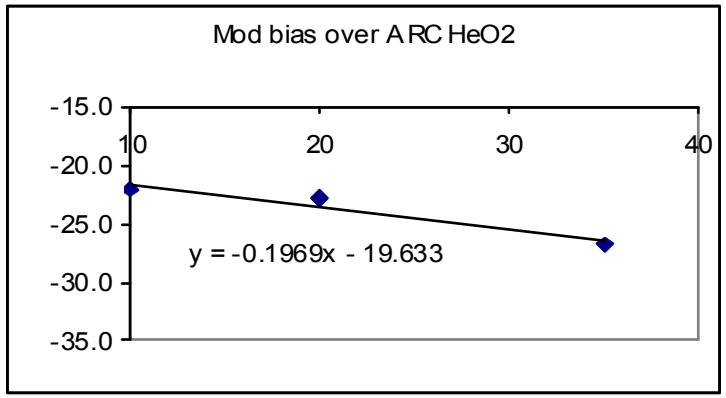
(65BP,20HeO2) post etch (-23nm mod bias)

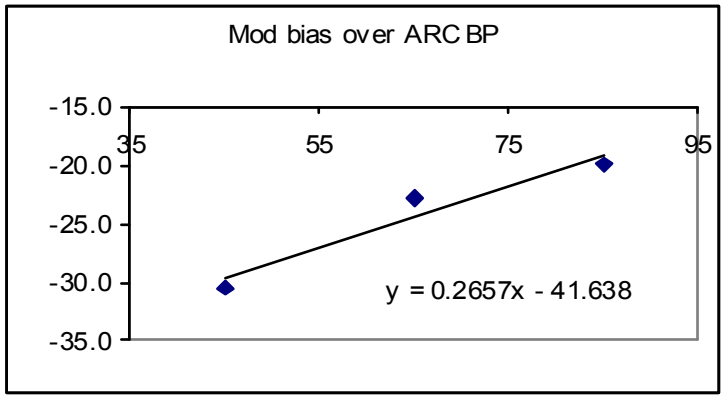


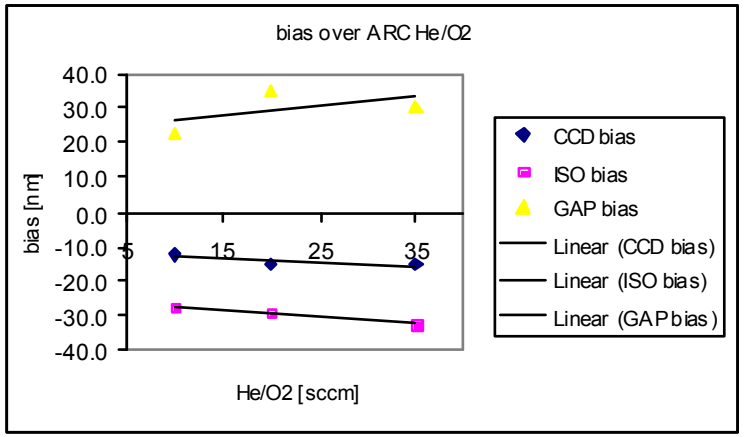
Resist remaining on shoulder ~850A

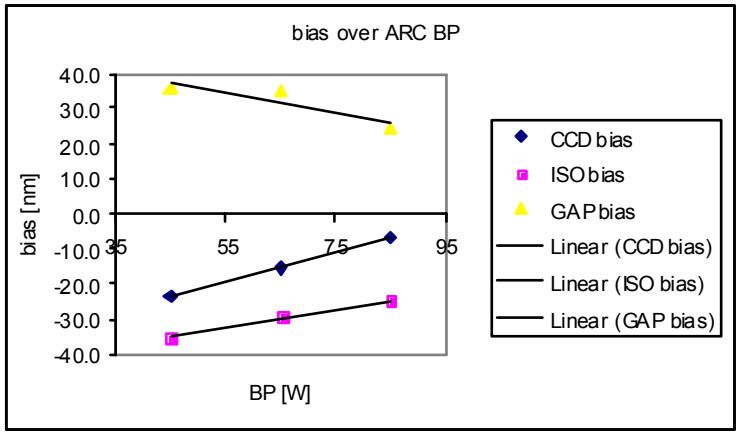
Gate Etch Line Trimming

- **Results - CD Performance**
  - CD trimming with ARC BP and ARC He/O2 is possible (>-35nm MOD141).









Other Metal Gate Risks

- **Risks**
  - **New Cleans need to be developed. H2O2 attacks Metal gate. Alternative solutions being looked at.**
  - **Current Alignment strategy may not work due to signal strength, reflectivity etc. Alternative solutions being looked at.**
  - **HM Film peeling/ new ReOX process etc. Solutions being worked on.**

APC/Integrated Metrology for CD Control

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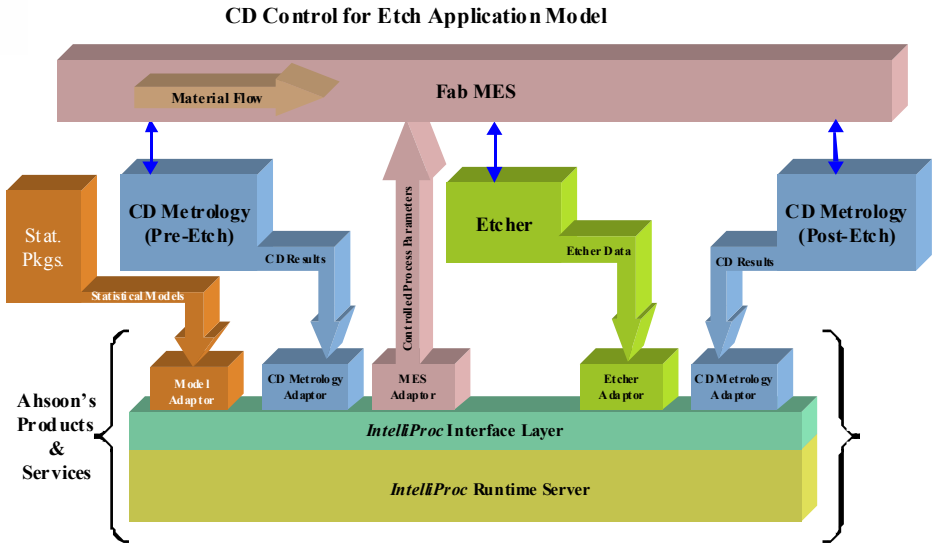
TRANSFORMA PATTERNING SYSTEM

- **Enables Improved CD Control:**
  - Allows compensation of incoming resist variation delivering higher speed devices without yield loss due to high leakage current.
- **Transforma Combines:**
  - Sub 100nm capable DPS II Silicon Etch chamber (300 / 200mm capable).
  - Centura 300 mainframe with Applied standard Factory Interface.
  - Integrated Optical CD Metrology.
- **Onboard Metrology:**
  - Provides real time non destructive measurement of critical dimension and profile of patterned lines.

- There is a need for APC for better L2L and W2W
- CD control, not necessarily new metrology tools

***IntelliProc* Product Concept**



Line Edge Roughness

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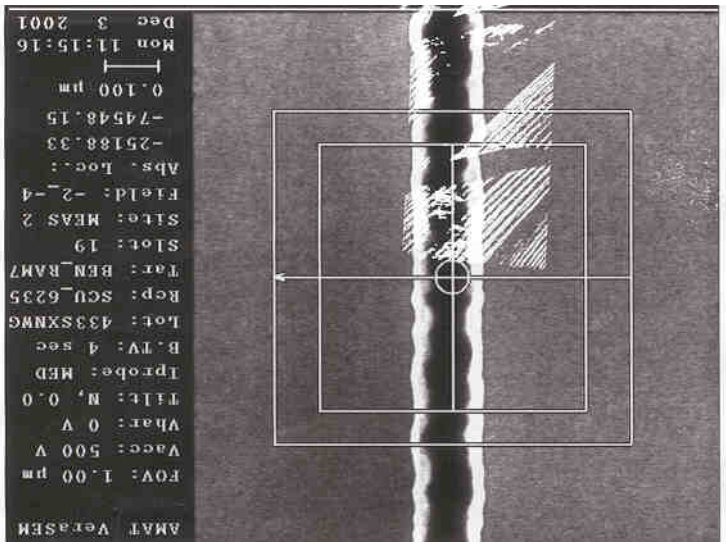
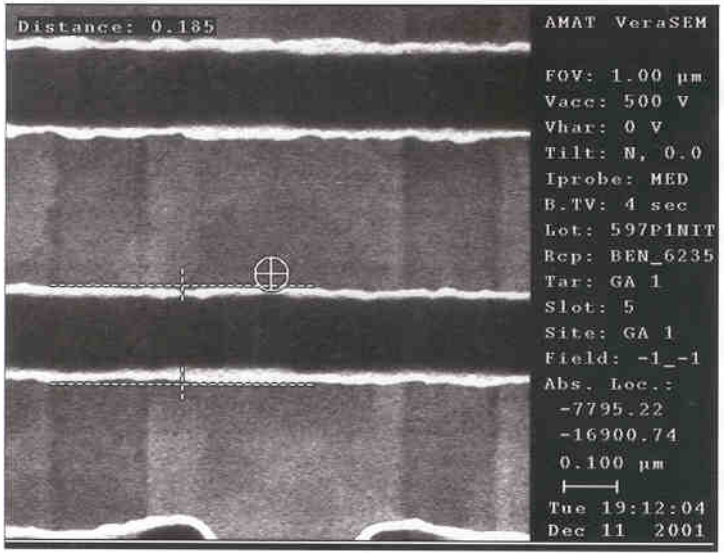
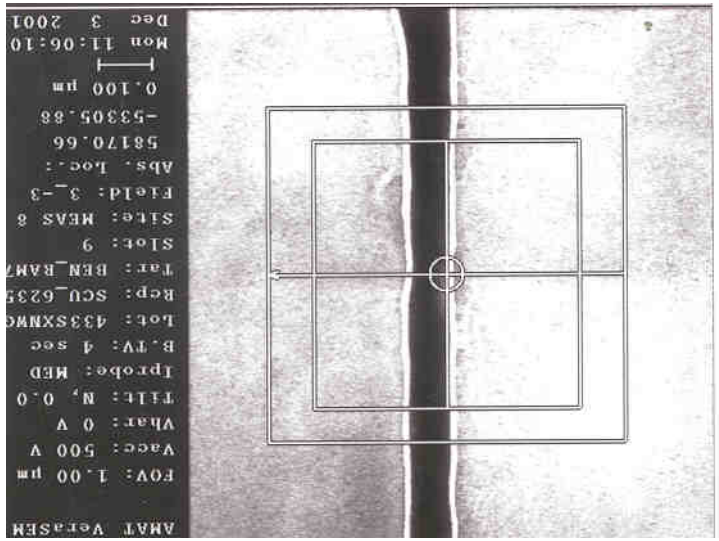


Process Development

to improve SiN:PR sel





What This means:

- Line edge roughness can be reduced by choosing higher SiN:PR sel process.
- New metrology methods being standardized for quantifying LER which may be an issue for 193 nm and its impact on device parameters

Acknowledgements

- Benjamin Schwartz, Sundar Narayan, Chan-lon Yang, Alain Blosse, Wade Xiong, Sam Geha, Shahin Sharifzadeh and K. Ramkumar Cypress Semiconductors R&D, San Jose
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