

NCCA VS Joint Users Group

Virtual Meeting (CMPUG, PAG, TFUG)

"Advanced Packaging Technology"

June 10, 2020

Wednesday, June 10, 2020

2:00-5:00 p.m. PST

Please check time accordingly:

[Link to time converter](#)

When: Jun 10, 2020 02:00 PM Pacific Time (US and Canada)

Topic: Packaging

Please click the link below to join the webinar:

<https://us02web.zoom.us/j/89255133331>

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Organizing Committee:

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Paul Werbaneth, 3D InCites

Rob Rhoades, Revasum

Zoran Misetic, Kurt J. Lesker Company

AGENDA:

2:00 pm: Intro and Welcome

2:05 pm: *Plasma Dicing - The "Next Normal"*

Richard Barnett, Senior Product Manager, Etch Products (SPTS Technologies Ltd, Newport, UK)

2:35 pm: *Heterogeneous Integration Roadmap and the Revolution Enabling Future Progress,*

Dr. Wilmer R. Bottoms, Chairman, Third Millennium Test Solutions

3:05 pm: *Surviving the Heat Wave -*

A presentation on thermally induced failures and reliability risks created by advancements in electronics technologies...and How Modeling Early in the Design Process can Identify these Issues,

Greg Caswell, ANSYS

3:35 pm: *Heterogeneous Integration Competence Center - An Open Access Innovation Incubator,*

Garrett Oakes, EV Group

4:05 pm: *Solving the DataCenter Energy Crisis with Silicon Photonics and Overcoming Photonics Wafer-level Test Challenges,*

Dr. Sia Choon Beng, FormFactor



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ABSTRACTS AND BIOS:

Plasma Dicing - The "Next Normal"

Richard Barnett, Senior Product Manager, Etch Products (SPTS Technologies Ltd, Newport, UK)

Silicon DRIE, also known as the Bosch Process, is a well-established plasma process for etching deep vertical features in silicon. Developed originally for the MEMS market, the process can also be used for deep TSV etch in 3D WLP and has more recently been further developed as an alternative to mechanical saw or LASER dicing. Plasma dicing offers low damage die singulation, resulting in stronger die, with significant cost/throughput advantages for small/thinner die. As the adoption of plasma dicing continues to build momentum, the barriers to adoption continue to be broken down. This paper will highlight some of our recent work in these areas. There will be examples of how SPTS, and our partners, have managed the necessary use of fluorinated chemistries and mitigated the potential risks for subsequent steps, investigating a range of conventional coatings, and both wet strip and novel dry strip options. Further development of the LASER groove will also be covered, underlining the importance of achieving a successful process integration with the DRIE step. A update on the development of plasma dicing of GaAs would also be presented.

Bio: Richard Barnett is Senior Product Manager for Etch Products at SPTS, with over 20 years' experience in a number of fields in the semiconductor industry.

In 2007, he joined what was then Aviza Technology, becoming a part of the etch product management team utilizing his background in DRIE processing to help achieve a market leading install base for that technology.

He is responsible for the management of SPTS' Mosaic plasma dicing product line and has written and presented many papers about this disruptive new approach to die singulation.

Richard graduated from The University of Nottingham in the UK with a Bachelor's degree in Materials Engineering and Electronics before entering the semiconductor industry. His roles have bridged the various parts of the supply chain including fab process engineering, wafer supply, equipment vendor process engineer and product management.

Heterogeneous Integration Roadmap

and the Revolution Enabling Future Progress, Wilmer R.

Bottoms, Chairman, Third Millennium Test Solutions

The electronic information technology market has reinvented itself from the first telegraph through telephones and television to the present. This technology now impacts every aspect of our lives. For more than 55 years the pace of progress was guided by Moore's Law and scaling CMOS was the clear path to progress. As scaling CMOS approached the limits of the physics it could no longer maintain the

pace of progress. The ITRS, built around scaling CMOS, was terminated and the last edition was published in July 2016.

In anticipation of this end of evolutionary progress, an agreement was signed in March of 2015 between the Heterogeneous Focus Team of the ITRS and what is now known as the IEEE Electronic Packaging Society. This was the initial formation of the Heterogeneous Integration Roadmap (HIR).

The purpose of the HIR is to identify difficult challenges and, where possible, potential solutions far enough in advance to stimulate pre-competitive collaboration to accelerate progress. The HIR published 2 internal versions in 2018 and 2019 at our annual meetings but did not release a copy to the public until fall of 2019. During this period, we hosted more than 20 workshops around the world each year with thousands of participants.

Today we see revolutionary changes in the 23 HIR Chapters. This presentation will briefly introduce the structure and governance of the HIR. The majority of the presentation will present the vision of the future presented in the 2019 HIR and the ongoing work for the 2020 edition to be released this fall.

Bio: Dr. Bottoms received a B.S. degree in Physics from Huntington College in Montgomery, Alabama in 1965, and a Ph.D. in Solid State from Tulane University in New Orleans in 1969 and is currently Chairman of Third Millennium Test Solutions. He has worked as a faculty member in the department of electrical engineering at Princeton University, manager of Research and Development at Varian Associates, founding President of the Semiconductor Equipment Group of Varian Associates and general Partner of Patricof & Co. Ventures.

Dr. Bottoms has participated in the startup and growth of many companies through his venture capital activity and through his own work as an entrepreneur.

He has served as Chairman and CEO of many companies both public. Some of his current responsibilities include:

- * Emeritus Member of the Board of Tulane University
- * Co-Chair of the Heterogeneous Integration Roadmap
- * Chairman of the SEMI's Awards Committee
- * Member of the Board of MIT's Microphotonic Center
- * Chairman of Fluence Analytics
- * Chairman of the Technology Board of Tulane's POLYRMC center.
- * Chairman of Third Millennium Test Solutions

Surviving the Heat Wave -

A presentation on thermally induced failures and reliability risks created by advancements in electronics technologies...and How Modeling Early in the Design Process can Identify these Issues, Greg Caswell, ANSYS

Since the advent of surface mount technology back in the 1970's we, as an industry, have continually worked to miniaturize our products. This evolution of product design has impacted us at the semiconductor, package, circuit board and system levels. So, the

question is, Why do Electronics Fail Under Thermal Cycling and What Can We Do About it During the Design Cycle?

At the package level issues with bond wires and stacked die add to the reliability impact. At the printed circuit board level issues with solder wearout, solder phase coarsening, PWB laminates and glass materials, plated through hole (PTH) fatigue, and the impact of potting can also affect reliability.

What drives these issues is that we use a variety of materials e.g. semiconductors, ceramics, metals and polymers. We then bond them together with other materials like solder and adhesives. Each of these materials has a Coefficient of Thermal Expansion (CTE) that is unique and therefore expands and contracts at different rates. Being able to model the assembly with respect to Reliability Physics is an effective way to identify the issues in a design even prior to creating a prototype. This talk will delineate some of the issues involved in device and PWB packaging as well as how a modeling approach can facilitate their identification so they can be corrected.

Bio: Greg Caswell, a Lead Consulting Engineer for Ansys Corporation, is an industry recognized expert in the fields of SMT, advanced packaging, printed board fabrication, circuit card assembly, and bonding solutions using nanotechnology. He has been well-regarded as a leader in the electronics contract manufacturing and component packaging industries for the past 50 years. He has presented over 270 papers at conferences all over the world and has taught courses at IMAPS, SMTA and IPC events. He helped design the 1st pick and place system used exclusively for SMT in 1978, edited and co-authored the 1st book on SMT in 1984 for ISHM and built the 1st SMT electronics launched into space. Be on the lookout for his new book entitled Design for Excellence in Electronics Manufacturing due out in September 2020.

* B.A., Management (St. Edwards University)

* B.S., Electrical Engineering (Rutgers University)

Heterogeneous Integration Competence Center - An Open Access Innovation Incubator,

Garrett Oakes, EV Group

Abstract and Bio Pending.

Solving the DataCenter Energy Crisis with Silicon Photonics and Overcoming Photonics Wafer-level Test Challenges,

Dr. Sia Choon Beng, FormFactor

Data centers and information technology (IT) communications around the world currently consume about 7% of the earth's total power output. To satisfy the increasing demands for cloud computing and services for various new emerging applications such as artificial intelligence, genomics revolution, data analytics and video transcoding etc, hyperscale data centers are being built around the

world at an accelerated pace, with analyst predicting up to 20% of earth's total power output consumed by data centers and IT communications by 2030. Optical fiber communications within data centers and the use of Silicon Photonics (SiPh) to implement these optical transceivers present a very attractive option, drastically reducing power consumption, cost and size of these transceiver modules. In addition, the mature silicon CMOS processing technologies and advanced packaging technologies both offer an established production solution to fabricate such silicon-based optical transceiver modules. For effective heterogeneous integration and packaging of these silicon-based optical transceivers, all individual functional dies, for example, logic, photonics and continuous wave laser etc must each be tested prior to stacking and packaging. One of the key challenges for wafer-level photonics tests and measurements is the need for full test automation to satisfy the high throughput requirements for these known-good-die tests - especially tedious when test engineers need to work with optical, DC, RF probes to handle unlimited permutations of possible test structure layouts at the same time. Another challenge is optimizing test time as optical and opto-electrical tests require long measurement time due to complexity of the fiber alignment/coupling procedure and fine sweeping steps needed during measurements. Finally, the ability to accurately test the final product is another big obstacle since most SiPh chips utilize edge coupler to transfer light in and out of the chip after packaging while majority of the commercially available wafer-level test solutions require grating couplers for wafer top-side light transfer. In this talk, proposed solutions to these challenges will be discussed, including layout rules and standardization for the ease of automation implementation, utilization of fiber array for parallel testing and optimization of input light for higher precision gauging and correlations with the final product performance.

Bio: Dr Sia Choon Beng is a SSG Fellow, conferred by the President of the Republic of Singapore. He is also a Nanyang Research Scholar and has received bachelor, master and doctorate degrees in Electronics Engineering from Nanyang Technological University, Singapore with 5 IEEE Transactions journal papers published for his Ph.D. dissertation. In his current work at FormFactor as a Test Technologist, Dr Sia develops solutions to overcome semiconductor wafer test challenges. His research interests include design, test and modelling of silicon-based RF devices, THz calibration and measurement for 5G and IoT applications, photonics and power device wafer tests for LIDAR/Autonomous Transport/Optical communication applications as well as applying data analytics, deep learning and artificial intelligence to wafer tests. Dr Sia is a senior member of the IEEE and serves in the IEEE MTT-3 technical committee which focuses on developing standards and best practices for RF measurements. He lectures graduate-level semiconductor courses for Singapore Semiconductor Industry Association and he is also a member of the IEC TC47 technical committee which is sponsored by SPRING, Singapore's National Standards board. Dr Sia represents Singapore as a Technical Expert in various IEC technical committees, developing standards for MEMs, optical and wafer-level reliability tests for semiconductor

devices. A wafer test and device modelling expert, Dr Sia is often consulted by international semiconductor companies, defence, government and medical research institutes. He is a frequent invited speaker and organizer of IEEE workshops, international test forums and presently holds 12 international patents. Dr Sia has published a total of 50 scientific journals and conference publications, of which >85% of them as the first author. Dr Sia's most recent technical papers on 5G and Silicon Photonics tests received two "Best Overall Presentation" and the "Most Inspirational Presentation" awards at the 2018 and 2019 Semiconductor Wafer Test Conferences.

All presentations will be requested to be posted on the TFUG Proceedings webpage approximately 1-2 weeks following the meeting.

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<https://nccavs-usergroups.avs.org/wp-content/uploads/2017/08/UG-Sponsor.pdf>

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