

Solving the Data Center Energy Crisis with Silicon Photonics & Overcoming Photonics Wafer-level Test Challenges

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Dr Choon Beng Sia

- Test Technologist, FFI Probe System Business Unit
- Ph.D. in RF Device Design and Modelling
 - Nanyang Research Scholar, 5 IEEE Journals for dissertation.
- IEEE Senior Member
- IEEE MTT-3 Microwave Measurement Committee
- IEC TC47 Technical Expert representing Singapore
- Research Interests:
 - DC, AC, 1/f noise, Power Device Characterization
 - Wafer-Level Optical Measurements, THz Calibration & Characterization of Devices
- 50 Technical Papers, 12 International Patents
- "Best Paper" awards for "5G Production Test" at 2018/2019 SWTest Conf.
- SSG Fellow conferred by President of Singapore



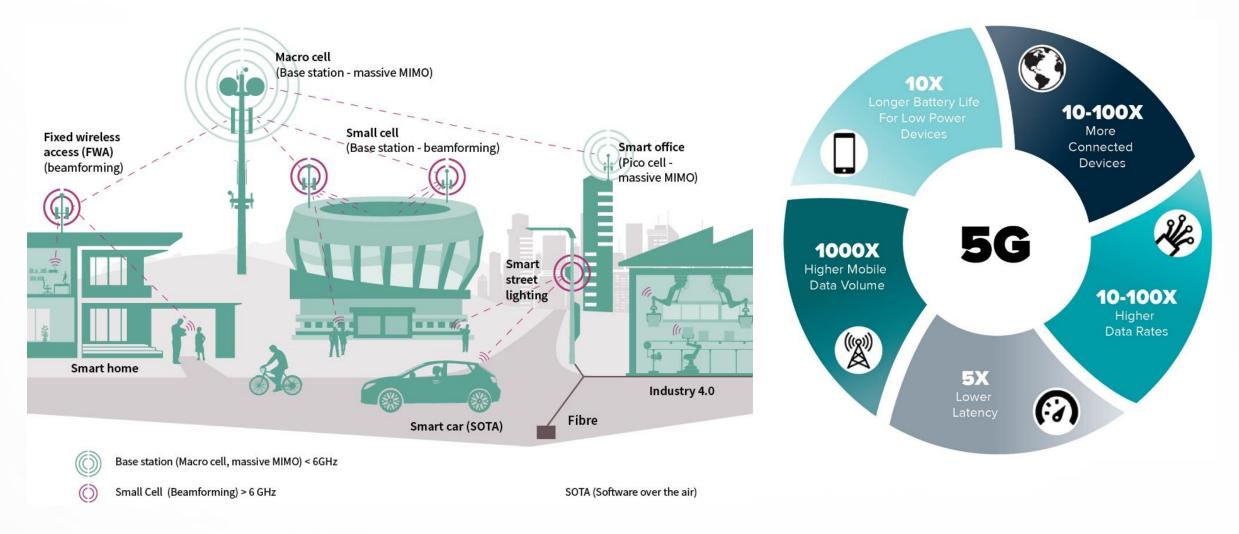


Overview

- Why Huge Demands for Silicon Photonics?
- Why Wafer-Level Photonics Tests?
- What are the Test Challenges & Solutions?
- Summary



Future Communication Landscape with 5G

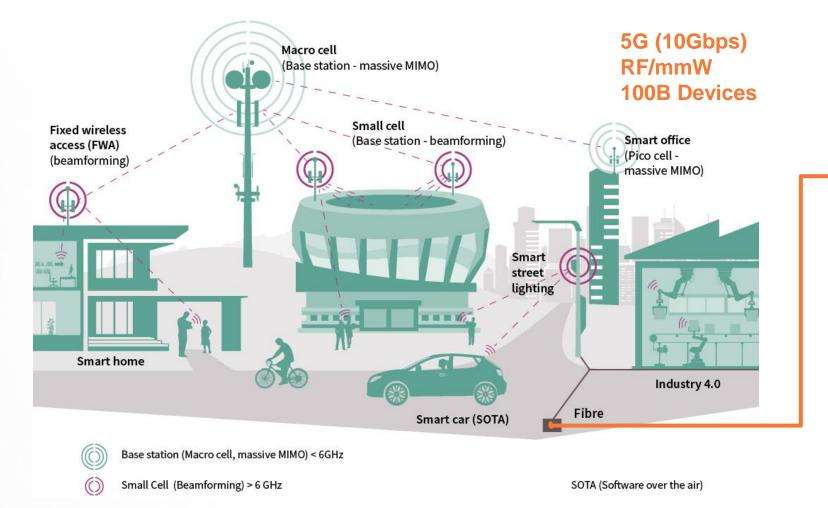


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Future Communication Landscape with 5G





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Data Center 100/400/800Gbps Optical Interconnects

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https://www.infineon.com/export/sites/default/media/press/Image/press_photo/Infographic-5G-e.png & https://www.sakura.ad.jp/en/corporate/datacenter/

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The Need for High Performance Network & Data Centers



Big Data Analytics



Artificial Intelligence



Genomics Revolution



Augmented Reality



Financial Acceleration







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Self-Driving Cars

Video Transcoding

Internet of Things

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Facebook's US\$1B HyperScale Data Center in Singapore

6th September 2018

- Facebook's 1st
 Data Center in
 Asia (Hub).
 - IT Talent & Fiber connectivity
 - 170,000m²
 - 150MW
- 5000 servers
 - Each server supports 100 petabytes or 100,000 TB*

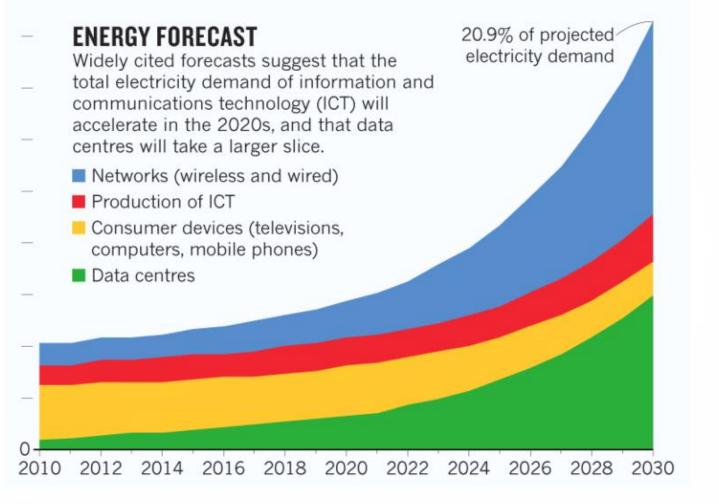




Energy Forecast for Information Technology

- Speed is not the main Challenge.
 - Reducing Energy Consumption is Key!
 - Data Center Power Usage:-
 - 40% Server & Switch
 - 40% Cooling
- By 2030, 20% of World's Energy produced to be consumed by Information Technology?

9,000 terawatt hours (TWh)



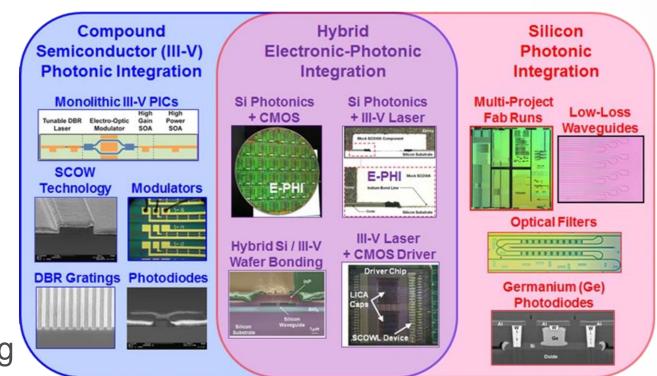
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*A. S. G. Andrae and T. Edler, "On Global Electricity Usage of Communication Technology: Trends to 2030", Challenges, Vol. 6, pp. 117-157, 2015.

Why Silicon Photonics?

Improvements in Thin Film Growth

- High Quality Ge on Si
 - Excellent Lattice Matching
 - Hi-Speed Ge-on-Si Photodiodes
- Exploiting Silicon Technologies
 - Low-Cost High-Volume Production
 - Low-Power Logic devices
 - High-Speed RFCMOS devices
 - Heterogenous Integration/Packaging

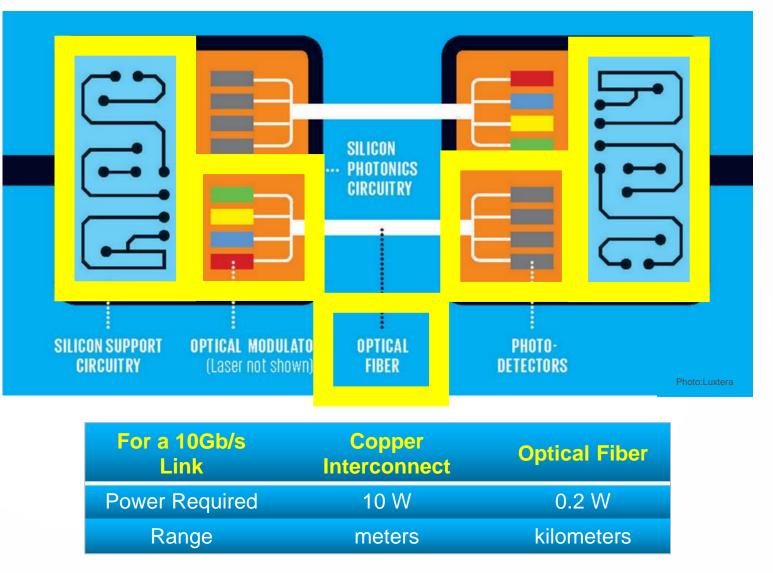




SiPh Optical Transceivers for Data Centers

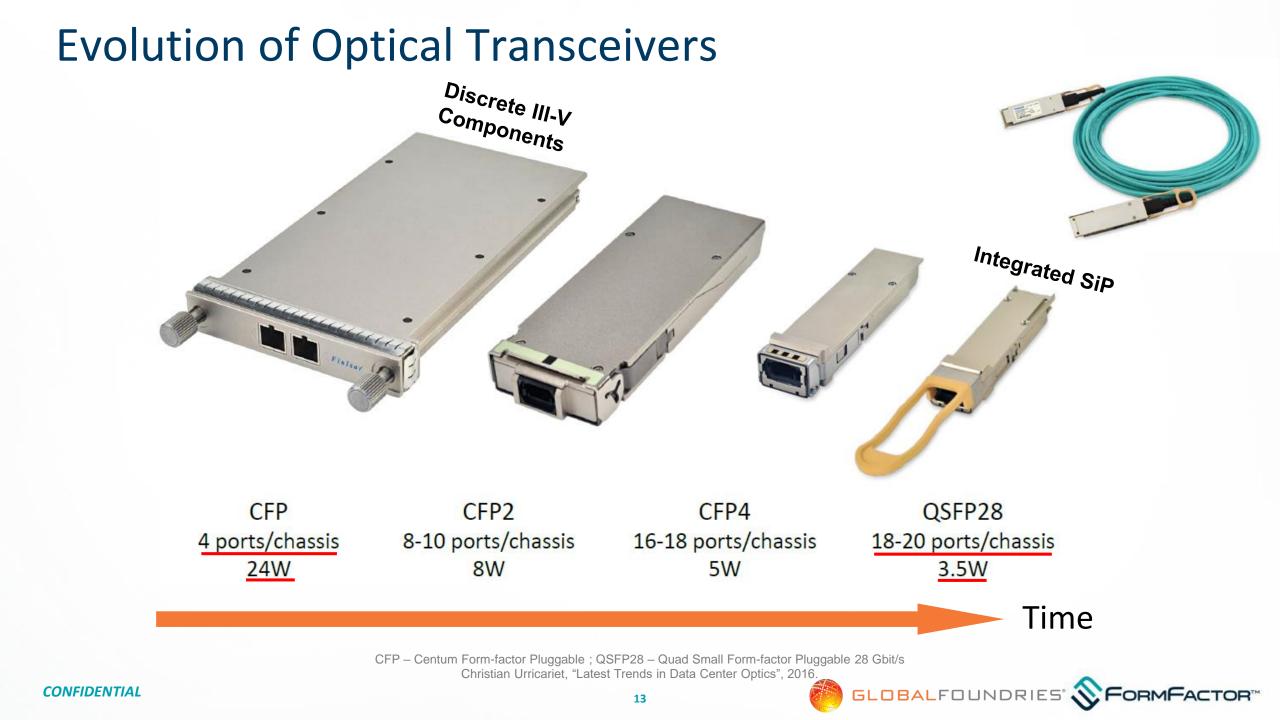
Components on SiPh Transceivers

- 1. CMOS Logic Chip
 - Data Encoding (also decoding)
- 2. Optical Transmitter
 - Optical Modulators Varying voltage modulate Data onto Light
 - Lasers not implemented on Silicon
- 3. Optical Receiver
 - Ge Photo detectors
 - Converts Light to Voltage
- 4. CMOS Logic Chip
 - Data Decoding (also encoding)

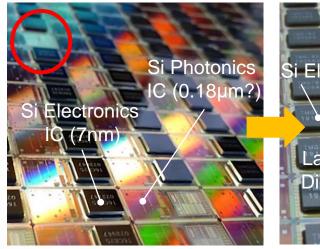


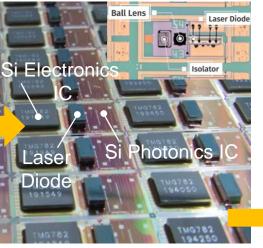
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Sources: IEEE Spectrum, Yole - New Technologies & Architectures for Efficient Data Center report – July 2015



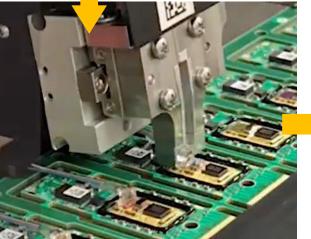
Why Wafer-level Test? – Heterogenous 3DIC Stacking



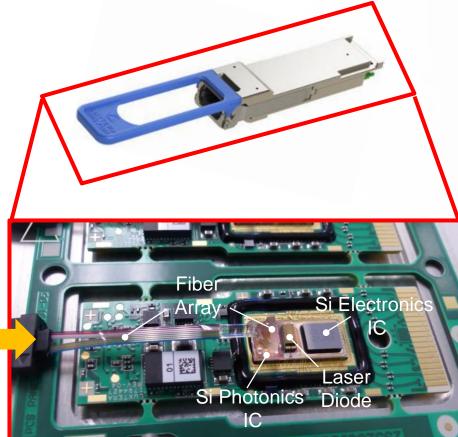


Si Electronics-Die attach onto Si Photonics-Die (TSV) Continuous Wave Laser Diode on Si Photonics-Die

Known-Good-Die (KGD) tests needed for 3DIC Heterogenous Integration.



Optical Fiber Array Aligned & Fused onto Photonics-Die



SiP-based Optical Transceiver Chipset for QSFP28 module

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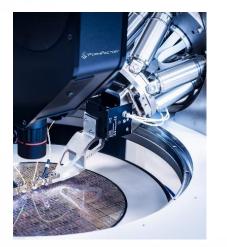
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Source: Luxtera's website, Luxtera acquired by CISCO in Dec 2018 for US\$660M.

Integrated Wafer-Level Photonics Test Solution



Optical Test Instruments & Software



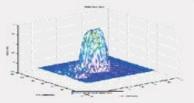
6-Axis/Piezoelectric Positioner, Single Fiber/Fiber Array, Displacement Sensors





RF probes, ISS, Cal. Software & DC probes





Software for Optical Positioners & Probe System



Fully Automatic Probe System with Wafer Loader

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- Why Wafer-Level Photonics Tests?
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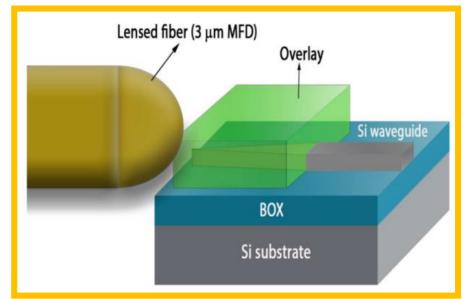


What are the Test Challenges & Solutions?

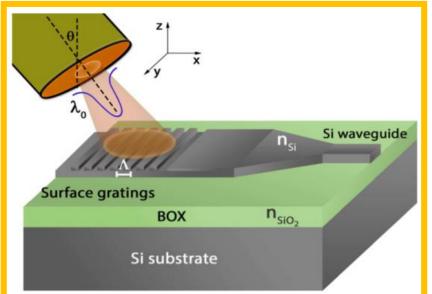
- How to Optimize Test Setup for Accurate & Repeatable Measurements?
 - How to couple light into a photonics chip (wafer-level)?
 - Achieving Fast and Repeatable Fiber-to-Coupler Alignment
 - Optimizing Fiber Height and Incident Angle.
- How to Correlate Wafer-Level Test to Final Product test?
 - Edge Coupling Optical Tests
- How to Achieve Fully Automatic Wafer-Level Production Solution?



How to Couple Light into a Photonics Chip (Wafer-level)?



- Edge Coupling
 - Final Product (Die Level)
 - Small, Sub-dB Loss Per Facet
 - 200nm 300nm Bandwidth
 - Low Polarization Sensitivity
 - Harder to Fabricate/Test
 - Fixed Interface (Edge of Chip)
 - Low Fiber-Chip Alignment Tolerance

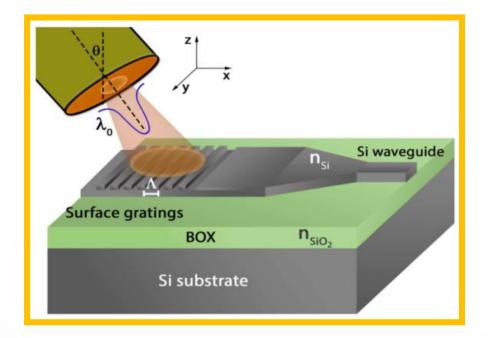


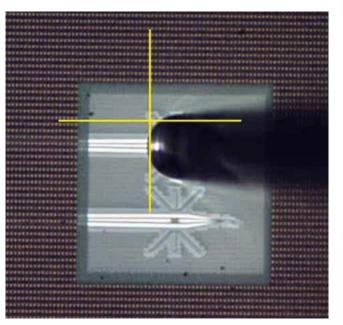
- Grating Coupling
 - Process Development & KGD (Wfr Level)
 - Larger, 2 to 4dB Loss per Grating Coupler
 - Typically 60nm Bandwidth
 - Polarization Dependent
 - Easier to Fabricate/Test
 - Flexibility of interface positions
 - High Fiber-Chip Alignment Tolerance

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Optimizing Setup – Optical Coupling for Photonics Tests • Grating Couplers (Wafer-Level Tests)

- Fast & Repeatable Fiber to Grating Coupler Alignment





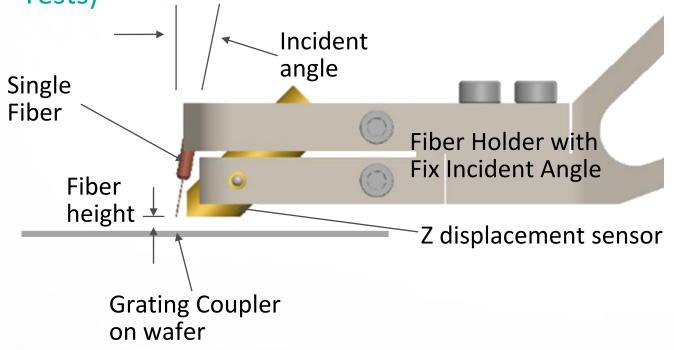
Fiber Alignment with Sinusoidal Scan

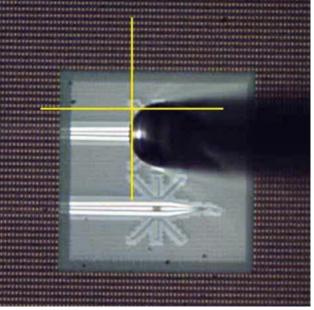


Optimizing Setup – Optical Coupling for Photonics Tests

Grating Couplers (Wafer-Level Tests)

- Fast & Repeatable Fiber to Grating Coupler Alignment
- Fiber Height (Constant Height to Prevent Damage)
- Incident Angle (Critical to determine Optimal Incident Angle before Production Tests)



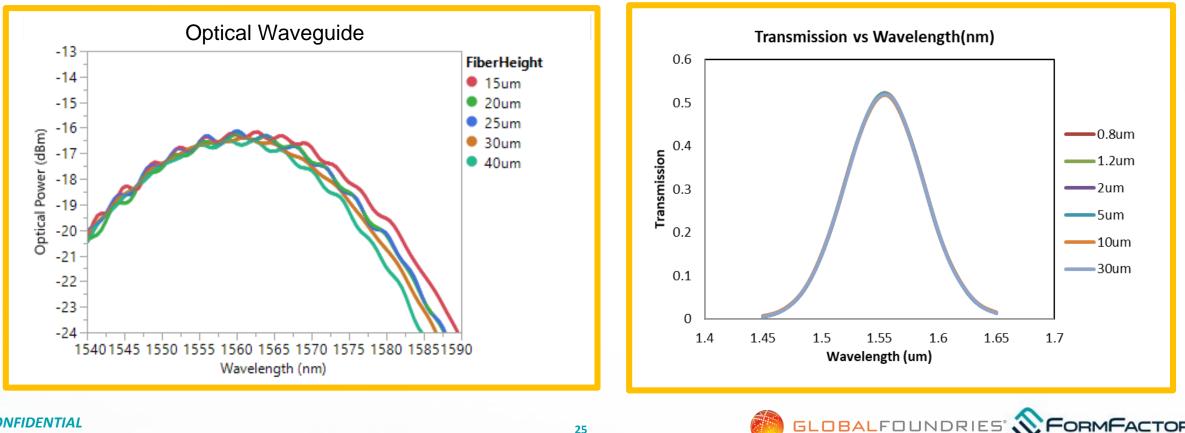


Fiber Alignment with Sinusoidal Scan

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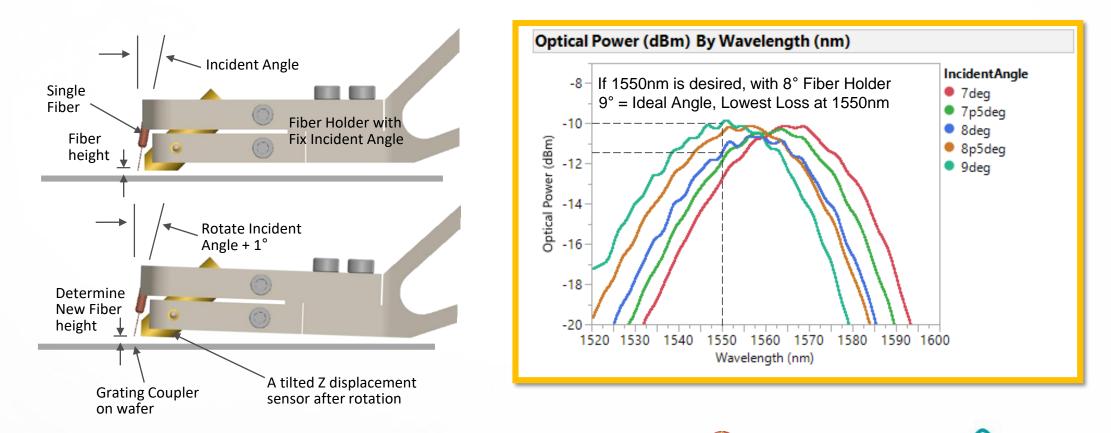
Optimizing Setup – Fiber Height (Wafer-Level)

- 1. Set Fiber Height, 2. Peak Search, 3. Make Measurements \rightarrow Repeat diff. Height
- No Significant Effect on Coupling Efficiency, Peak Wavelength & Bandwidth.
- Good Agreement with Simulation Data.



Optimizing Setup – Incident Angle (Wafer-Level)

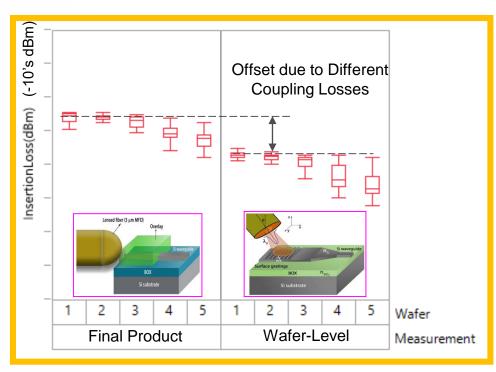
- 1. Set Incident Angle, 2. Peak Search, 3. Make Measurements → Repeat diff. Angle
 - Use 6-axis positioner to vary incident angle ±1°; Fiber height set with Z sensor (Pivot Cal needed).
- Critical to determine Optimal Incident Angle before Production Tests (1.5dB improvement).



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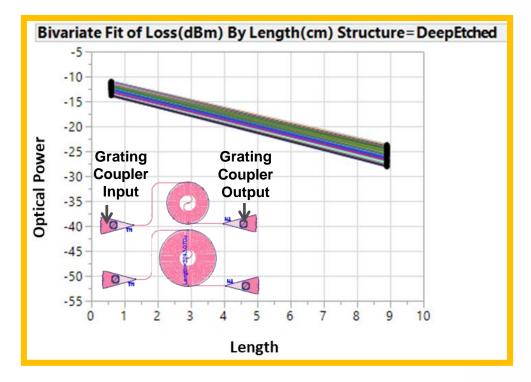
Wafer-Level vs Final Product Tests (Passive Device)

Offset bet wfr-level & final product



- Critical to correlate Wafer-Level & Final product Tests
- Using Optical Waveguides as Test Structures
 - Different Insertion Losses observed

Obtaining Coupling Losses

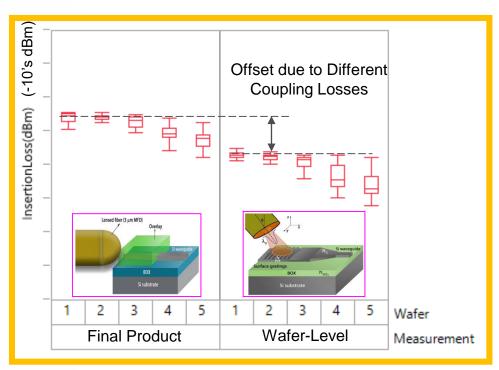


- Edge Coupling & Grating Coupling losses are obtained by Cut Back method.
 - Comparing output intensity of waveguides with different length



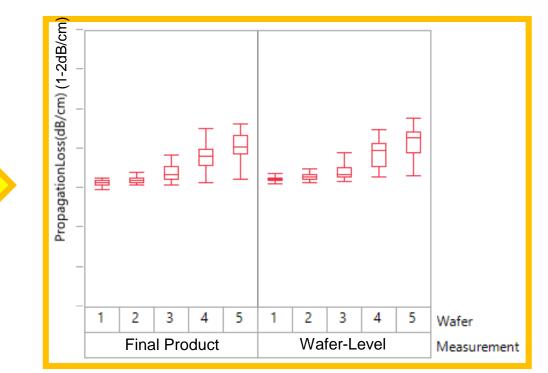
Wafer-Level vs Final Product Tests (Passive Device)

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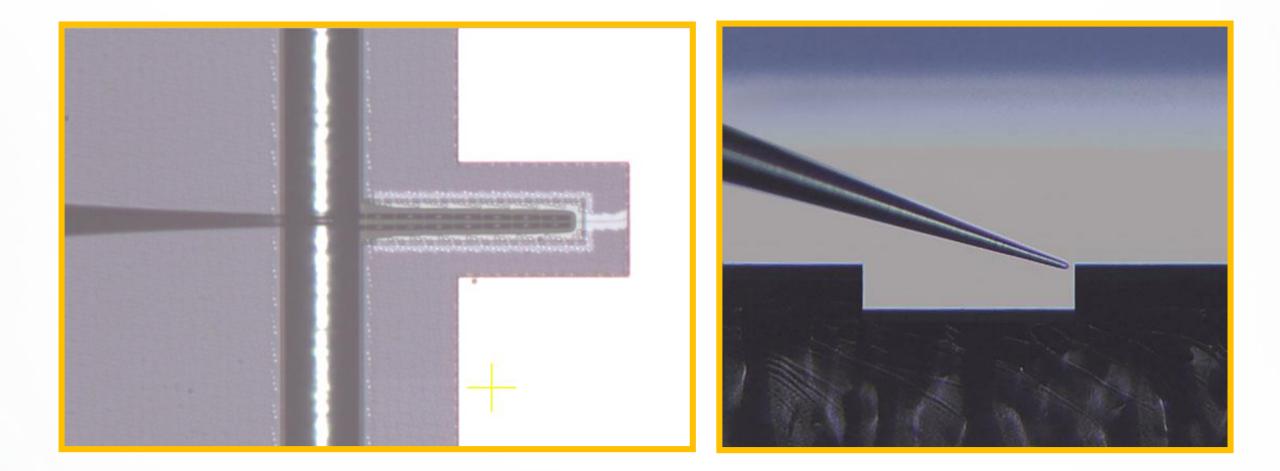
- Critical to correlate Wafer-Level & Final product Tests
- Using Optical Waveguides as Test Structures
 - Different Insertion Losses observed

After Coupling Losses Correction



- Remove Coupling Loss
- Comparable Propagation Loss per unit Length.
- Establish Good Correlations between Wfr-level and Final product Tests!

Wafer-Level Edge Coupling





Challenging for one Test Setup to handle...

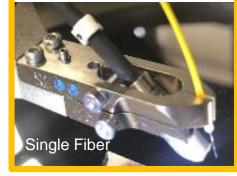
- Passive vs Active Device
- Single Photonics Device & Complex Photonics Integrated Circuit Tests
- Endless Permutations of Test Layouts

- Establish Design Rules, 9	Unit	Probes Needed
(Designateroarestability)	nA	
-N/ProplephendulAtertRasistaiceT	esting	architecture
Heater Resistance	ohm	
Waveguide Propagation Loss	dB/cm	
Y-splitter splitting ratio	%	Optical Fiber Probes
Tap Coupler Coupling Strength	%	
Modulator Extinction Ratio	dB	Optical Fiber Probe(s)
Photodiode Responsivity	A/W	+ DC Probes
Modulator Bandwidth	GHz	Optical Fiber Probe(s)
Photodiode Bandwidth	GHz	+ RF Probes









Photonics Device Tests

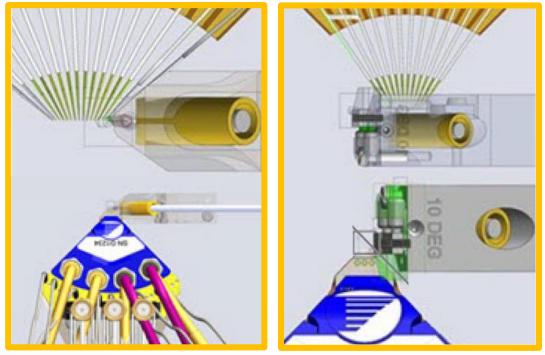


Fiber Array

Photonics IC Tests

Layout Design Rules & I/O Standardization

- Establish Test Pads vs Grating Couplers Layout Design Rules.
- Fix DC @North, RF @South, Optical I/Os @East&West side of the DUT.



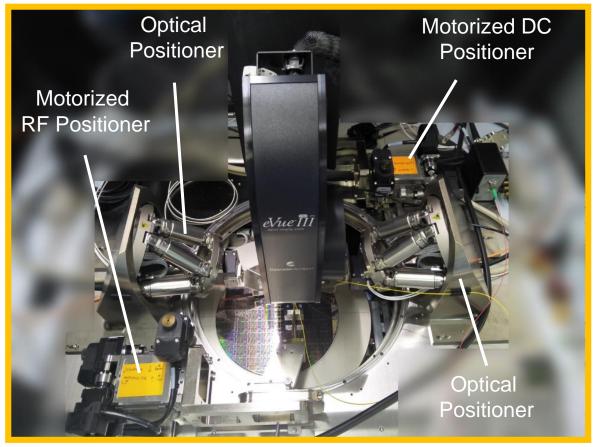
Design Rules for Single Fiber

Design Rules for Fiber Array

Optical Input Fiber (Tunable Laser) KF Probe (Lightwave Component Analyser)

DC Probe (SMU)





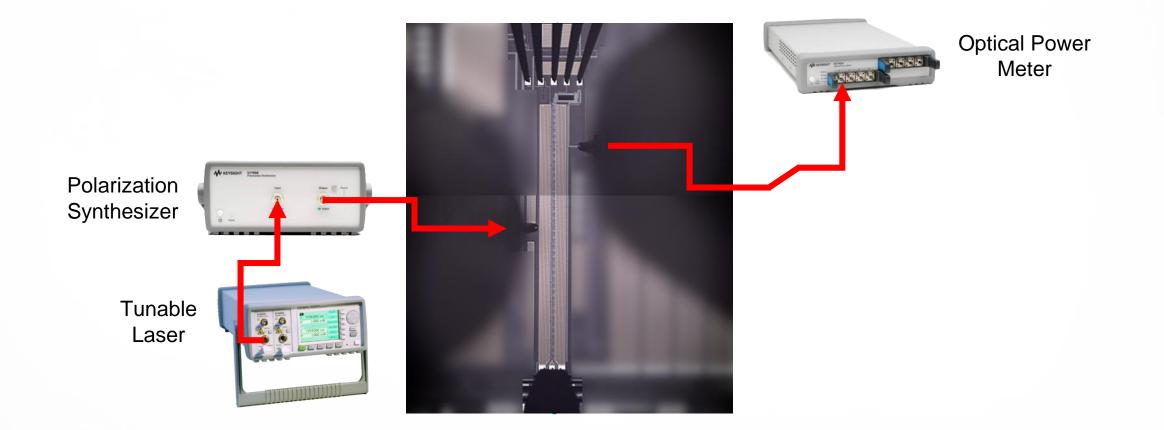
- 2 Optical & 2 Motorized DC/RF positioners
- Handle diff. layout with remote commands



- Fully Automatic 300mm Probe System
- Automatic Wafer Loading/Unloading

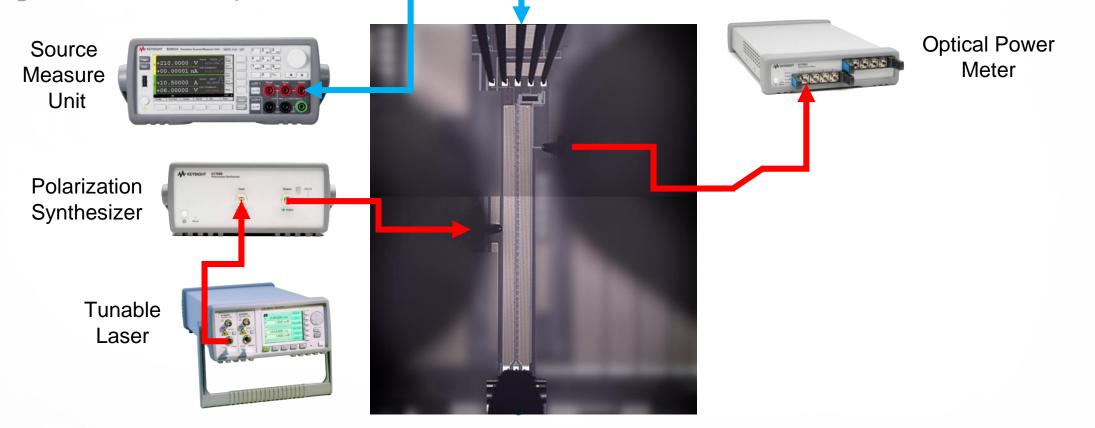


- Implement Automatic Testing Architecture Modulator as Example
 - Peak Search; Optimizing Polarization → Setup optical path



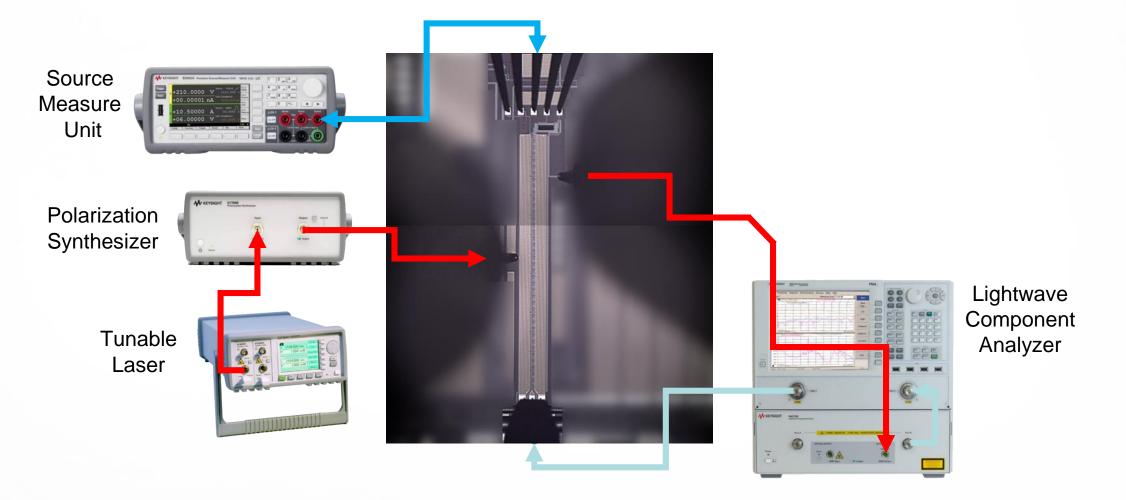


- Implement Automatic Testing Architecture Modulator as Example
 - Bias Tuning to Measure Extinction Ratio (ratio of optical power levels of a digital signal, "1" and "0")



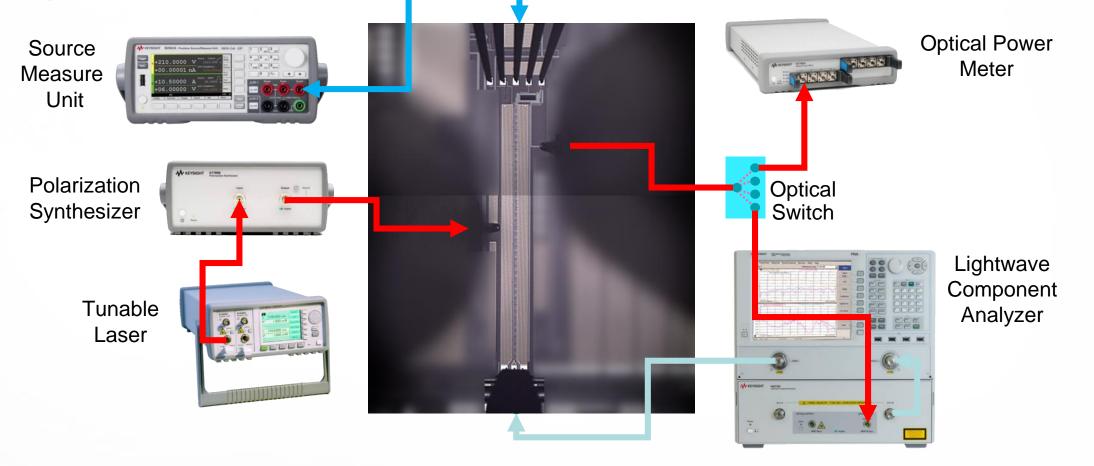


- Implement Automatic Testing Architecture Modulator as Example
 - Connect to LCA for RF Frequency Sweep to Measure Modulator Bandwidth

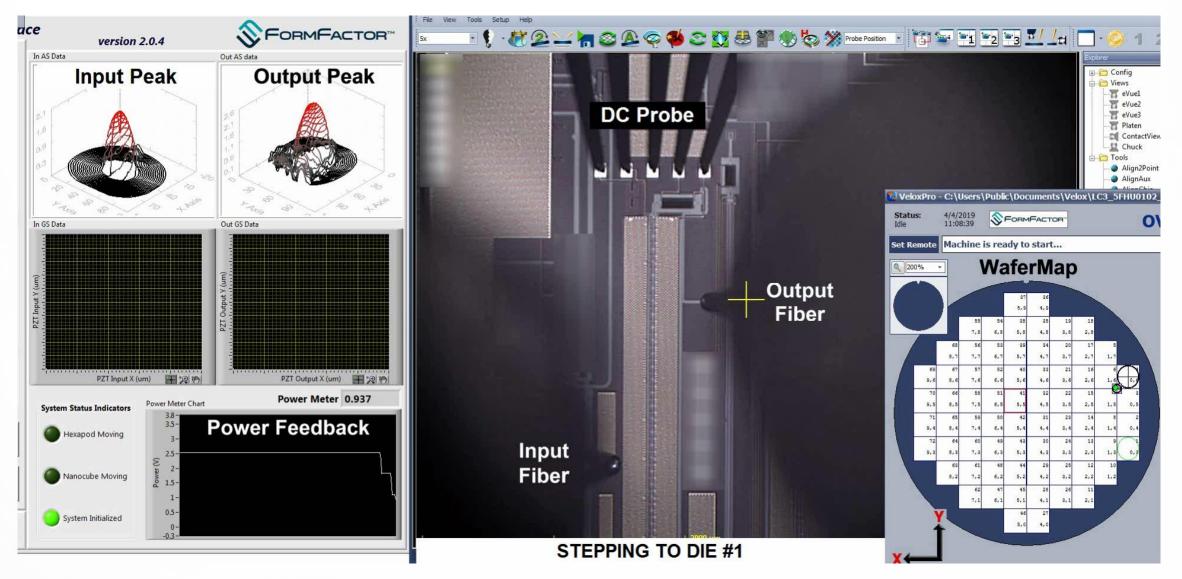


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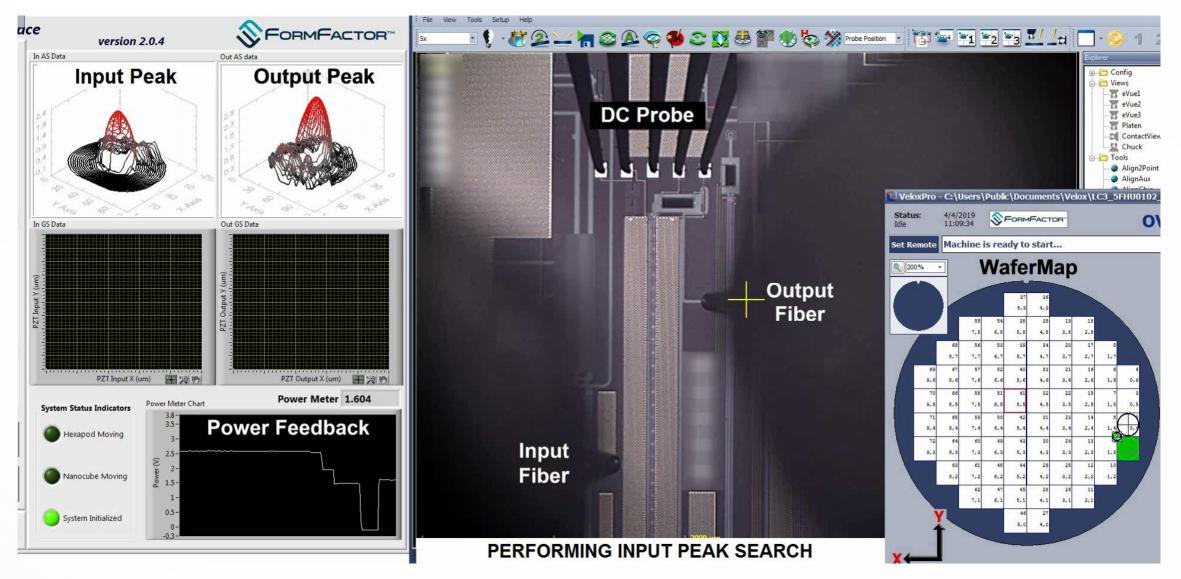
- Implement Automatic Testing Architecture Modulator as Example
 - Instrument Automation implemented with an Optical Switch. (automation vs power budget)



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Summary

- Why Huge Demands for Silicon Photonics?
 - Need for Energy-Efficient Data Centers is driving huge demands for SiPh.
- Why Wafer-Level Photonics Tests?
 - Determine Known-Good-Dies & Shorten Product Time to Market.
- What are the Test Challenges & Possible Solutions?
 - Fast and Repeatable Fiber-to-Coupler Alignment
 - Must Optimize the Incident Angle for Production Tests.
 - Achieve Good Correlations between Wafer-level & Final Product Tests.
 - Establish Design Rules, Standardize Layout & Implement Automatic Testing Architecture = Fully Automatic Photonics Tests.







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FFI

Thank You!

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