Surviving the Heat Wave

A Presentation on Thermally Induced Failures and Reliability Risks Created by Advancements in Electronics Technologies…and How Modeling Early in the Design Process Can Identify These Issues

June 10, 2020

NCCAVS Presentation

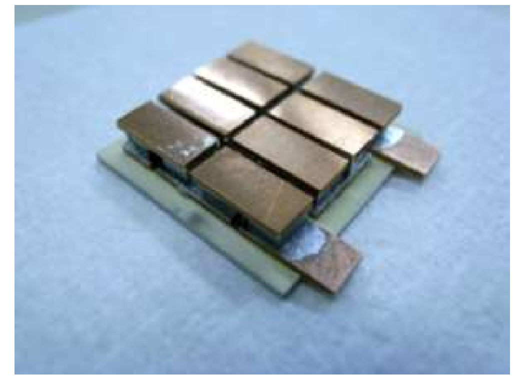
Ansys

Applications

ARINC 429-Mil-Std-1553 Module

Enphase/Solarbridge Micro-Inverter

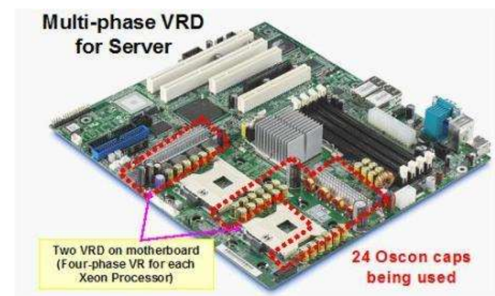
Thermo-Electric Module



Cobham-Carson Sikorsky Suite

IGBT

Voltage Power Modules



What Do They All Have in Common?

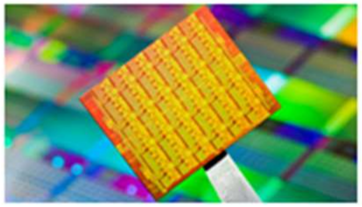
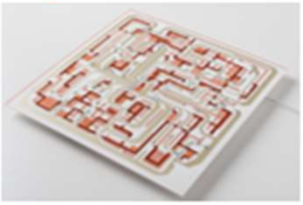
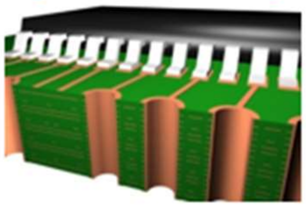
- High Temperature Environments
- Vibration and Shock Environments
- Temperature and Power Cycling Environments
- High Current Flows and Thermal Transfer Requirements
- A variety of materials forming the product

Failure Mechanisms

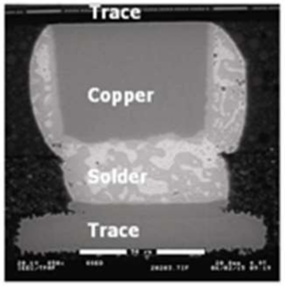
- Thermo-mechanical fatigue induced failures
  - CTE mismatch
  - Temperature swings
- Bond Wire Fatigue
  - Shear Stresses between bond pad and wire
  - Repeated flexure of the wire
  - Lift off (fast temperature cycling effect)
  - Heel Cracking
- Die Attach Fatigue
- Solder Fatigue
  - Voids
- Device Burn Out

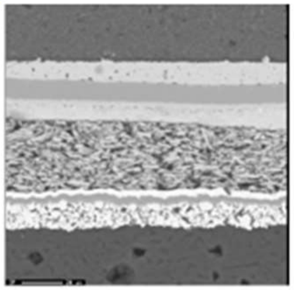
Why Do Electronics Fail Under Thermal Cycling?

- A. We use lots of different materials
  - Semiconductors, Ceramics, Metals, Polymers


- B. We bond these different materials together
  - Plating, **<u>Solder</u>**, Adhesive

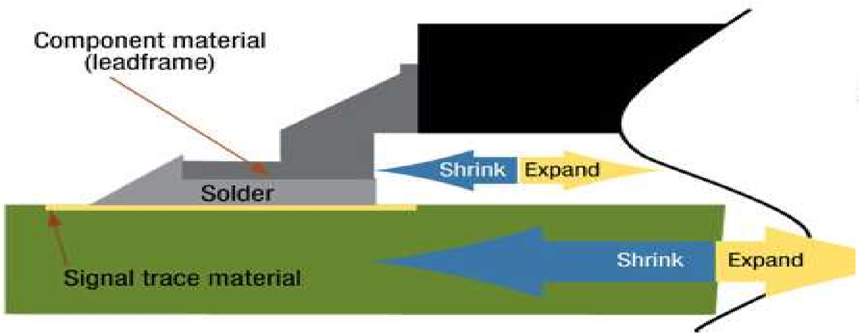


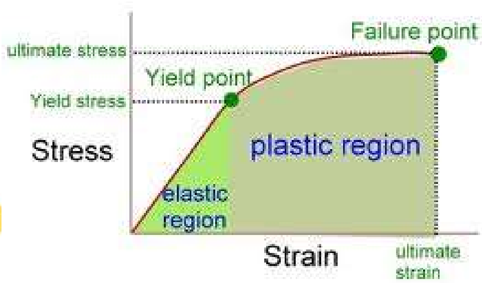


- C. These materials expand/contract at different rates

Why Do Electronics Fail Under Thermal Cycling?

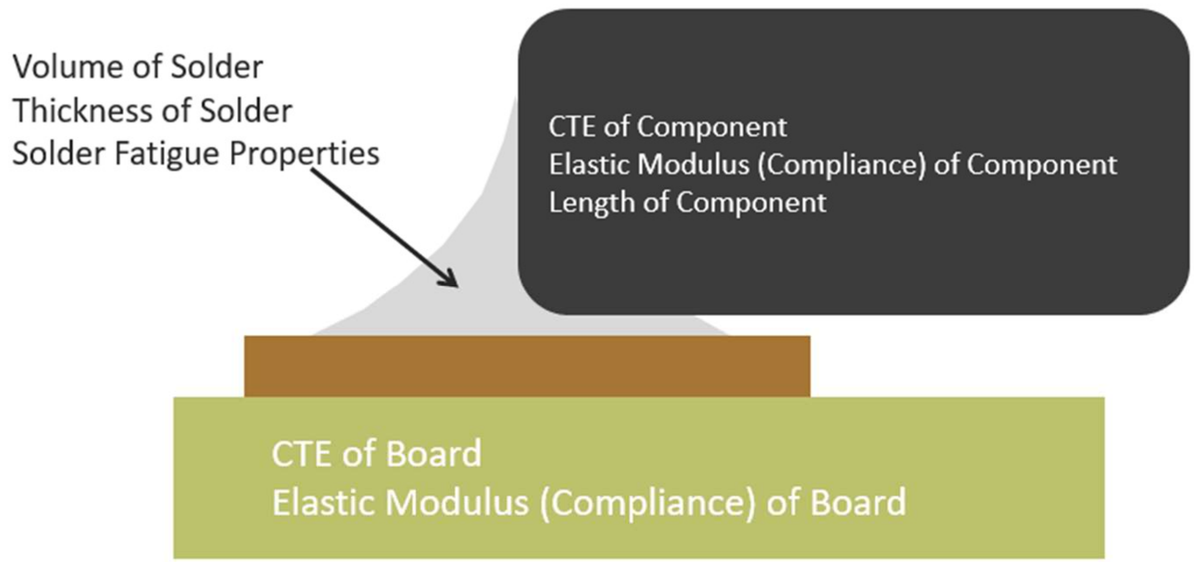
- Two different expansion/contraction behaviors
  - Because solder is connecting two materials that are expanding / contracting at different rates (GLOBAL)
  - Because solder is expanding / contracting at a different rate than the material to which it is connected (LOCAL)
- This differential expansion and contraction introduces stress into the solder joint
  - This stress causes the solder to deform (aka, elastic and plastic strain)
- The extent of this strain (that is, strain range or strain energy) tells us the lifetime of the solder joint
  - The higher the strain, the more the solder joint is damaged, the shorter the lifetime





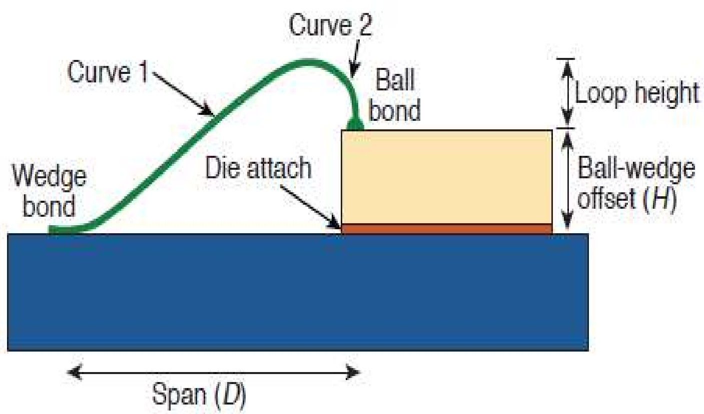
Drivers for Solder Joint Thermo-Mechanical Failures

- Knowing the critical drivers for solder joint fatigue, we can develop predictive models and design rules



Bond Wires

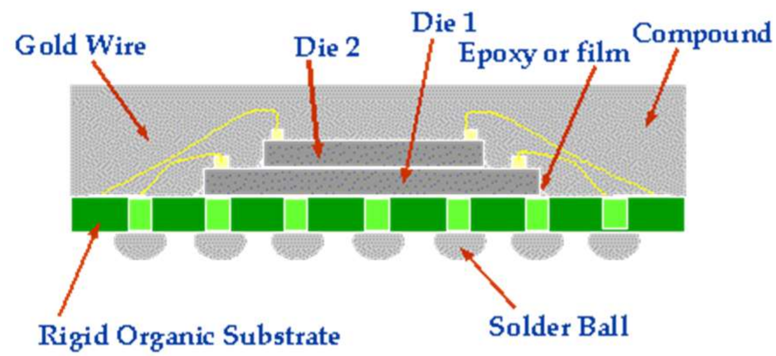
- Wire bonding has been the most common interconnect for IC packages for over 50 years. The most common materials are gold, aluminum, and more recently copper. The most common bond pad material is aluminum.

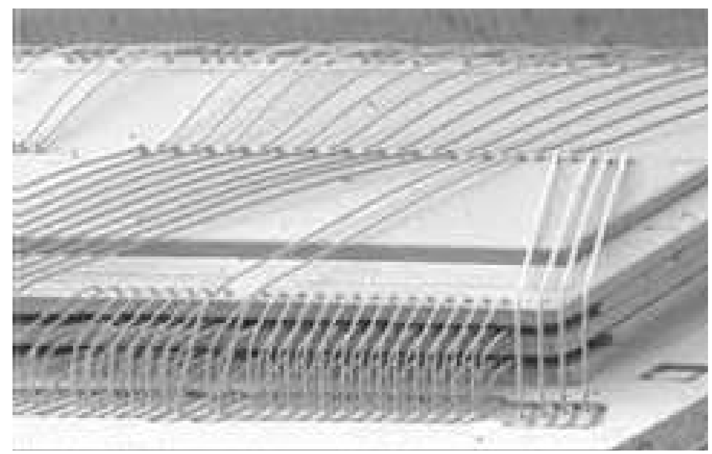


- Wire bonds tend to fail if exposed to elevated temperatures (intermetallic formation), exposure to elevated temperature and humidity (corrosion) and exposure to temperature cycling (low cycle fatigue).

Stacked Die Configuration

- Die stacking technologies have been demonstrated to > 9 high stacks
  - Most stack ups are limited to 4 die
  - Driven by test, yield and logistic limitations
- Stacked die packaging comes in three flavors
  - All driven by need to provide ledges for wire bonding
- Pyramid or 'cake' configuration
  - Smaller die are placed on larger die
- Stacking traps heat (higher junction temperatures)
  - Increase in upset events, shorter lifetimes

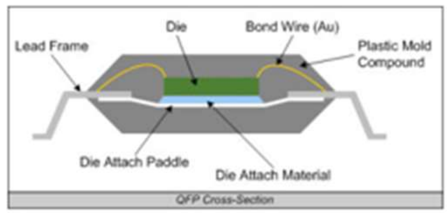




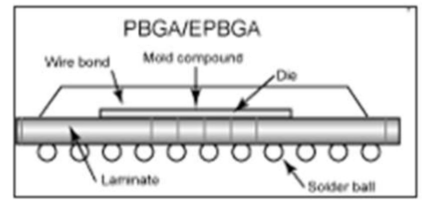
Solder Wearout

- Elimination of leaded devices
  - Provides lower RC and higher package densities
  - Reduces compliance

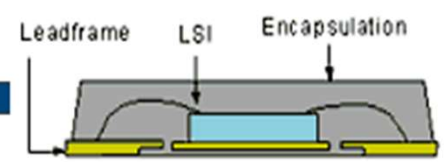
Cycles to failure
-40 to 125C



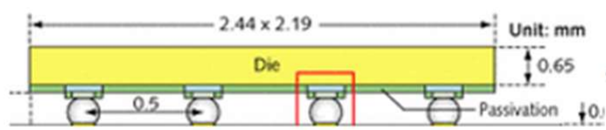
QFP: >10,000



BGA: 3,000 to 8,000



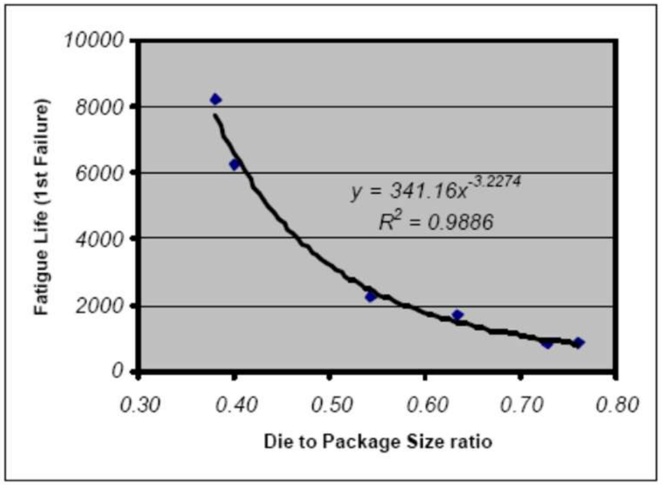
QFN: 1,000 to 3,000



CSP / Flip Chip: <1,000

Solder Wearout

- Design change: More silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)
- Hotter devices due to increases change in temperature (ΔT)



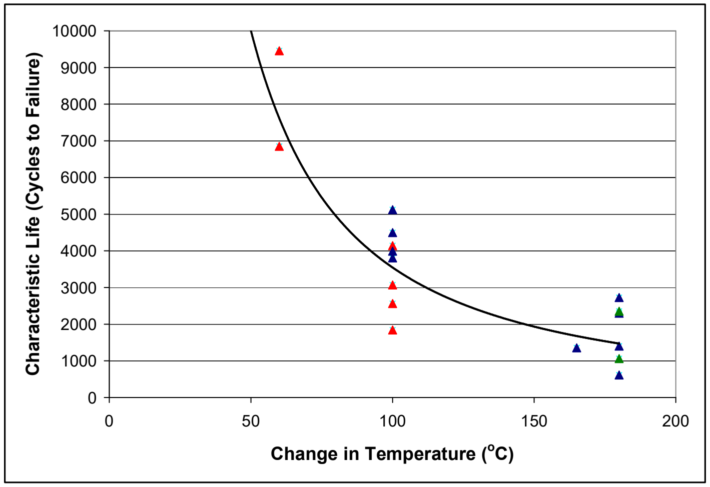
BOARD LEVEL ASSEMBLY AND RELIABILITY CONSIDERATIONS FOR QFN TYPE PACKAGES, Ahmer Syed and WonJoon Kang, Amkor Technology.

$t_f = \Delta T^n$

n = 2 (SnPb)

n = 2.3 (SnNiCu)

n = 2.7 (SnAgCu)



Ansys

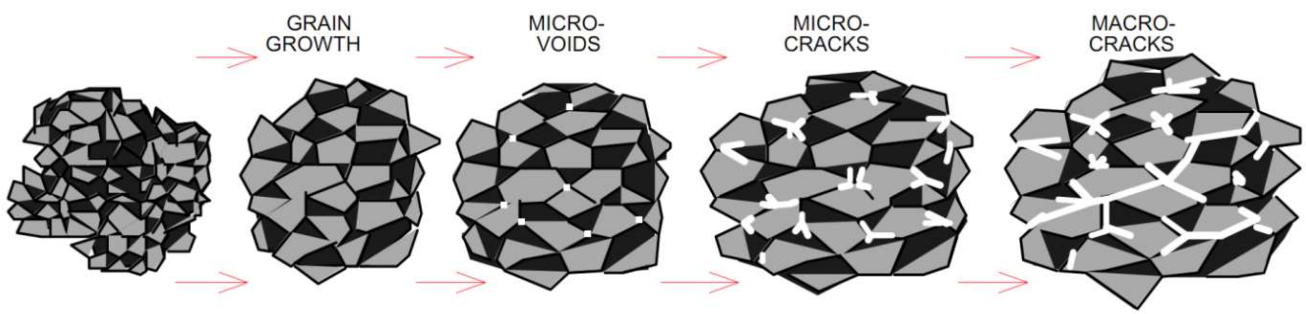
Solder Phase Coarsening

- There are two fundamental forces that drive grains in polycrystalline materials to grow. Grains coarsen because grain boundaries are areas of high potential energy. This is the primary driving force in single-phase materials. During grain coarsening, as grains grow larger, the total grain boundary area decreases, which, in turn lowers the free energy of the system.

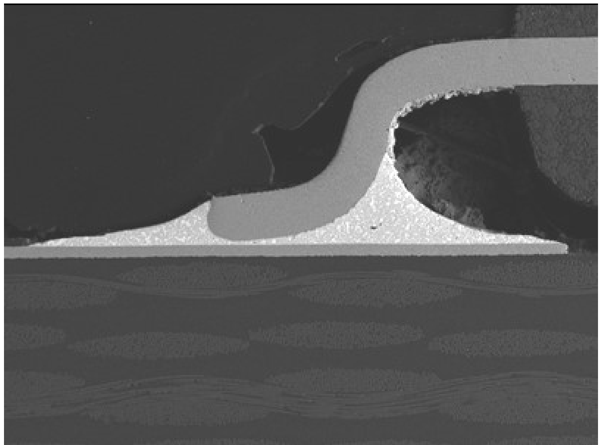
- Particles with smaller size tend to combine into a larger particle one with lower total interfacial energy. Grain growth is driven by the local boundary curvature and the presence of triple junctions, which remain in equilibrium and act as anchors to grain boundary mobility. Grain boundary mobility is highly dependent upon grain orientations across the boundary.

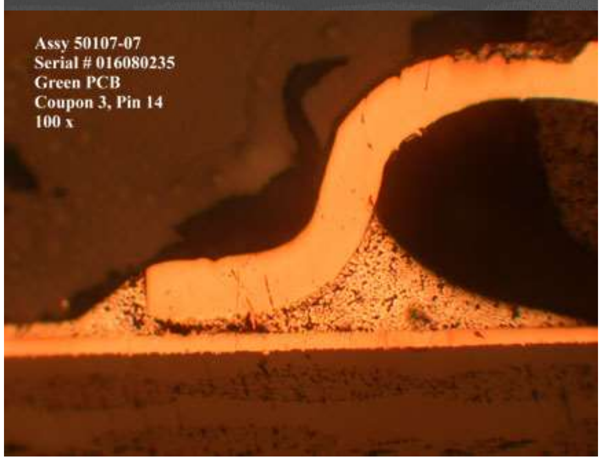
Solder Phase Coarsening

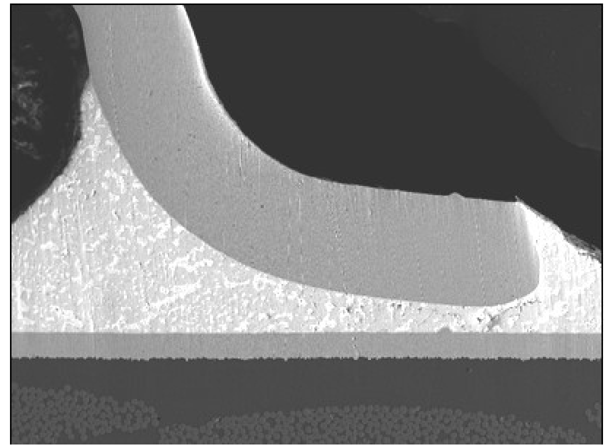
- From the original solder joint (left) the grains will grow as the solder joint is stressed. The growing grains will cause micro-voids to appear on the grain boundaries. The micro-voids will connect with each other to create micro-cracks and eventually macro-cracks. If the load is distributed evenly across the joint this will happen everywhere at the same time. In BGA balls this will happen in an entire layer of the bulk solder. If the load is not even then the grain growth and micro cracks are formed in the stress concentration and the micro-crack is advancing along a crack path.

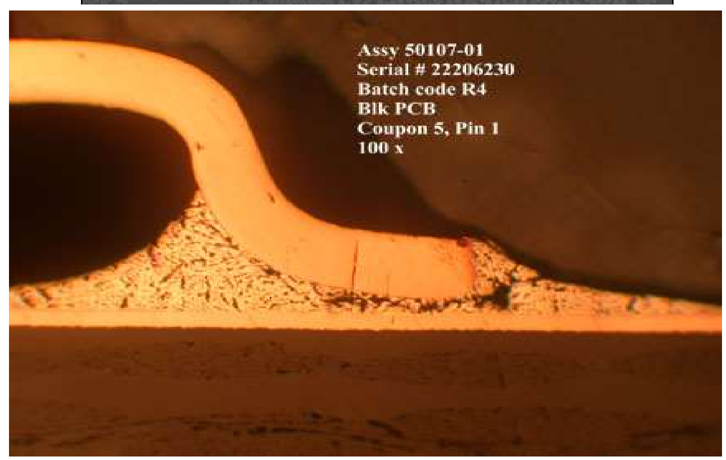


Solder Joint Coarsening Due to Thermal Stresses



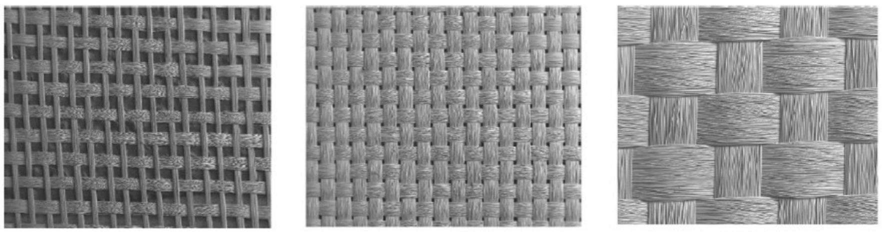






Printed Circuit Board Analysis – Glass Style

- PCB laminates (and prepregs) are fabricated with a variety of glass styles



1080 2116 7628

- Problem: Most datasheet properties are for laminate with 7628 glass style
  - Most laminate (and prepreg) in complex PCBs have a low volume fraction of glass (i.e., 1080 or 106)

Glass Style	Resin Volume Content	Fiber Volume Content
1027	0.86	0.14
1037	0.86	0.14
106	0.84	0.16
1067	0.84	0.16
1035	0.83	0.17
1078	0.82	0.18
1080	0.79	0.21
2313	0.74	0.26
2116	0.71	0.29
3313	0.71	0.29
3070	0.68	0.32
1647	0.66	0.34
1651	0.66	0.34
2165	0.66	0.34
2157	0.66	0.34
7628	0.64	0.36

Printed Circuit Board Analysis – Effect of Glass Style

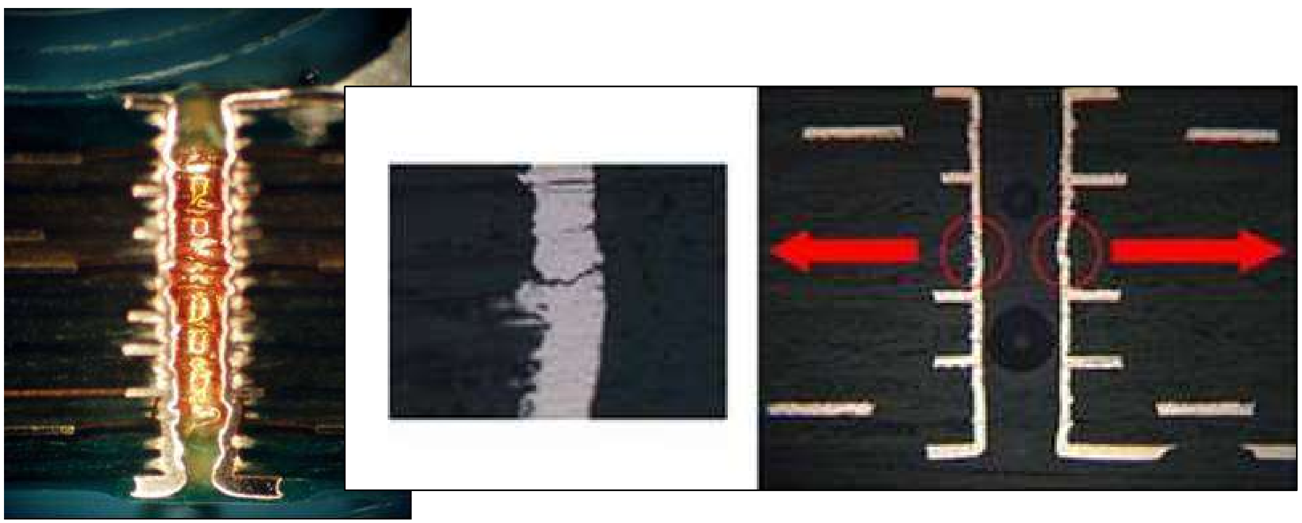
- Realistic target for board CTE is between 15 and 17 ppm/°C
- Most laminate suppliers provide CTExy values

Property		370HR Typical Value
Glass Transition Temperature (Tg) by DSC, spec minimum		180
Decomposition Temperature (Td) @ 5% wt loss		340
T260 Deg C (TMA)		60
T288 Deg C (TMA)		30
CTE, Z-axis	A. Pre-Tg	45
	B. Post-Tg	230
CTE, X-, Y-axes	A. Pre-Tg	13/14
	B. Post-Tg	14/17

- Key concern, these values are typically for a low resin content laminate (46%-50% resin content by weight, 7628 glass style)
- However the most popular laminates have much higher resin contents
  - Higher resin content = higher CTE
  - Lower modulus

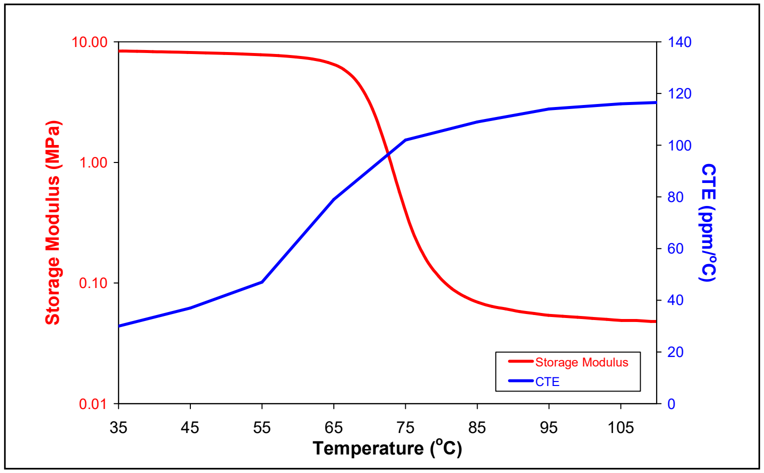
Plated Through Hole Fatigue

- PTH fatigue is the circumferential cracking of the copper plating that forms the PTH wall
- It is driven by differential expansion between the copper plating (~17 ppm) and the out-of-plane CTE of the printed board (~70 ppm)
- Validated industry failure model available - IPC-TR-579
- When a PCB experiences thermal cycling the expansion/contraction in the z-direction is much higher than that in the x-y plane. The glass fibers constrain the board in the x-y plane but not through the thickness. As a result, a great deal of stress can be built up in the copper via barrels resulting in eventual cracking near the center of the barrel as shown in the cross section photos below.



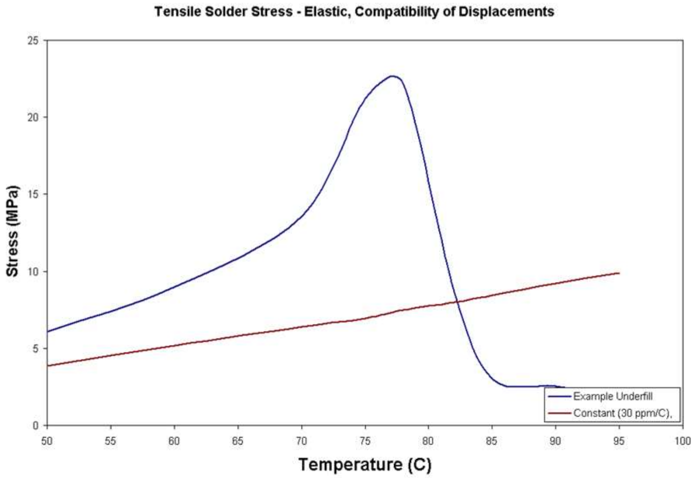
Tg Behavior

- Near the glass transition temperature (Tg), CTE changes more rapidly than modulus
  - Changes in the CTE in polymers tend to be driven by changes in the free volume
  - Changes in modulus tend to be driven by increases in translational / rotational movement of the polymer chains
- Increases in CTE tend to initiate before decreases in modulus because lower levels of energy (temperature) are required to increase free volume compared to increases in movement along the polymer chains



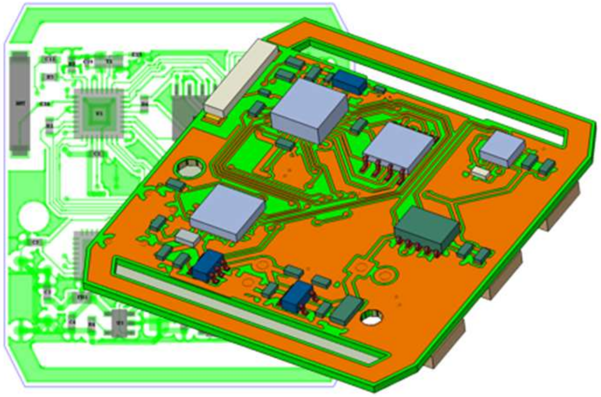
Polymer Science and Technology, Chapter 4: Thermal Transitions in Polymers, Robert Oboigbaotor Ebewele, CRC Press, 2000

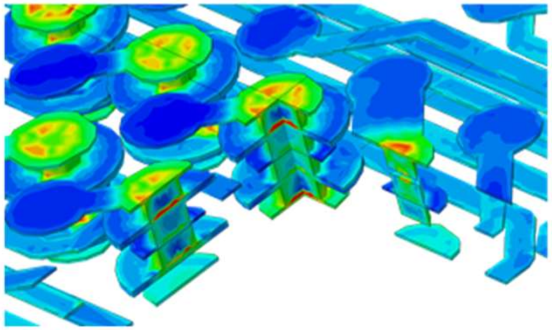
High stresses generated due to CTE increase before modulus decrease



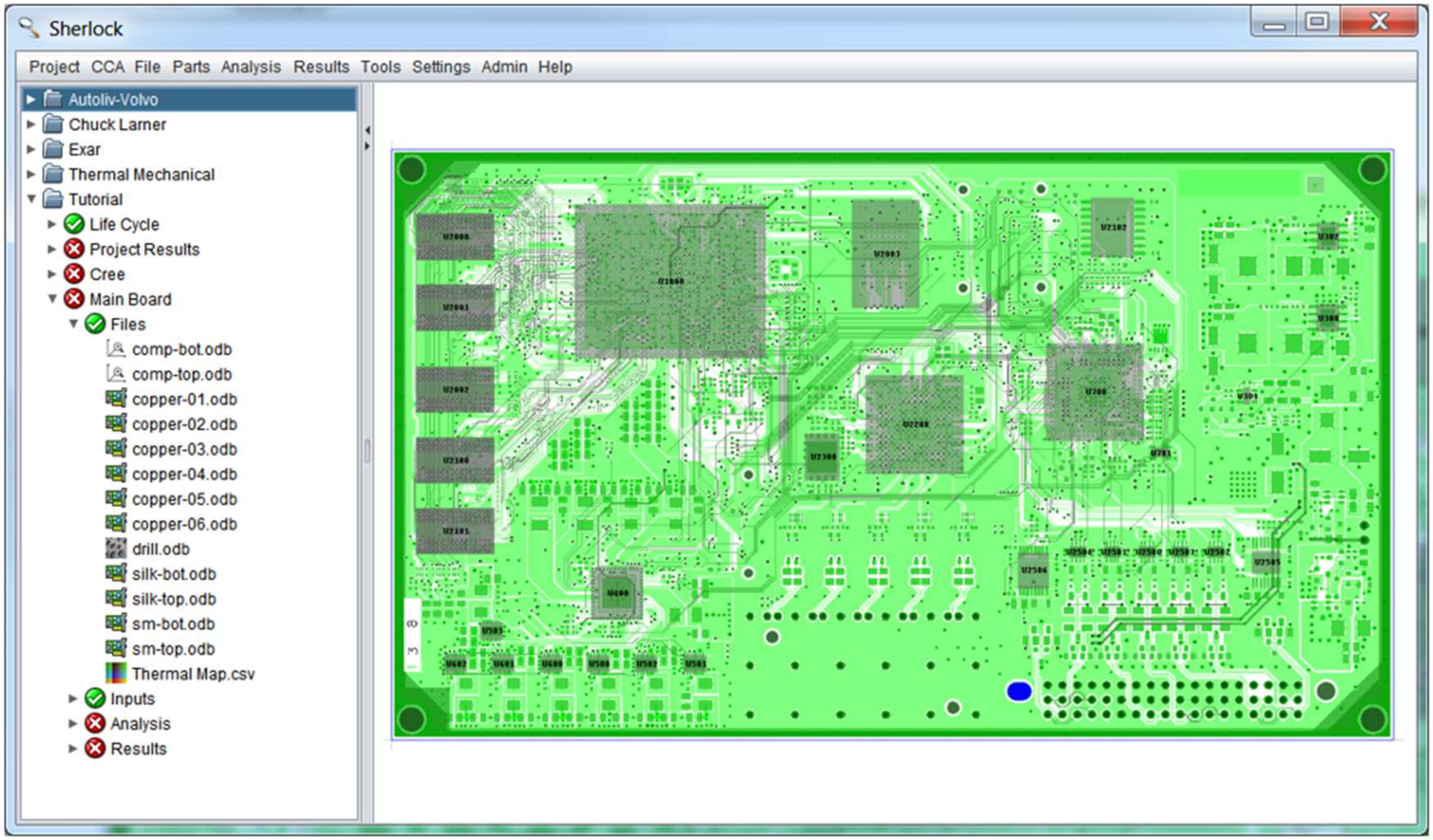
Reliability Physics Modeling – Fastest Way to Analyze

- Data Transition to Sherlock
  - How can we model the PWB, parts, interconnect materials, stresses in the products lifetime and reliability metrics, utilizing reliability physics.
    - Import GERBER or ODB++ files for the PWB layout
    - Import a csv delimited BOM for the parts list data
    - Load the mechanical and thermo-mechanical stresses the product will encounter
    - Load the reliability requirements for life expectancy,

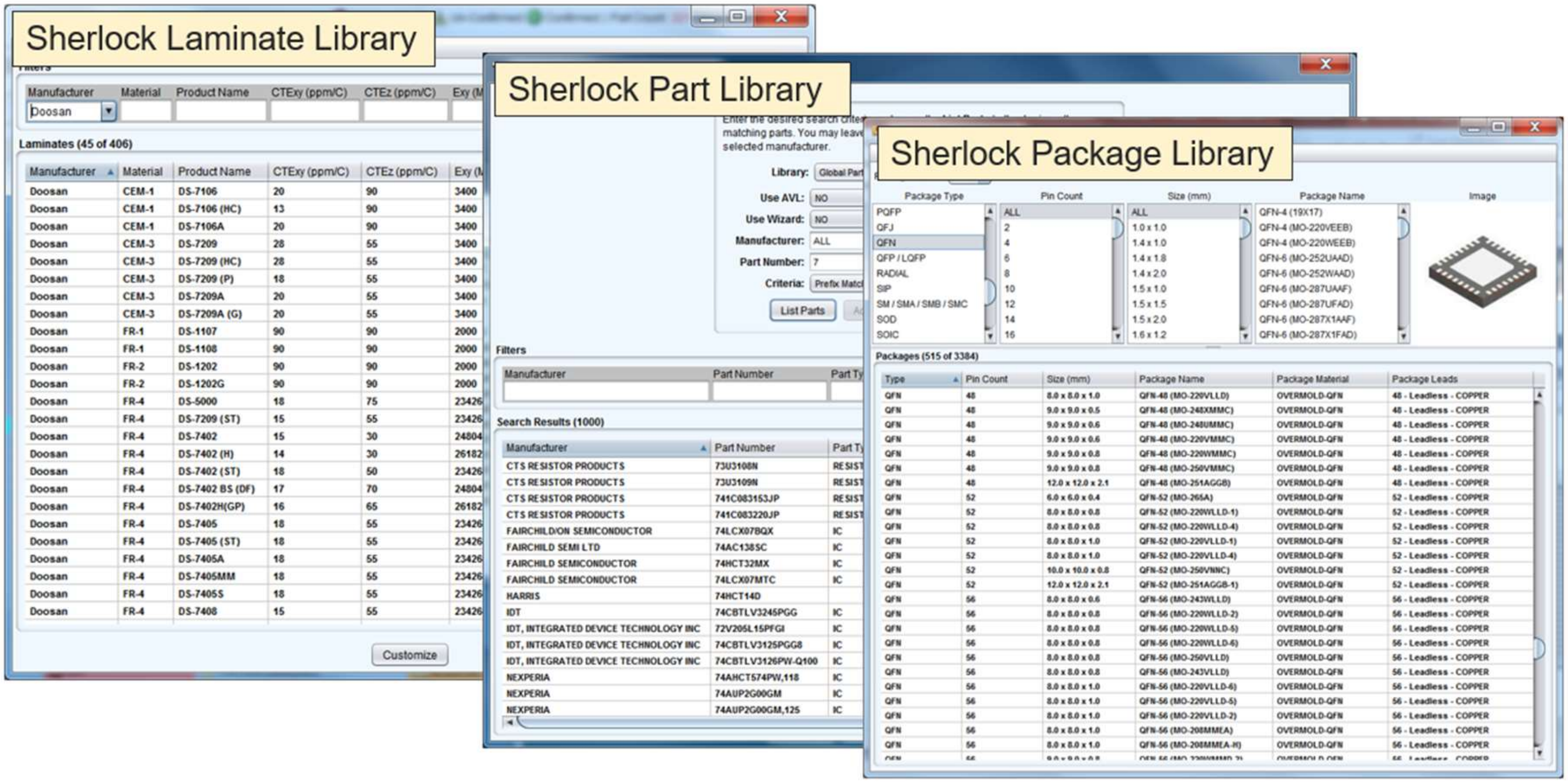




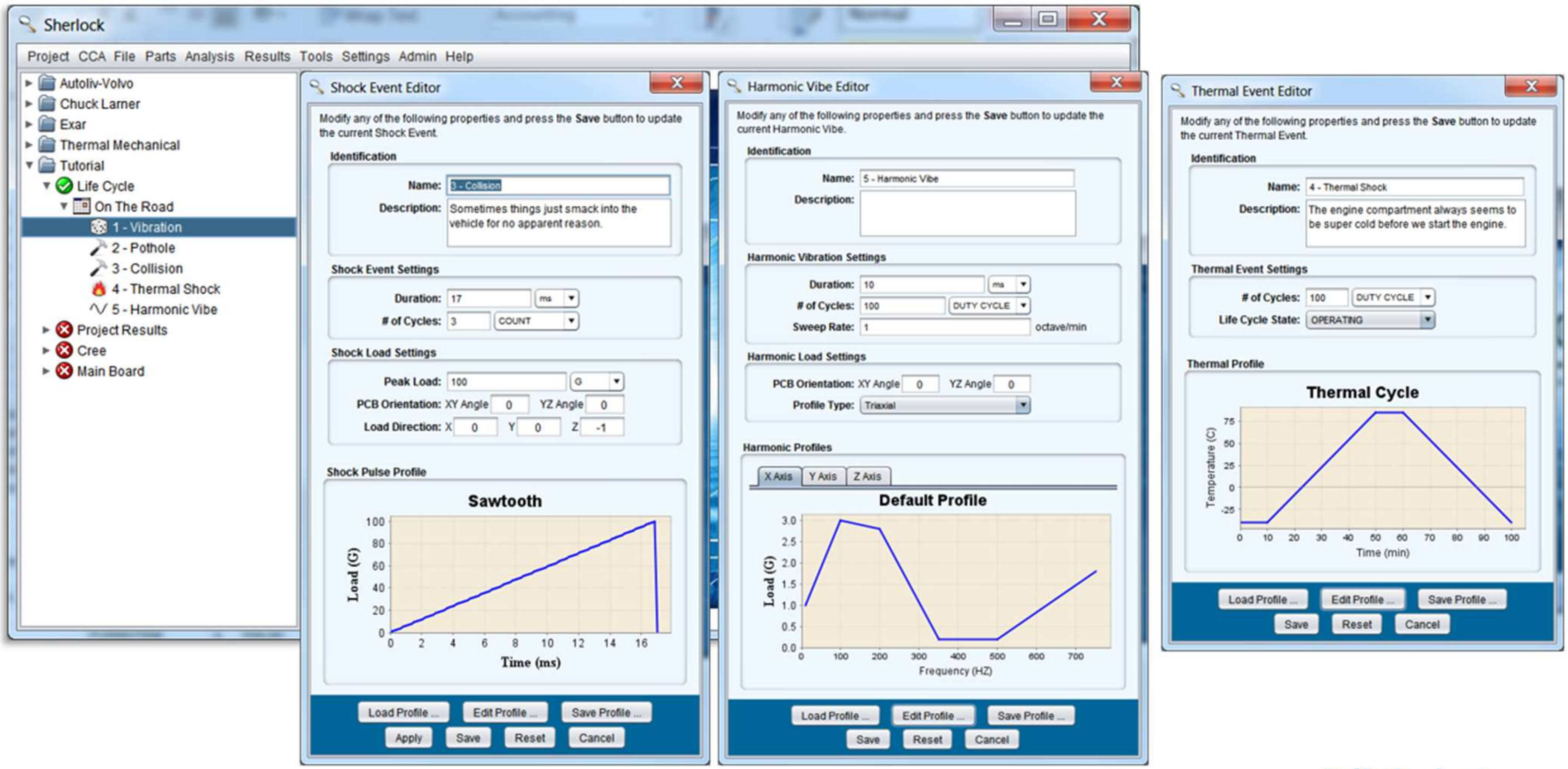
Import Electronic Design Files (GERBER/ODB++/IPC-2581)



Sherlock Libraries

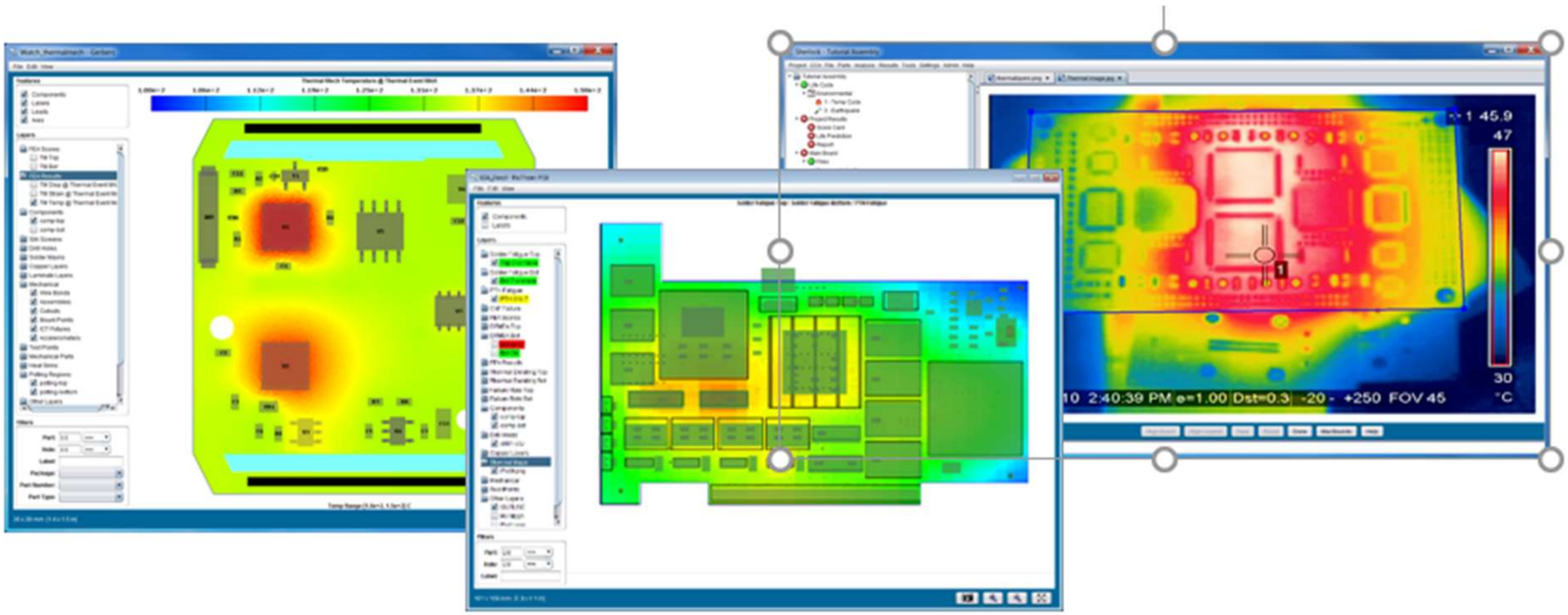


Life Cycle Conditions

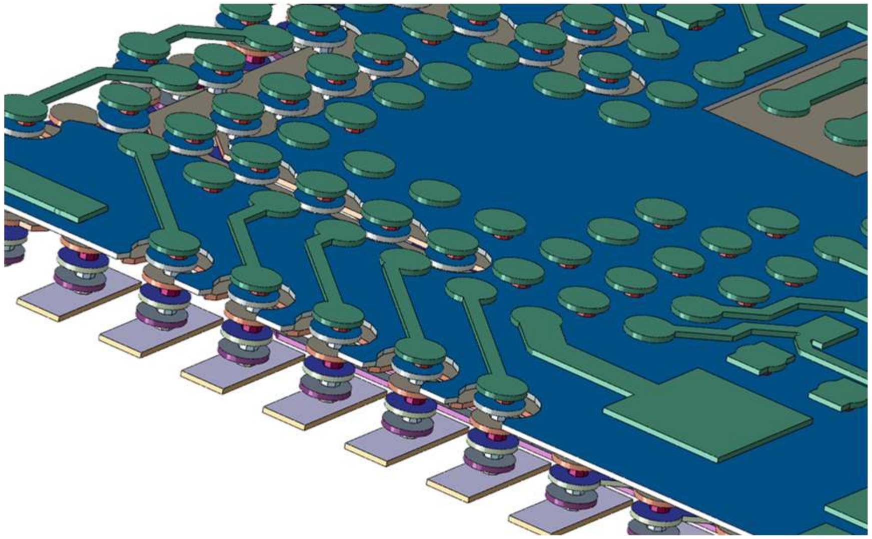


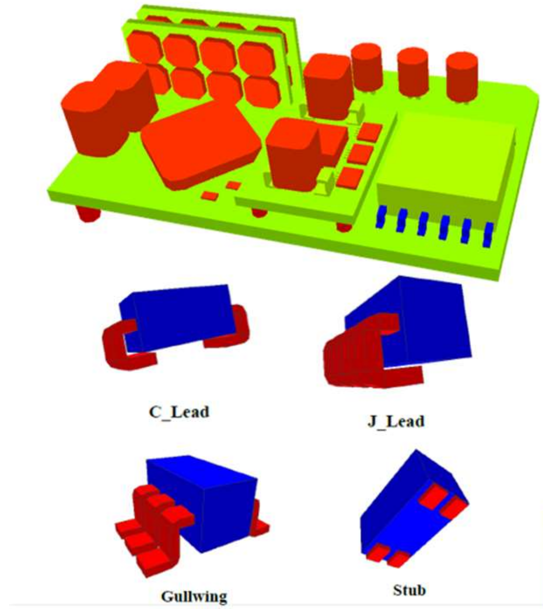
Virtual Power Cycling

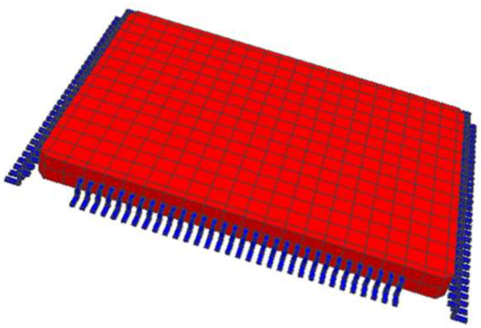
- You can override the isothermal temperatures in the event editor by uploading component temperatures, or thermal maps (analysis or IR camera).

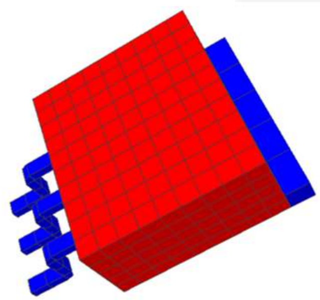


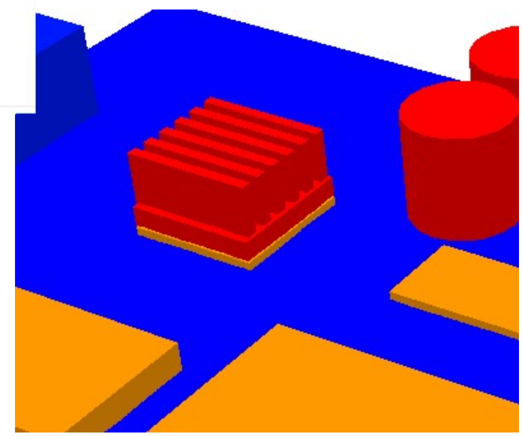
Sherlock Modeling



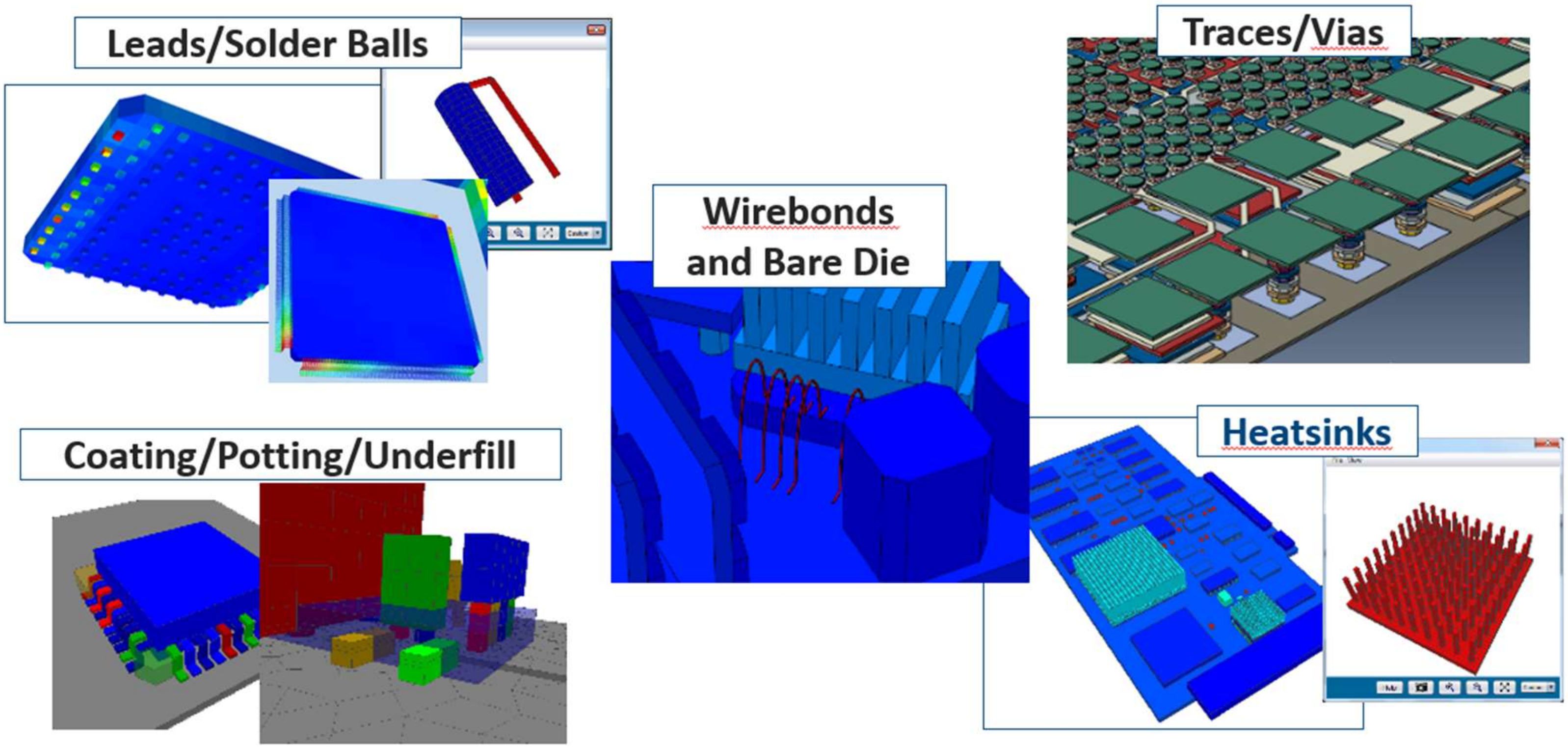






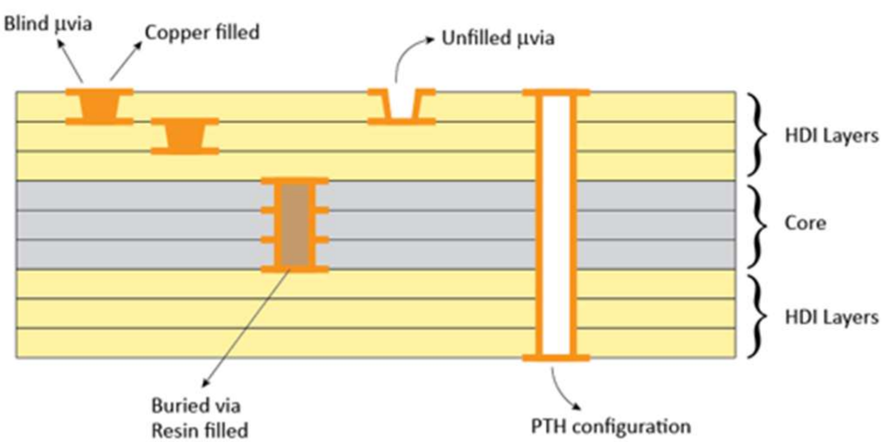


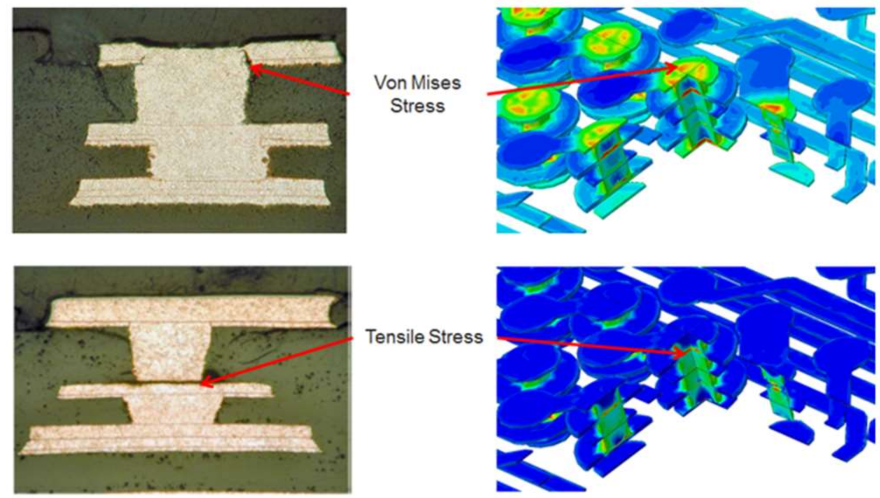
Geometries, Properties, Conditions, Loads



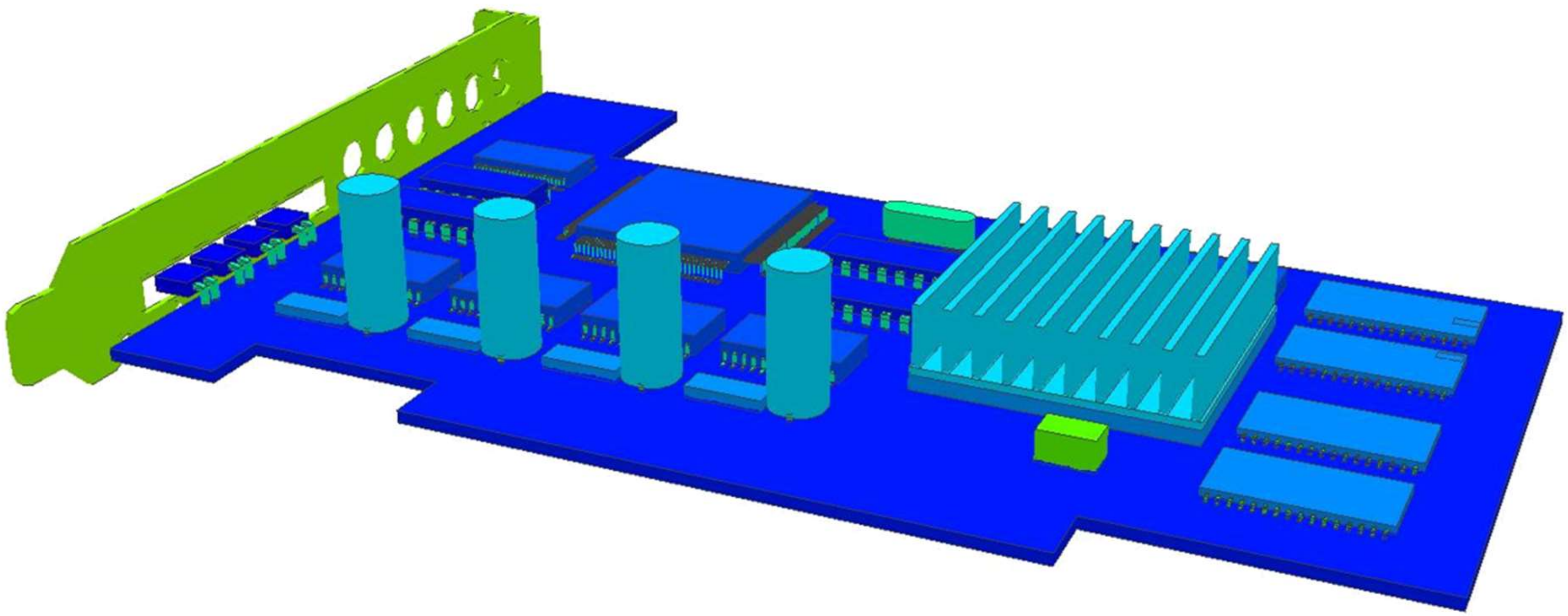
Via Design Rules

- Stacked Vs. Staggered
  - Mosaic mesh
  - Trace modeling



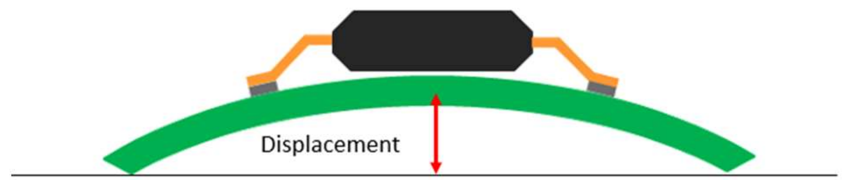


Example

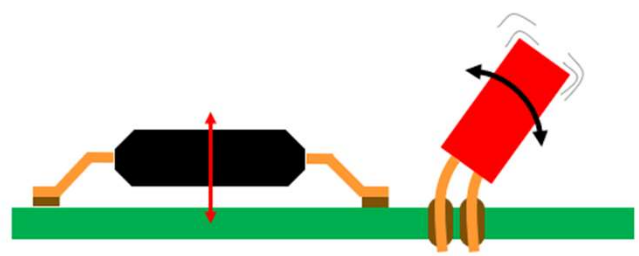


Example: Effects of Vibration

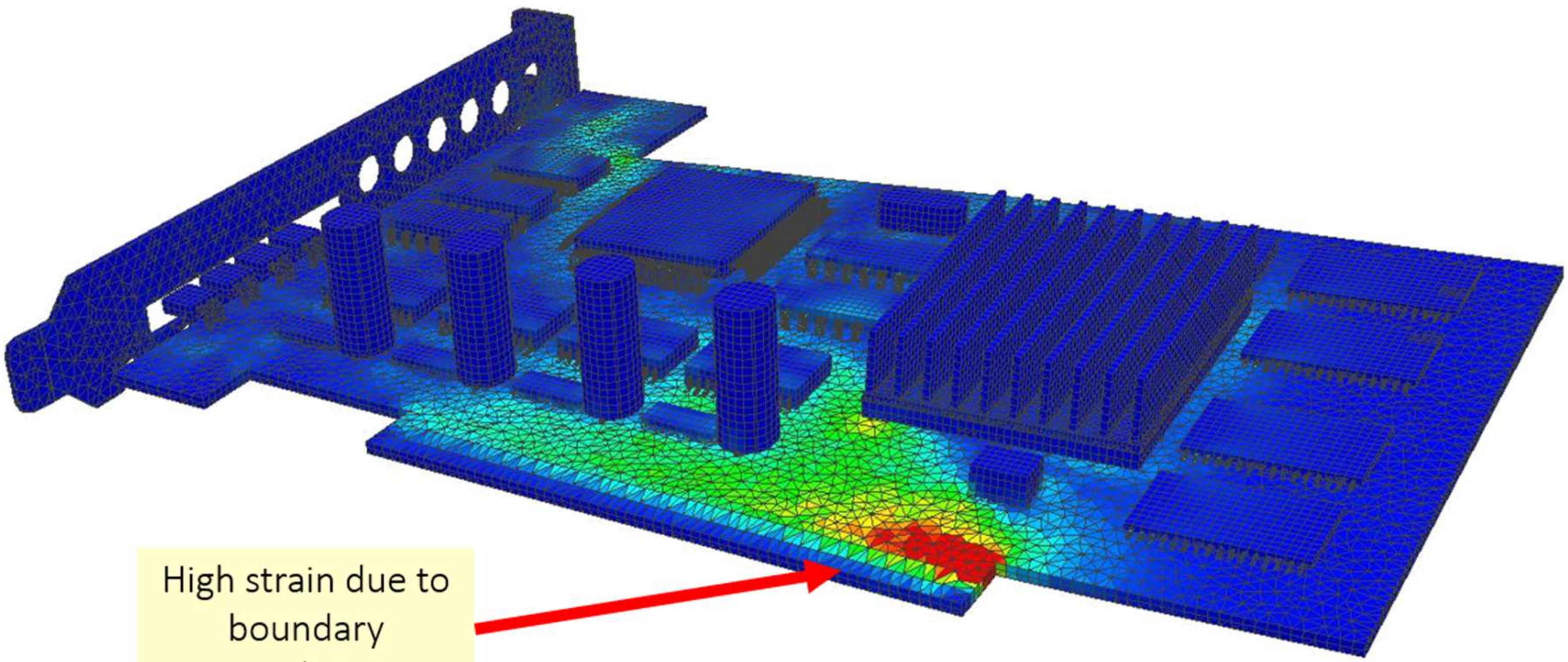
- Board Bending
  - Components can shake off due to fatigue in leads or solder



- Component Resonance
  - Lead and solder fatigue due to component motion

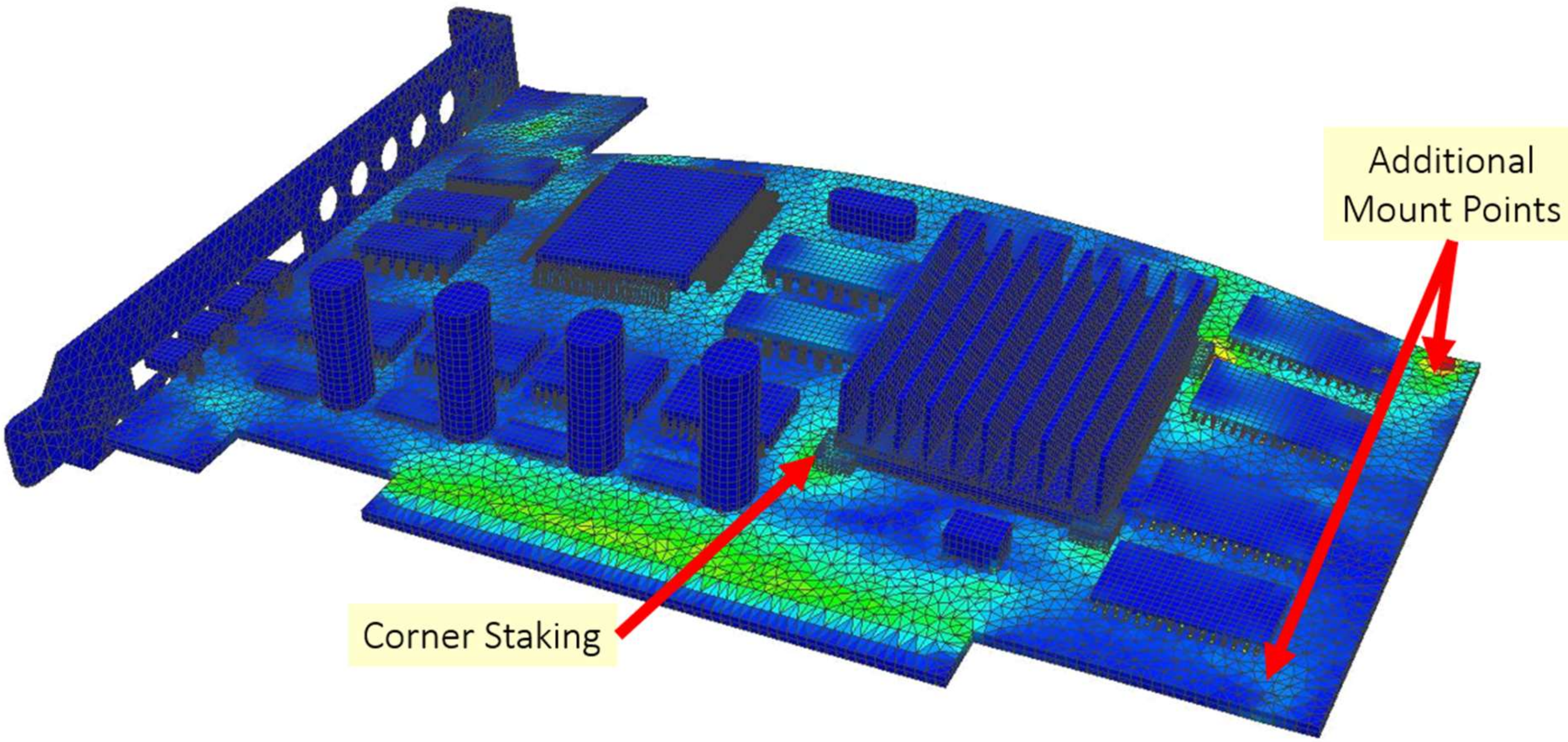


Example: Effects of Vibration



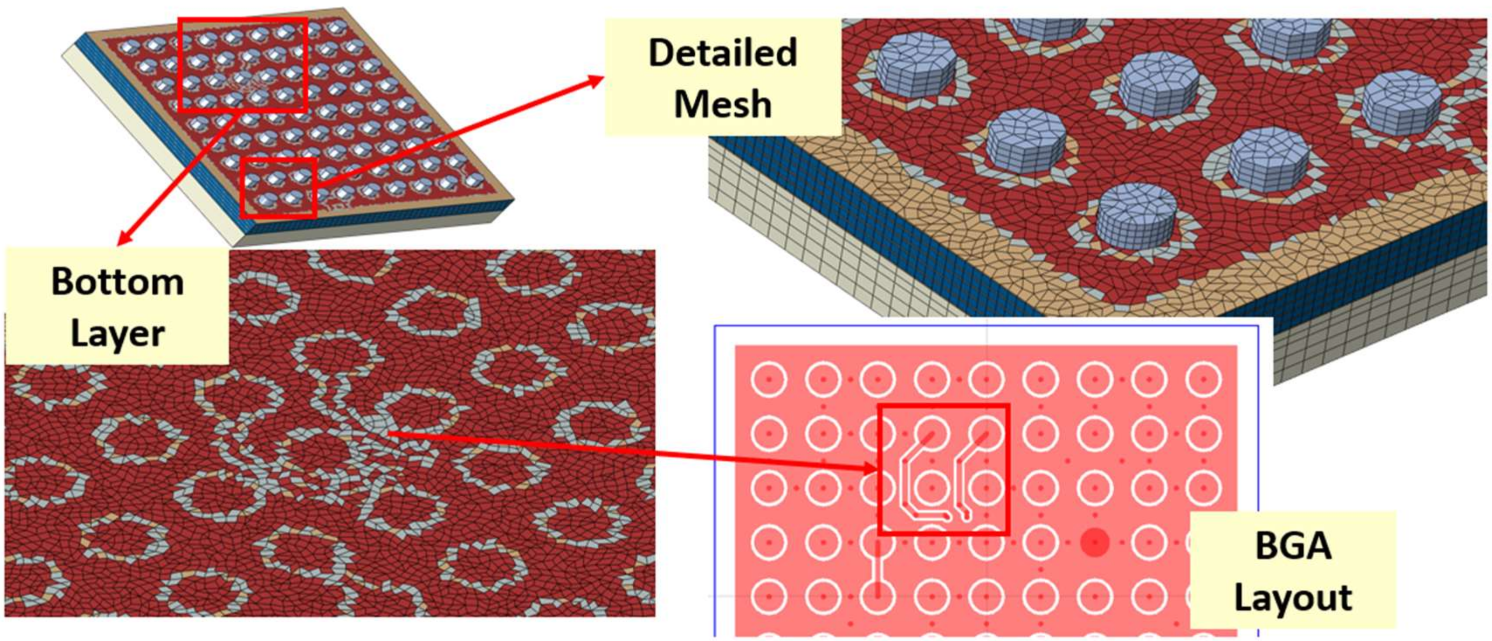
High strain due to boundary condition

Simulation of Mitigation Strategy

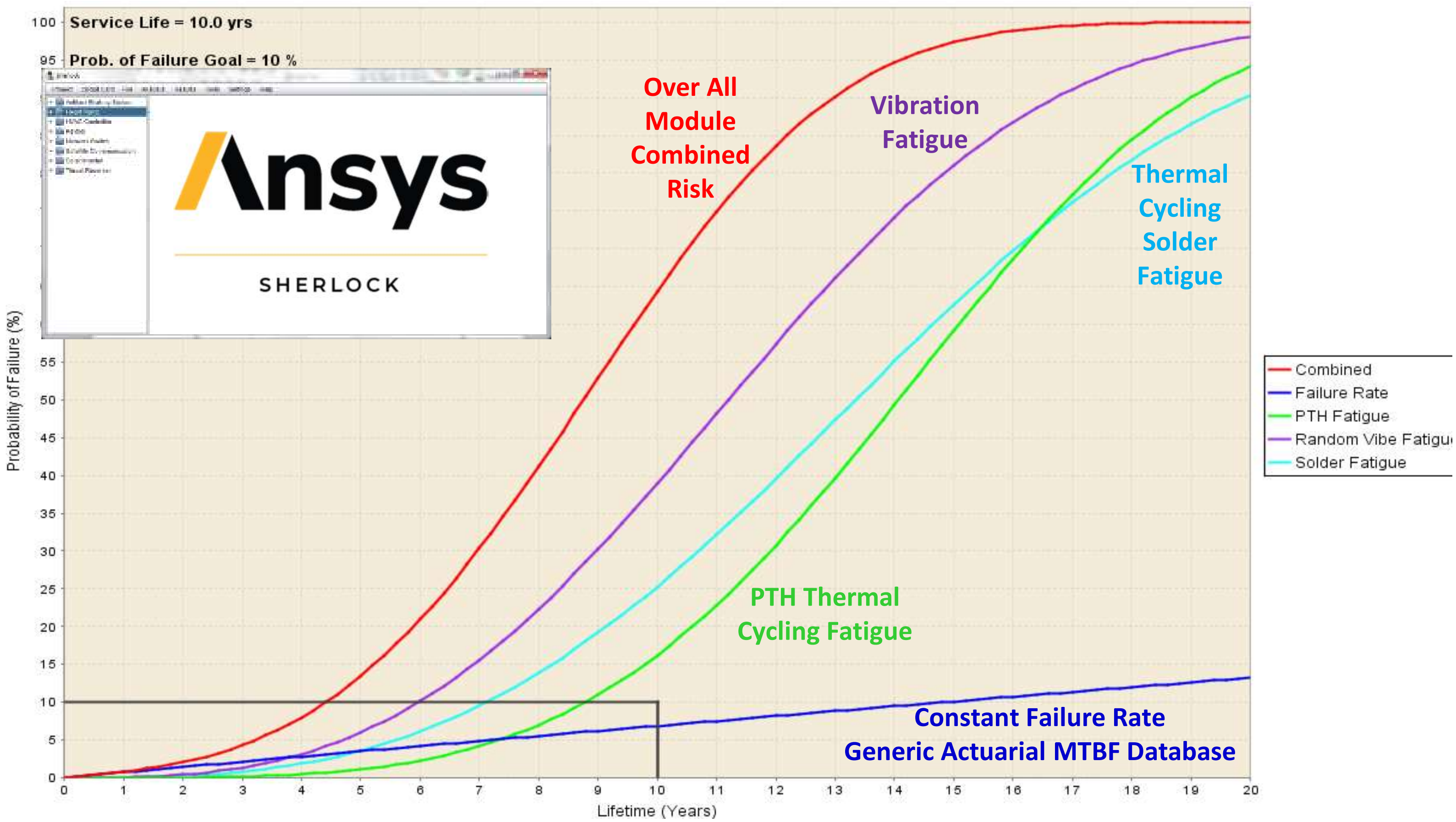


Creating a Model for BGA Packages

- Sherlock can export a detailed mesh for all the layers of the BGA



Life Curves



Service Life = 10.0 yrs
Prob. of Failure Goal = 10 %
Ansys
SHERLOCK
Over All Module Combined Risk
Vibration Fatigue
Thermal Cycling Solder Fatigue
PTH Thermal Cycling Fatigue
Constant Failure Rate
Generic Actuarial MTBF Database
Combined
Failure Rate
PTH Fatigue
Random Vibe Fatigu
Solder Fatigue
Probability of Failure (%)
Lifetime (Years)

Conclusions

- Modeling today's complex electronics using simulation tools is a cost-effective way to assess the reliability of a design prior to committing to manufacturing.
- Electronics, due to the myriad of materials implemented in the component packages, interconnects and circuit board make failure isolation and identification very difficult.
- Assessing the potential effects of failures early in the design process allows the designer to implement adjustments to obviate these failure issues.

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