Development and R2R Scale up of a Hybrid Printed CMOS Silicon TFT Process

Patricia Beck
Principal Engineer

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Thin Film Electronics ASA

1 Near Field Communications (NFC) for IoT enablement

2 Global leader in printed electronics

3 Scaling to the billion of units by roll based manufacturing

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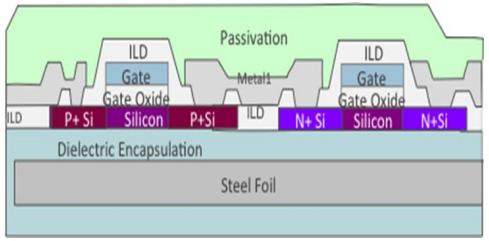
Outline

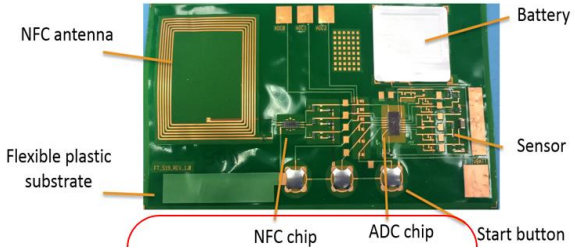
IoT of Everyday Objects using Near Field Communication (NFC)

CMOS Silicon TFT with Silicon on Stainless Steel Substrate



Volume Scaling to Low Cost with Roll Processing

Product Evolution with Sensors



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Thinfilm's Vision

Add a

little bit

of intelligence

to *a lot* of things.

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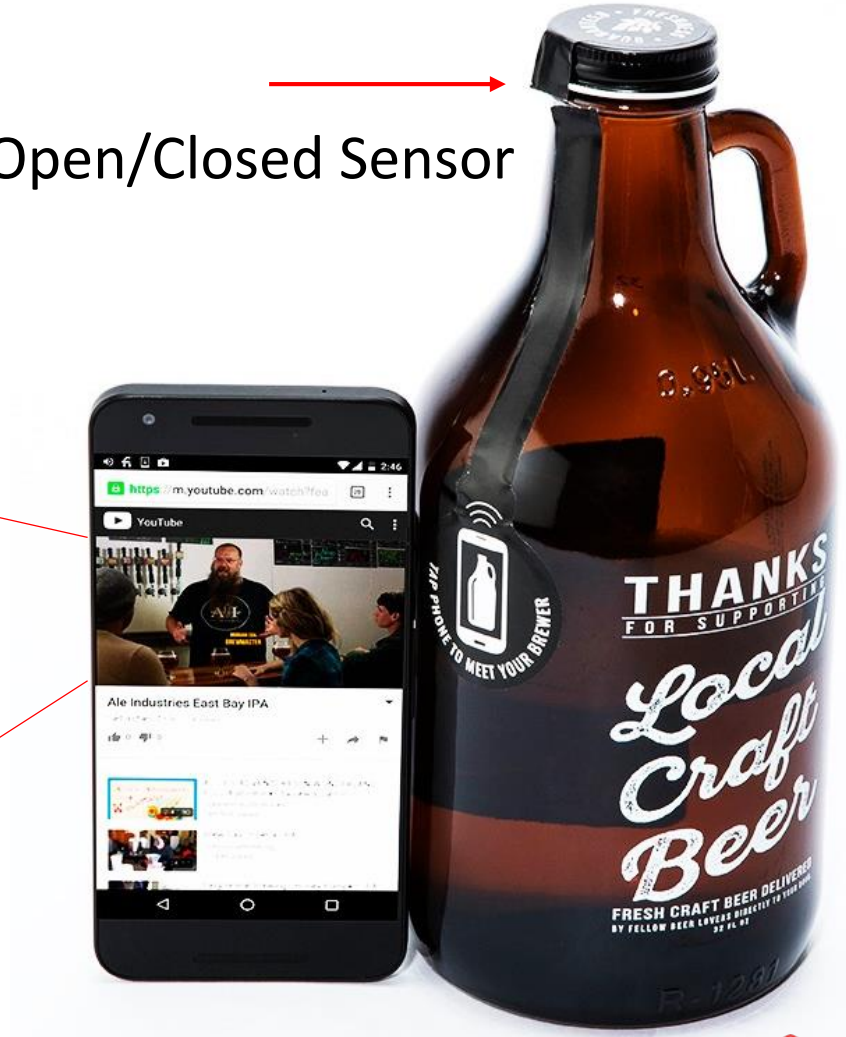
Near Field Communication (NFC):

HOPSY.

Instant launch of
brew master video

Single Bit Open/Closed Sensor



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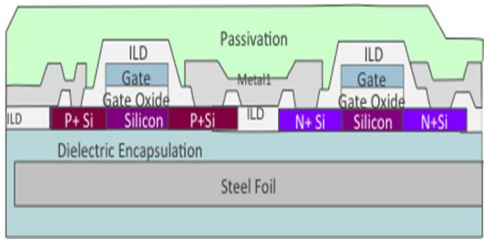

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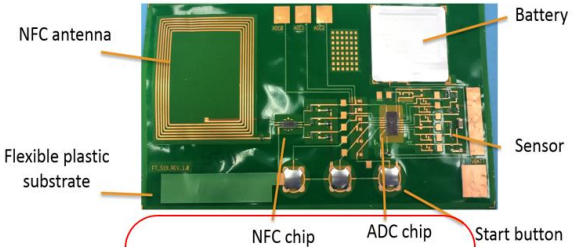

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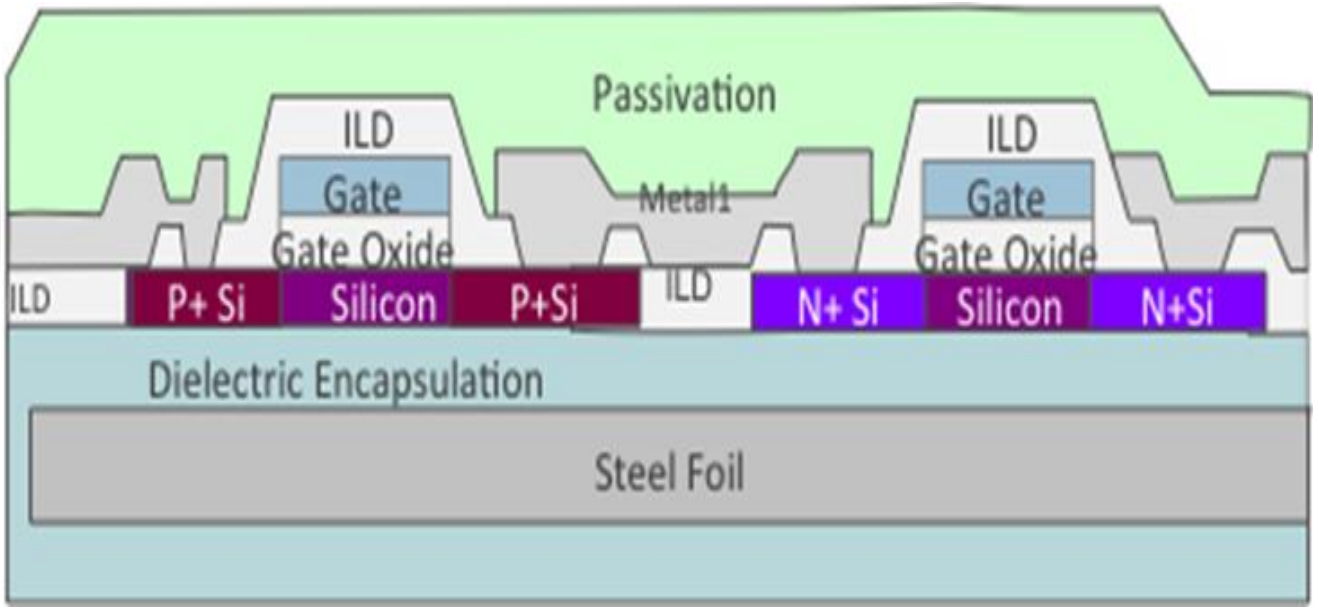
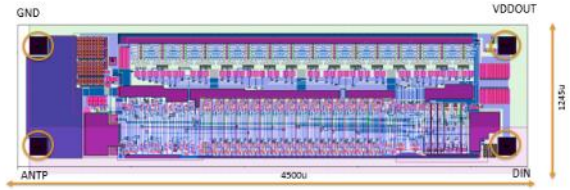
Printed Dopant CMOS Poly-TFT Process on Stainless Steel Foil





Rolled Steel → Barrier → Silicon Crystallization Litho → Gate Stack Litho → Print Dopant Anneals → Via + Litho → Metal + Litho → Encoding → Print Passivation

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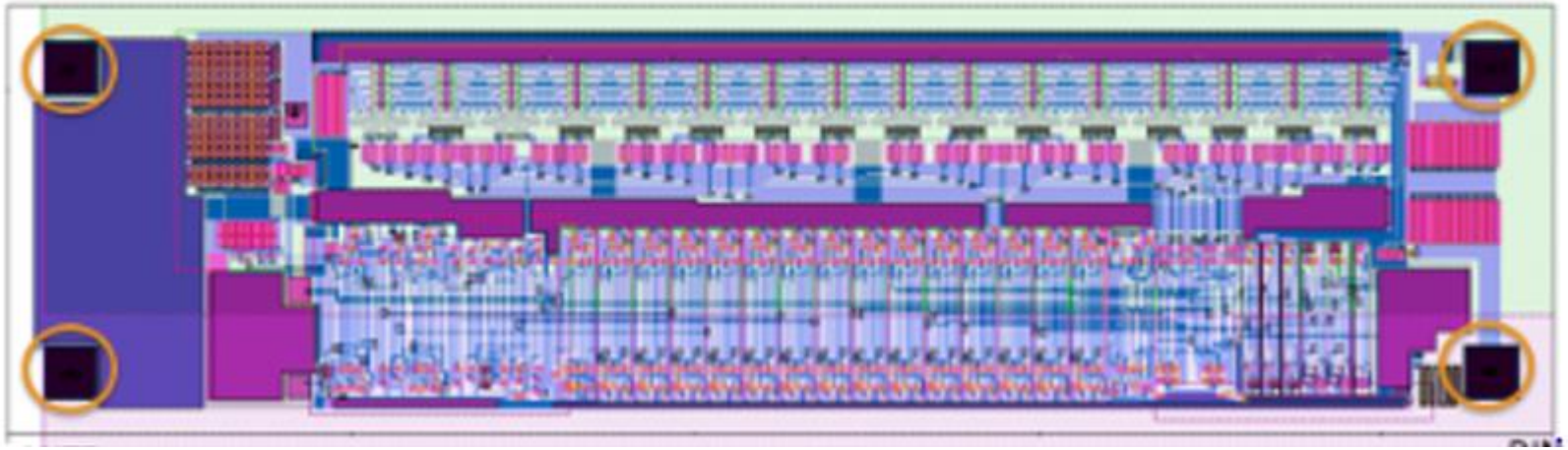
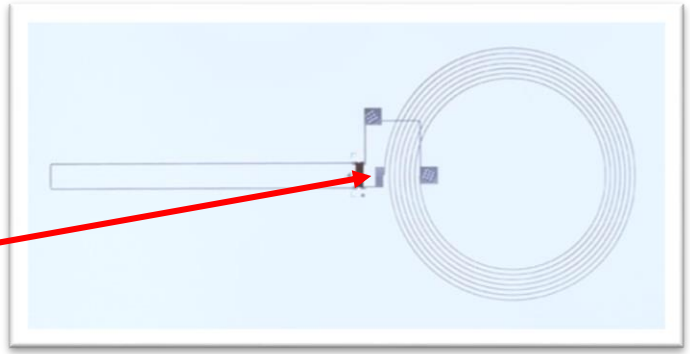
128 Bit CMOS NFC



- 13.56 MHz Operation
- 128 Bit ROM (cannot be rewritten)
- Tags Talk First Protocol: 5ms Read Times
- Adequate Area for Interface to Sensor Pads
- Optimized Die Size for Low Cost Attach to Antenna



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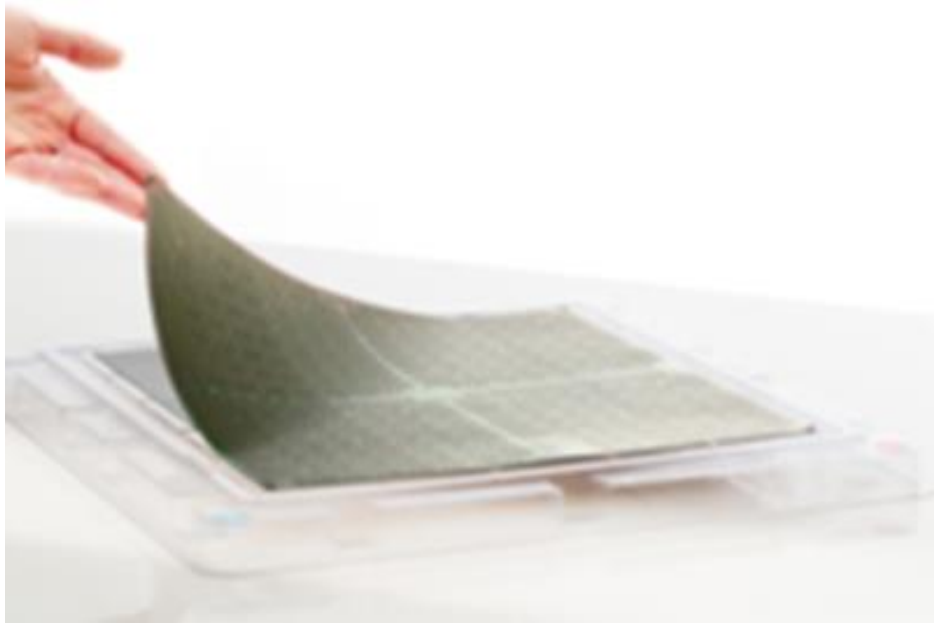
Key Technology Requirements

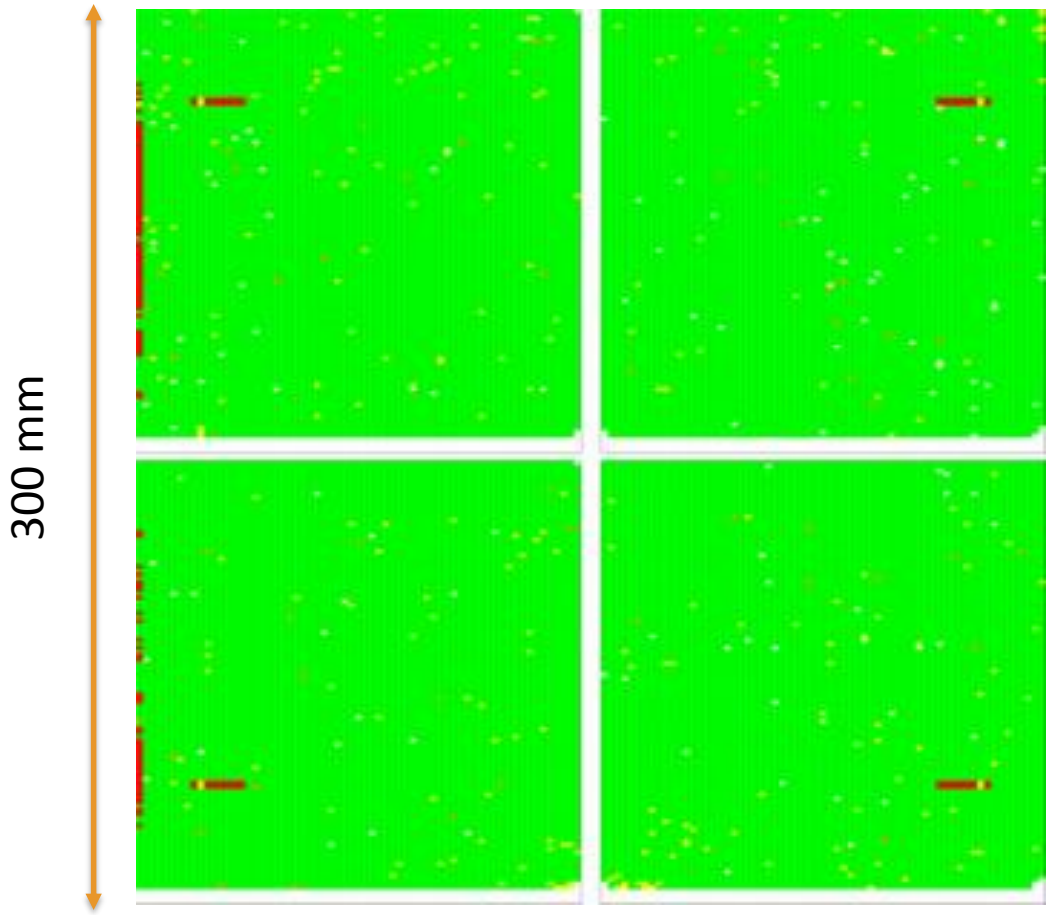
- Low Cost, Low Step-Count TFT based Roll-to-Roll Manufacturing
  - Billions - trillions of low cost units at scale
    - *R2R compatible process and assembly*
  - Roadmap to lowest step-count and capital cost
    - *Maximize print content with excellent overlay capability*
    - *Hybrid processing (lithography) where print cannot yet support critical design rules*
- RF (13.56 MHz) Capable Circuits and Materials
  - High mobility, low power circuits with adequate transistor density
    - *Self-aligned top-gate CMOS*
    - *Laser crystalized, polysilicon based TFT*
  - Thin, unbreakable form factor with low cost and excellent dimensional stability
    - *100um Stainless steel substrate with a roadmap to <50um*
    - *No need for backgrind and thinning*
  - *Printed semiconductor-grade inks and films (silicon and dopants)*

Stainless Steel Substrate: Key Advantages

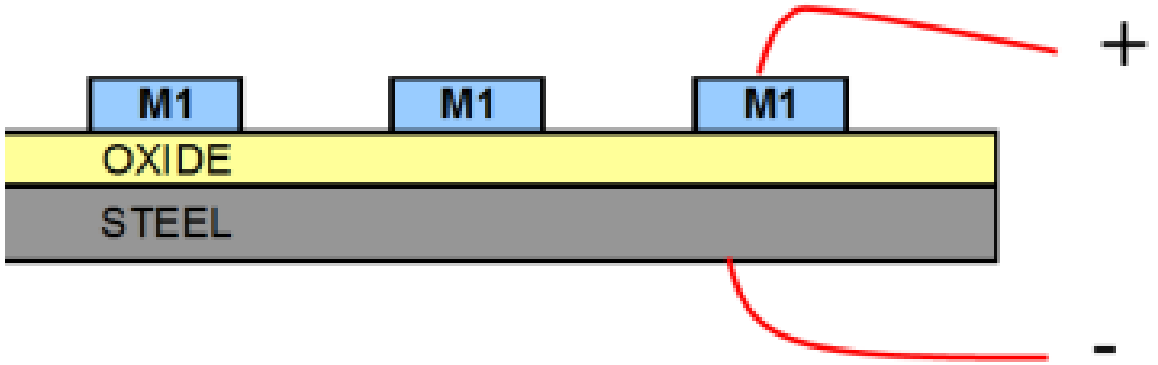
- Low Cost
- Large Area, Thin, Unbreakable Form Factor
- High Reflectivity and Smoothness
  - *Polished Surface <20um flatness*
- Compatible with Dicing and Assembly Processes
- Scalable to Roll Format
  - *Dimensional Stability*
  - *High Temperature Compatible*
  - *High Quality Diffusion Barrier*



Stainless Steel Substrate: Defectivity



Substrate yield map



Schematic cross section of MIM capacitors (not to scale)

- Green die represent tens of thousands of yielding capacitors tested at voltages up to tens of volts
- Individual capacitor areas are several mm^2 with negligible substrate shorts
- **Substrate roughness is not a concern in terms of product yield!**

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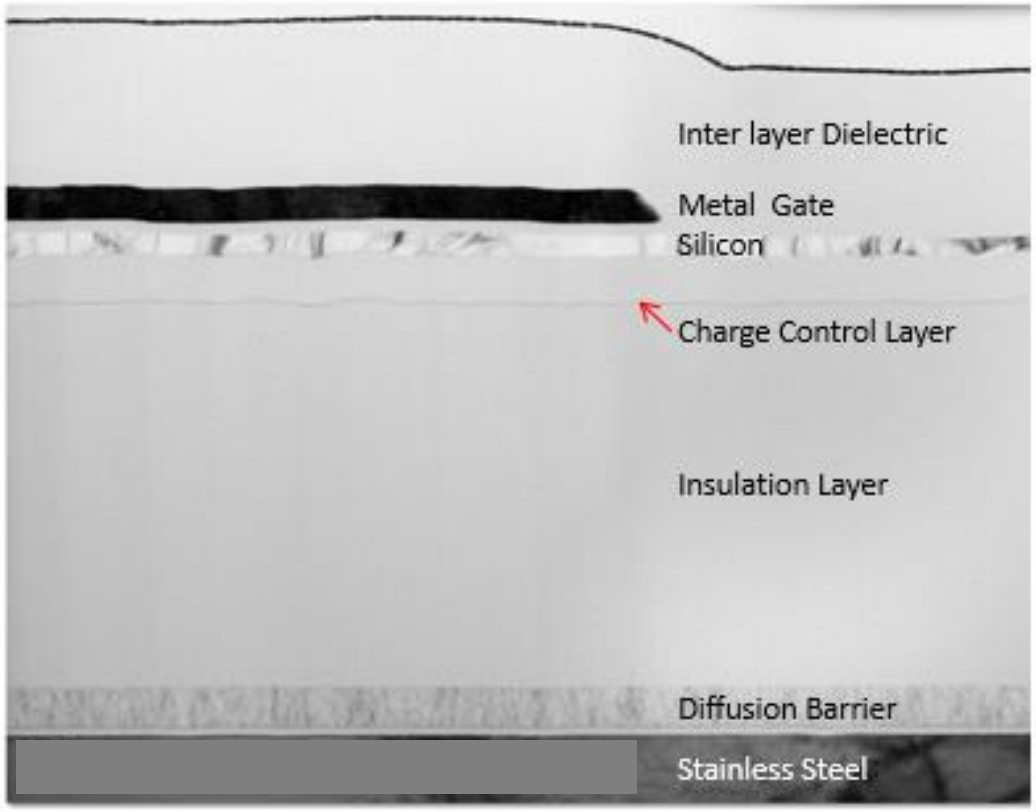
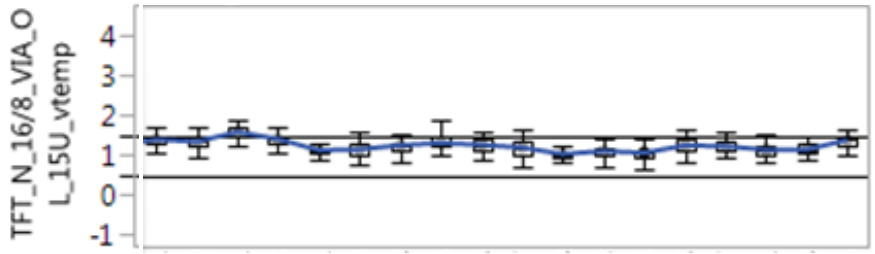
Vt and Charge Control



PDPS Transistor (TFT) Stack



NMOS lot-to-lot Vt variation (volts)

Ten 300 x 300 mm sheets/lot

No Vt adjust ion implantation is used in the PDPS process flow.

Manufacturing Vt Control and targeting achieved using stack and device parameter engineering

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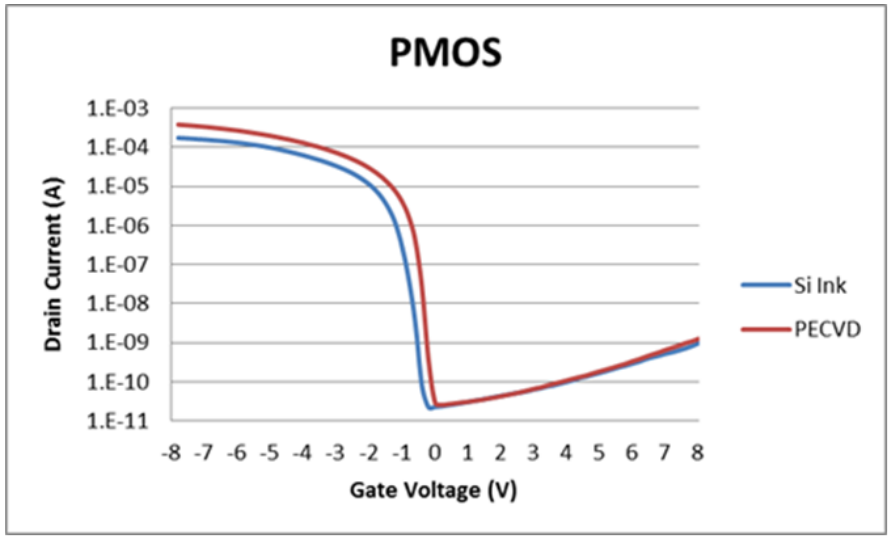
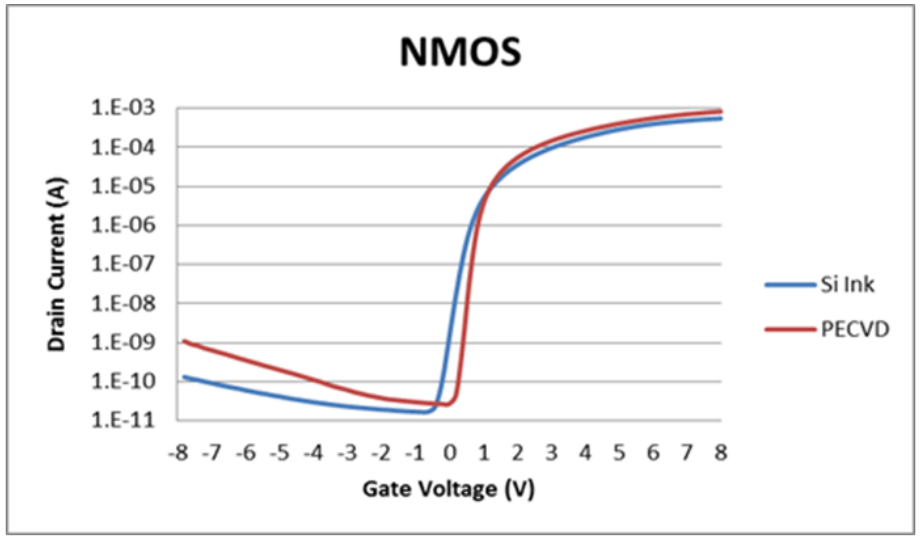
TFT Characteristics: PECVD vs Liquid Silicon Ink



Id-Vg characteristics of PMOS TFT devices prepared with ink-based and PECVD methods. W/L = 8µm/4µm



Id-Vg characteristics of NMOS TFT devices prepared with ink-based and PECVD methods. W/L = 8µm/4µm

Typical TFT Parameters of PECVD and ink-based transistors with printed dopant on 300mm x300mm stainless steel substrate.

TFT type	PMOS		NMOS	
Film Deposition metho	PECVD	Ink	PECVD	Ink
Mobility sat [cm2/Vs]	80	80	200	200
Threshold Voltage[V]	-0.6	-0.9	1.0	1.0
Slope [V/decade]	0.25	0.25	0.25	0.25
On/Off	1.00E+07	1.00E+07	1.00E+07	1.00E+07

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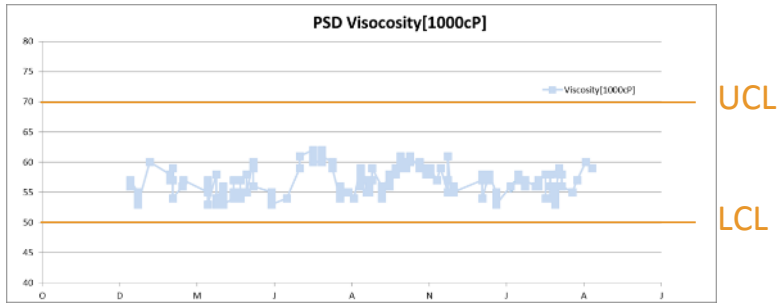
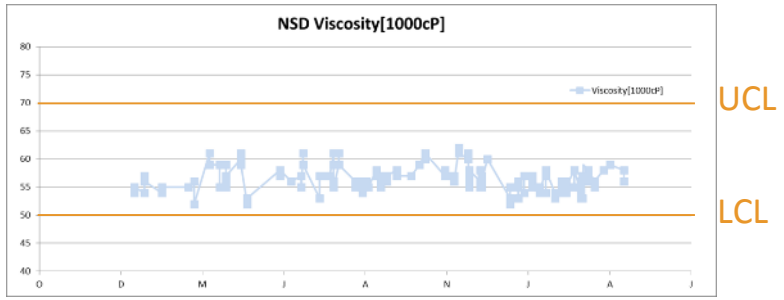
Screen Printed N and P Dopants: No ion implant

Key Printed CMOS Enabling Technology

- Low maintenance, high throughput, low step count module.
- Eliminates High capex Ion Implantation and Lithography
- *Potentially Applicable to c-silicon solar process*



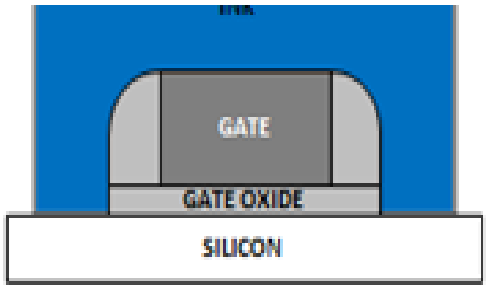
Batch-to-batch P dopant ink viscosity



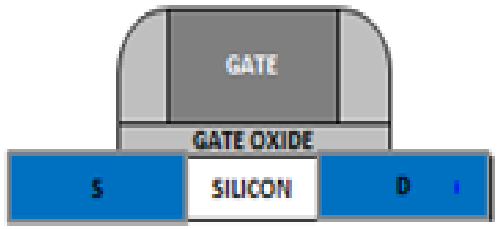
Batch-to-batch N dopant ink viscosity

Ink Formulation and Printing Process

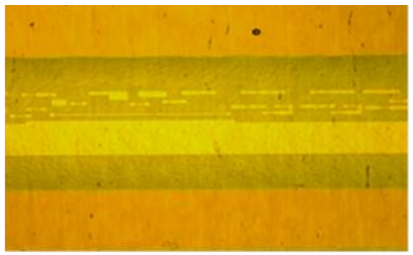
- Semiconductor grade purity
- Excellent batch viscosity control in a manufacturing environment



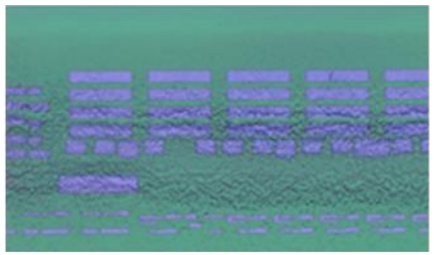
PRINT P or N -TYPE DOPANT



FURNACE DRIVE IN



Typical Screen Printed Line before thermal annealing.



Surface after annealing

Surface Post clean

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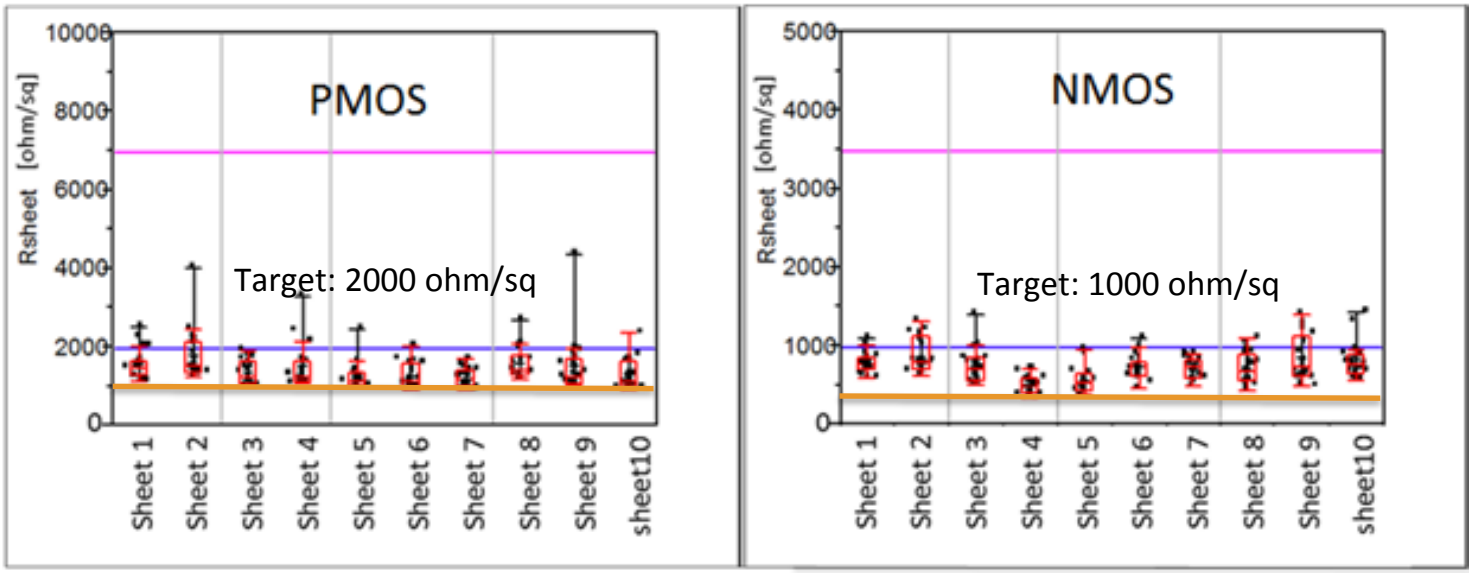
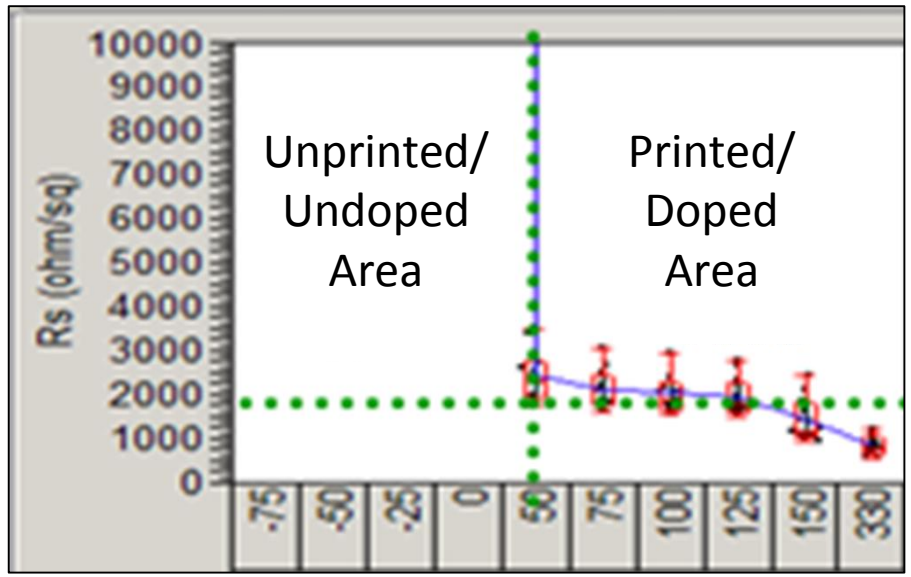
Doping Control

- Tight silicon sheet resistance (Rs) distributions (thermally activated).
- Rs can be targeted from 200-2000 ohm/square based on surface engineering, ink formulation and activation method.
- Highly Selective Doping. N and P doped areas can abut limited only by print resolution.



Sheet resistance distributions within a lot of 10 sheets. Rs values for P+ and N+ doped resistors.



Location dependent doping. The “0” mark is at the edge of the printed dopant area. The x-axis unit is microns.

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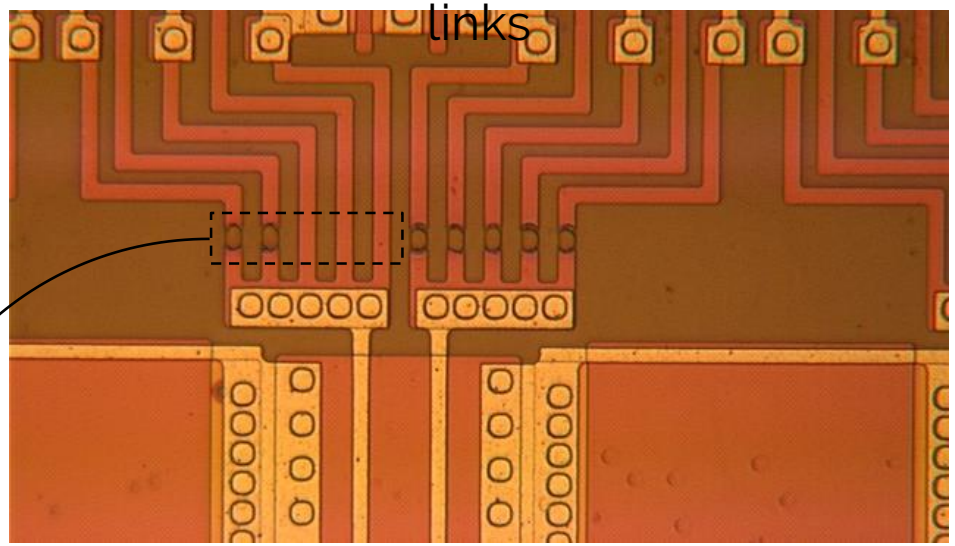
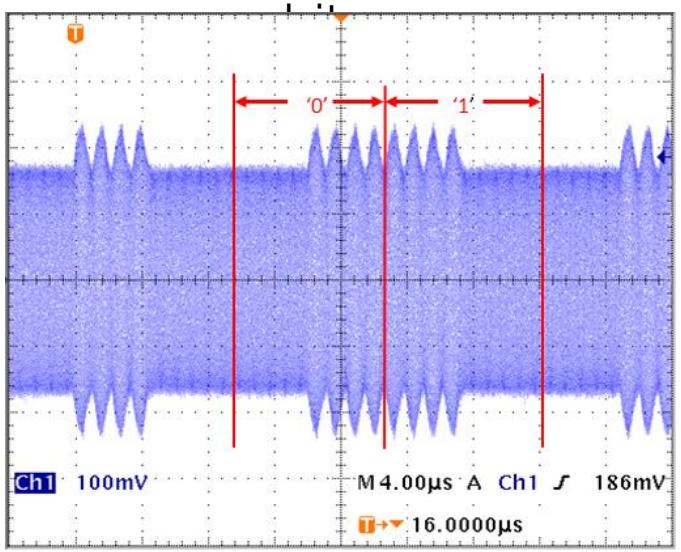
Encoded Read Only Memory

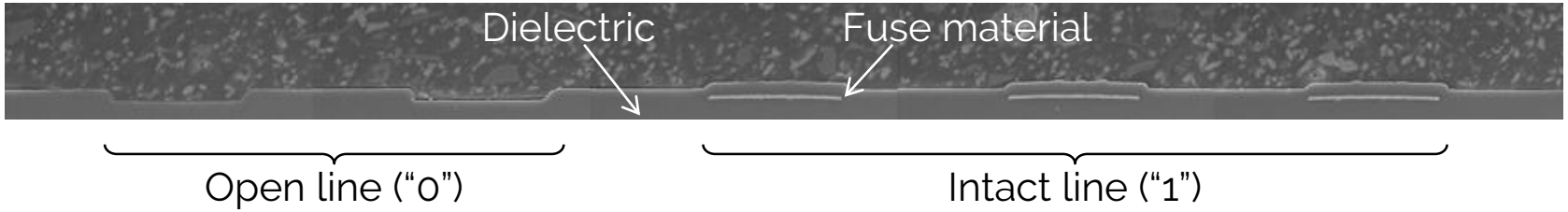
Top view of open (“0”) and intact (“1”) fuse links



Preferentially ablated material produces a reliable open state

Oscilloscope Readout of “0” and “1”





Cross section of encoded fuses

Laser Encoding is key to a factory programmed, unalterable NFC 128 bit code

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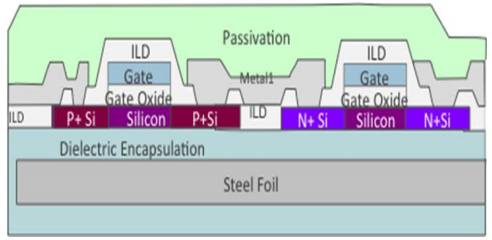
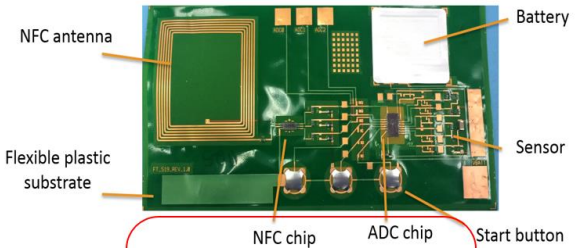


Volume Scaling to Low Cost with Roll Processing

Product Evolution with Sensors



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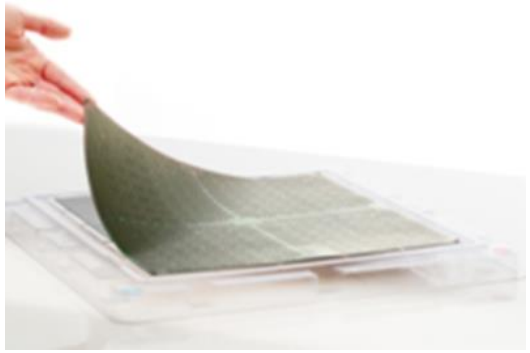
Scale up



300 mm x 300 mm	320 mm x 200 meters
100 um thick	75 to 50 um
10s of Millions	Billions

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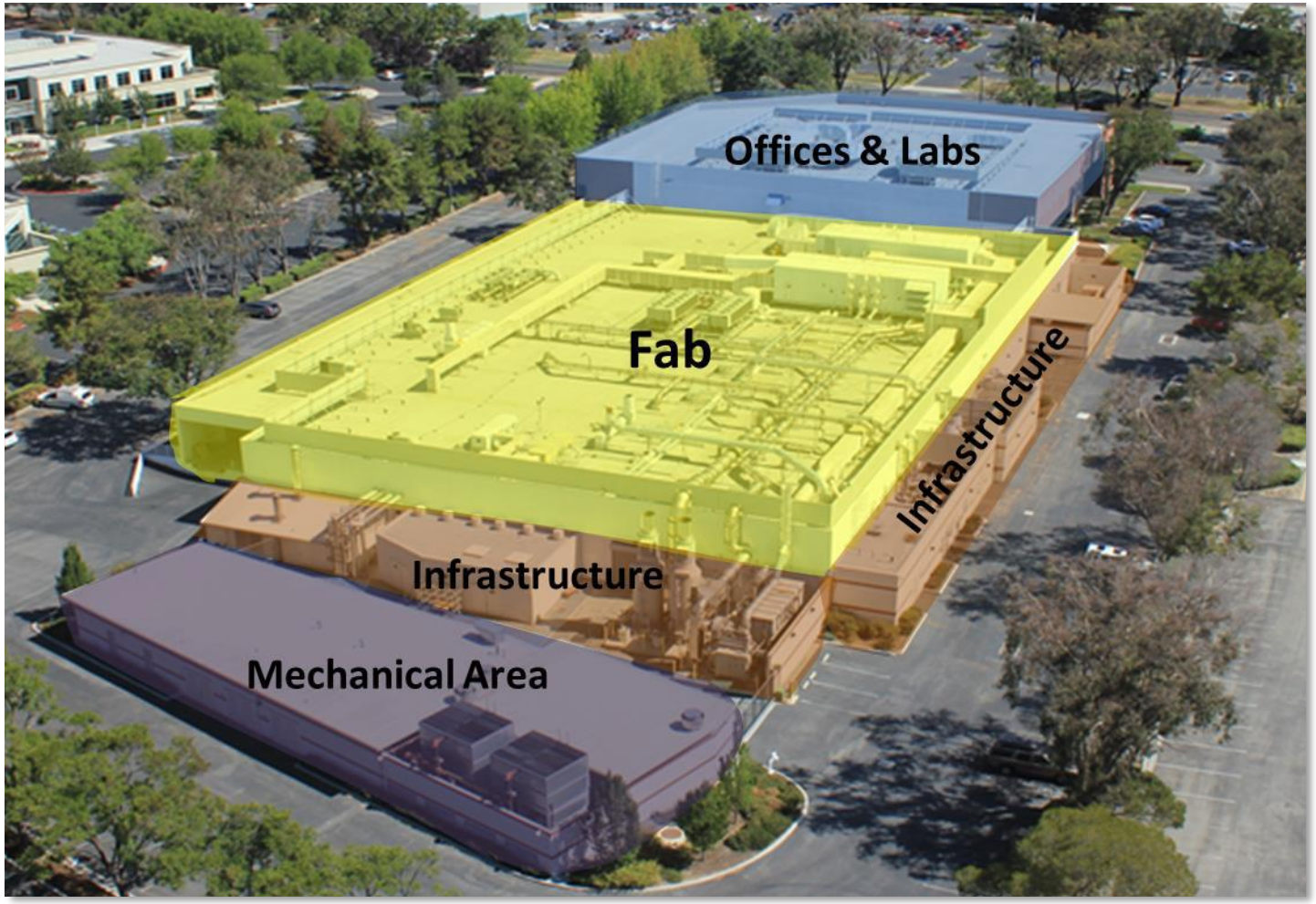
Scaling to Billion-Unit Volumes for EAS and NFC in new facility using R2R manufacturing



2581 Junction Avenue, San Jose, California

Scaling to Billion-Unit Volumes

- Up to 7 billion unit NFC annual capacity (SpeedTap™ / OpenSense™)
- 320mm wide steel web
- Discrete process modules combining print and lithography where appropriate
- Total front-end die cost reduced by 10x, material dominated

Roll-to-Roll Unit Operations

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Ultra Scale R2R Processing

Vacuum

15 Toolsets including Metrology and Test
In various stages of install and build

Litho

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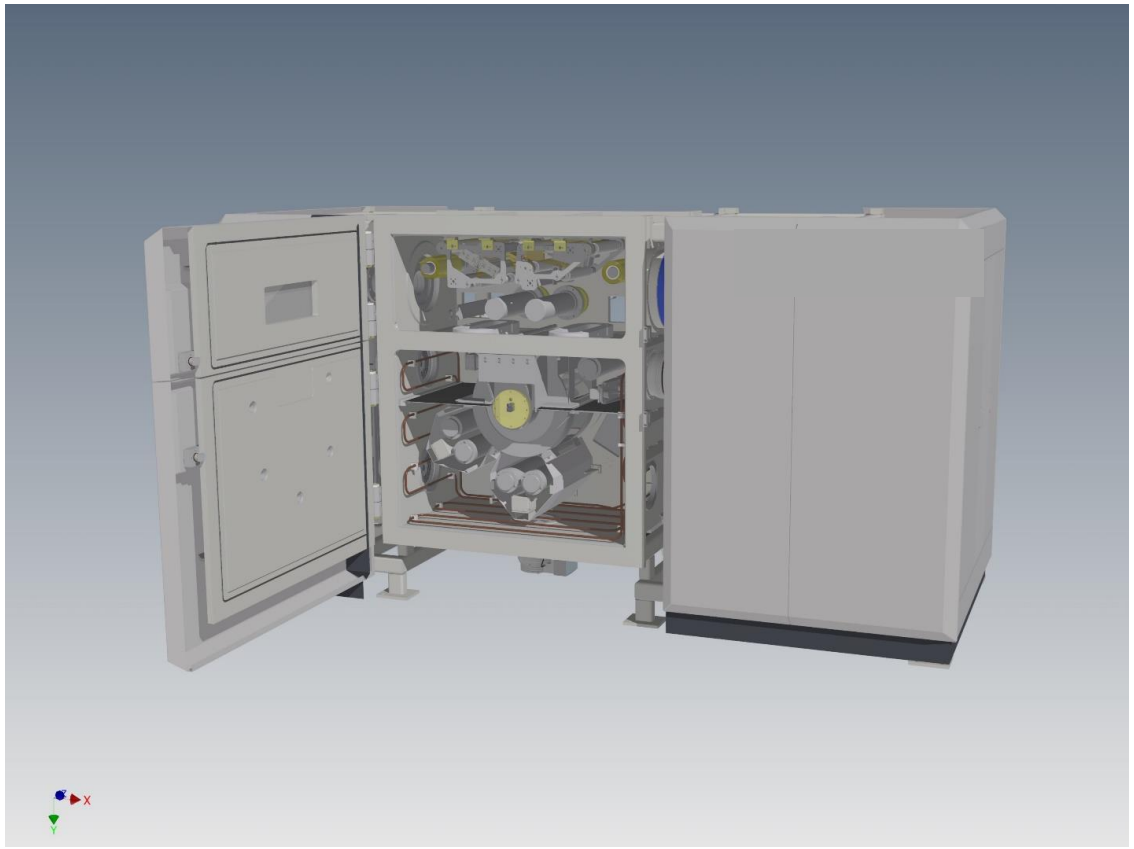
Example: Modular Metal Sputter Tool



Three materials are run in one tool without re-tooling.

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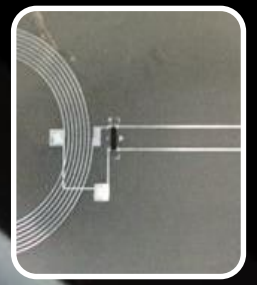
Roll-to-Roll Flow in Backend - Inlay Manufacturing

Attach



Conversion

Test

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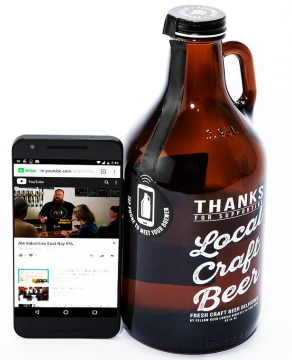
IoT of Everyday Objects using Near Field Communication (NFC)



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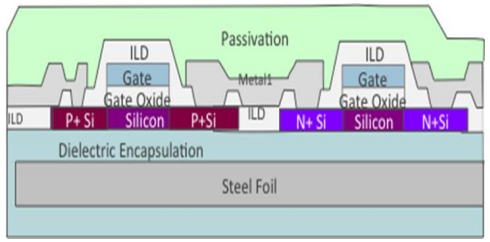

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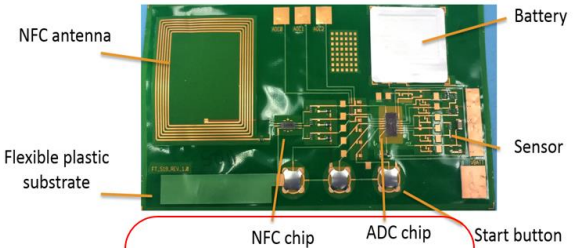

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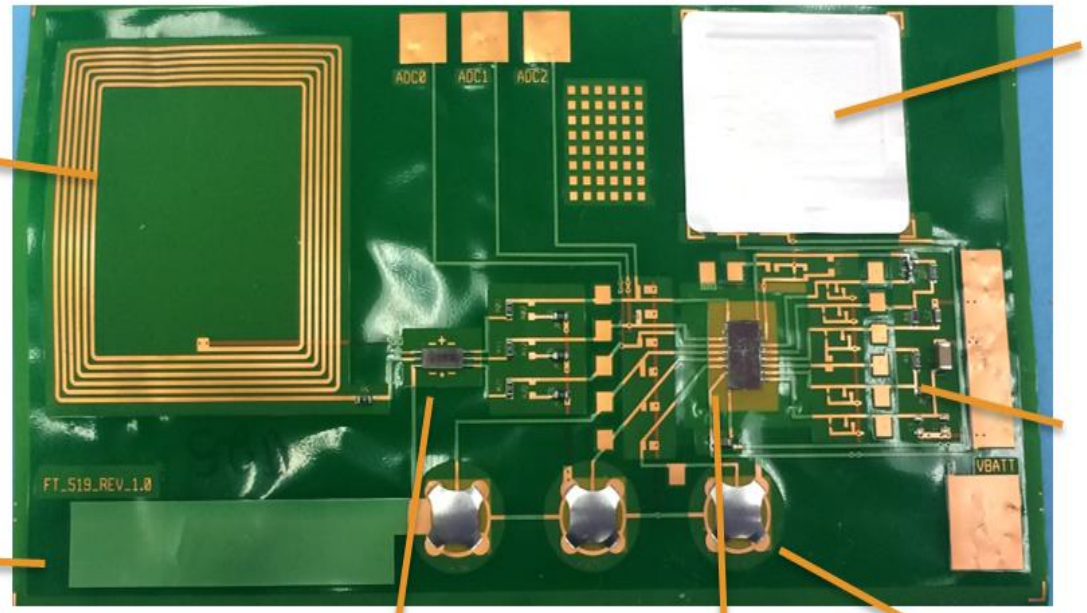
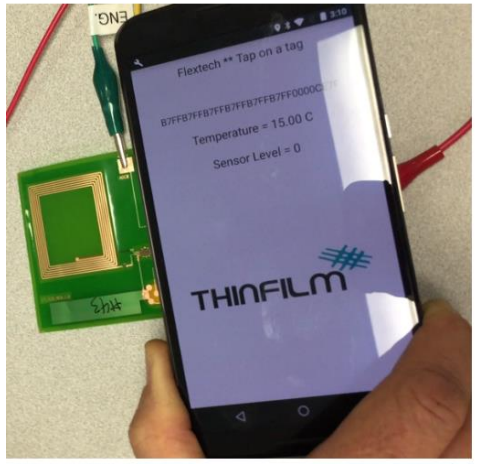
Flexible NFC Sensor Label: 3 Bit ADC + NFC Readout





CMOS TFT on Stainless Steel

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NFC Label Types: Common Sensor Platform

TEMPERATURE SENSOR LABEL

- Sensor: Resistive Thermistor
- Temperature Range :15^0C-25^0C
- Accuracy = +/-1.25^0C

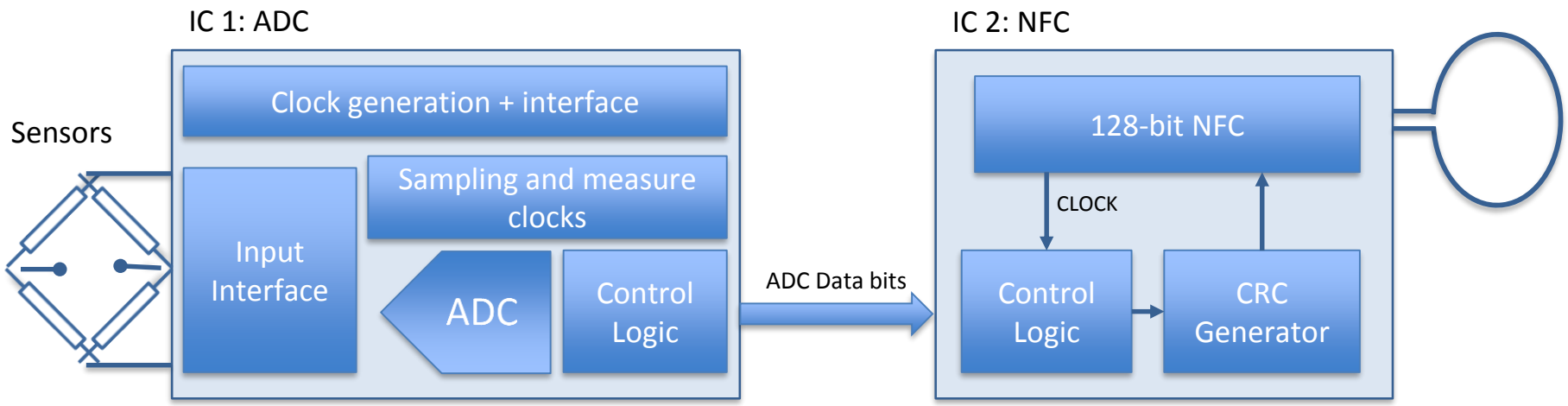
HUMIDITY SENSOR LABEL

- Sensor: Capacitive
- Relative Humidity Range :10%-80%
- Accuracy = ± 10%

LIGHT SENSOR LABEL

- Sensor: Light (Current)
- Light Range: 200 – 800Lux
- Accuracy = ± 85Lux

- Frequency variations from a reference generates 8 levels of ADC code.
- 8 unique NFC 128-bit data streams based on 3-bit ADC input



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NFC Label Types: Sensor Data

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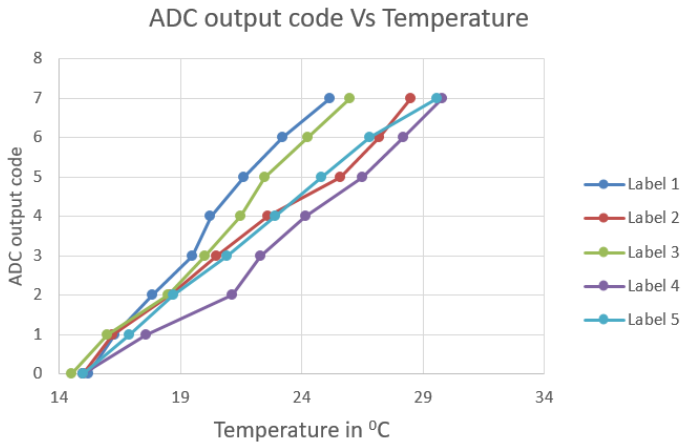
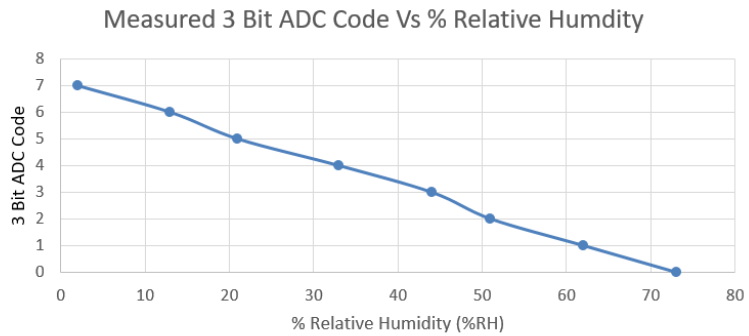


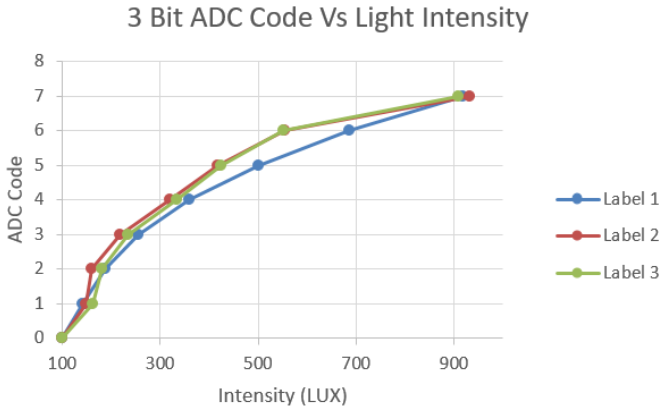
HUMIDITY SENSOR LABEL

- Sensor: Capacitive
- Relative Humidity Range :10%-80%
- Accuracy = ± 10%



LIGHT SENSOR LABEL

- Sensor: Light (Current)
- Light Range: 200 – 800Lux
- Accuracy = ± 85Lux



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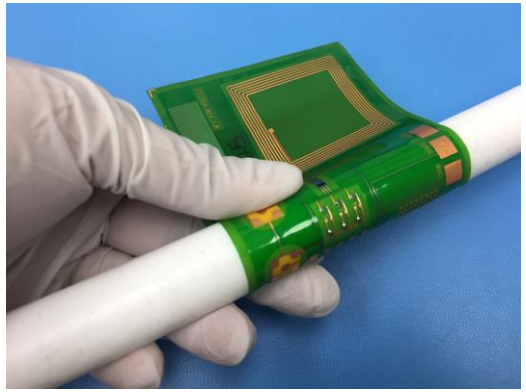
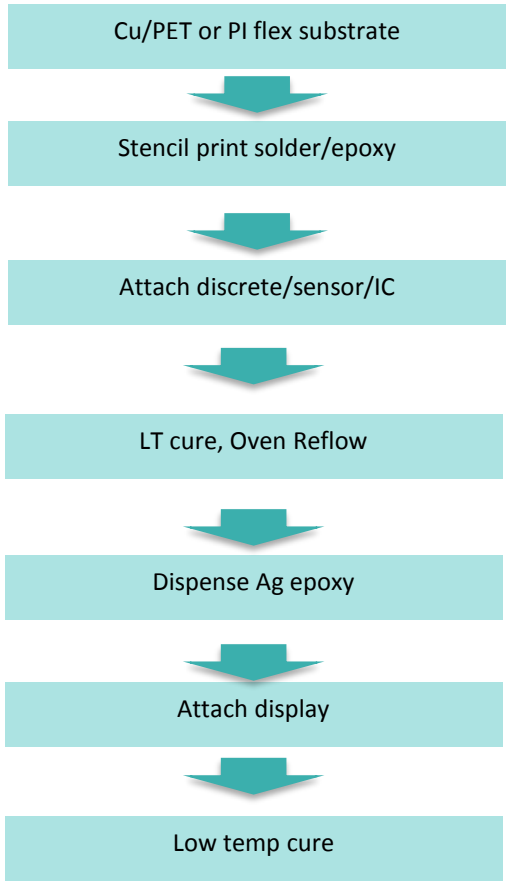
Low Temperature Flexible Label Assembly

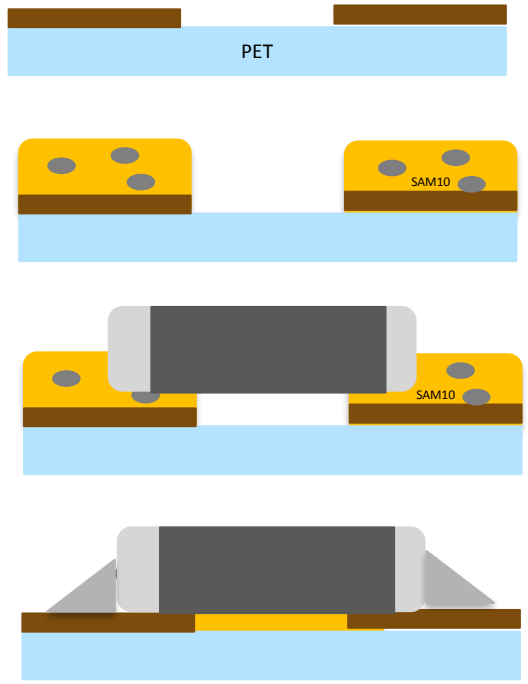
- A novel ink formulation of low temp solder and resin

- Key Points
  - One step electrical and mechanical connection
  - Self Aligned during Cure
  - Minimal process steps
  - PET Compatible assembly





LT Solder/Epoxy Phase separation



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