

ADVANCED PACKAGING TECHNOLOGY

NCCAUS CMPUG/TFUG/PAG Joint Meeting

Meeting Date: June 12, 2018

Time: 12:00 pm - 4:30 pm

Location: SEMI Headquarters

673 South Milpitas Blvd.

Milpitas, CA 95035

FREE TO ATTEND, JUST SHOW UP!

Co-Chairs:

Rob Rhoades (CMPUG), rob.rhoades@revasum.com

Paul Werbaneth (TFUG), pfwerbaneth@gmail.com

Jeff Shields (PAG), Jeffrey.shields@att.net

This meeting focuses on technologies and applications related to Advanced Packaging Technology. The purpose of this meeting is to bring together leading researchers in academia, government, and industry with innovative technologies to nurture a free exchange of triumphs and challenges in packaging technology

SPEAKERS/AGENDA

12:00 pm – Meeting Start and Lunch, **FREE LUNCH** – Sponsored by **Kurt J. Lesker Company**

1:00 pm – Welcome

1:10 pm – **Dr. Caitlin Chapin, XLab, Stanford**

Title: “Monolithic Integration of GaN Sensors and Electronics for Harsh Environments”

Abstract: Sensors and electronics that can survive and operate in harsh environments are desired by the space, aeronautics, automotive, and energy industries in order to ensure safety, improve reliability, decrease costs, and investigate new environments. Harsh environments can include high temperatures (>300°C), thermal cycling, large radiation doses, high shocks and pressures, and corrosive environments. Traditional silicon sensors are unlikely to meet the demands of high temperature environments due to a high generation of thermal carriers and material softening at temperatures >500°C.

New electronic material platforms are being studied to overcome the challenges of high temperature operation. Gallium nitride (GaN) is a wide bandgap material that has become popular in the power and communication electronics communities, due to its low on-resistance, high electron mobility, and high breakdown voltage. GaN is also a promising high temperature material; InAlN/GaN transistors has been shown to operate up to 1000°C. Additionally, GaN offers unique sensing opportunities since it has a direct bandgap, and is piezoelectric, pyroelectric and piezoresistive. Within the Extreme Environment Microsystems Laboratory, pressure sensors, UV photodetectors, micro-hot plates, thermoelectric heat flux sensors, and Hall effect magnetic sensors have been microfabricated by leveraging the GaN heterostructure. The ability to build sensors and electronics from the same GaN heterostructure will enable monolithic integration (i.e. co-fabrication of sensors, amplifiers, logic circuits, and analog to digital converters, etc.). Monolithic integration of sensors and electronics would improve the potential success of devices in harsh environments because packaging is difficult and space is generally limited. Thus, this talk will discuss the potential to build sensing technology and the required electronics for harsh environments using GaN heterostructures as a material platform.

Bio: Caitlin Chapin is currently working as a postdoctoral researcher in Extreme Environment Microsystems Laboratory (XLab) at Stanford University. Several of her current projects include studying the impact of electronic traps on gallium nitride sensors, developing high temperature metallization schemes for GaN, and building MEMS resonators for Venus applications. Caitlin received her B.S. in mechanical engineering from the Georgia Institute of Technology. During her time at Georgia Tech, she also worked at the Institute for Nanotechnology and Electronics as an assistant process engineer. Caitlin received her M.S. (2018) and Ph.D. (2018) at Stanford

University in the mechanical engineering department. Her Ph.D. work was funded by the NASA Space Technology Research Fellow program where she had the opportunity to collaborate with researchers at NASA Glenn, NASA Ames and the Jet Propulsion Laboratory. Her thesis focused on the design, microfabrication, and characterization of a temperature-tolerant, pressure sensor to support sensing in high temperature environments based GaN heterostructures.

1:40pm – Laura Rothman Mauer, Veeco Instruments, Inc.

Title: “Equipment and Process Challenges for the Advanced Packaging Landscape”

Abstract: The advanced packaging market spans multiple applications and approaches. There is no single roadmap for advanced packaging, but a landscape of choices. The growth drivers for advanced packaging include Big Data, smartphones, IoT, automotive and memory. Due to challenges with scaling at the device level, there is a critical need for heterogeneous integration at the package level. There are multiple approaches to packaging for a wide variety of devices for different applications. These approaches include 3D, TSV, and numerous 2.5D schemes using FOWLP concepts. In addition, the form factor (wafer vs. panel) and size have not been standardized. The various approaches that exist means tool suppliers must be able to quickly adapt and customize their technology to different wafer sizes and formats, integration sequences, materials, chemistries and process conditions. However, providing process flexibility while minimizing cost of ownership and tool footprint is challenging. This presentation will describe several different approaches to advanced packaging with examples, and explore the challenges and possible solutions associated with each.

Bio: Laura Rothman Mauer is the chief technical officer of Veeco’s Precision Surface Processing (PSP) division. For over 35 years Mauer has worked in the semiconductor industry in technical areas including semiconductor and packaging process development, reliability engineering, contamination control, environmental technologies and knowledge management. Her time as program manager for IBM, chief technology officer at SC Fluids, and director of research and development for Brewer Science gave her the well-rounded know-how and perspective that enables her to confidently lead Veeco PSP into new and growing fields of the semiconductor industry.

2:10pm – Annette Teng, Promex Industries.

Title: “Heterogeneous Integration Needs Heterogeneous Package Assembly”

Abstract: IN PROGRESS.

Bio: Annette Teng is currently the Chief Technology Officer at Promex Industries. She has previously worked in components packaging and assembly at Philips Semiconductor, Linear Technology and Corwil Technology. Prior to joining Promex, she was Package Assembly Manager at Silanna in Australia. She has also worked at Hong Kong University of Science and Technology. She graduated with a Ph.D. in Materials Engineering from University of Virginia after receiving a BS from Sweet Briar College.

2:40pm – Break: Refreshments sponsored by [UC Components](#)

3:10pm - Jon Woodyard, SiPAQ LLC

Title: “Fan-out IC Packaging trends and the impact on equipment capital structures (e.g., wafer processing versus traditional PCB styles) today and in the future.”

Abstract: The wafer level package revolution that accelerated with the adoption of the Smartphone radically changed the Semiconductor packaging industrial equipment infrastructure from lower capital-intensive chip attach and wire bonders to higher cost fab equipment. Over the last decade Outsourced Subcontract Assembly and Test (OSAT) companies like Amkor and ASE have spent close to half of their capital budgets on annually on fab-based assets representing billions of dollars of capital equipment currently in volume production. Simultaneously, TSMC has entered the packaging arena leveraging their own existing infrastructure. These assets create opportunities for newer packaging styles like fan-out wafer level packaging. But while opportunities exist competitive solutions using laminate substrates and lead-frames continue to cut costs and stay off market conversion. This presentation will discuss trends in Fan-out from its beginnings, where it is today and what mechanisms are likely required to experience the tipping point toward much broader adoption.

Bio: Jon Woodyard is a 25-year professional from the semiconductor packaging industry attaining roles of Vice President of Technical Applications and Strategic Accounts as well as VP of Business Operations supporting wafer services and wire bonded fBGA product lines at Amkor Technology. Jon and his team focused on winning and growing business, developing marketing strategies, deploying advanced products from standalone wafer-based products to highly integrated modules enabling customer's next generation roadmaps. In 2017 revenue in his region exceeded 25% year over year growth. During his tenure in the business unit Jon's team grew the business 10x over 4 years (63% CAGR against an industry average of 18%). Currently, Jon is the Founder and Principal Consultant for SiPAQ, a consulting company geared toward helping businesses understand the complex landscape of IC packaging and then better navigate their packaging roadmaps to achieve time to market objectives, cost targets, sustainable capacity and product quality goals.

3:40pm – David Lishan, Plasma-Therm, Inc.

Title: "Low temperature, low damage plasma technologies for advanced packaging applications"

Abstract: Trends in advanced packaging for precision, performance, reliability, size, shape, costs and package integration are some of the requirements driving manufacturers to employ front-end technologies, like dry etching. However, integrating such plasma-based solutions can be challenging as the substrates and materials can be very sensitive to high temperatures and plasma damage. The plasma solutions and chemistries need to be compatible with the exposed materials on a finished wafer such as bump-metals, dielectrics, passivation, and other organic materials to reduce damage risks.

In this presentation, we will look at some low temperature (<150C), low damage dry etch solutions in a range of applications that include PR/polymer striping, surface activation/modification, TSV reveal/thinning, conformal liners, and plasma dicing.

Bio: David Lishan received his Bachelor's degree in Chemistry from UC, Santa Cruz and M.S. and Ph.D. from UC, Santa Barbara in Solid State Electrical Engineering. He has worked and published on wide range of material, semiconductor, and chemistry R&D projects in the areas of photochemistry, x-ray mask fabrication, PVD, and plasma processing. During his nearly 20 years at Plasma-Therm, he has had business unit management and worldwide marketing responsibilities as well as managing development of the plasma dicing product for advanced packaging. Currently he is in the roles of Principal Scientist and Director in Technical Marketing, and recently organized and presented plasma processing workshops at leading institutions throughout the world. His primary focus is on the application of plasma processing for R&D, MEMS, photonics, data storage, power, and compound semiconductor applications. He holds two patents in the area of semiconductor processing and has over 60 publications and conference presentations.

4:10 pm – Open Forum Discussion – Moderator: Robert L. Rhoades, Revasum, Inc.

4:40 pm – End Meeting

All presentations will be requested to be posted on the CMPUG, TFUG & PAG Proceedings webpage approximately 1-2 weeks following the meeting.