# Low Temperature Plasma Technologies for Advanced Packaging Applications

NCCAVS - Northern California Chapter AVS
Joint User Group Meeting (CMP, PAG, & TFUG)

**David Lishan**

June 12, 2018

Science and Technology of Materials, Interfaces, and Processing

# Outline

- Plasma-Therm Introduction
- Deep Silicon Etching / TSV
- Low Temperature Strip / Clean
- TSV Isolation and Seed Layer
- Surface Activation
- Plasma Dicing

# Plasma-Therm
## Semiconductor equipment manufacturer

**Headquarters in FL, USA**

Relocated to
St. Petersburg, FL

Incorporated

1974 1975 1983 1990 1994 2000 2009 2010 2011 2013 2014 2015 2016 2017 2018

Origin:
RF power supplies

Industry first single wafer production
plasma etch reactor

First ever Photomask plasma etch
system introduction

Acquired by oerlikon

*Established*
Critical machining
capabilities

ADVANCED VACUUM™
*Acquired*

*Launched*
Industry first
Plasma dicing
System in production

CELEBRATING 40 YEARS OF INNOVATION

*Acquired*
HDRF™
Stripping/Cleaning

IBE/IBD

*Acquired*

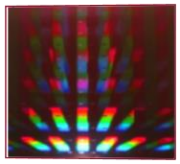
DISCO

*Partnership*
Combined
solution

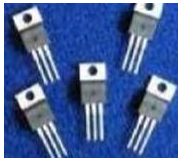
F.A.S.T.® ALD-CVD

memsstar
Trymax®

# Etch and Deposition Solutions Lab-to-Fab





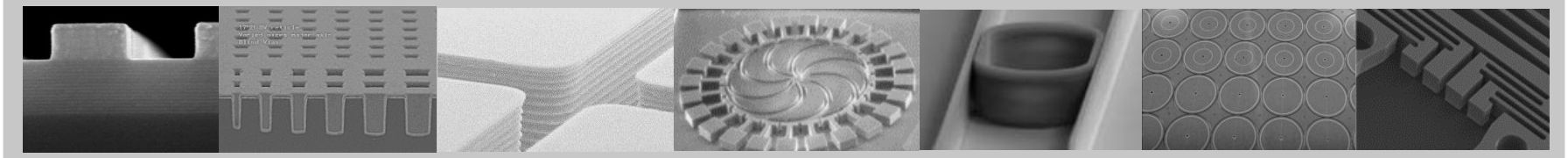




| Adv. Photomask & Imprint | Wireless | Solid State Lighting | Photonics | MEMS NEMS | Power | Data Storage | Failure Analysis | R&D |
|---|---|---|---|---|---|---|---|---|

Etch & Clean Solutions: ICP, RIE, PE, PHF-RIE, DRIE, HDRF, IBE, RIBE, HF release

Deposition Solutions: PECVD, ICP-CVD, IBD, FAST-CVD

Plasma Dicing Solutions

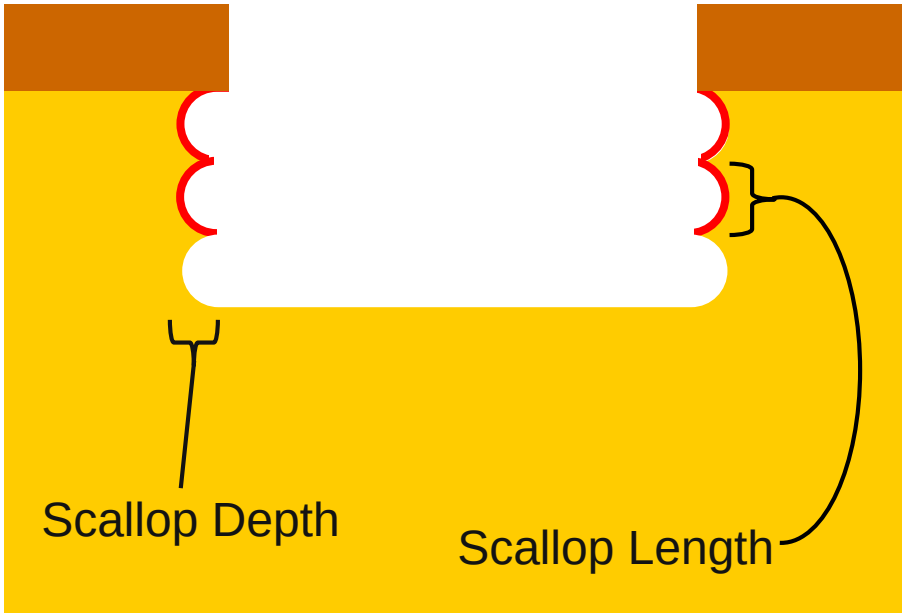


# DEEP SILICON ETCHING / TSV

# DRIE – Deep Reactive Ion Etching

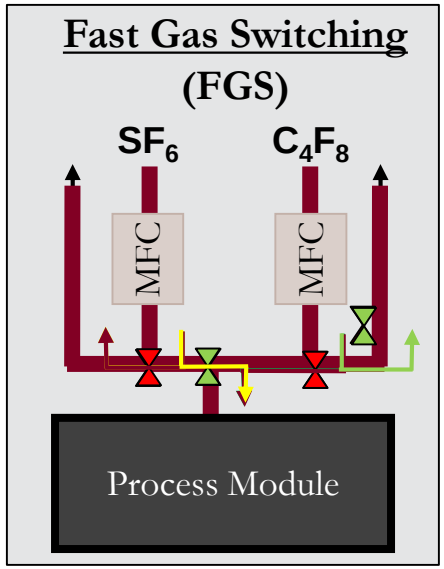
- Passivation ($C_4F_8 \rightarrow (CF_2)_n$)
- Selective passivation removal
- Isotropic etching of Si ($SF_6$)

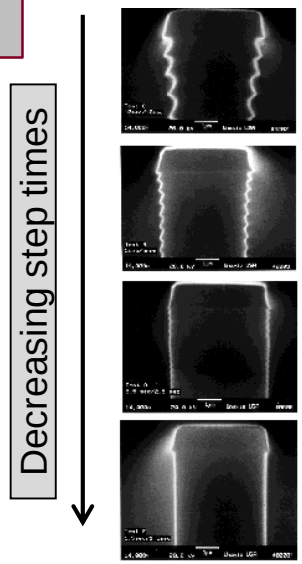
- Low temperature
- Highly chemical etch mechanism
- High material selectivities (<250:1 to PR, 700:1 to $SiO_2$)
- High etch rates (25um/min)
- Anisotropic

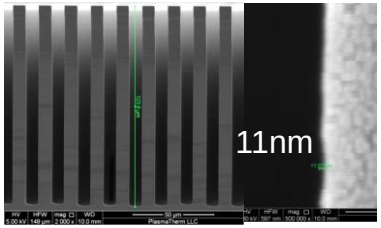


# DRIE – High F Radical Concentrations
# Fast Process Steps and Process Control

## Low scalloping

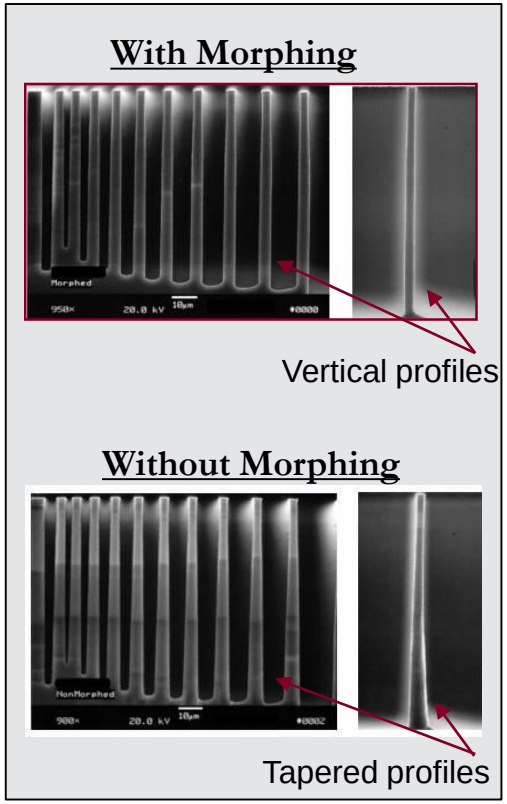


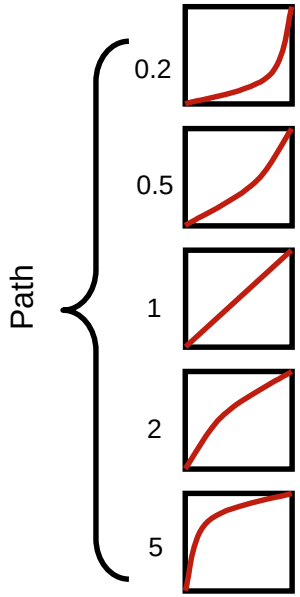




- Fast valve response time
- No MFC overshoot pressure

## Profile Control



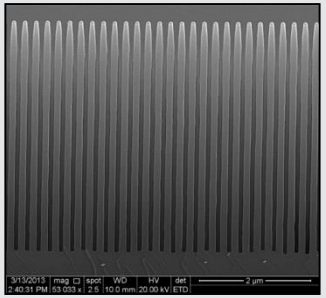

| *Parameter* | *start* | *end* | *path* |
|---|---|---|---|
| electrode Bias | 375 | 550 | 0.2 |
| Dep time (sec) | 1.5 | 3 | 2 |



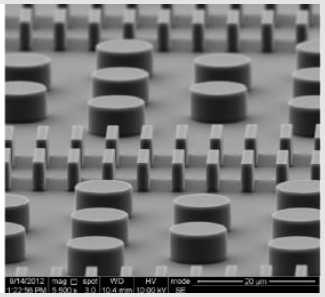
# DRIE

## Wide range of etch capabilities

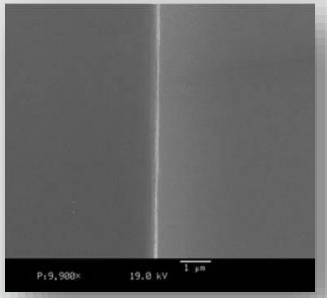
**Aspect ratio 60:1**



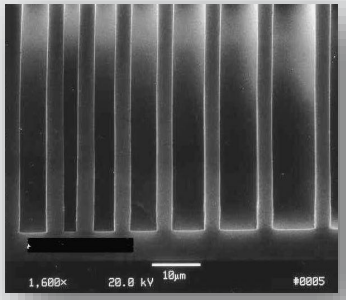
**High Load**



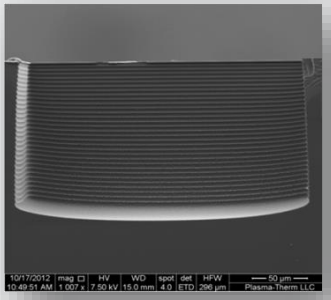
**Smooth sidewalls roughness < 10 nm**



**Notch reduction on SOI**

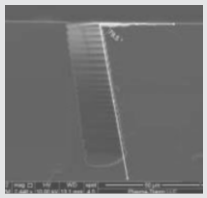


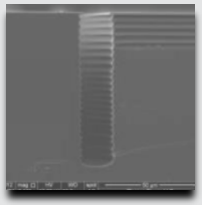

**High Etch Rate > 25 µm/min**



**High selectivity**
**Si:PR > 200:1**
**Si:$SiO_2$ > 700:1**

**Low Tilt Angle <0.2°**

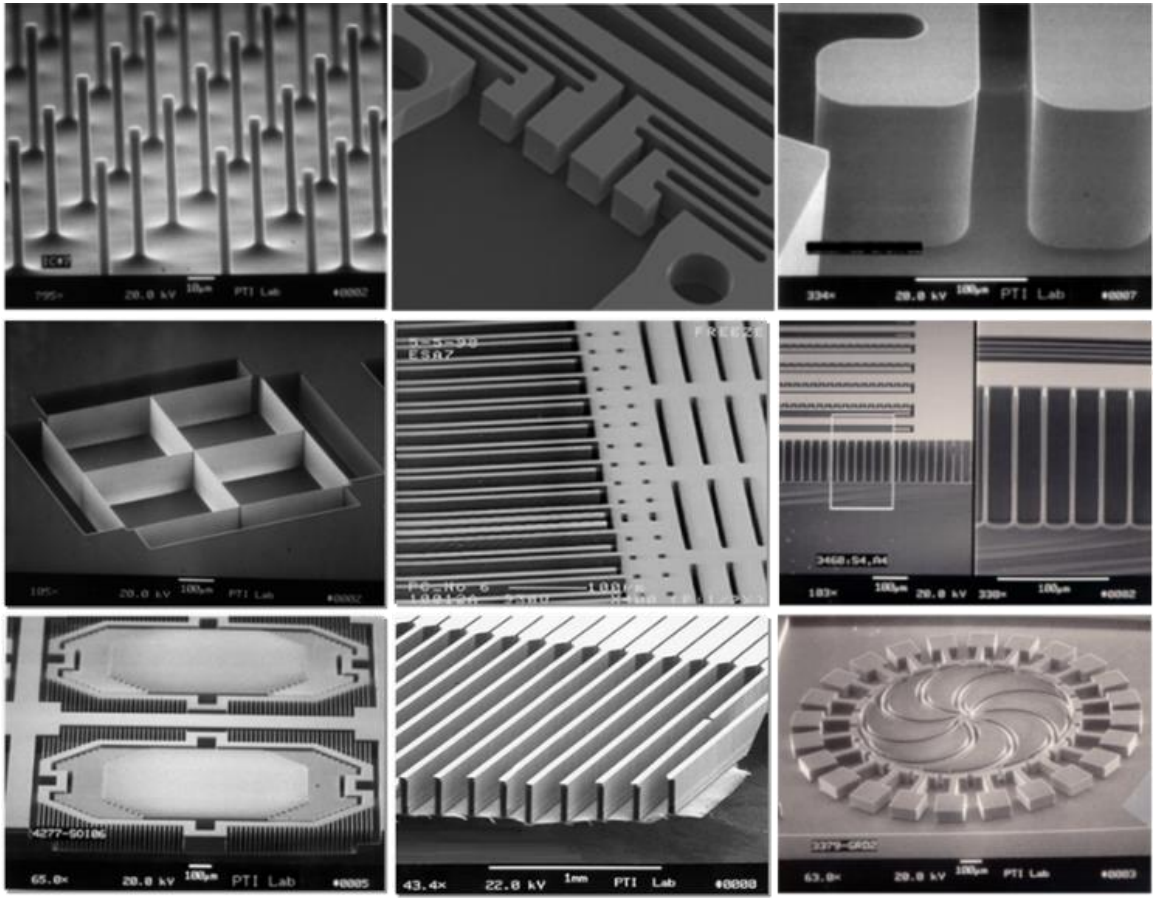




**Optimized reactor**

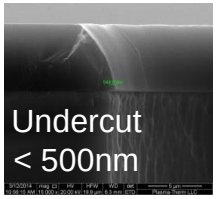
# DRIE

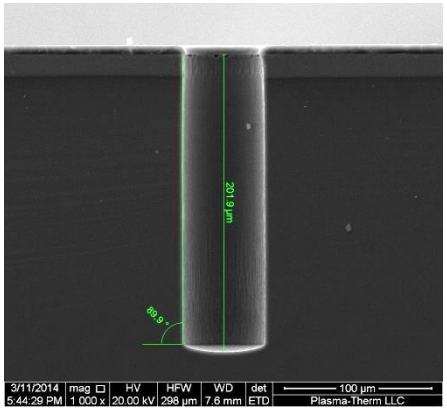
## Wide range of applications

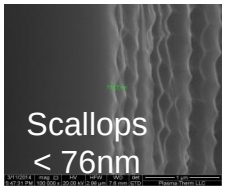


# DRIE – TSV Applications

## 50µm Via diameter
200µm deep

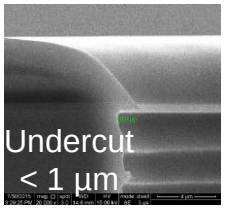


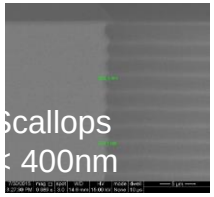



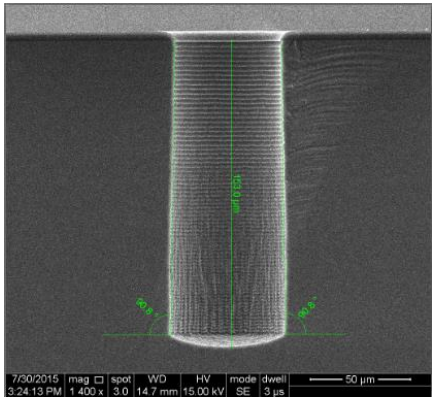




**Etch Rate > 7 µm/min**
Uniformity <1.5%
Selectivity Si: PR > 175:1
**Straight profile 89.9** +/-0.1

## 50µm Via diameter
150µm deep

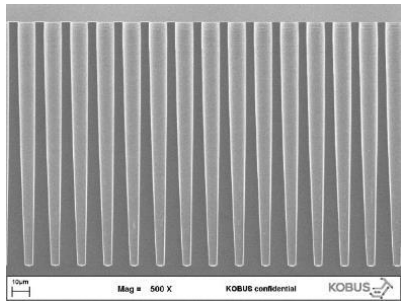


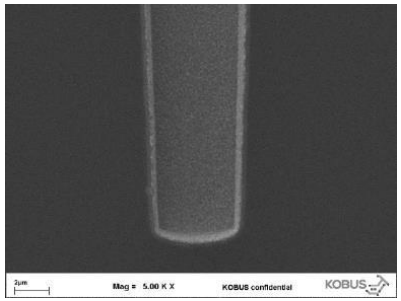




**Etch Rate > 14 µm/min**
Uniformity < 5%
**Straight profile 90.5** +/-0.5

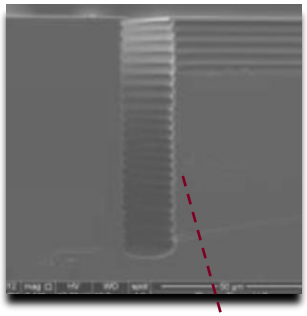
## 10µm Via diameter
100µm deep

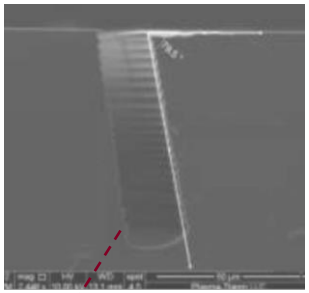


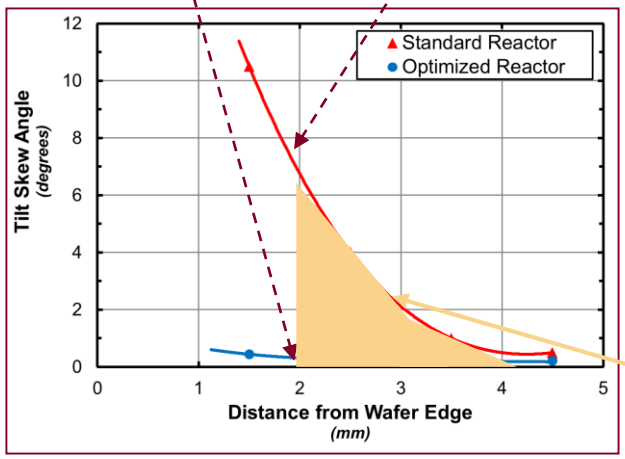



# Low Tilt & SOI Applications

## Low Tilt Angle





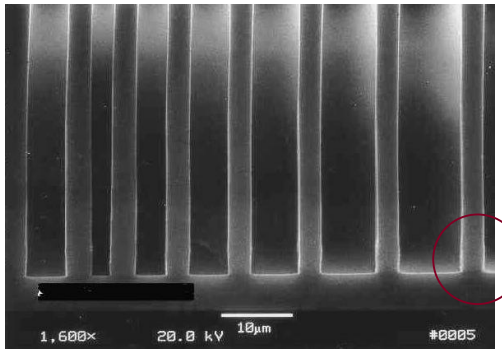


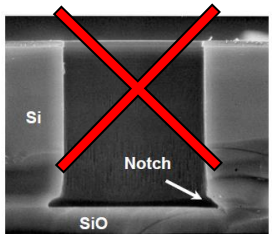

More good dies per wafer

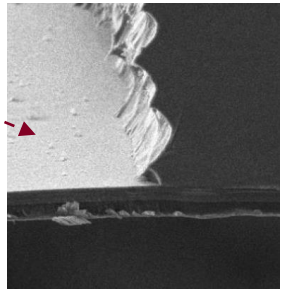
## Notch reduction on SOI wafer

**2 to 10µm wide trench**

40µm deep



**Etch Rate > 7µm/min**

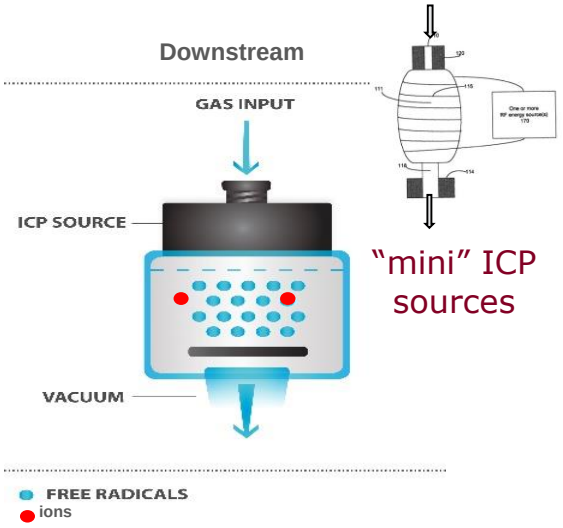
Uniformity 2%

* Si open area 15%

# LOW TEMPERATURE STRIP / CLEAN

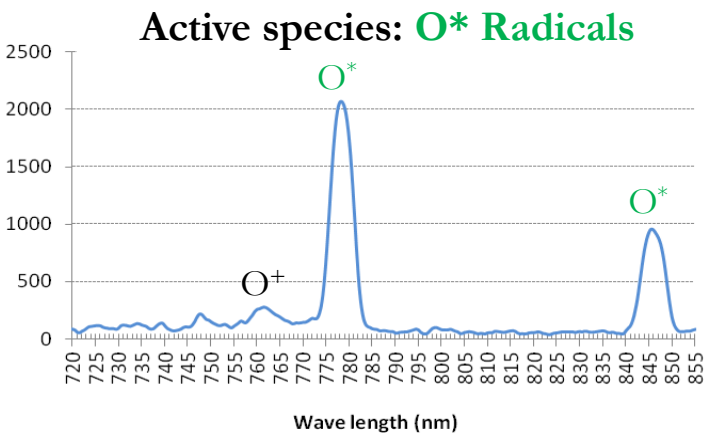
# Plasma-Therm: HDRF™

## High Density Radical Flux

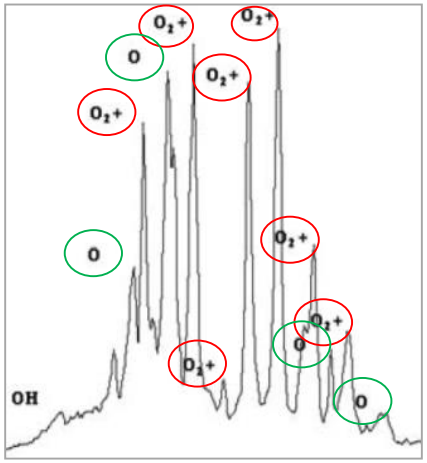



"mini" ICP sources

**HDRF™ technology**




**Conventional RF**




- **High plasma density ICP source**
  - Radicals density > 1E17 $cm^{-3}$
  - Mainly O* radicals at wafer level
- **Low damage on sensitive devices**
  - Low ions at wafer level
  - Low temperature processing < 80°C

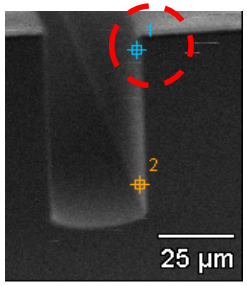
**Active species: O* + Ions**

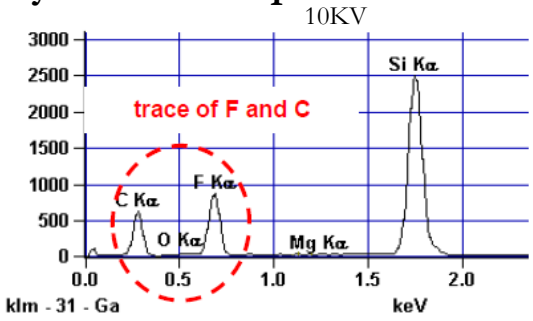
Ions = damage, heating

# DRIE polymer removal

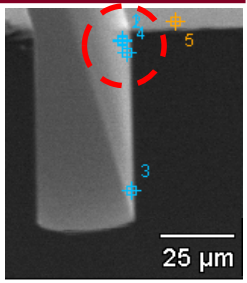
## EDX analysis (Energy Dispersive X-ray Spectroscopy)

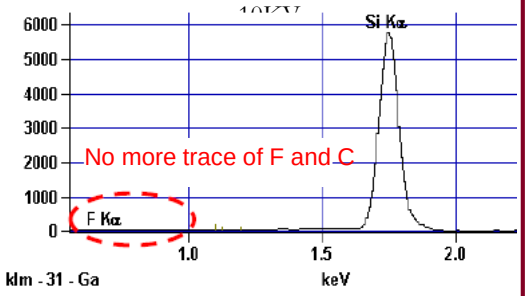
### DRIE Bosch polymer – Via top



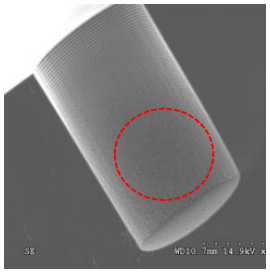

After HDRF

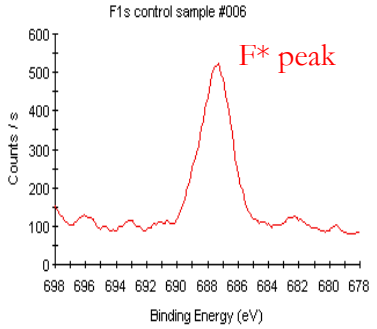


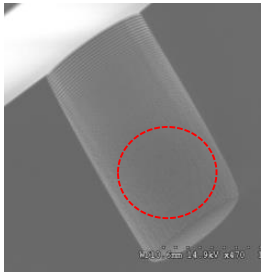

## XPS analysis (X-ray Photo-electron Spectroscopy)

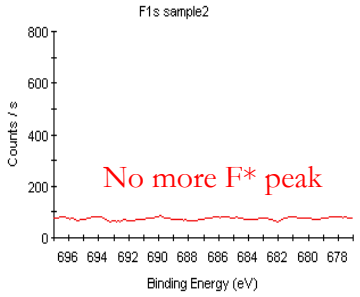
### DRIE Bosch polymer – Via bottom






After HDRF



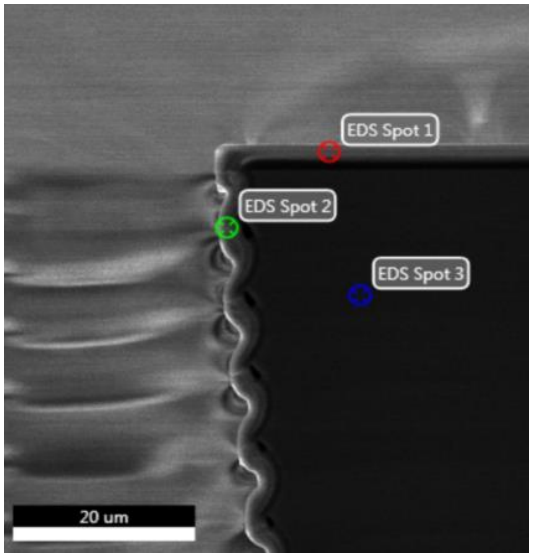


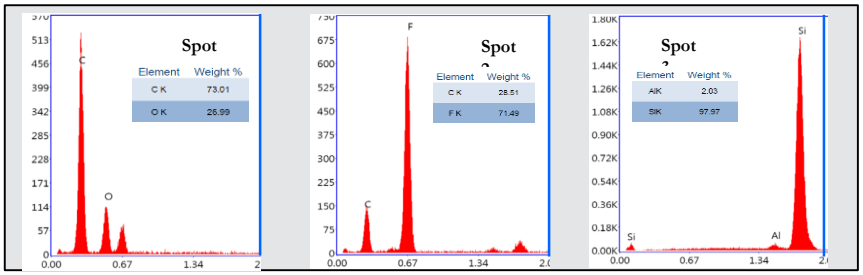

**Efficient dry cleaning technology, to remove fluor-carbon polymers**

Plasma-Therm

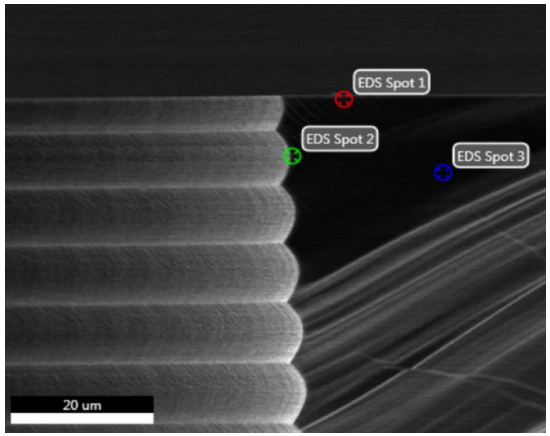
# PR & Polymer removal

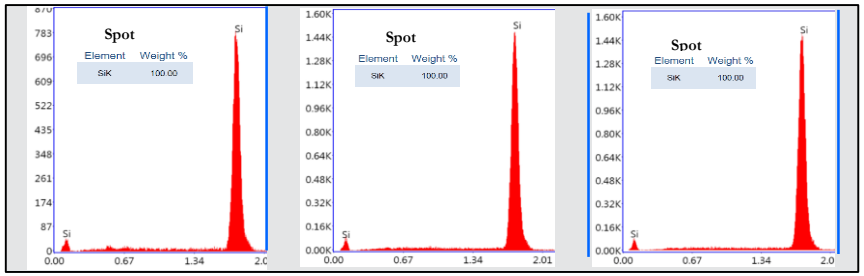
## SEM and EDAX *Pre → Post measurement*



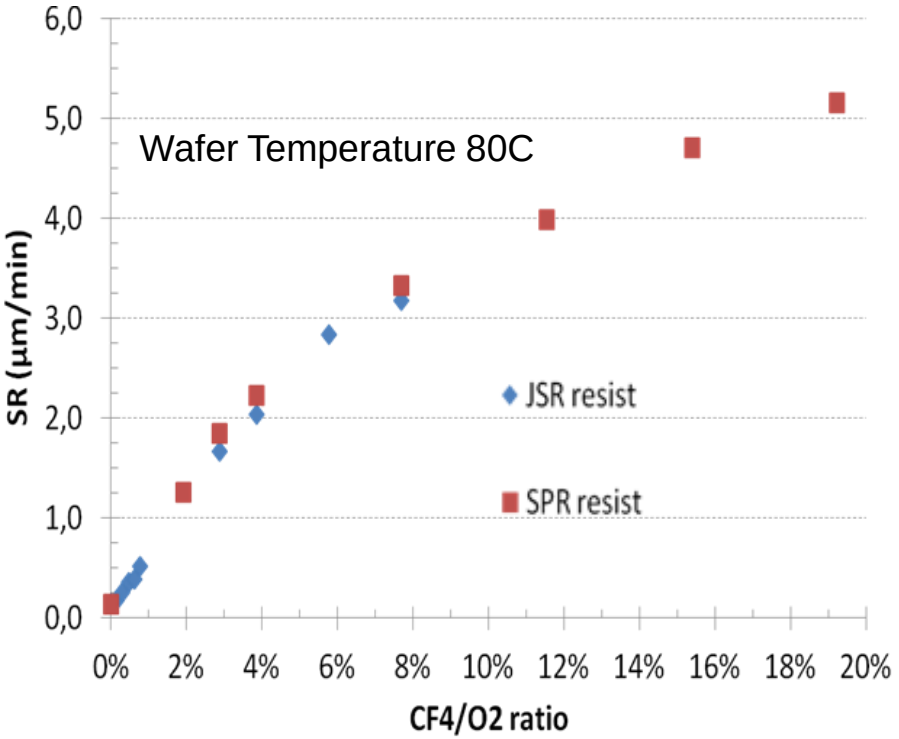

| | C (Weight %) | O (Weight %) | F (Weight %) | Si (Weight %) |
|---|---|---|---|---|
| Spot 1 (PR) | 73 → **0** | 27 → **0** | 0 → **0** | 0 → **0** |
| Spot 2 (polymer) | 29 → **0** | 0 → **0** | 71 → **0** | 0 → **0** |
| Spot 3 (baseline) | 0 → **0** | 0 → **0** | 0 → **0** | 98 → **100** |

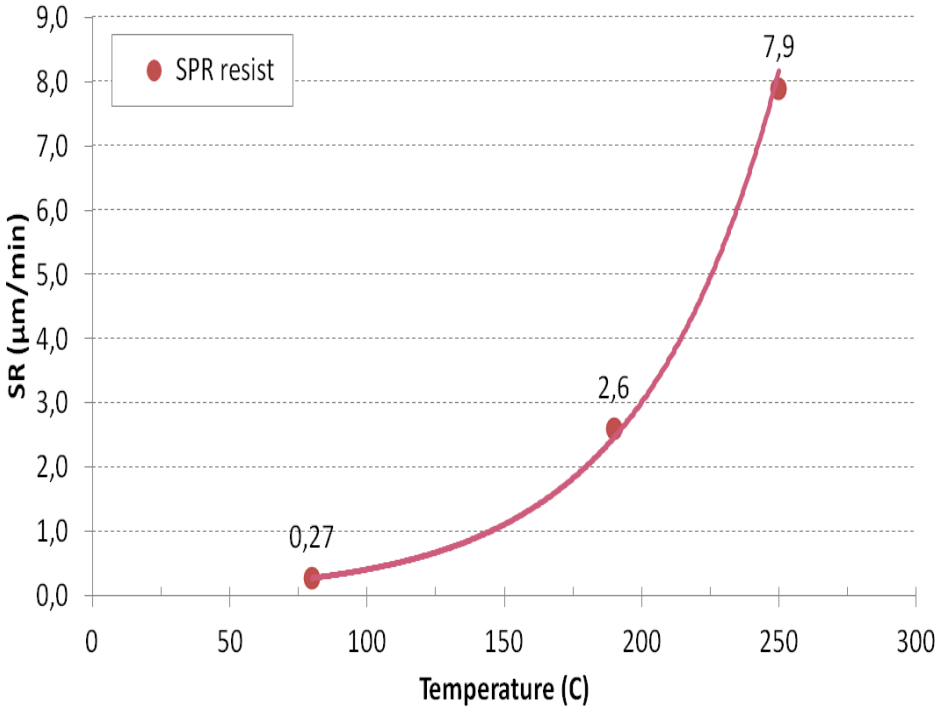



Plasma-Therm

# Low-temperature PR (and polymer) strip




**Low temperature HDRF process**
**For temperature sensitive applications**

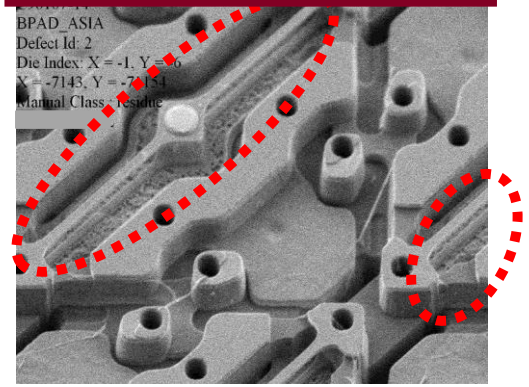
**Higher strip rate with increasing temperature**

Plasma-Therm

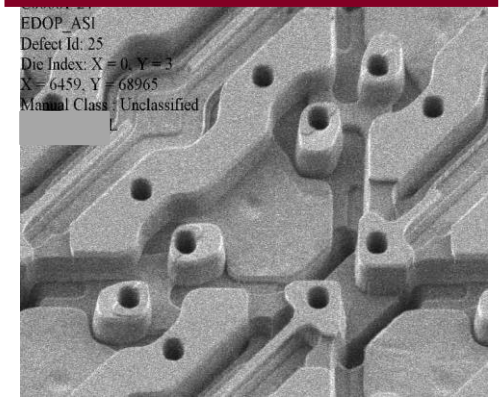
# Micro Mirrors Cleaning

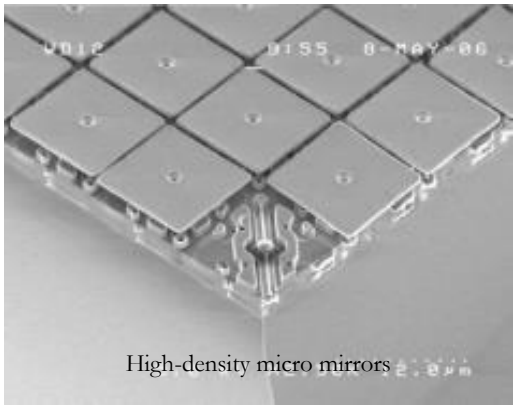
- Elimination of mirror tilt due to residues
- Damage-free. No electrical charging
- Yield improvement

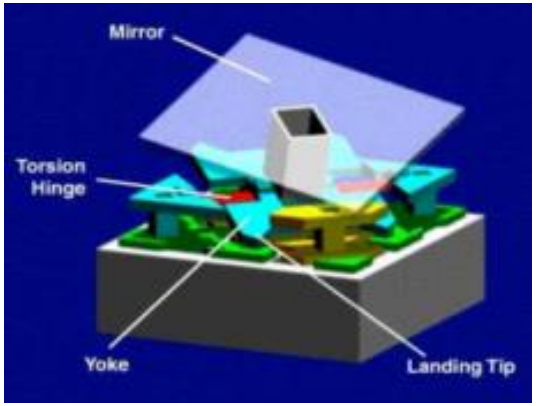
Wet treatment




With plasma treatment



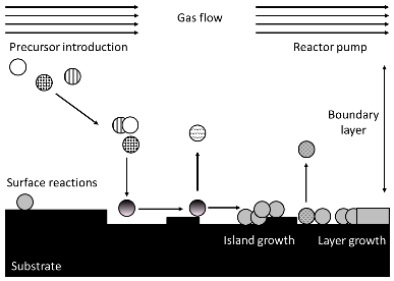


High-density micro mirrors

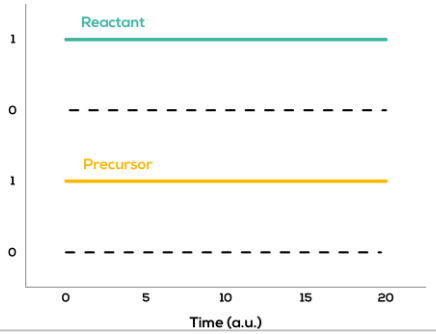


# TSV ISOLATION and SEED LAYER

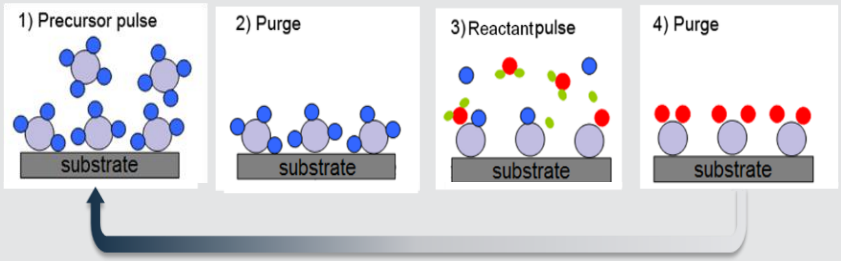
# F.A.S.T.® Crossroads of ALD and CVD

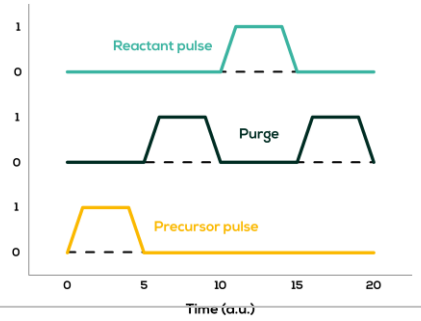
**(PE)CVD**



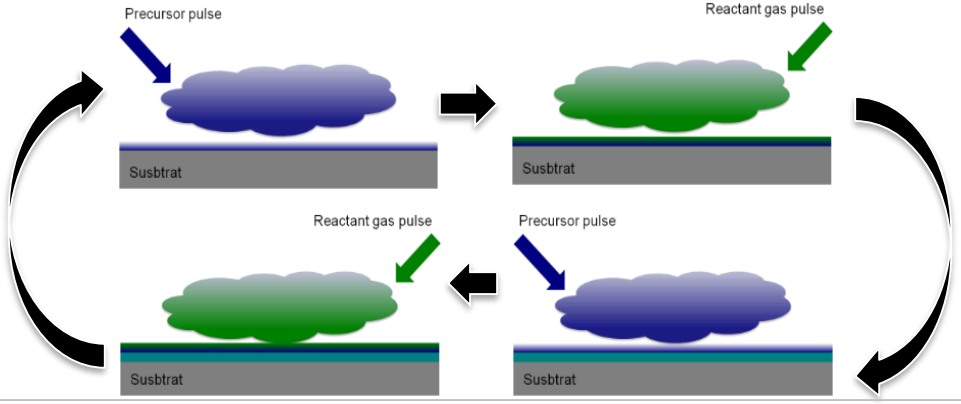

**(PE)ALD Monolayer growth**

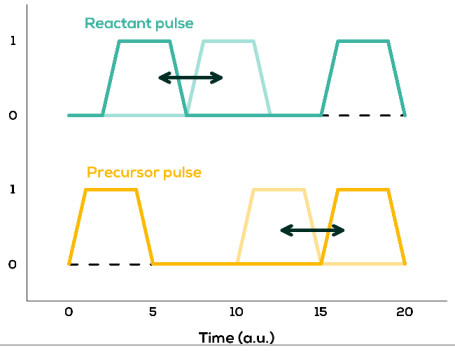



**Fast Atomic Sequential Technology**

Multilayer growth

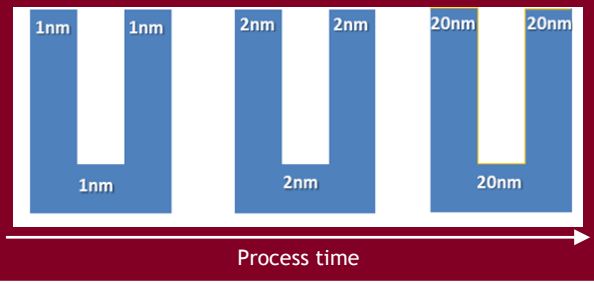



Plasma-Therm

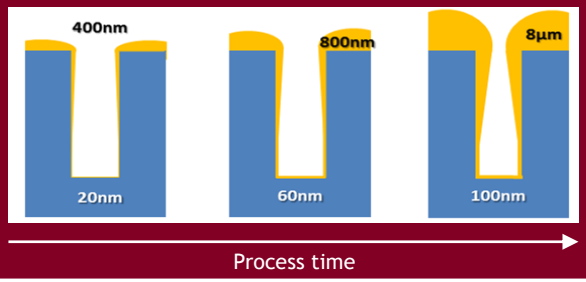
# 3D Technology Approaches for TSV

ALD
PEALD



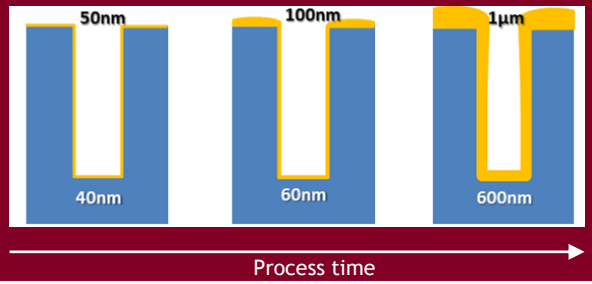

Very Thin
&
Conformal

PECVD



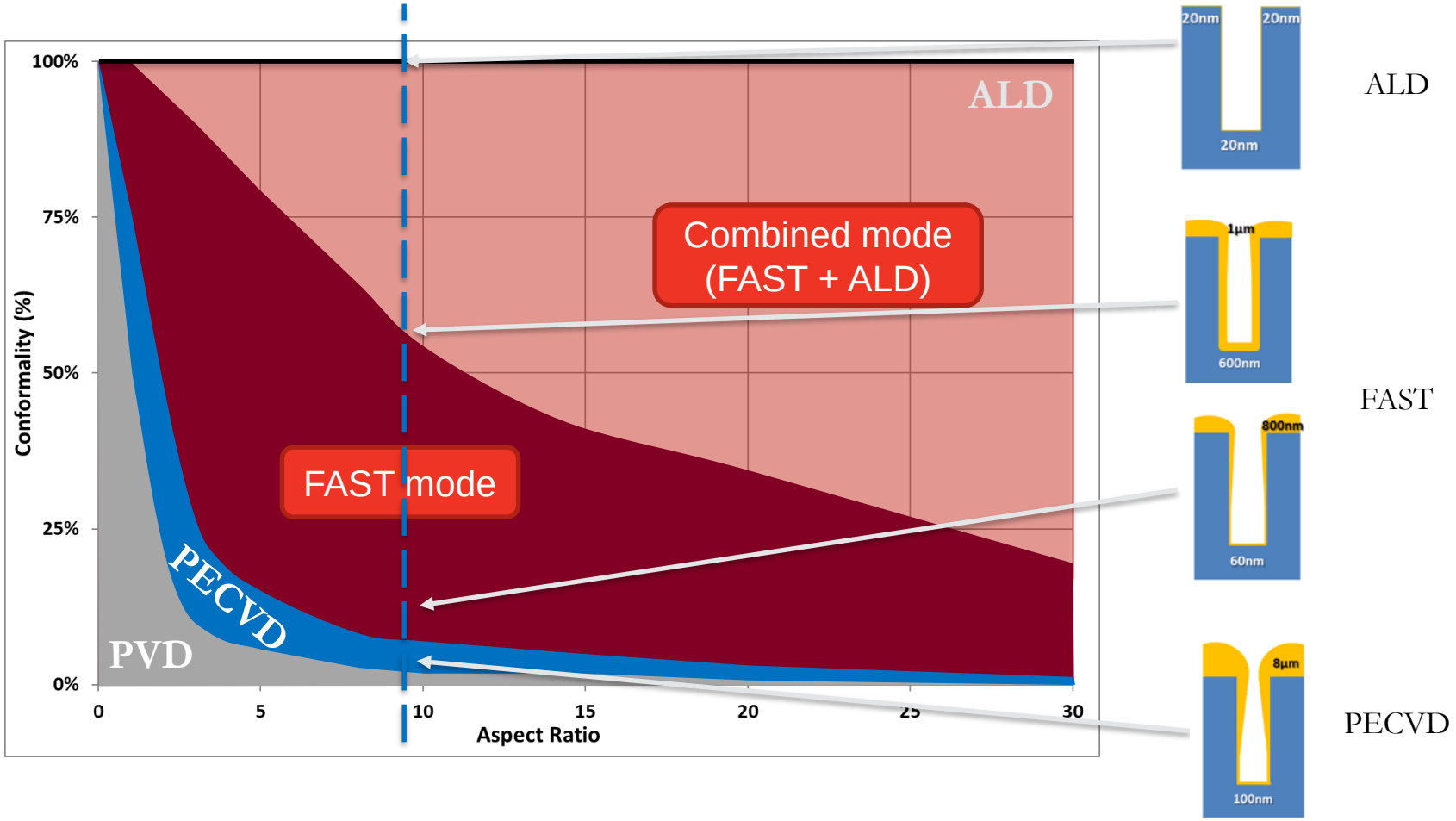

Very thick
&
Non-conformal

FAST

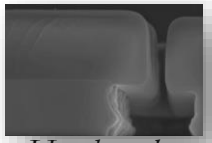



Thick
&
Conformal

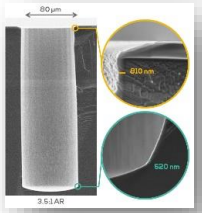
# Provides increased conformality vs. PECVD, PVD



# Wide material range and applications



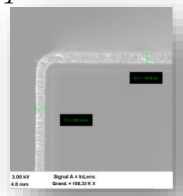
*Hardmask*

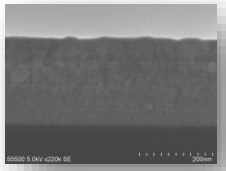


*Insulators*

*Planar layers*

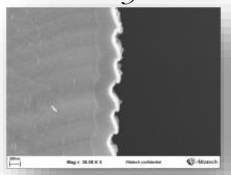
*Optical materials*

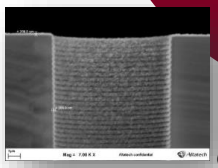




*Metal alloys*

*Barrier layers*

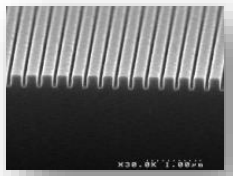




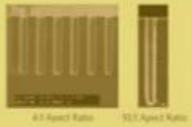
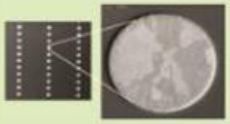
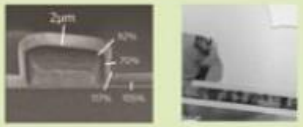
*Conductive films*

*Plug contact*

*Protective coatings*

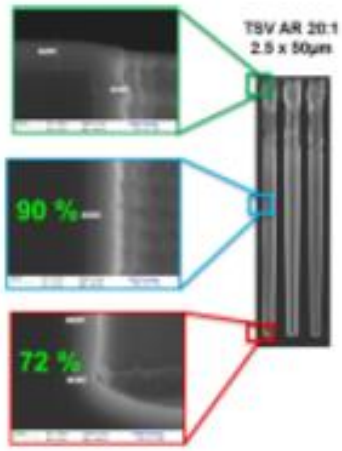


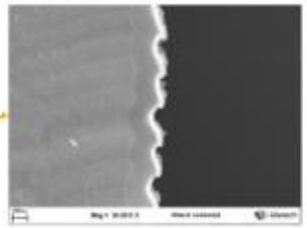
# 3-D Integration

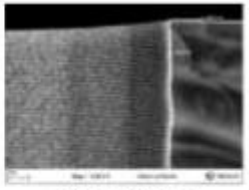
| | TSV Via Etch | TSV CVD Liner | TSV PVD Barrier/Seed | TSV ECD Fill | TSV CMP | RDL and Bump PVD, ECD, CVD |
|---|---|---|---|---|---|---|
| Process Step |  |  |  |  |  |  |
| Criteria | • High etch rate, resist selectivity<br>• In-situ oxide open<br>• Vertical profile<br>• Smooth sidewall<br>• Depth uniformity<br>• Si recess etch | • Conformality<br>• Sidewall thickness<br>• Thermal budget<br>• Adhesion<br>• Breakdown voltage<br>• Leakage current<br>• Dielectric constant | • Up to 10:1 aspect ratio<br>• Continuous Seed<br>• Copper Barrier<br>• Temperature management<br>• Process bonded substrates | • Up to 10:1 aspect ratio<br>• Void free fill<br>• Low overburden<br>• Thermal stability<br>• High throughput | • High removal rate, low CoC<br>• Good surface finish<br>• Process /Endpoint control to ensure uniformity<br>• Tunable topography<br>• Low defects | **PVD & ECD**<br>• Process bonded substrates<br>• Glass, Silicon carriers<br>• Temperature management<br>• Wafer bow management<br>**CVD**<br>• Step coverage<br>• Adhesion<br>• Breakdown voltage<br>• Leakage current<br>• Particle control |
| Current Capability |  |  |  |  |  |  |

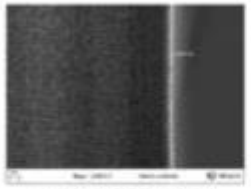
**F.A.S.T. $SiO_2$**

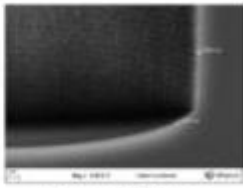
**F.A.S.T. TiN/Cu**



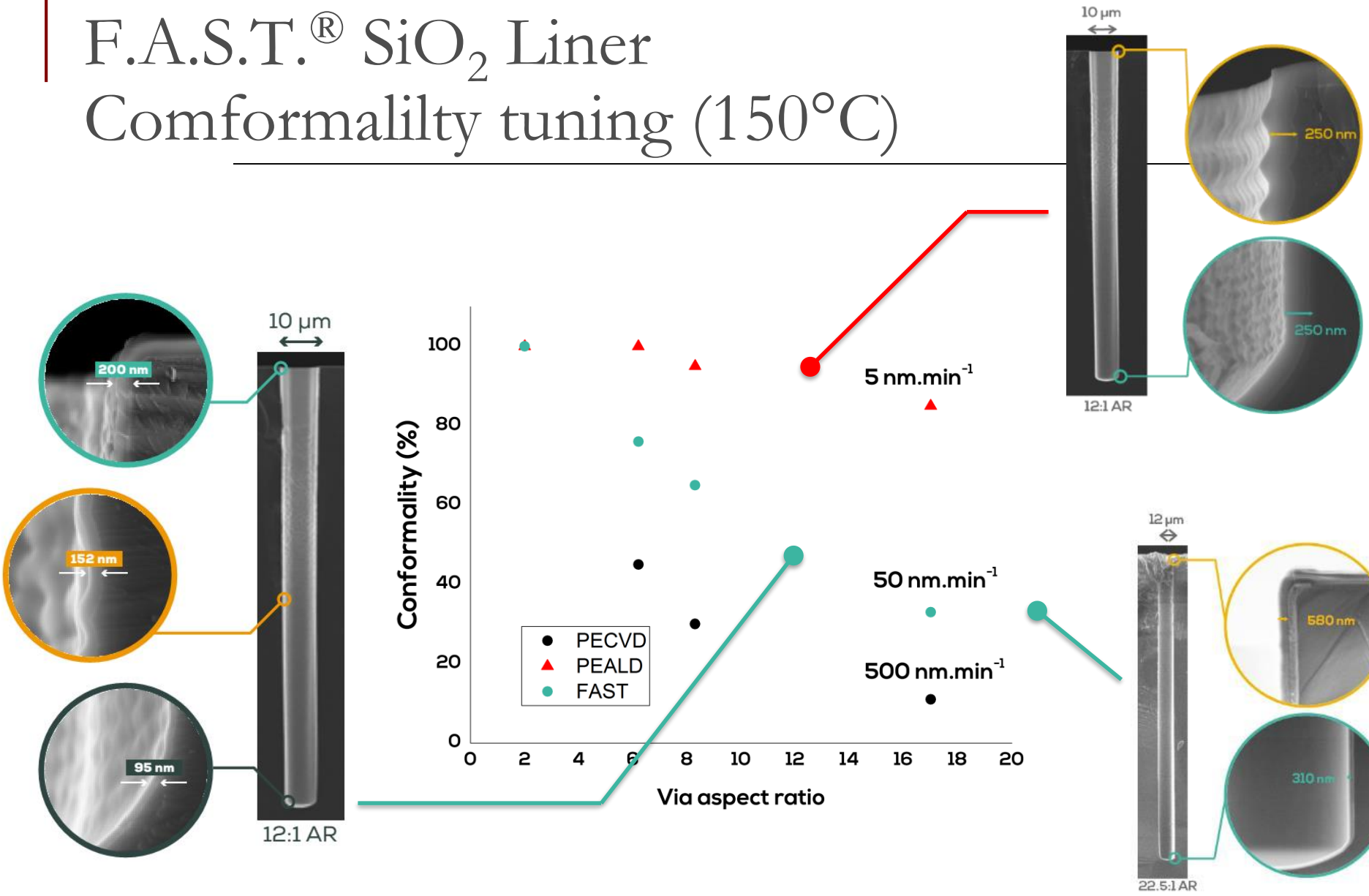




Top: 220 nm

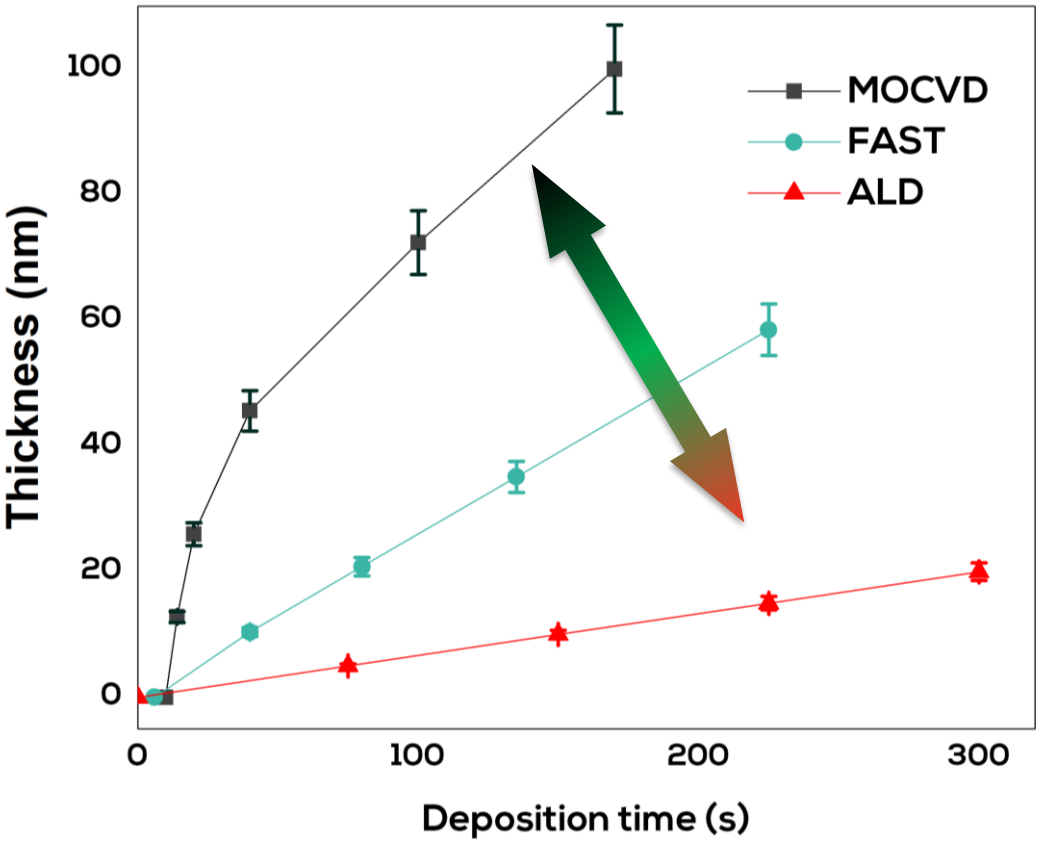

Middle: 220 nm


Bottom: 220 nm

# F.A.S.T.® $SiO_2$ Liner Comformalilty tuning (150°C)



# TiN example with FAST (375C)




**MOCVD:**

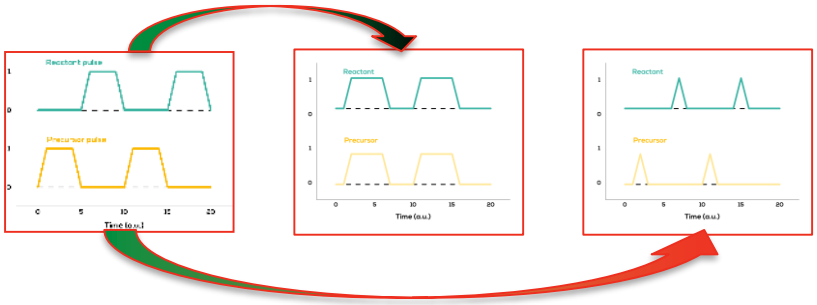
- High, non-linerar growth rate

**ALD:**

- Low deposition rate

**FAST:**

- Linear, fast growth rate, wider process window

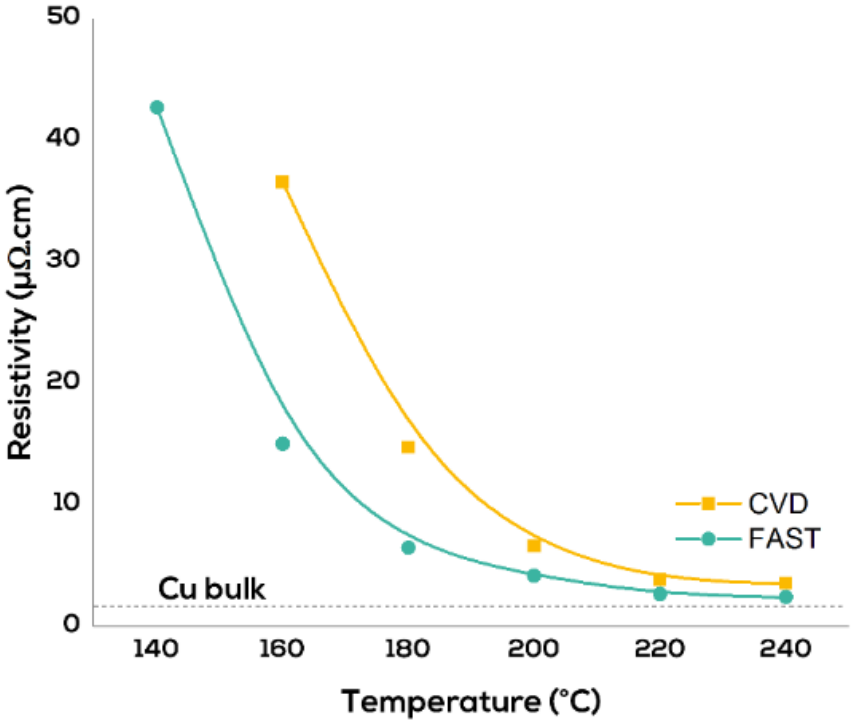


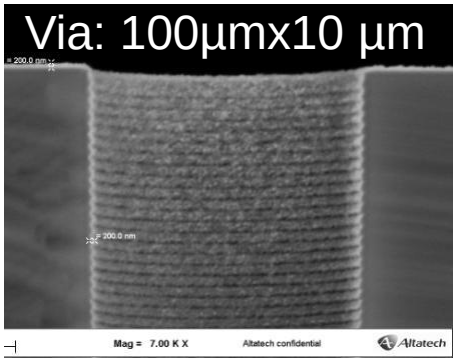
Wider process window

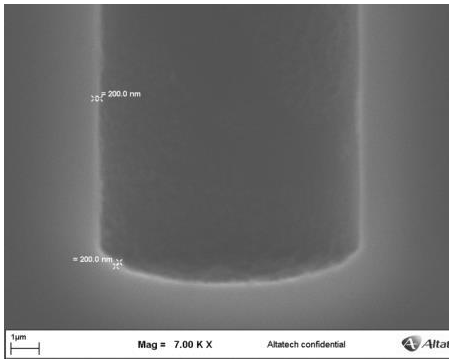
# Cu film performances

**Deposition**

- Using Cupraselect® precursor and $H_2$
- Deposition rate 30nm/min
- Deposition temperature below 200°C



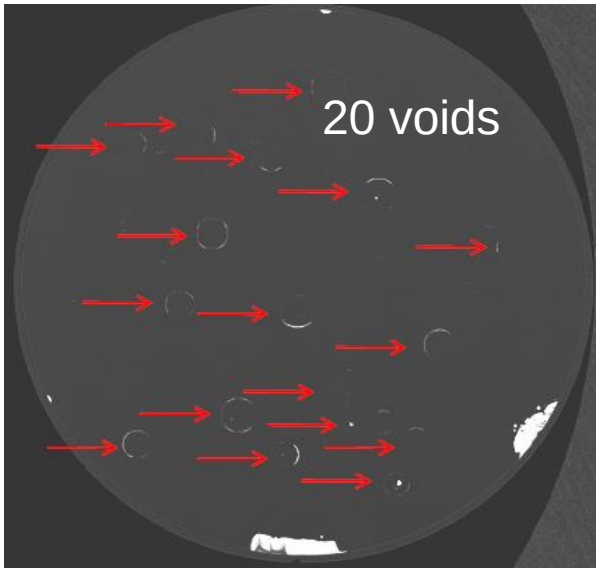




95% CONFORMITY
10:1 AR

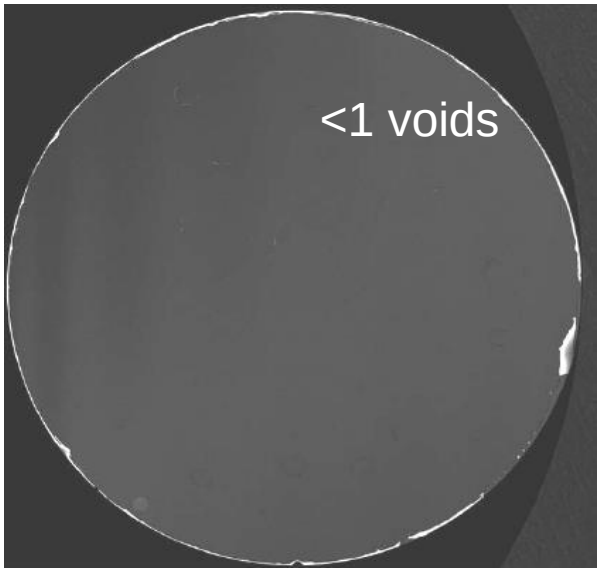
# SURFACE ACTIVATION

# Surface Activation and Cleaning for Wafer Bonding

Without plasma treatment




With plasma treatment

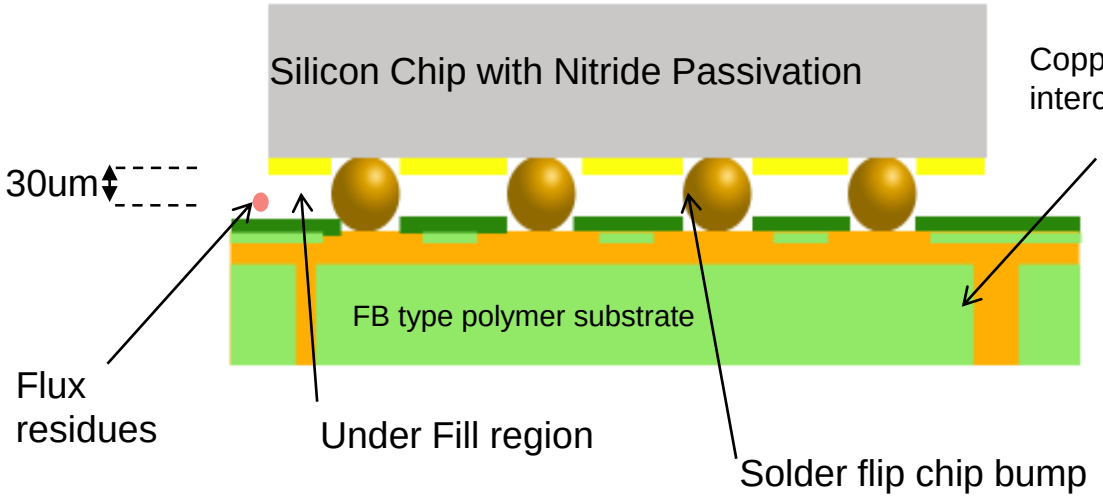



150mm wafer
Scanning Acoustic
Microscope

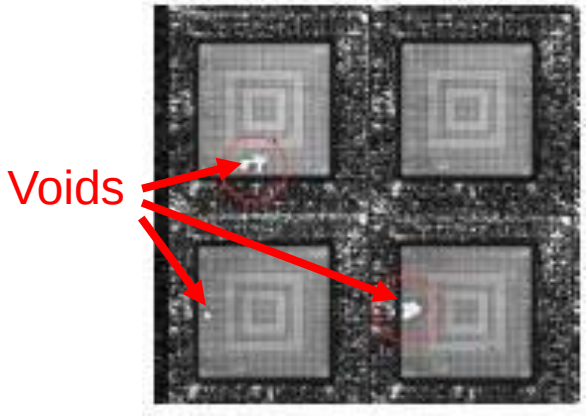
Silicon to Silicon and Silicon to Quartz. Si-OH + HO-Si → Si-O-Si + $H_20$

HDRF plasma: reduced ion-impact allowing longer exposure to radicals.
Lower surface activation energy promotes bonding

# Underfill – surface activation at low temperature




Conventional Treatment

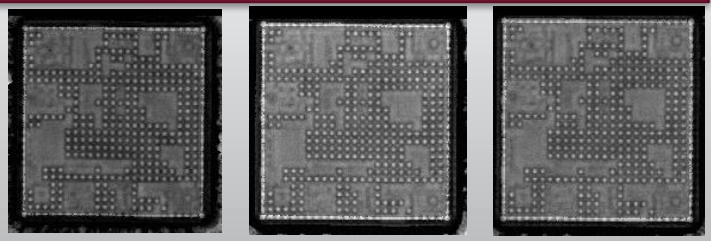



**Benefits**:

- Better epoxy wetting and reflow
- Fewer voids, increased yield

Chemical, low UV and ions, low temp

High density radical plasma treatment
*O2/Ar at 50°C*



Void-free underfil distribution

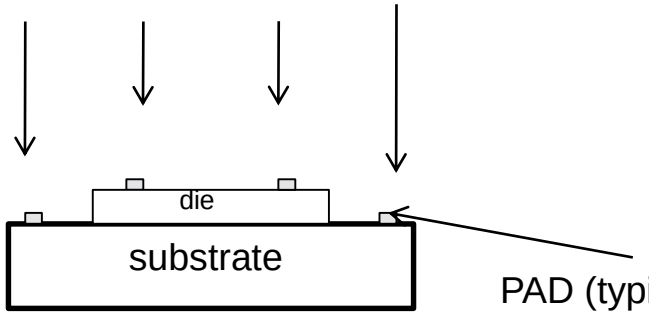
Example: contact angle from 60-80° to 10° with O* radical exposure

# Wire Bonding Pad Cleaning

Organic cleaning with O2

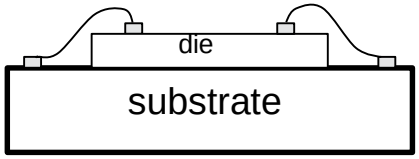
+

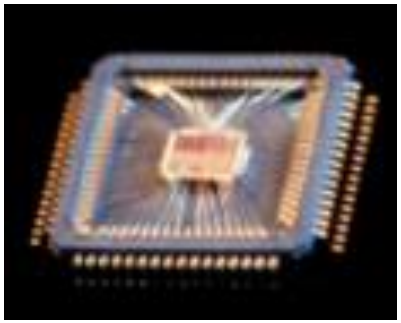
2nd step de-oxydation with H2




PAD (typically Ni, Au, Cu…)

After wire bonding



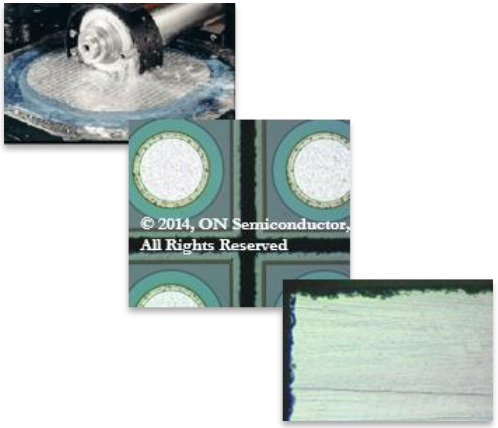



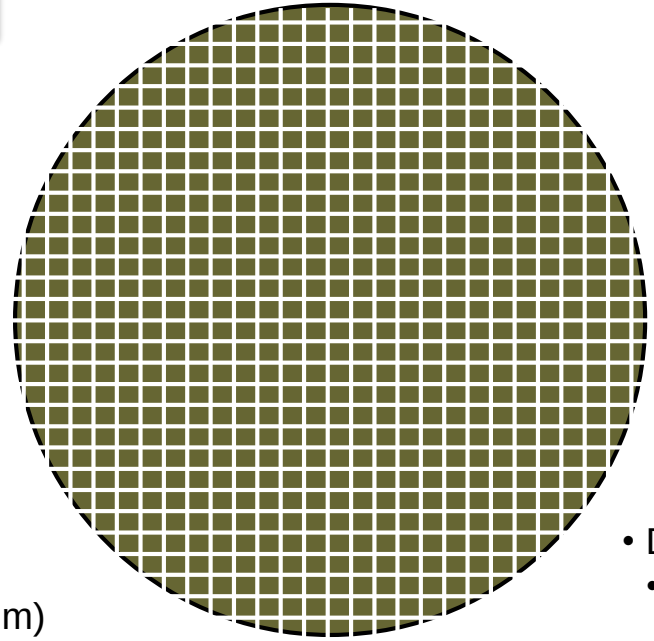
Contamination and/or oxidation removal from the bond pads prior to wire bonding to increase reliability and yields

# PLASMA DICING

# Current Wafer Dicing Technology - Sequential Processes

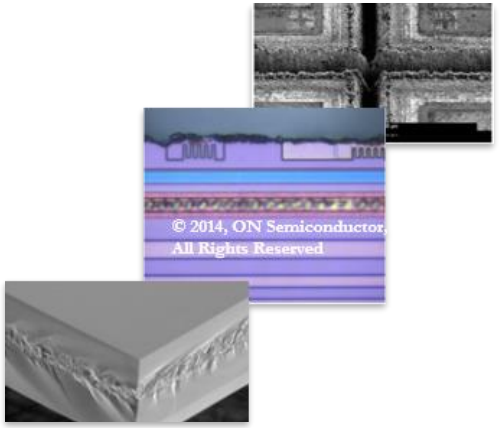
## Blade Dicing



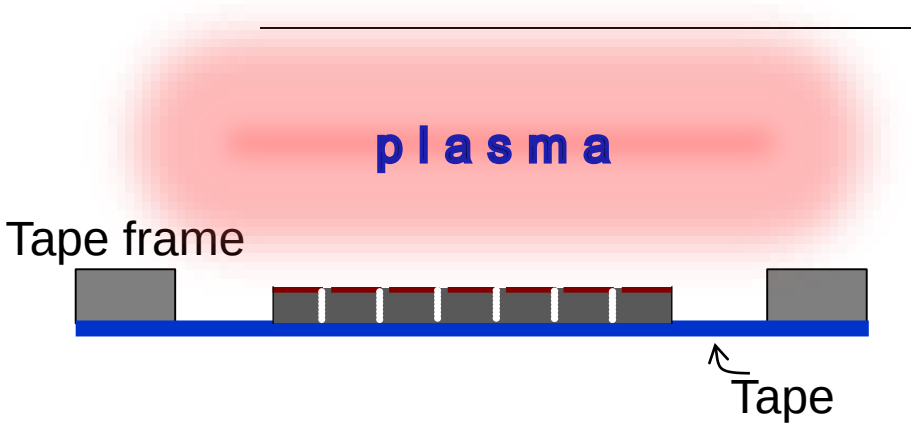
- Damage: cracks/chips
- Orthogonal layouts required
- Slower for thin wafers (<100µm)
- Slower for small die
- Poor accuracy
- Debris and water residues

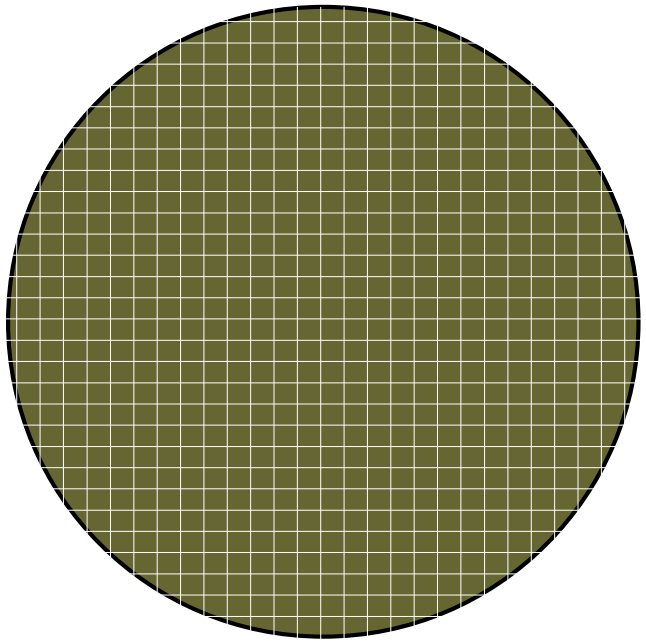
## Laser Dicing




- Damage:
  - thermal, recast, debris, delamination, micro-cracks
- Orthogonal layouts required
- Slower for small die
- Multiple passes for thicker wafers

# Plasma Dicing: Parallel Process

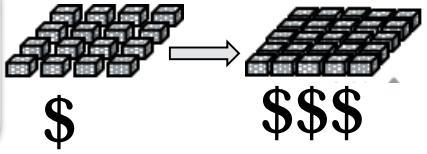


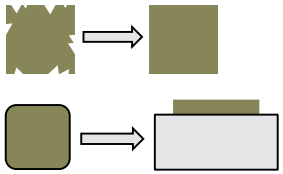



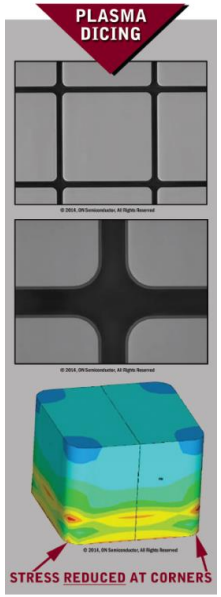
- Chemical process – low temperature
- No silicon damage
- Thinner wafers = shorter process
- High selectivity = low setup cost
  - No additional mask required
- No tape damage
- Accurate and precise ontrol of die sze
- Dice any shapes/layouts

# Plasma Dicing Benefits

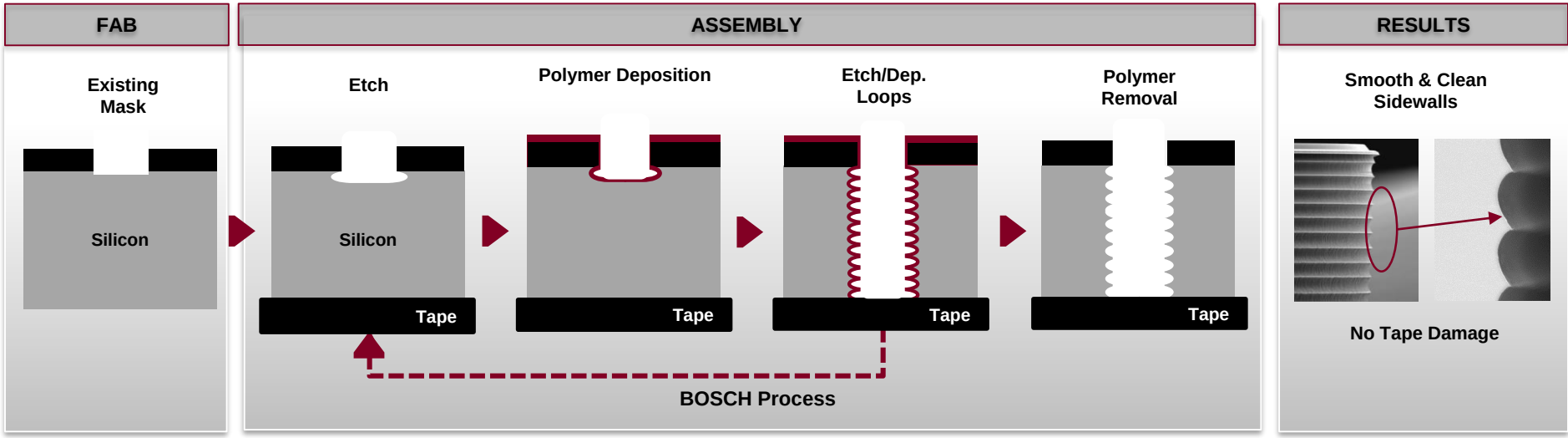
| | |
|---|---|
| Lower Cost Per Die | • Thinner wafers = faster dicing speed 50µm thick wafer < 3 min for dicing |
| More Die per Wafer | • Ultra narrow streets (~ < 5µm)<br>• Less wafer starts, more capacity |
| No Layout Design Constraints | • Freedom to dice any shape, multi-product wafers<br>• Rethink/relocate test/alignment areas |
| Higher Die Strength | • No chipping or micro-cracking<br>• No mechanical or thermal stress |
| Highest Accuracy | • Die size variation determined by the mask |

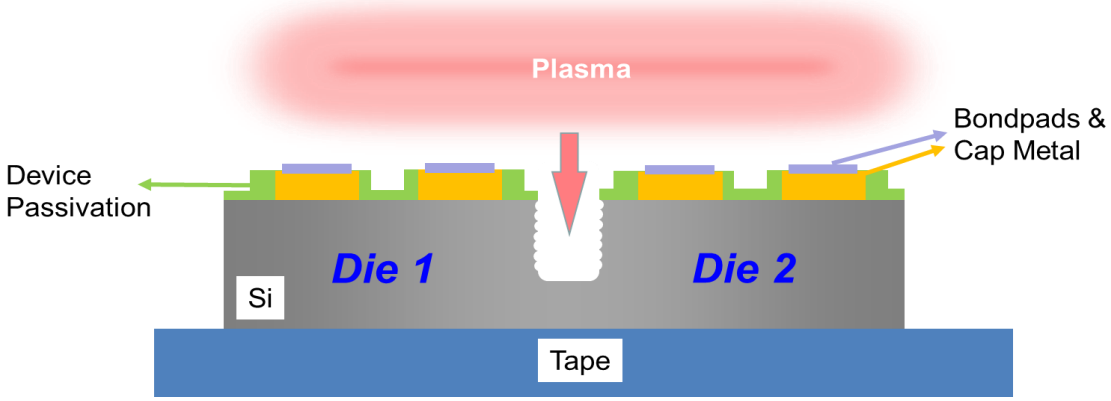




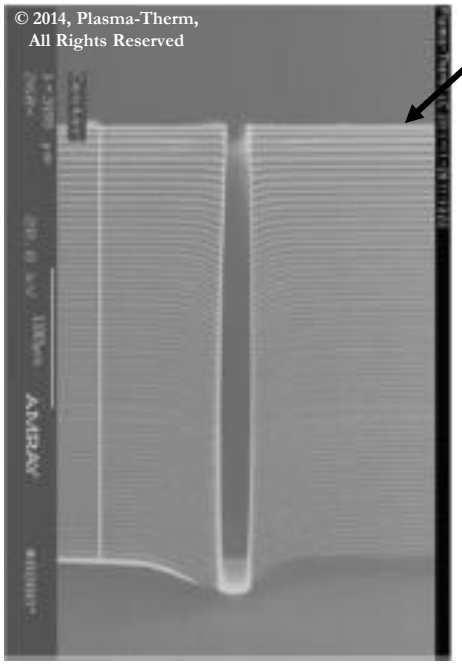
# Plasma Dicing on Tape
## Low temperature, highly selective DRIE Bosch

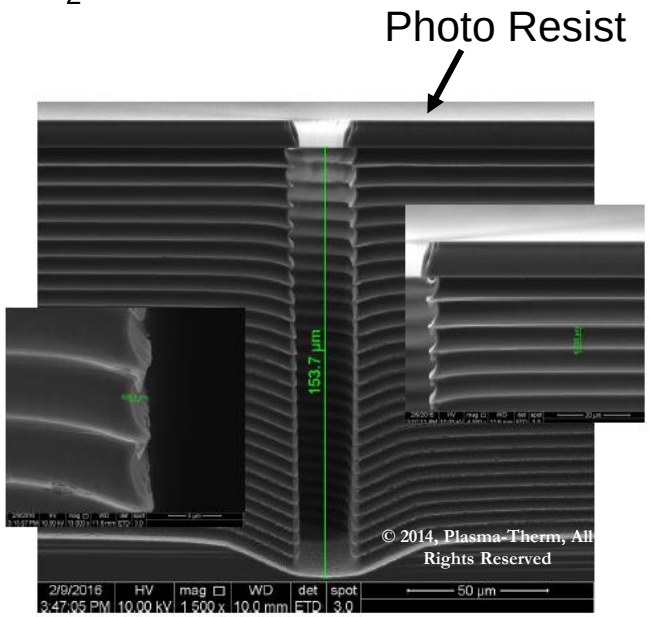


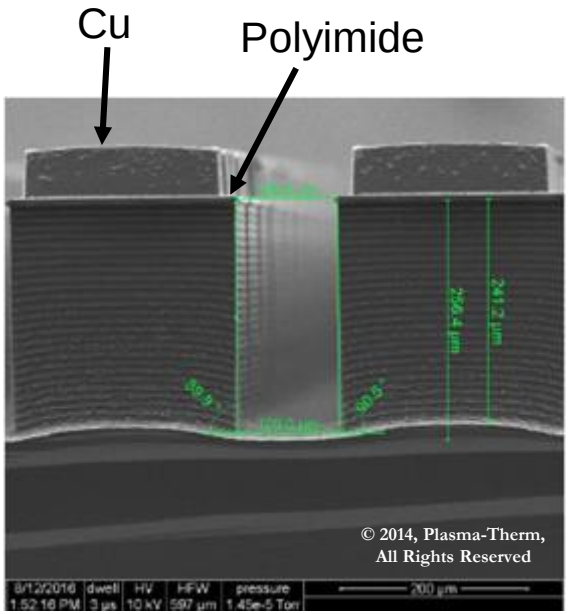




Using the device's passivation, the plasma etches the silicon in the streets

# A Variety of Passivation Materials Can Serve as Masks



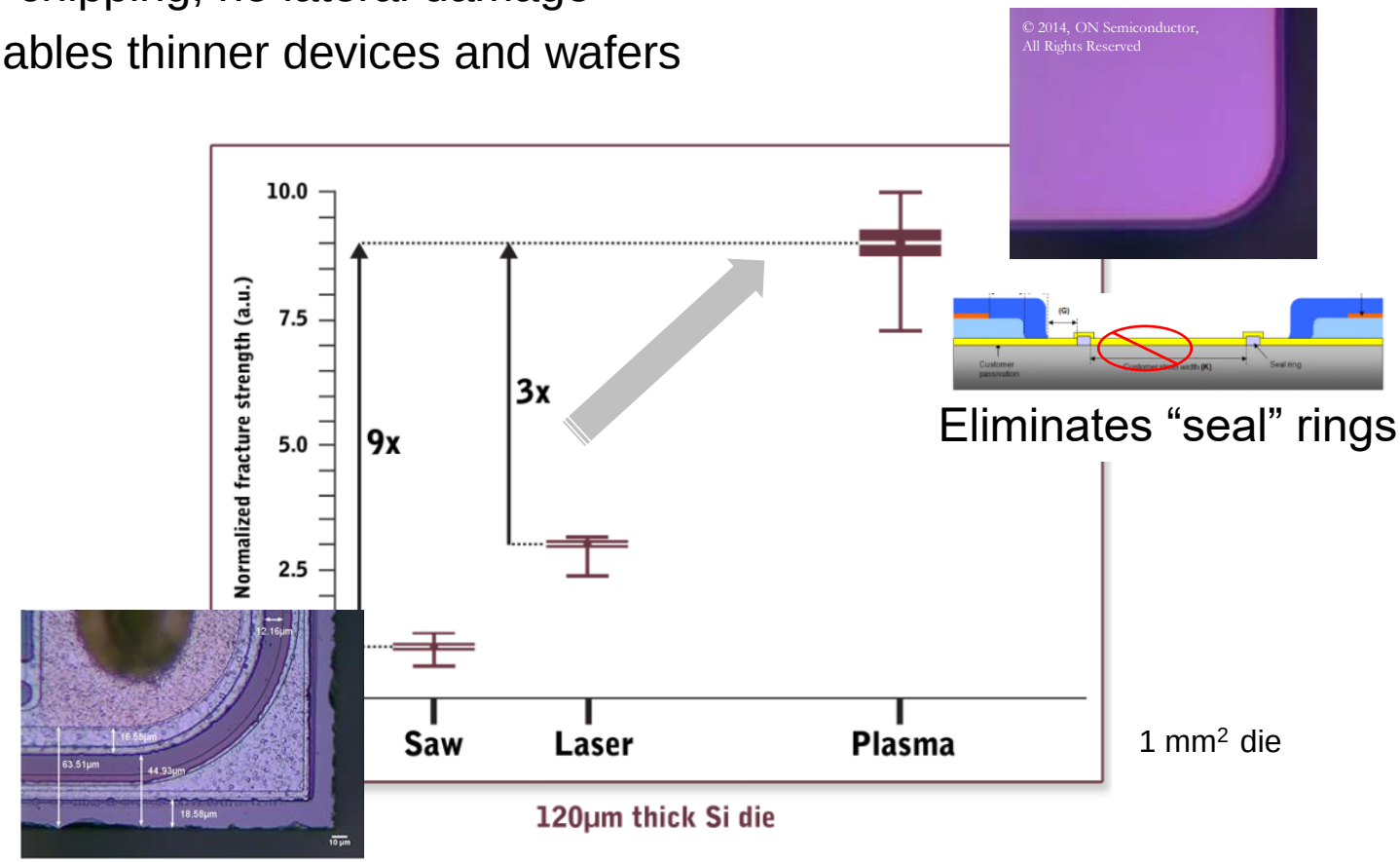



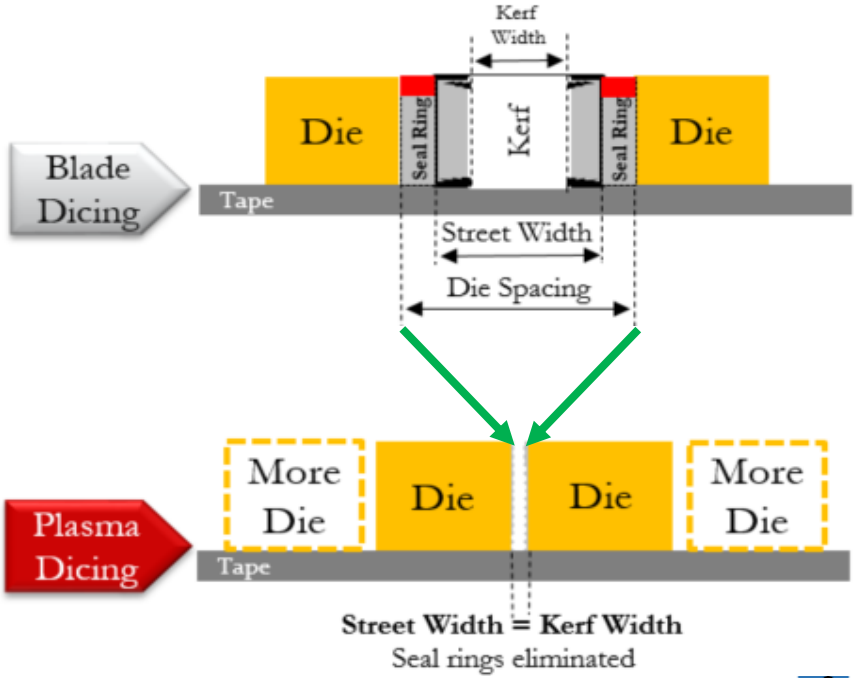

- $SiO_2$ Mask
  - Depth: 300µm
  - Width: 15µm
  - Selectivity: >800
  - No notching
- PR Mask
  - Depth: 150µm
  - Width: 15µm
  - Selectivity: >430
  - No notching
- PI and exposed Cu
  - Depth: 250µm
  - Width: 100µm
  - Selectivity: >250
  - No notching

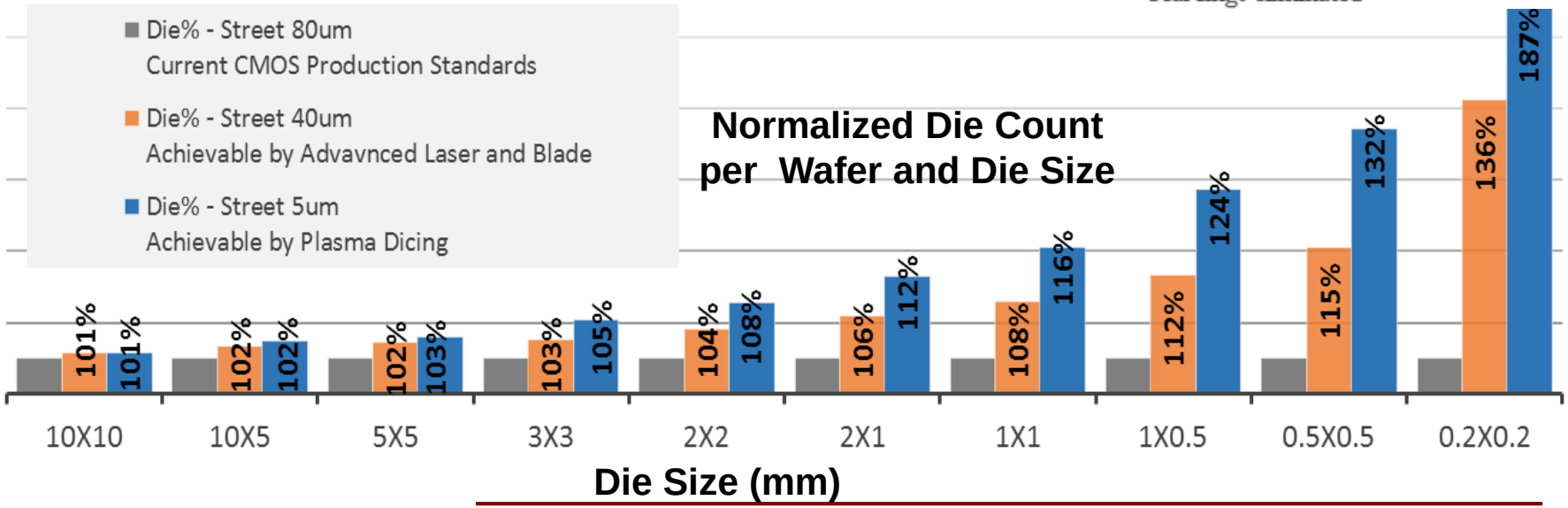
# Better dicing → Better die quality
## Superior Die Strength

- No chipping, no lateral damage
- Enables thinner devices and wafers



# More Die Per Wafer

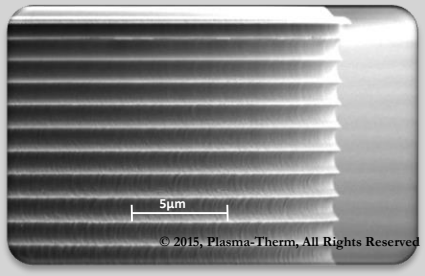



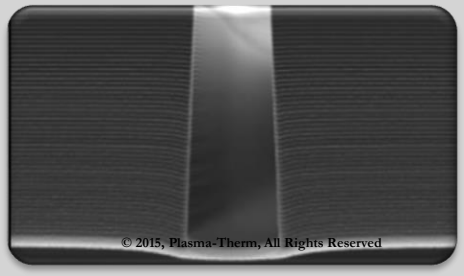



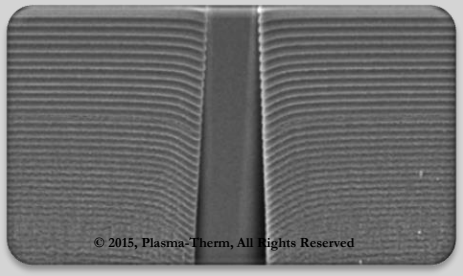

** Similar results for 200mm & 300mm wafers
** 3mm exclusion region used in calculations

Plasma-Therm

# New Dicing Capabilities with Sidewall Profile Control




**Additional Sidewall Surface Area**

Application-tailored scallop size, without chipping

**Tapered Profiles**

Improved epoxy reflow & mold encapsulation

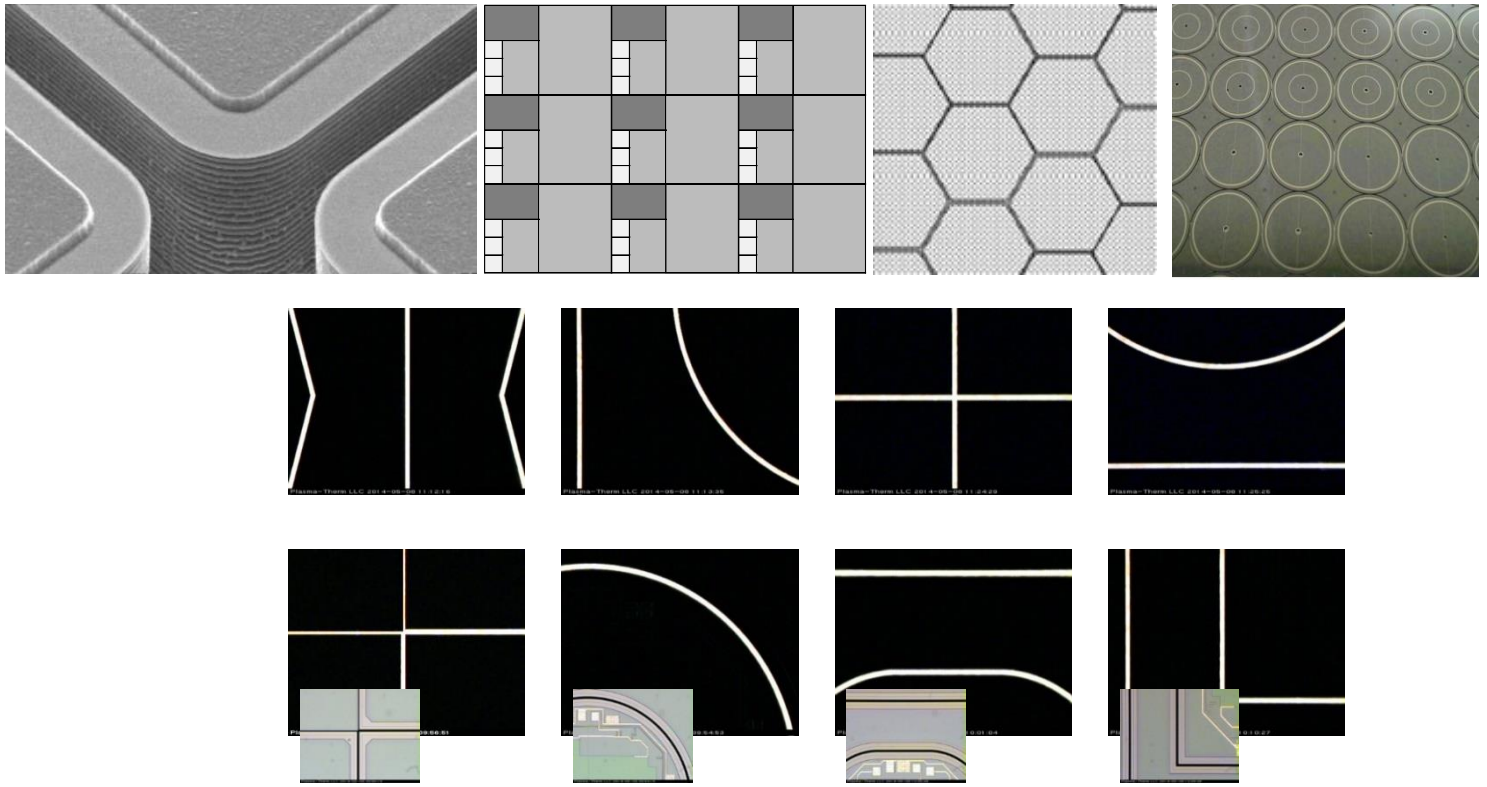
**Variable Sidewall Quality**

Deliver smoother sidewalls in active area and in non-active area.

Plasma dicing provides smoother sidewalls, a ndnew sidewall profile capabilities which can solve downstream packaging challenges

# New Dicing Capabilities
## Dice any shape or layout

**Examples:** Power devices, multi-product wafers, RF devices, LEDs, image sensors, microphones



# Plasma Dicing Adoption

| | Qualified (in production on MDS) | | | | Under Qualification | | |
|---|---|---|---|---|---|---|---|
| | **Power** | **LED** | **RFID** | **IR Image sensor** | **3D MEMS** | **III-V** | **CMOS** |
| **Wafer size** | 6 & 8” | 4 & 6” | 8” | 8” | 8” | 3 & 4” | 8” & 12” |
| **Wafer type** | Si, GaN/Si | Si, Ge | Si | Si | Si | GaAs | Si |
| **Street size** | 10µm | <5µm | 7µm | Round die | 20µm | 30µm | 10µm |
| **Wafer thickness** | >50µm | ≤120µm | 100µm | 400µm | 100+300µm | 300µm | 50 to 750µm |
| **Assembly** | Wirebond Flip Chip | Wirebond | Flip Chip | Confidential | Flip Chip | Wirebond | Flip Chip |
| |   |   |   | Customer confidential | Customer confidential |   |   |

# Acknowledgements

Christopher Johnston, Plasma Therm
Thierry Lazerand, Plasma Therm
Dr. Marco Notarianni, Plasma Therm
Dr. Kenneth Mackenzie, Plasma Therm
Yannick Pilloux, Plasma Therm
Julien Vitielo, Plasma Therm
Gordy Grivna, ON Semiconductor
Jason Doub, ON Semiconductor
Dr. Tomotak Tabushi, DISCO
Dr. Frank Wei, DISCO
Hideyuki Sando, DISCO
JS Jung, DISCO

Thank your for your contributions and materials to prepare this presentation

# Thank you


**Contact**: david.lishan@plasmatherm.com

Plasma-Therm