Low Temperature Plasma Technologies for Advanced Packaging Applications

NCCAVS - Northern California Chapter AVS Joint User Group Meeting (CMP, PAG, & TFUG)

David Lishan

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Outline

Plasma-Therm Introduction
Deep Silicon Etching / TSV
Low Temperature Strip / Clean
TSV Isolation and Seed Layer
Surface Activation
Plasma Dicing
Etch and Deposition Solutions
Lab-to-Fab

Etch & Clean Solutions: ICP, RIE, PE, PHF-RIE, DRIE, HDRF, IBE, RIBE, HF release
Deposition Solutions: PECVD, ICP-CVD, IBD, FAST-CVD
Plasma Dicing Solutions
DEEP SILICON ETCHING / TSV
DRIE – Deep Reactive Ion Etching

- Passivation ($C_4F_8 \rightarrow (CF_2)_n$)
- Selective passivation removal
- Isotropic etching of Si ($SF_6$)

- Low temperature
- Highly chemical etch mechanism
- High material selectivities (<250:1 to PR, 700:1 to SiO$_2$)
- High etch rates (25um/min)
- Anisotropic

Scallop Depth

Scallop Length
DRIE – High F Radical Concentrations
Fast Process Steps and Process Control

Low scalloping

Fast Gas Switching (FGS)
- SF$_6$
- C$_4$F$_8$

Decreasing step times

Profile Control

- With Morphing
  - Vertical profiles
- Without Morphing
  - Tapered profiles

- Fast valve response time
- No MFC overshoot pressure

**Path**

- 0.2
- 0.5
- 1
- 2
- 5

**Parameter**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>start</th>
<th>end</th>
<th>path</th>
</tr>
</thead>
<tbody>
<tr>
<td>electrode Bias</td>
<td>375</td>
<td>550</td>
<td>0.2</td>
</tr>
<tr>
<td>Dep time (sec)</td>
<td>1.5</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

11nm
DRIE

Wide range of etch capabilities

- Aspect ratio 60:1
- High Load
- Smooth sidewalls roughness < 10 nm
- Notch reduction on SOI
- High Etch Rate > 25 µm/min
- Low Tilt Angle <0.2º
- High selectivity Si:PR > 200:1
  Si:SiO₂ > 700:1

Optimized reactor
DRIE

Wide range of applications
DRIE – TSV Applications

50µm Via diameter
200µm deep

Etch Rate > 7 µm/min
Uniformity <1.5%
Selectivity Si: PR > 175:1
Straight profile 89.9 +/-0.1

Undercut < 500nm
Scallops < 76nm

50µm Via diameter
150µm deep

Etch Rate > 14 µm/min
Uniformity < 5%
Straight profile 90.5 +/-0.5

Undercut < 1 µm
Scallops < 400nm

10µm Via diameter
100µm deep

Etch Rate > 14 µm/min
Uniformity < 5%
Straight profile 90.5 +/-0.5

Scallops < 400nm
Low Tilt & SOI Applications

Low Tilt Angle

Notch reduction on SOI wafer

2 to 10µm wide trench
40µm deep

Etch Rate > 7µm/min
Uniformity 2%

* Si open area 15%

More good dies per wafer
LOW TEMPERATURE STRIP / CLEAN
Plasma-Therm: HDRF™
High Density Radical Flux

HDRF™ technology
Active species: O* Radicals

Conventional RF
Active species: O* + Ions
Ions = damage, heating

- High plasma density ICP source
  - Radicals density > 1E17 cm⁻³
  - Mainly O* radicals at wafer level

- Low damage on sensitive devices
  - Low ions at wafer level
  - Low temperature processing < 80°C

“mini” ICP sources

Plasma-Therm
DRIE polymer removal

EDX analysis (Energy Dispersive X-ray Spectroscopy)

DRIE Bosch polymer – Via top

trace of F and C

After HDRF

No more trace of F and C

XPS analysis (X-ray Photo-electron Spectroscopy)

DRIE Bosch polymer – Via bottom

F* peak

After HDRF

No more F* peak

Efficient dry cleaning technology, to remove fluor-carbon polymers
**PR & Polymer removal**

**SEM and EDAX**  \( Pre \rightarrow Post \) measurement

<table>
<thead>
<tr>
<th>Spot</th>
<th>C  (Weight %)</th>
<th>O  (Weight %)</th>
<th>F  (Weight %)</th>
<th>Si (Weight %)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spot 1 (PR)</td>
<td>73 → 0</td>
<td>27 → 0</td>
<td>0 → 0</td>
<td>0 → 0</td>
</tr>
<tr>
<td>Spot 2 (polymer)</td>
<td>29 → 0</td>
<td>0 → 0</td>
<td>71 → 0</td>
<td>0 → 0</td>
</tr>
<tr>
<td>Spot 3 (baseline)</td>
<td>0 → 0</td>
<td>0 → 0</td>
<td>0 → 0</td>
<td>98 → 100</td>
</tr>
</tbody>
</table>
Low-temperature PR (and polymer) strip

Low temperature HDRF process
For temperature sensitive applications

Higher strip rate with increasing temperature
Micro Mirrors Cleaning

- Elimination of mirror tilt due to residues
- Damage-free. No electrical charging
- Yield improvement
TSV ISOLATION and SEED LAYER
F.A.S.T.® Crossroads of ALD and CVD

(PE)CVD

(PE)ALD Monolayer growth

Fast Atomic Sequential Technology

Multilayer growth
3D Technology Approaches for TSV

ALD PEALD

Very Thin & Conformal

Process time

PECVD

Very thick & Non-conformal

Process time

FAST

Thick & Conformal

Process time
Provides increased conformality vs. PECVD, PVD

Combined mode (FAST + ALD)
Wide material range and applications

**OXIDES**
- TiO₂
- SiO₂
- HfO₂
- Al₂O₃
- Ta₂O₅
- ZnO

**NITRIDES**
- TiAlN
- TiN
- TaN
- TaCN
- SiN

**METALS**
- GeSbTe
- Cu
- W

**Conductive films**

**Insulators**
- Metal alloys
- Planar layers
- Optical materials
- Barrier layers

**Protective coatings**

**Hardmask**

**Plug contact**
# 3-D Integration

<table>
<thead>
<tr>
<th>Process Step</th>
<th>Criteria</th>
<th>Current Capability</th>
</tr>
</thead>
</table>
| TSV Via Etch | • High etch rate, resist selectivity  
• In-situ nozzle open  
• Vertical profile  
• Smooth side-wall  
• Depth uniformity  
• Si recess etch | ![Image of TSV Via Etch] |
| TSV CVD Liner | • Conformality  
• Sidewall thickness  
• Thermal budget  
• Adhesion  
• Breakdown voltage  
• Leakage current  
• Dielectric constant | ![Image of TSV CVD Liner] |
| TSV PVD Barrier/Seed | • Up to 10:1 aspect ratio  
• Continuous Seed  
• Copper Barrier  
• Temperature management  
• Process bonded substrates | ![Image of TSV PVD Barrier/Seed] |
| TSV ECD Fill | • Up to 10:1 aspect ratio  
• Void-free fill  
• Low overburden  
• High stability  
• High throughput  
• Low defects | ![Image of TSV ECD Fill] |
| TSV CMP | • High removal rate, low CuC  
• Good surface finish  
• Process/endpoint control to ensure uniformity  
• Tunable topography  
• Low defects | ![Image of TSV CMP] |
| RDL and Bump PVD, ECD, CVD | • PVD & ECD  
• Process bonded substrates  
• Glass, Silicon carriers  
• Temperature management  
• Wafer bow management  
• Package control  | ![Image of RDL and Bump] |

**F.A.S.T.**  
- SiO₂  
- TiN/Cu
F.A.S.T.® SiO$_2$ Liner
Comformalilty tuning (150°C)
TiN example with FAST (375C)

MOCVD:
- High, non-linear growth rate

ALD:
- Low deposition rate

FAST:
- Linear, fast growth rate, wider process window

Wider process window
Cu film performances

**Deposition**

- Using Cupraselect® precursor and H$_2$
- Deposition rate 30nm/min
- Deposition temperature below 200°C

![Graph showing resistivity vs. temperature](image)

- CVD
- FAST

- 95% CONFORMITY
  - 10:1 AR

![SEM image of via](image)
SURFACE ACTIVATION
Surface Activation and Cleaning for Wafer Bonding

Without plasma treatment

With plasma treatment

Silicon to Silicon and Silicon to Quartz. \( \text{Si-OH} + \text{HO-Si} \rightarrow \text{Si-O-Si} + \text{H}_2\text{O} \)

HDRF plasma: reduced ion-impact allowing longer exposure to radicals. Lower surface activation energy promotes bonding.
Underfill – surface activation at low temperature

Benefits:
- Better epoxy wetting and reflow
- Fewer voids, increased yield

Chemical, low UV and ions, low temp

Example: contact angle from 60-80° to 10° with O* radical exposure
Wire Bonding Pad Cleaning

Organic cleaning with O2
+ 2nd step de-oxidation with H2

Contamination and/or oxidation removal from the bond pads prior to wire bonding to increase reliability and yields
Current Wafer Dicing Technology - Sequential Processes

**Blade Dicing**
- Damage: cracks/chips
- Orthogonal layouts required
- Slower for thin wafers (<100μm)
- Slower for small die
- Poor accuracy
- Debris and water residues

**Laser Dicing**
- Damage:
  - thermal, recast, debris, delamination, micro-cracks
  - Orthogonal layouts required
  - Slower for small die
  - Multiple passes for thicker wafers
Plasma Dicing: Parallel Process

- Chemical process – low temperature
- No silicon damage
- Thinner wafers = shorter process
- High selectivity = low setup cost
  - No additional mask required
- No tape damage
- Accurate and precise control of die size
- Dice any shapeslayouts
Plasma Dicing Benefits

**Lower Cost Per Die**

- Thinner wafers = faster dicing speed
  - 50µm thick wafer < 3 min for dicing

**More Die per Wafer**

- Ultra narrow streets (~ < 5µm)
- Less wafer starts, more capacity

**No Layout Design Constraints**

- Freedom to dice any shape, multi-product wafers
- Rethink/relocate test/alignment areas

**Higher Die Strength**

- No chipping or micro-cracking
- No mechanical or thermal stress

**Highest Accuracy**

- Die size variation determined by the mask

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Plasma-Therm
Plasma Dicing on Tape
Low temperature, highly selective DRIE Bosch

Using the device’s passivation, the plasma etches the silicon in the streets.
A Variety of Passivation Materials Can Serve as Masks

- **SiO$_2$ Mask**
  - Depth: 300µm
  - Width: 15µm
  - Selectivity: >800
  - No notching

- **PR Mask**
  - Depth: 150µm
  - Width: 15µm
  - Selectivity: >430
  - No notching

- **PI and exposed Cu**
  - Depth: 250µm
  - Width: 100µm
  - Selectivity: >250
  - No notching
Better dicing → Better die quality
Superior Die Strength

- No chipping, no lateral damage
- Enables thinner devices and wafers

Eliminates “seal” rings

1 mm² die

120µm thick Si die

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Plasma-Therm
More Die Per Wafer

Normalized Die Count per Wafer and Die Size

** Die% - Street 80um
Current CMOS Production Standards

** Die% - Street 40um
Achievable by Advanced Laser and Blade

** Die% - Street 5um
Achievable by Plasma Dicing

Die Size (mm)

101% 101% 102% 102% 103% 103% 105% 104% 108% 106% 108% 112% 116% 112% 124% 115% 132% 136% 187%

10X10 10X5 5X5 3X3 2X2 2X1 1X1 1X0.5 0.5X0.5 0.2X0.2

** Similar results for 200mm & 300mm wafers
** 3mm exclusion region used in calculations
New Dicing Capabilities with Sidewall Profile Control

Additional Sidewall Surface Area
Application-tailored scallop size, without chipping

Tapered Profiles
Improved epoxy reflow & mold encapsulation

Variable Sidewall Quality
Deliver smoother sidewalls in active area and in non-active area.

Plasma dicing provides smoother sidewalls, and new sidewall profile capabilities which can solve downstream packaging challenges.
New Dicing Capabilities
Dice any shape or layout

Examples: Power devices, multi-product wafers, RF devices, LEDs, image sensors, microphones
## Plasma Dicing Adoption

<table>
<thead>
<tr>
<th></th>
<th>Qualified (in production on MDS)</th>
<th>Under Qualification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>LED</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>RFID</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>IR Image sensor</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>3D MEMS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>III-V</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CMOS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Wafer size</strong></td>
<td>6 &amp; 8”</td>
<td>3 &amp; 4”</td>
</tr>
<tr>
<td><strong>Wafer type</strong></td>
<td>Si, GaN/Si</td>
<td>GaAs</td>
</tr>
<tr>
<td><strong>Street size</strong></td>
<td>10µm</td>
<td>20µm</td>
</tr>
<tr>
<td><strong>Wafer thickness</strong></td>
<td>&gt;50µm</td>
<td>100+300µm</td>
</tr>
<tr>
<td><strong>Assembly</strong></td>
<td>Wirebond</td>
<td>Flip Chip</td>
</tr>
<tr>
<td></td>
<td>Flip Chip</td>
<td>Wirebond</td>
</tr>
<tr>
<td></td>
<td>Confidential</td>
<td>Flip Chip</td>
</tr>
<tr>
<td></td>
<td>Confidential</td>
<td></td>
</tr>
</tbody>
</table>

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Contact: david.lishan@plasmatherm.com