Heterogeneous Integration Needs Heterogeneous Package Assembly

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Our Global Reach

423,000+ Members

46 Technical Societies and Councils

160+ Countries

Our Technical Breadth

1,800+ Annual Conferences

4,200,000+ Technical Documents

190+ Top-cited Periodicals
Globally http://eps.ieee.org
2300 members worldwide
30 chapters in US, Asia and Europe
Silicon Valley www.cpmt.org/scv
250 EPS members

Very active Silicon Valley Chapter with monthly technical talks at TI auditorium
Chapter chair - Dr. Annette Teng (Promex)
Vice-Chair - Dr. Gamal Refai-Ahmed (Xilinx)

ECTC – http://www.ectc.net
1750 international attendees at Premier Packaging Conference May 28th - Jun 1st, 2018
What is Heterogeneous Integration?

Heterogeneous Integration uses packaging technology to integrate dissimilar chips with different functions into a system or subsystem, rather than integrating all the functions into a single chip.

Why Heterogeneous Integration?

This is because End of Moore’s law is fast approaching and it is more difficult and costly to reduce the feature size and squeeze excessive functions on a single chip.

What’s driving Heterogeneous Integration?

Faster Time-to-market, Lower Cost, flexibility, Improved power consumption and performance.
Heterogeneous Integration is defined as the integration of separately manufactured components into a higher level assembly (SiP) that in the aggregate provides enhanced functionality and improved operating characteristics.
HI Example-Xilinx’s VIRTEX

3 Field Programmable Gate Array dies

2 High Bandwidth Memory die (stacked memory chips)

It should be noted that HBM represents a significant leap in system performance, as it moves a large amount of memory much closer to the active IC. However, this memory is still on a separate piece of silicon, which must be integrated into the package.

Warpage management
Single Si interposer

S. McCann et al, Xilinx 2018 ECTC
HI – Multichip Package

Wire bond
Over mold (~170μm)
LPDDR4 Memory (105μm)
Coreless substrate
Underfill
A10 AP (165μm)
3RDLs
Contact Pad ~1300 solder balls at 0.4mm pitch
Binghamton University/Prismark

15.5mm x 14.4mm x 825μm
So many options:
Silicon/glass interposer
Redistributed Layers on Wafer

2DO
2DS (without TSV)

2D PoP

3D F2F

3D TSV

2DO PoP

2DS with TSV
Traditional HI assembly

1. Flex & PCB substrates
2. Ceramic substrates
3. Metal substrates
HI Assembly on Flex & PCB

1. Design and order flex/PCB
2. Solder paste stenciling
3. FC & component attach + Reflow
4. Attach additional fragile parts
5. Wirebond or Print conductors
6. Underfill, Glob top, Dam & Fill
7. Singulate (Optional)
Flex HI Assembly

Imagers on Flex - requires Class 100 Clean room

High precision placement
Ceramic film printing for HI

Conductive & Dielectric film printing

Attach Die & Component

Wirebond

Encapsulate-Mold, Dam & Fill

Singulate
METAL LEADFRAME for HI

1. Die & component attach / stack
2. Interconnect - Wirebond or Flipchip
3. Encapsulate - Mold or Dam & Fill
4. Etch and coat
5. Singulate
Process Flow of HDL (High Density Lead-frame)

- Metal Frame Std 150um
- Pattern Etching and Leadframe Manufacturing
- Bonding Layer
  - Ag Plating
- Die Attach and Wire Bonding
- Encapsulation
- Final Etching
- Solder Resist Coating
- Solder Ball Generation
Example of HI on a QFN
9x9mm 80L HDL @ 0.50 mm pitch

Top View

Bottom View

Cross Section A-A
Thin is In

Ultrathin < 50um
extreme thin < 5um

Samsung K9UGB8S7M 48L V-NAND Flash memory showing 40um dies interlayered with DAF.
Assembly processes are evolving to meet the demands of ultrathin dies and stacked die

1. Wafer Thinning
2. Die Singulation
3. Thin die pick
4. Thermocompression bond
5. Compression mold
ASSEMBLY FLOW

1. Background

- Wafer (≥0.70mm)
- Apply front side tape
- Rough grind
- Remove front side tape
- Fine grind
- Wash wafer

2. Singulation

- Singulate/dicing
- Remove front side tape
- Assembly
Wafer Backgrind

Grinding Feed

~2500 rpm

Grinding Wheel

~250 rpm

Chucktable Axis

Wafer
Dice Before Grind

Groove

Wafer Frontside

Dicing tape

BackGrind

Backgrind tape

Wash

Tape and frame

Tape Flip

Wafer Frontside

10um Si dies

10um silicon chip
Plasma Dicing

**Figure 11.** The Bosch deep Si etch process loop illustration.
Precision Pick and Place

Datacon 2200 APM & EVO
- Automatic die attach & flipchip bonder
- Excellent Die placement accuracy
- Up to 12 “ wafer chuck
- 0.5mm die size
- Built-in Adhesive dispense
- Built-in UV cure
- Configured for lead frame or substrates
- Configured for DAF attach
Vacuum assisted die pick

- Peel tape from die edge
- Vacuum suction
- Contouring ejector surface

Ultrathin die

Pepper-pot
Full thickness
Samsung K9UGB8S7M 48L V-NAND Flash memory showing 40um dies interlayered with DAF.

Die attach film
Thermocompression bonding

Toray’s Collective TCB of Stacked Chips

- Pre Bonding: Bond-force = 30N; Temp. = 150°C; ~1s
- Stage temperature = 80°C
- Post Bonding: ~10s

1st step (3s): Bond-force = 50N; Temp. = 220-260°C
2nd step (7s): Bond-force = 70N; Temp. = 280°C

Peripheral portion

Area portion

Toray, Sept. 2015, IEEE/3DIC conference
Molding comparison

Transfer Molding

Compression Molding

100% resin usage
Compression Molding

![Diagram of Compression Molding Process]

- **MOLD PRESSURE**
- **UPPER CHASE MAIN CAVITY BLOCK**
- **LOWER CHASE HOLDER**
- **MIDDLE PLATE**
- **UPPER CHASE HOLDER**
- **LOWER CHASE HOLDER**
- **LOWER BASE PLATE**
- **LOWER MAIN CAVITY BLOCK**

Key Parts:
- **RESIN**
- **RELEASE FILM**
- **O-RING**
- **FILM CLAMPER**
- **LOWER FRAME CLAMP BLOCK**
- **MOLDING PRODUCT**

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Compression Molded Panel

1. Warpage control
2. No trapped voids
3. Uniform Filler distribution
4. Wire-sweep control
5. Minimum MC waste
Takeaway

• Heterogenous Integration is here
• HI Roadmap Task force set up -publication 2018
• 2 categories of HI
  • Wafer/Panel level (silicon/glass/wafer RDL)
  • Substrate level (ceramics, metal, flex, PCB)
    • Ceramics – thick film/thin film/co-fired
    • Metal – Leadframe etching / mold
    • Organic – PCB and Flex
• Examples of new packaging technologies using vacuum (or Pressure) for improved process control.
  • Thin die dicing
  • Thin die peeling
  • Thermocompression bonding
  • Compression molding
Thank you.