Equipment and Process Challenges for the Advanced Packaging Landscape

Veeco Precision Surface Processing

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June 2018
Outline

» Advanced Packaging Market Landscape

» Packaging Concepts and Equipment Challenges

» Approaches and Examples

» Summary
Advanced Packaging Landscape - Markets

- Smartphones
- Memory
- Connectivity
- Data centers
- Automotive
- Smart Home
Moore’s Law and More than Moore

Market Based Roadmap –
Chip Functions and Applications
Heterogeneous Integration

Scaling Roadmap

Moore’s Law and beyond

130nm
90nm
65nm
45nm
32nm
22nm
14nm

Analog/RF
Passives
Power
MEMS/Sensors
LED
BioChips

Si
SiC
GaAs
Sapphire
Ge

CMOS
NVM
SOI
FinFET

SoC and SiP → Advanced Packaging
3D High Performance Devices Require TSV

Hybrid Memory Cube (HMC)

High End Graphics

Figure 2.1. AMD’s Fiji with silicon interposer and HBM.

High Bandwidth Memory (HBM)

1GB HBM up to 128GB/s (@1.2V, x1024)

Ref: Samsung
2.5D Interposers for Heterogeneous Integration

A configuration where dies are mounted side by side on one side of a thin (~ 100 um) **silicon, glass, or organic interposer** using through **silicon** vias (TSV), through **glass** vias (TGV) or through **organic** vias (TOV), respectively through the interposer to connect the dies with the package substrate.
Other Technologies for Heterogeneous Integration

SLIM™ Silicon-Less Integrated Module

SWIFT™ Silicon Water Integrated Fan-out Technology

TSMC

Intel

Source: ASE.

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Wafers / Panels / Sizes for Advanced Packaging

Source: Yole
Panel Size Uncertainty for Large Area Fan-Out

Larger bubble indicates panel size use by multiple companies

Source: TechSearch International
Dimensions and Cost
Advanced Packaging Options

- **Package Max Size**: <15mm
- **Substrate Form Factor**: Wafer/Panel 300/330/450/500+
- **Chip Placement**: 2D/Stacked/Embedded
- **Materials**: Si/Glass/Organic
- **Dimensions**: Line/Space Via/Pitch
- **Cost**
- **Bandwidth Performance Yield**
- **# I/O per mm**
- **Performance CTE**
Equipment and Process Flexibility for Advanced Packaging Options

Substrate Handling
- Wafer/Panel Size
- Bow/Warp/Thickness

Cost

Chemistry
- Selectivity for Materials
- Recirculation
- Replenishment

Cleanliness
- Debond Clean
- Post Dice Clean

Process Control
- Endpoint Detection
- Profile Match For Uniformity

Equipment and Process Flexibility for Advanced Packaging Options
Chemistry Example: Wafer Thinning
Requirements for 2.5D and 3D Wafer Thinning Applications

**TSV Reveal**

- No etch of SiO2 liner or Cu TSV
- Fast Si etch rate
- Smooth surface finishing
- Good etch uniformity
- Cost effective

**Si Etch for TSV Reveal:**

- No etch of SiO2 liner or Cu TSV
- Fast Si etch rate
- Smooth surface finishing
- Good etch uniformity
- Cost effective

**FOWLP**

- Compatible with materials present in package structure such as Cu, Ti/TiW, SiO2, Si3N4, PI, and PBO
- Fast Si etch rate
- Good etch uniformity
- Cost effective

**Si Etch for FOWLP:**
Silicon Wet Etch Options

> **KOH (Potassium Hydroxide)**
  > Good etch rate and selectivity (Silicon to Oxides /Cu)
  > Ionic contamination (K+)

> **TMAH (Tetramethyl Ammonium Hydroxide)**
  > Safety concerns (toxicity) at high concentration
  > Slow etch rate

> **HF / Nitric based chemistry – “Spinetch”**
  > High etch rates but poor selectivity (Silicon to Oxides /Cu)

> **SACHEM Reveal Etch™**
  > Lower toxicity than TMAH
  > Higher etch rate and good selectivity (Silicon to Oxides /Cu)
Etch Selectivity

Ability to etch silicon and stop on a variety of materials without causing damage

* Spinetch D 1:6:2:1 HF:Nitric:Phosphoric:Sulfuric
Two-Step Etch Process Developed

> **Step 1**

» Spinetch D (HF / Nitric mixture)
  » To smooth surface and eliminate grind marks
  » Contour silicon thickness for improved uniformity

> **Step 2**

» SACHEM Reveal Etch™ (or ST2011)
  » Selective etch of silicon
    » TSV oxide liner and Cu via
  » Other materials present at end of silicon etch for FOWLP
Etch Uniformity

> Post Grind non-uniformities can have radial dependence
  » Center to edge variations

> Single wafer etch process can compensate for radial nonuniformities
  » More/Less etch in center of wafer

> Resulting Silicon wafer thickness is more uniform
Integrity of Via and Oxide Liner for TSV Reveal

- No attack of oxide liner
- No preferential attack along sidewall
FOWLP Silicon Etch Results

Strong Alklaine Etch (TMAH) caused damage to underlying RDL structure

Use of acid etch or 2 step etch process provides good results with no damage to underlying structure

“High Density TSV-Free Interposer (TFI) Packaging with Submicron Cu Damascene RDLs for Integration of CPU/GPU and HBM”
IMF presentation at ECTC 2018
Process Control: Etch and Undercut
UBM/RDL Etch and Dimensions

- Smaller bumps with increased density
- Need for less undercut and controlled etch
  » PSP WaferChek® Process Monitor for endpoint detection
- Recent demonstration on 10 and 20µm pitch bumps
UBM Etch – smaller bumps and higher density

Before Cu Etch

20µm Pitch

After Cu Seed Layer Etch

10µm Pitch
RDL Etch – Pattern Density Challenges

Isolated and Dense Features

Embedded structures
Undercut and Overetch

- Isotropic etch results in undercut equal to thickness of film if etch stopped at endpoint

- For narrow Line/Space dimensions undercut must be minimized
  - Reduce Thickness of seed layer
  - Eliminate / Reduce overetch
Process Requirements

➢ Completely etch away field metal (barrier and seed metals)
➢ Keep overetch to a minimum for bump integrity, electrical performance and throughput
➢ No substrate attack
➢ Low Cost - $/wafer processed
Undercut and Etchant Selection

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HF

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TiE-100
Quantifying the Impact of Over-Etch on WPY Under Bump Metallization (UBM) Etch Example

Undercut vs. Etch Time
(dependent on pitch and barrier metal)

Example: Over-Etch Impact on T/P

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<th>Etch Example*</th>
<th>Cu or Ti Etch</th>
<th>Production Loss</th>
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<td>Etch Time (sec)</td>
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<td>SRD Time</td>
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<td>Overall Process Time (chambers in Parallel)</td>
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<td>Handling (wafers in/ out)</td>
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<tr>
<td>Number of Chambers</td>
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Throughput (wph) with WaferChek
- Impact of 30% over-etch (wph): 22
- Impact of 100% over-etch (wph): 18

Available Production Hours: 7,862

Wafers Per Year with WaferChek
- Wafers Per Year at 30% over-etch: 174,720
- Wafers Per Year at 100% over-etch: 138,748

*Process times will vary depending on feature dimensions, barrier metals, thickness, etchant
Substrate Handling Example: Cleaning on Film Frame
Cleaning Wafers on Film Frames – post debond from carrier

Larger than 300mm wafer ~380mm

Removing residual adhesive without affecting tape film frame → combination of appropriate chemistry and physical force
Removing thick layer of adhesive without damage

PRE – as received

Immediately after processing
Cleaning post debond on film frames

- Fixturing to handle and support wafer on film frame
- Chemistry for cleaning/stripping residual and compatible with tape
- Use of physical force (high pressure spray / high velocity spray) to assist in cleaning
Summary

> No single road being followed for Advanced Packaging

> Many different types of packages depending upon application requirements

> Equipment flexibility and versatility will be needed to address
  » Substrate size and form factor
  » Shrinking dimensions
  » Materials

> Process solutions combine equipment and chemistry
Thank you