NCCAVS
CMPUG/TFUG/PAG Joint Meeting
ADVANCED PACKAGING TECHNOLOGY
Tuesday June 12, 2018

Equipment and Process Challenges for the Advanced Packaging Landscape

Veeco Precision Surface Processing

Laura Mauer

June 2018

Outline

- Advanced Packaging Market Landscape
- Packaging Concepts and Equipment Challenges
- Approaches and Examples
- Summary

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Advanced Packaging Landscape - Markets

- Smartphones
- Memory
- Connectivity
- Data centers
- Automotive
- Smart Home

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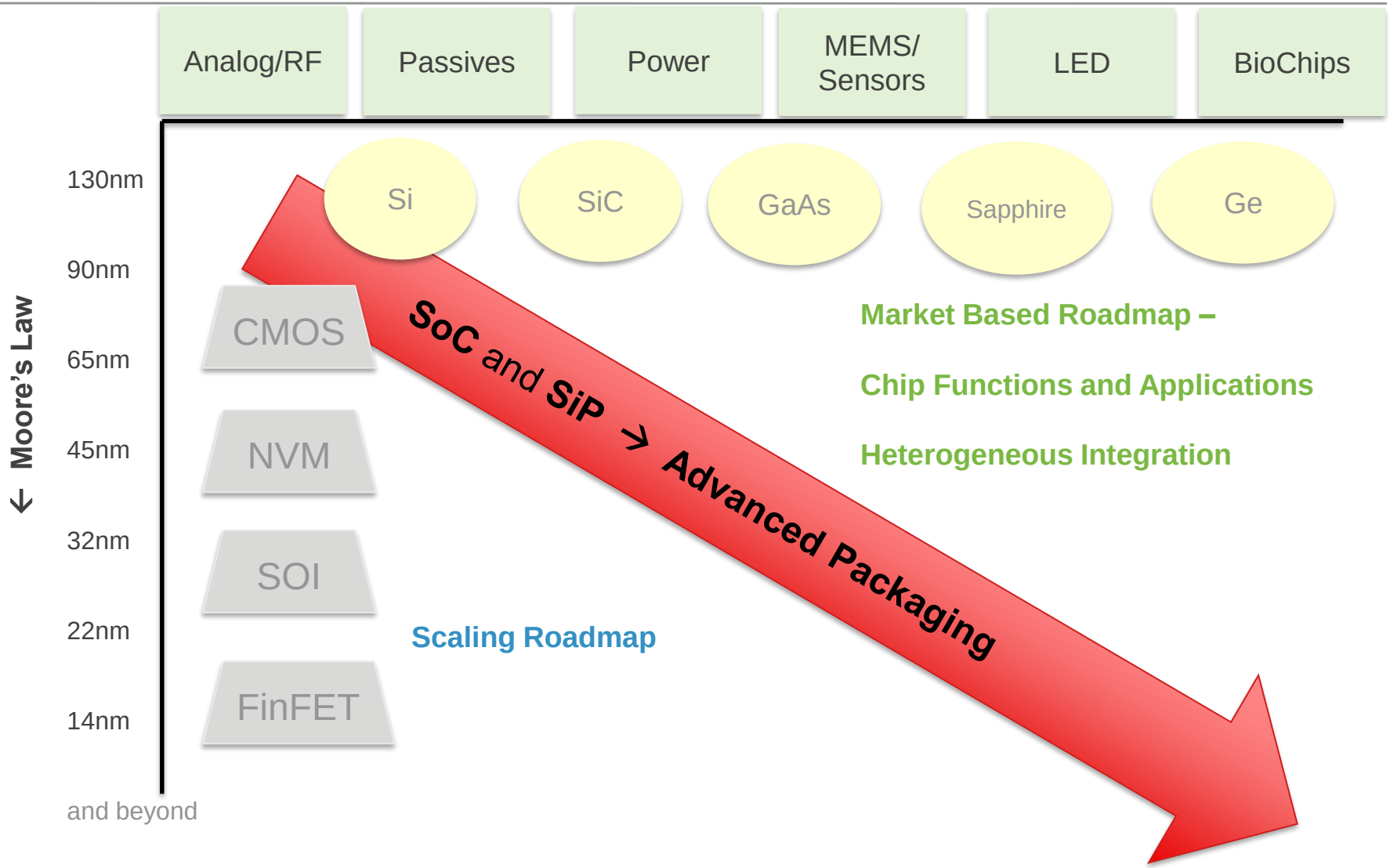
Moore's Law and More than Moore



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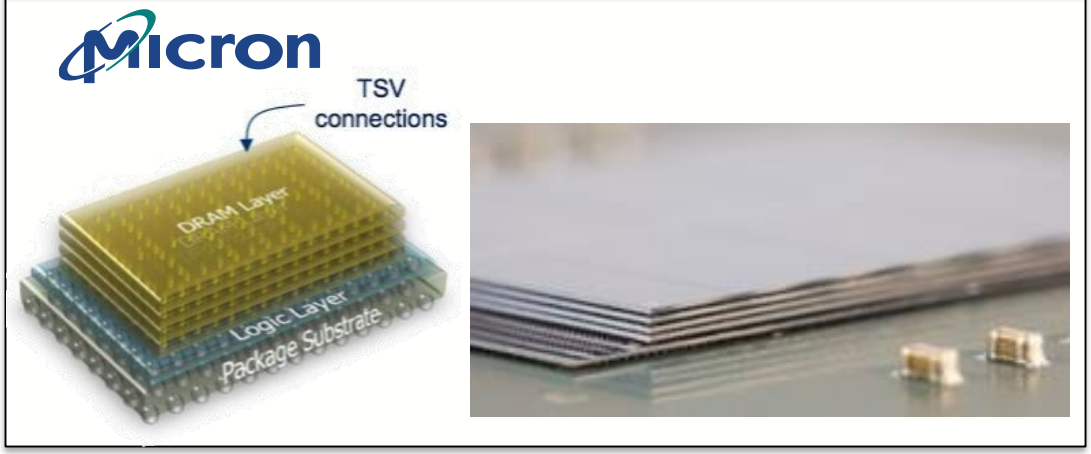
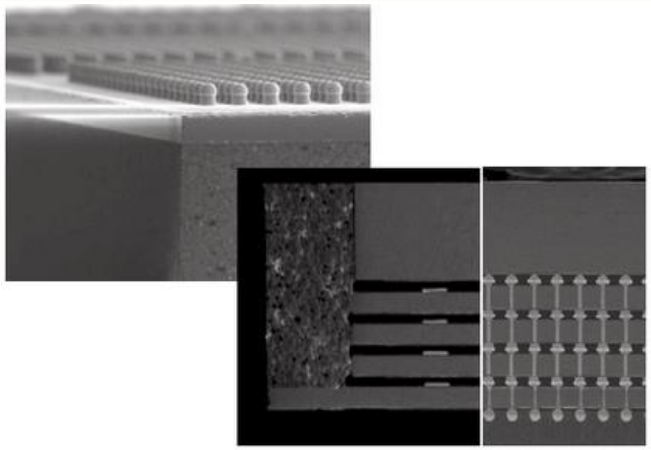
3D High Performance Devices Require TSV

Hybrid Memory Cube (HMC)

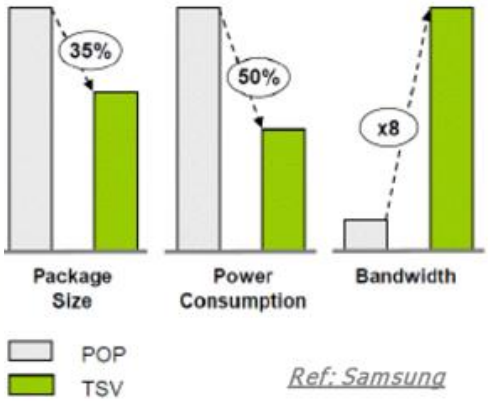


High Bandwidth Memory (HBM)



1GB HBM up to 128GB/s(@1.2V, x1024)

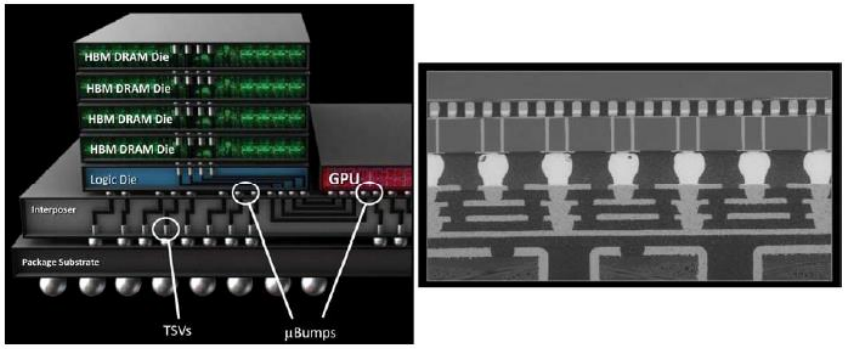
SK hynix



Ref: Samsung

High End Graphics

Figure 2.1. AMD's Fiji with silicon interposer and HBM.



Source: AMD.

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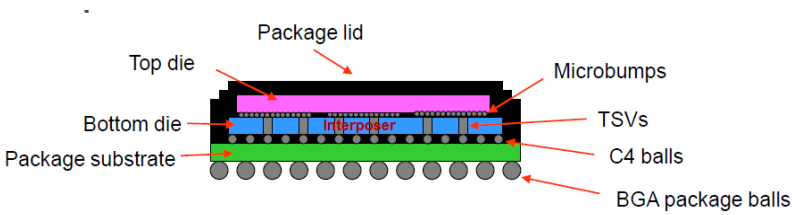
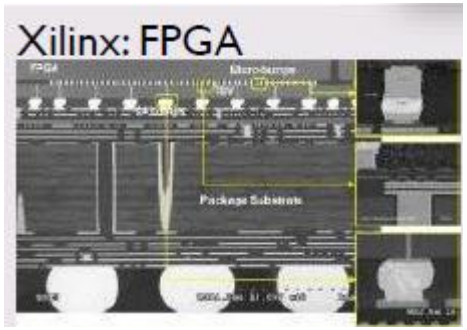
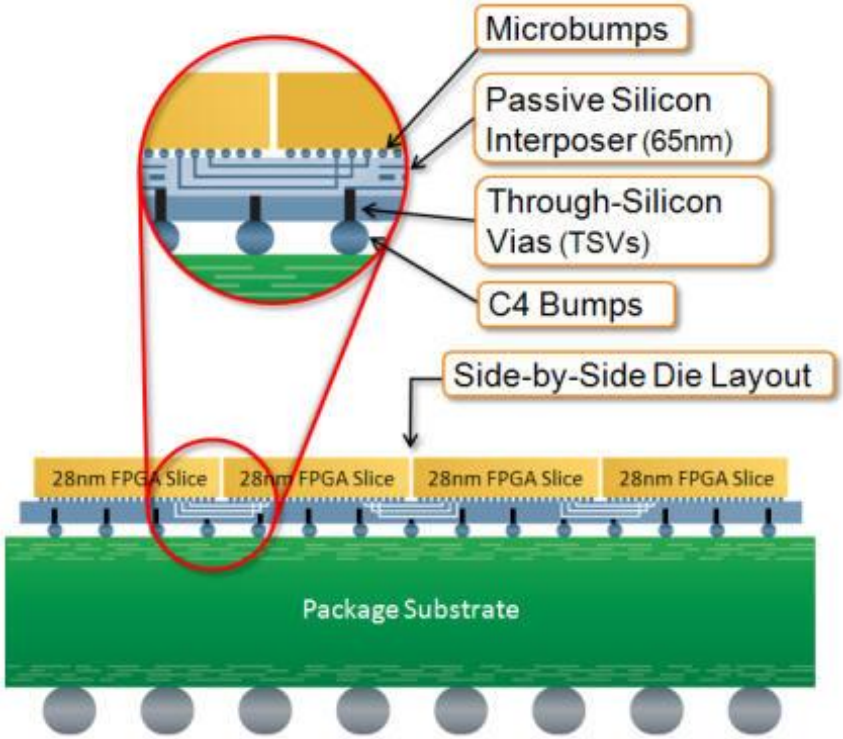
2.5D Interposers for Heterogeneous Integration

A configuration where dies are mounted side by side on one side of a thin (~ 100 um) silicon, glass, or organic interposer using through *silicon* vias (TSV), through *glass* vias (TGV) or through *organic* vias (TOV), respectively through the interposer to connect the dies with the package substrate.







Xiinx's Virtex 7 FPGA

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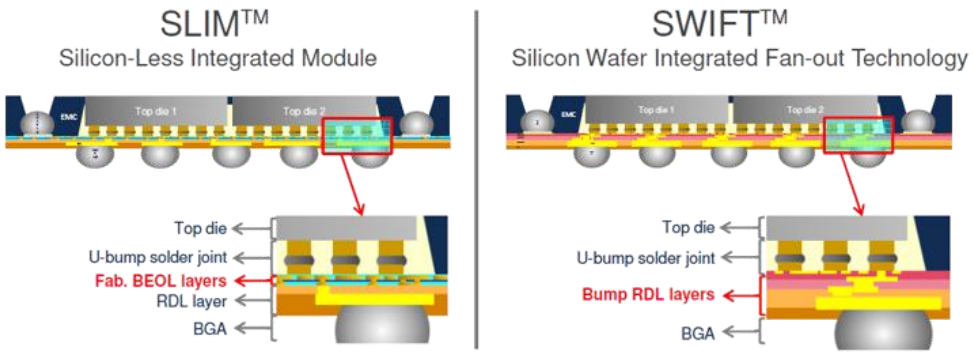
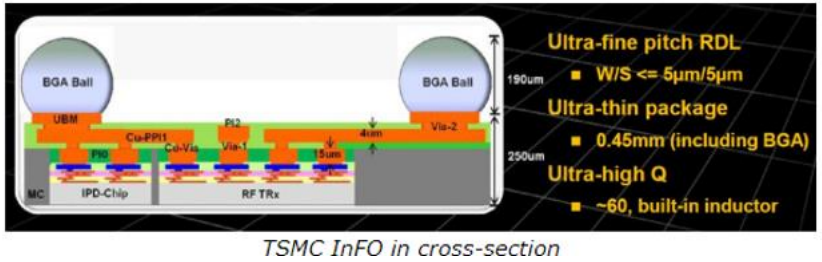
Other Technologies for Heterogeneous Integration

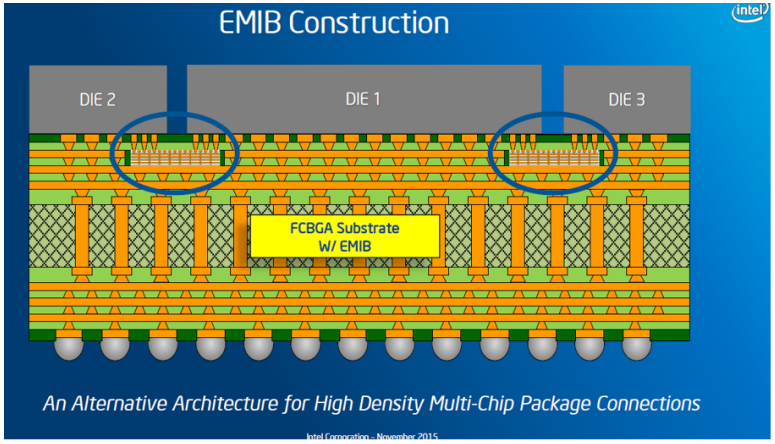


Amkor



TSMC InFO in cross-section

TSMC



Intel

Source: ASE.

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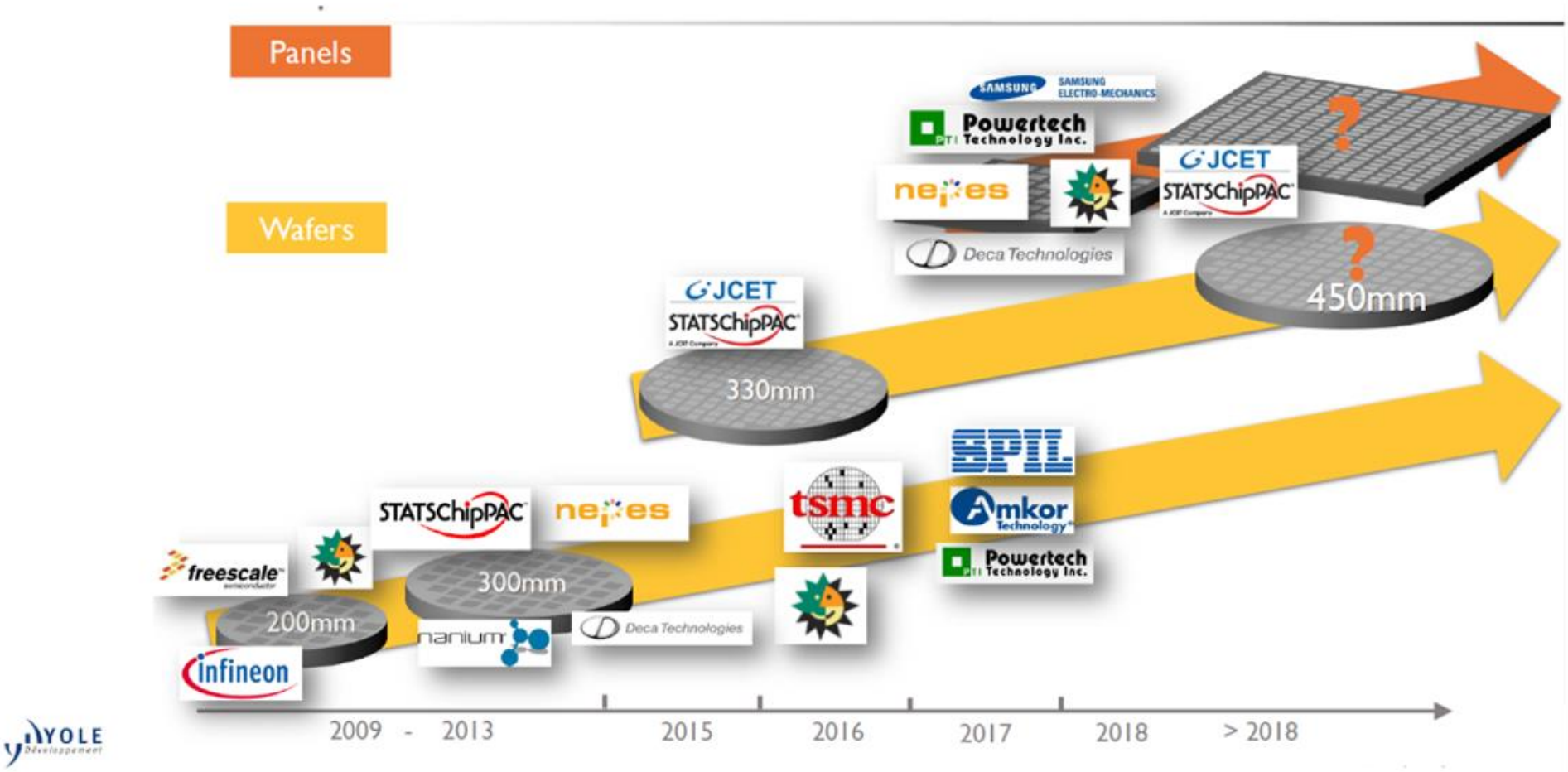
Wafers / Panels / Sizes for Advanced Packaging



Source: Yole

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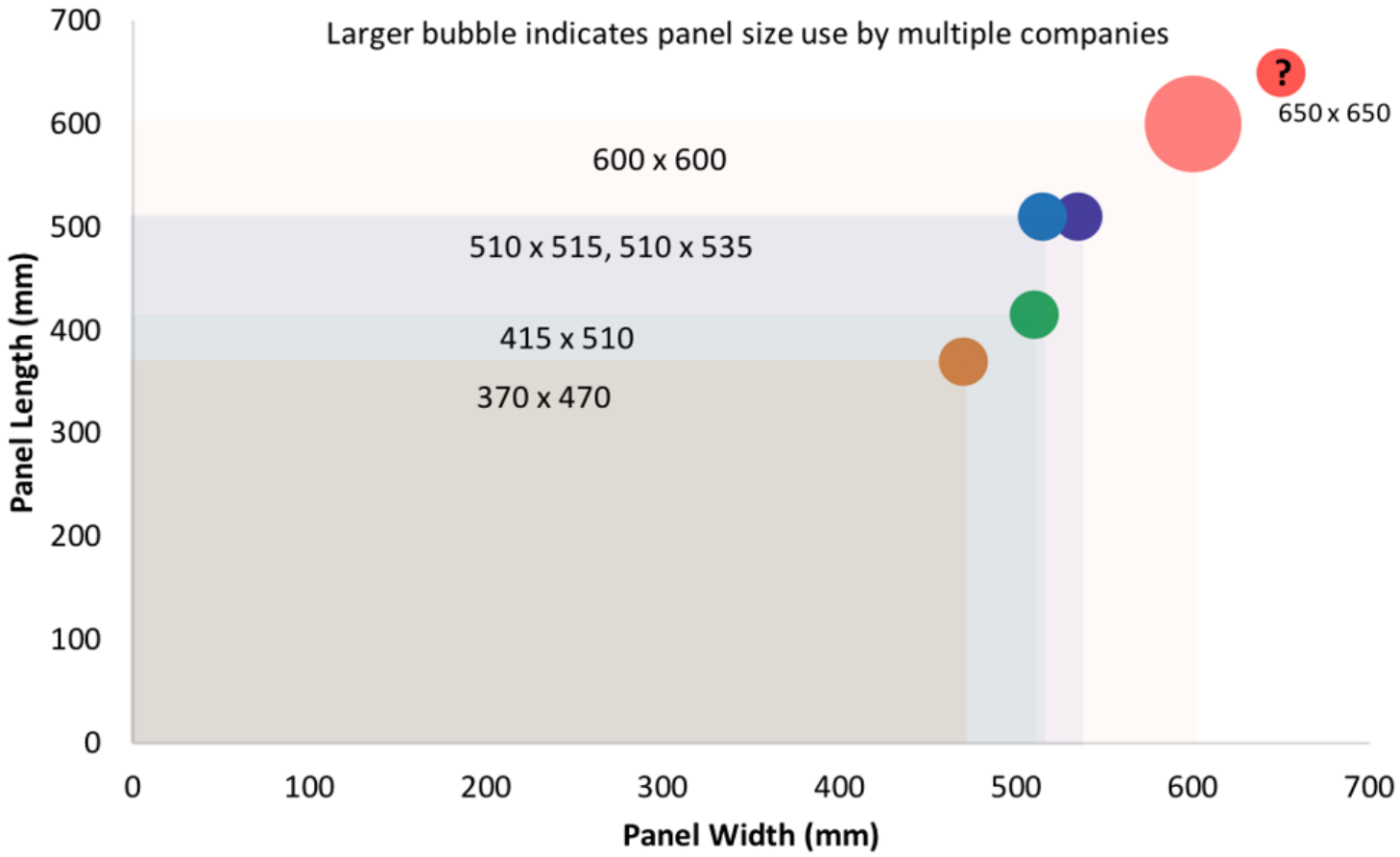
Panel Size Uncertainty for Large Area Fan-Out



Source: TechSearch International

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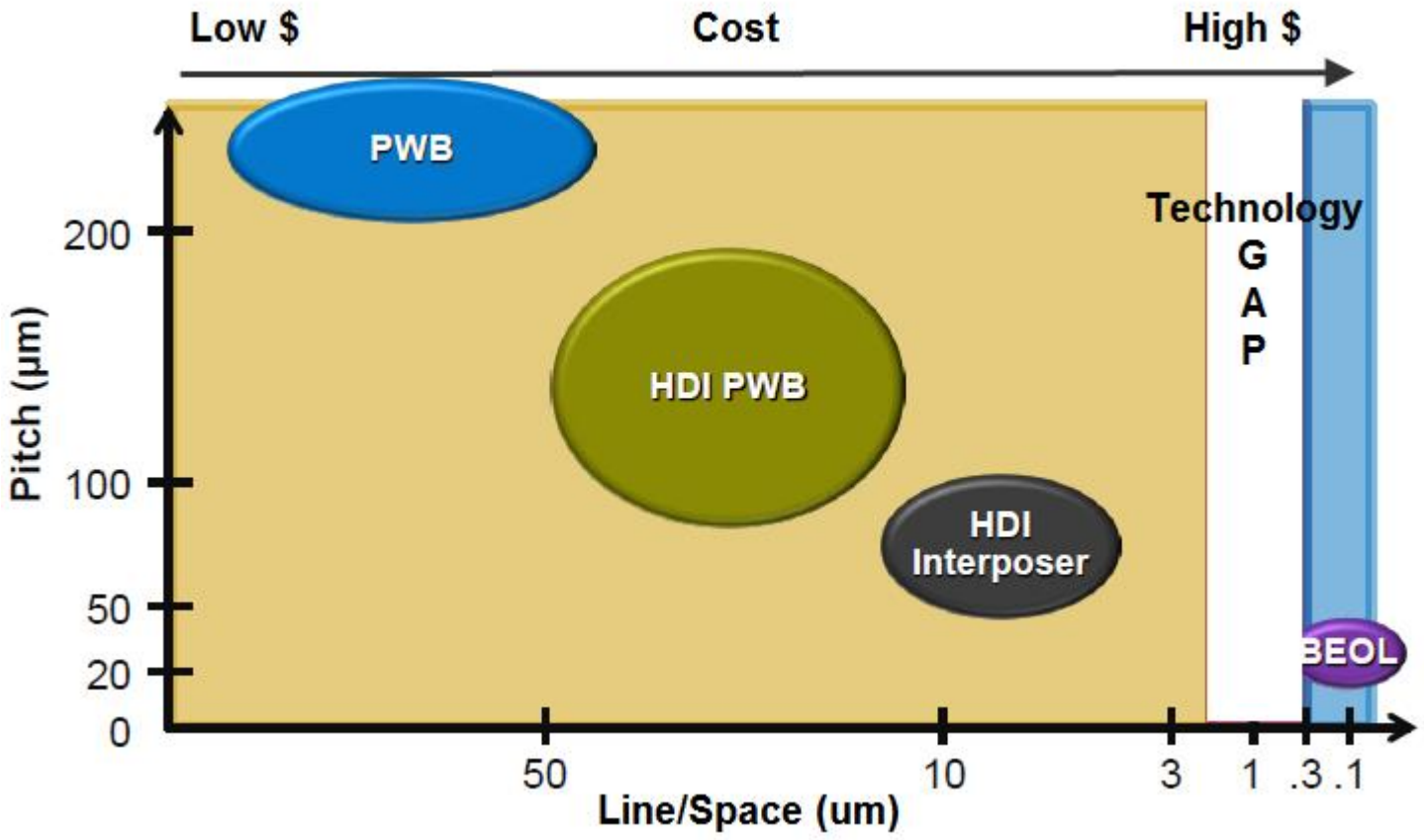
Dimensions and Cost



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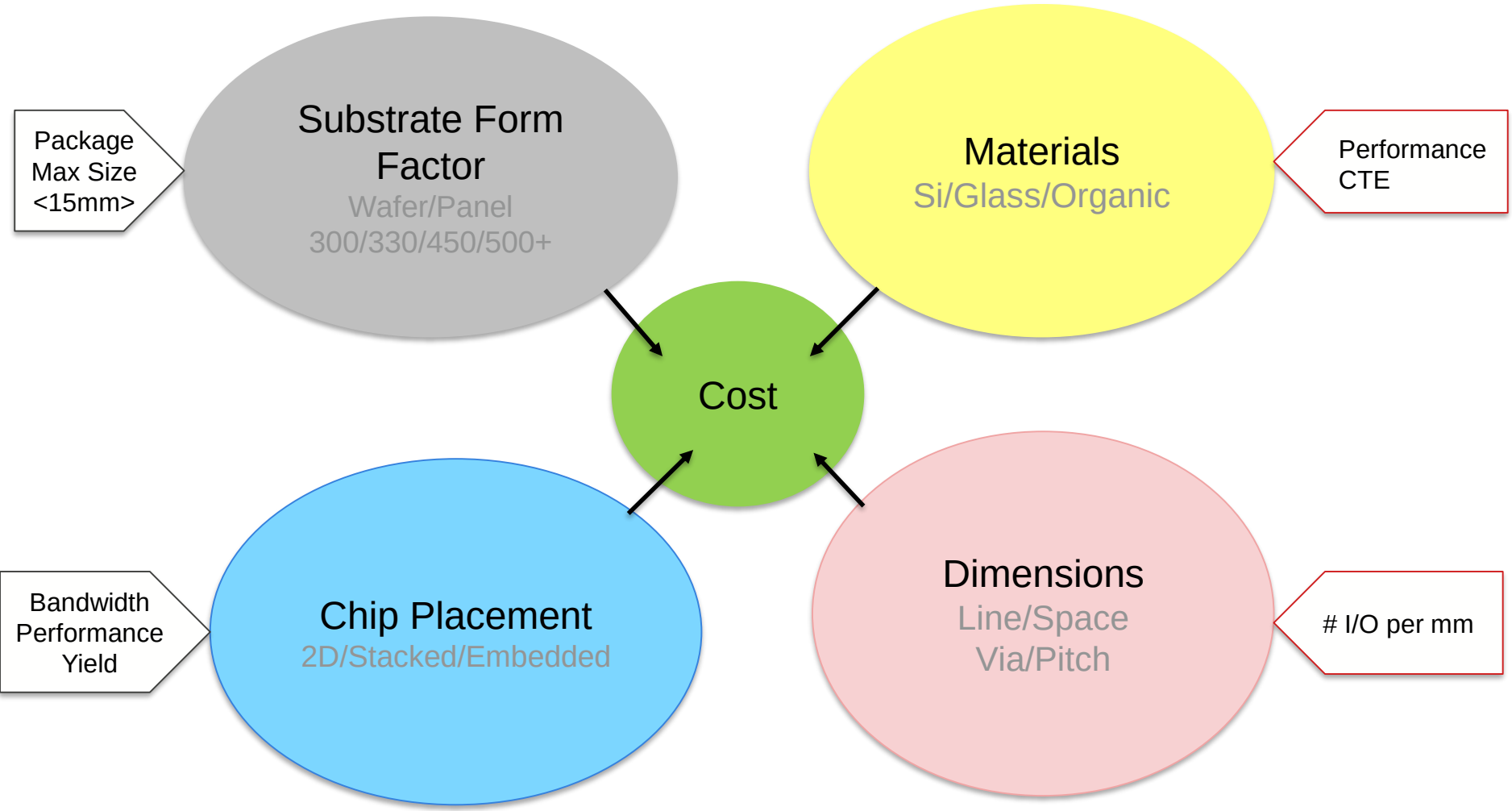
Advanced Packaging Options



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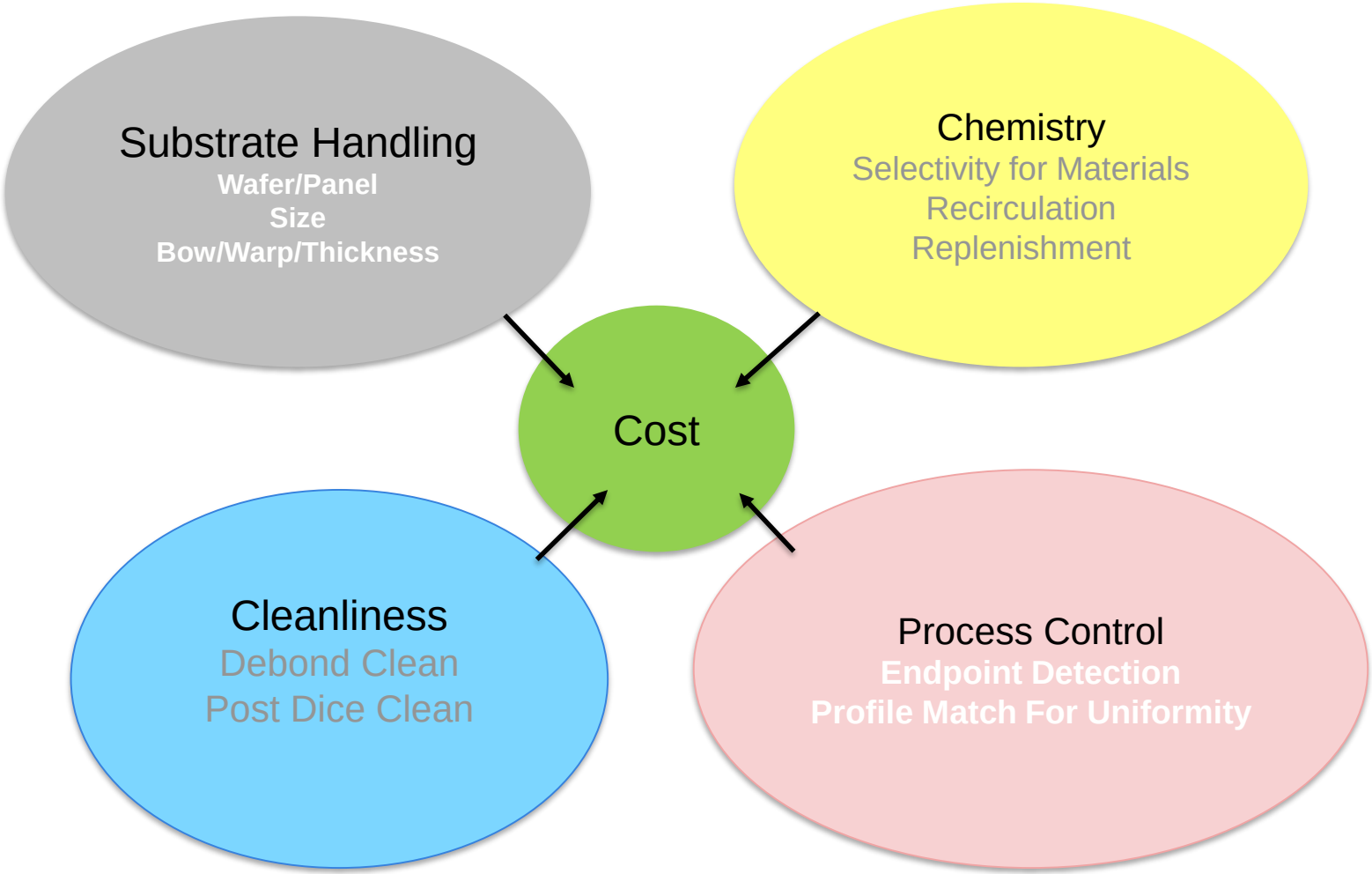
Equipment and Process Flexibility for Advanced Packaging Options



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Chemistry Example: Wafer Thinning

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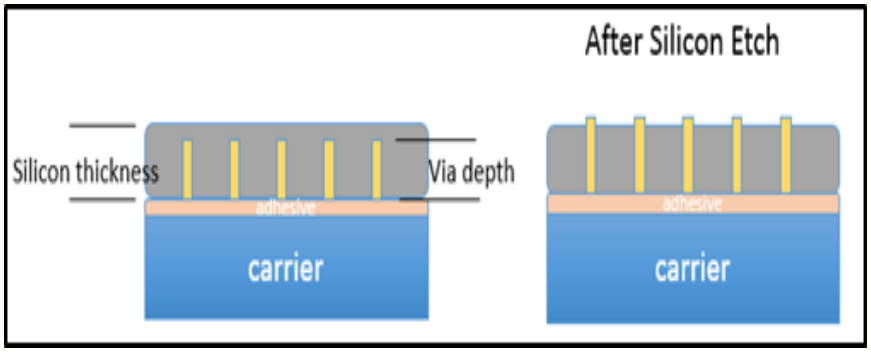
Requirements for 2.5D and 3D Wafer Thinning Applications

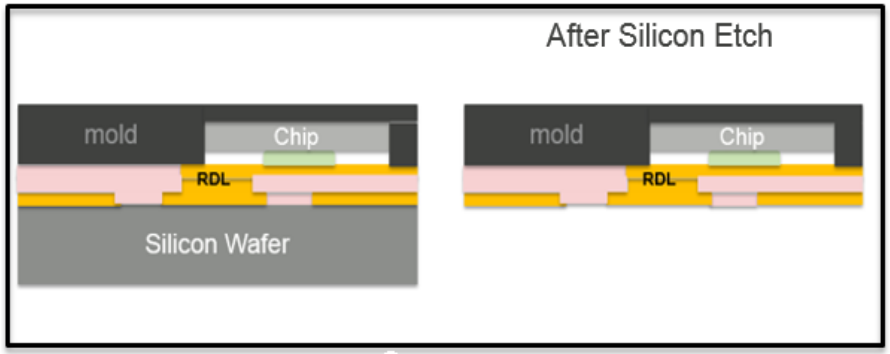
TSV Reveal



Si Etch for TSV Reveal:

- No etch of SiO2 liner or Cu TSV
- Fast Si etch rate
- Smooth surface finishing
- Good etch uniformity
- Cost effective

FOWLP



Si Etch for FOWLP:

- Compatible with materials present in package structure such as Cu, Ti/TiW, SiO2, Si3N4, PI, and PBO
- Fast Si etch rate
- Good etch uniformity
- Cost effective

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Silicon Wet Etch Options

- KOH (Potassium Hydroxide)
  - Good etch rate and selectivity (Silicon to Oxides /Cu)
  - Ionic contamination (K+)
- TMAH (Tetramethyl Ammonium Hydroxide)
  - Safety concerns (toxicity) at high concentration
  - Slow etch rate
- HF / Nitric based chemistry – “Spinetch”
  - High etch rates but poor selectivity (Silicon to Oxides /Cu)
- SACHEM Reveal Etch™
  - Lower toxicity than TMAH
  - Higher etch rate and good selectivity (Silicon to Oxides /Cu)

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Etch Selectivity

- Ability to etch silicon and stop on a variety of materials without causing damage

HF/Nitric Mixture*		
Material	Etch Rate (nm/min)	Selectivity to Silicon
Si	9000	
SiO2	50	180
Si3N4	2.7	3333
Cu	2400	3.8
Ti	750	12
TiW	144	63
PI	0	>10000
PBO	0	>10000

SACHEM Reveal Etch™		
Material	Etch Rate (nm/min)	Selectivity to Silicon
Si	711	
SiO2	0.5	1422
Si3N4	0	> 10000
Cu	12	59
Ti	0	>10000
TiW	1.9	374
PI	5.6	95
PBO	7.5	126

SACHEM ST2011		
Material	Etch Rate (nm/min)	Selectivity to Silicon
Si	150	
SiO2	0.5	300
Si3N4	0	>10000
Cu	0	>10000
Ti	0	>10000
TiW	0	>10000
PI	0	>10000
PBO	0	>10000

* Spinetch D 1:6:2:1 HF:Nitric:Phosphoric:Sulfuric

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Two-Step Etch Process Developed

- Step 1
  - Spinetch D (HF / Nitric mixture)
    - To smooth surface and eliminate grind marks
    - Contour silicon thickness for improved uniformity
- Step 2
  - SACHEM Reveal Etch™ (or ST2011)
    - Selective etch of silicon
      - TSV oxide liner and Cu via
      - Other materials present at end of silicon etch for FOWLP

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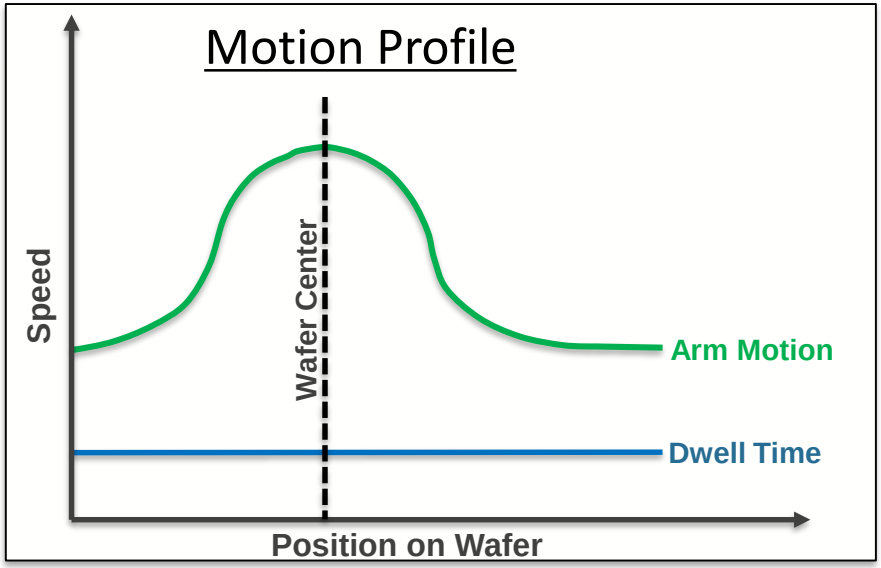
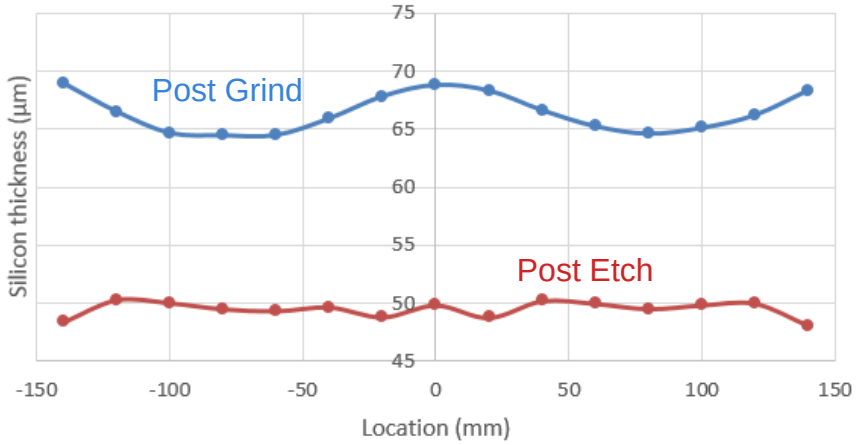
Etch Uniformity

- **Post Grind non-uniformities can have radial dependence**
  - Center to edge variations
- **Single wafer etch process can compensate for radial nonuniformities**
  - More/Less etch in center of wafer
- **Resulting Silicon wafer thickness is more uniform**





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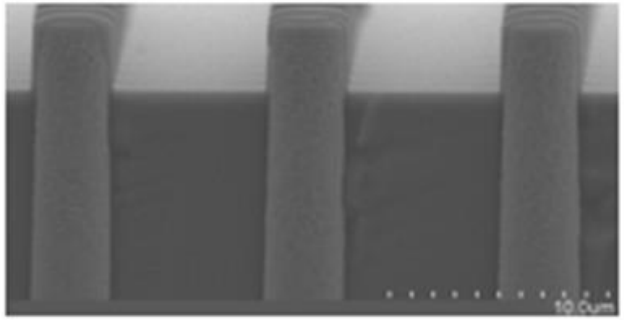
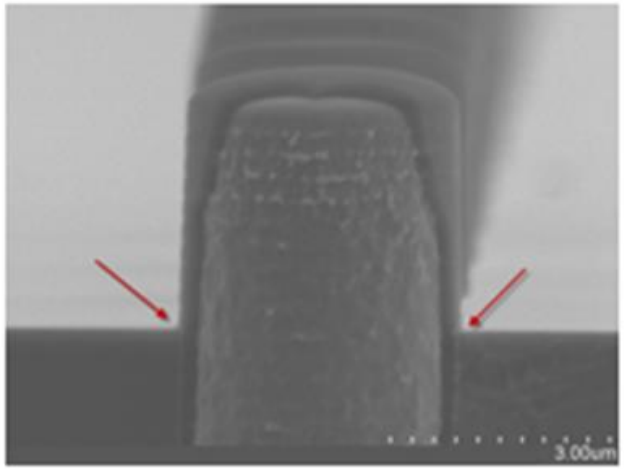
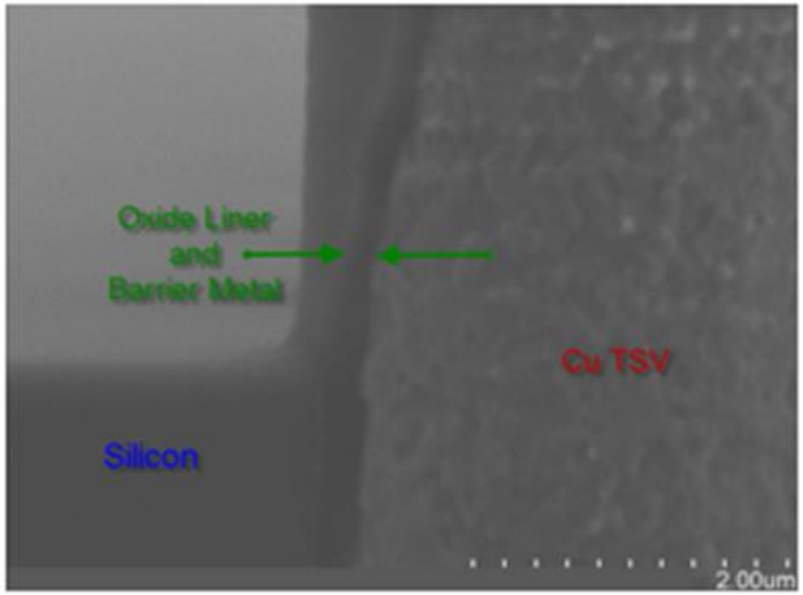
Integrity of Via and Oxide Liner for TSV Reveal







- No attack of oxide liner
- No preferential attack along sidewall

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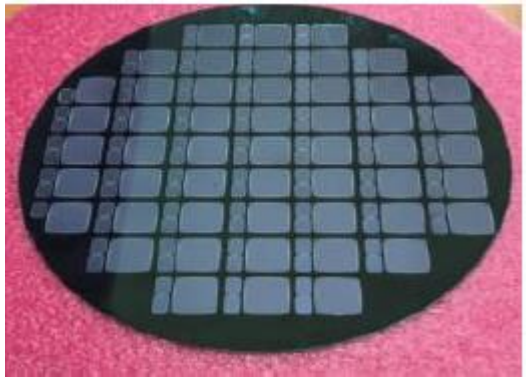
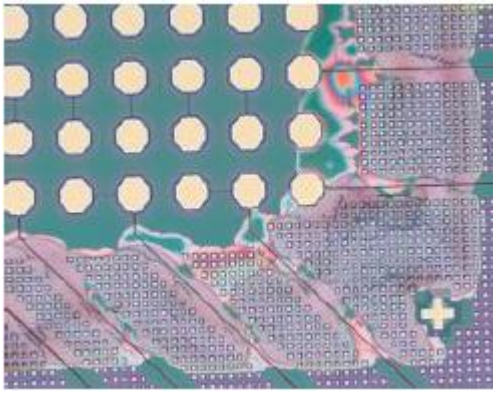
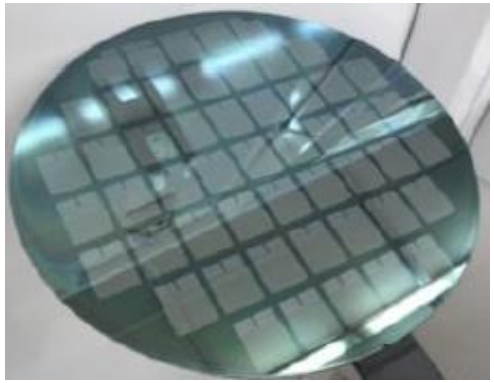
FOWLP Silicon Etch Results

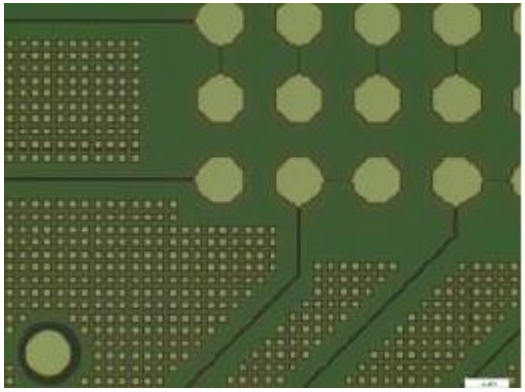
Strong Alklaine Etch (TMAH) caused damage to underlying RDL structure





Use of acid etch or 2 step etch process provides good results with no damage to underlying structure





"High Density TSV-Free Interposer (TFI) Packaging with Submicron Cu Damascene RDLs for Integration of CPU/GPU and HBM" IME presentation at ECTC 2018

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Process Control: Etch and Undercut

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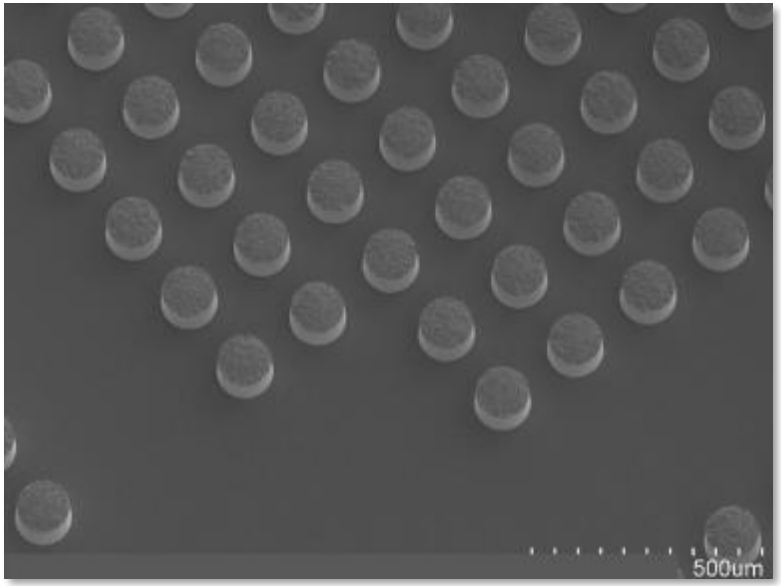
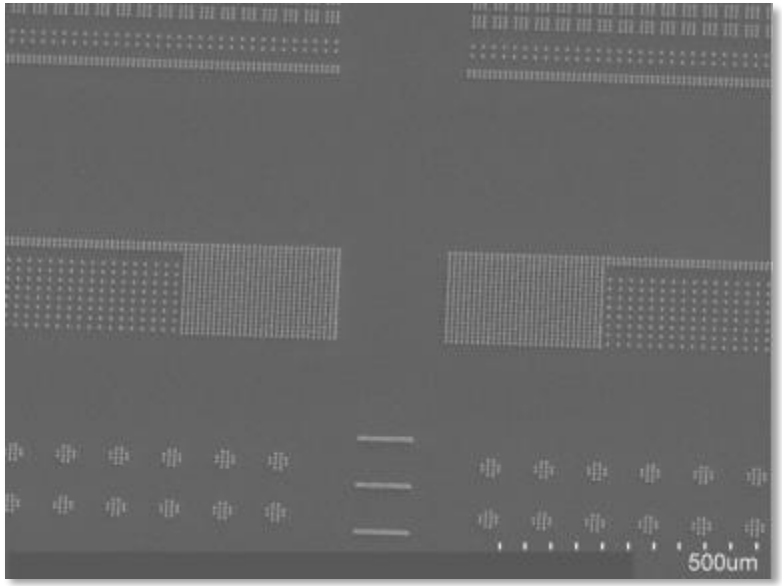
UBM/RDL Etch and Dimensions

- **Smaller bumps with increased density**
- **Need for less undercut and controlled etch**
  - PSP WaferChek® Process Monitor for endpoint detection
- **Recent demonstration on 10 and 20µm pitch bumps**



Current Products



Future

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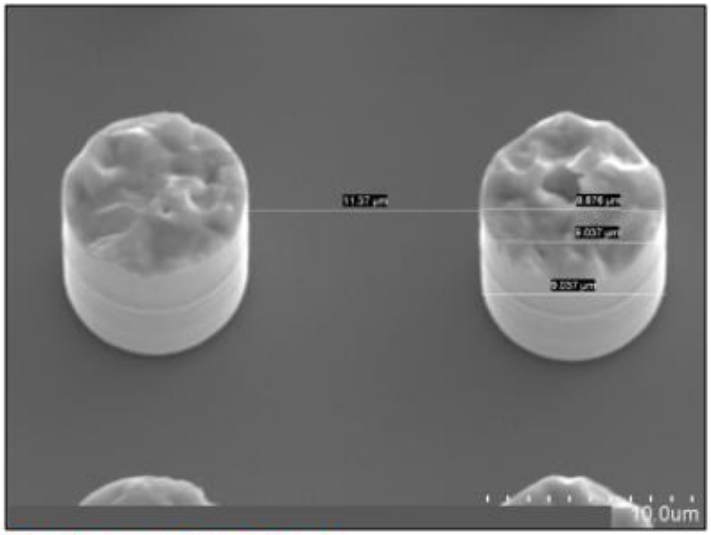
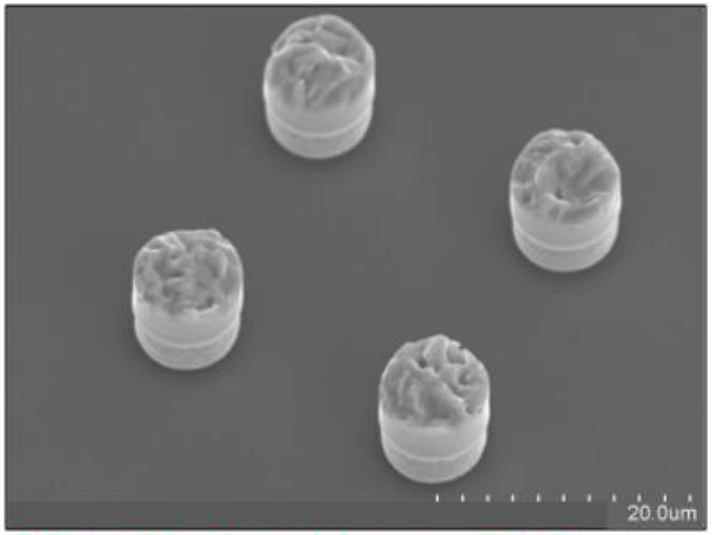
UBM Etch – smaller bumps and higher density

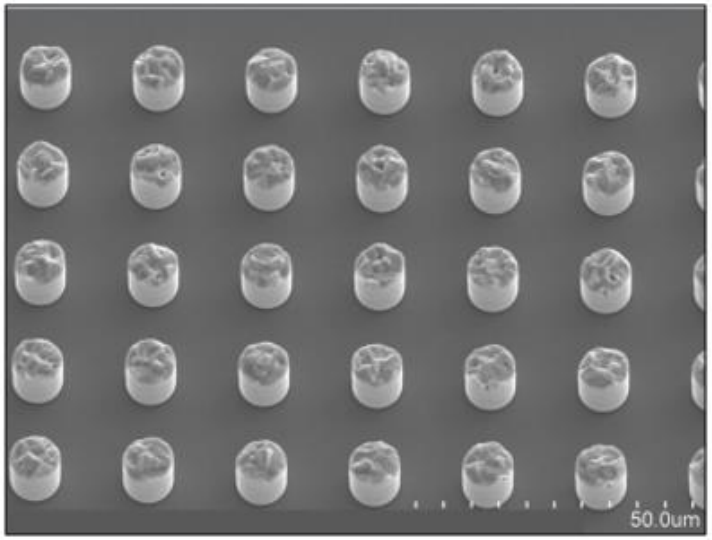


Before Cu Etch

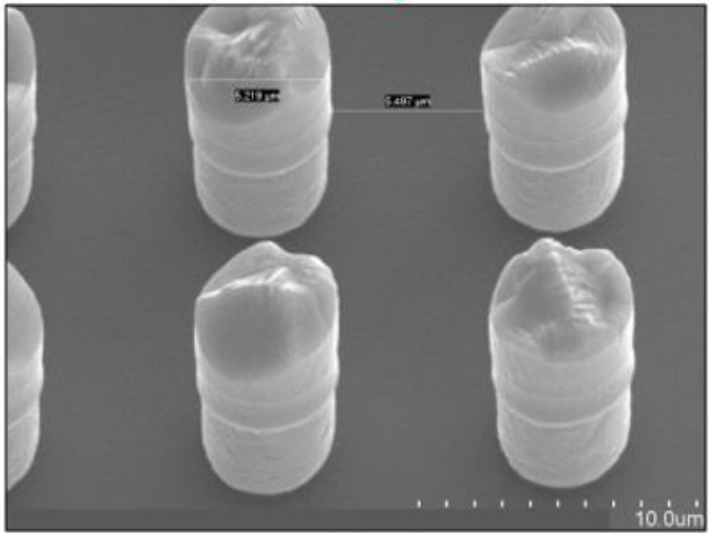
20µm Pitch



After Cu Seed Layer Etch



10µm Pitch



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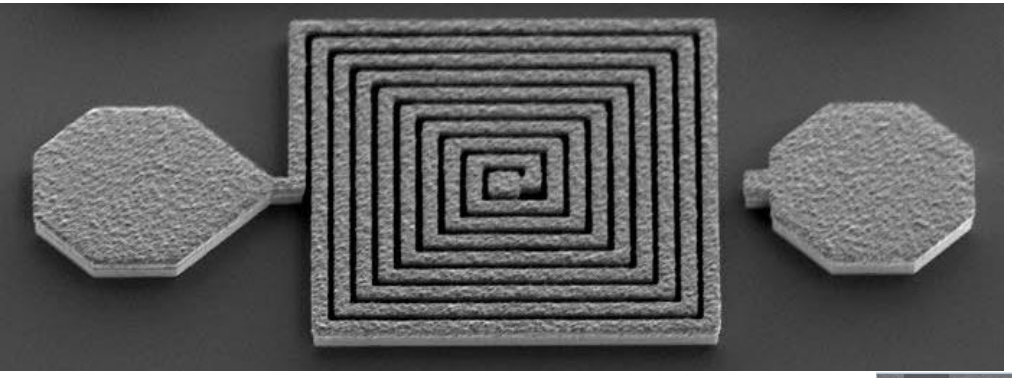
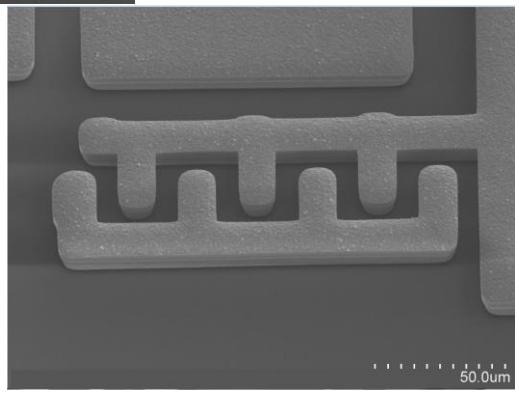
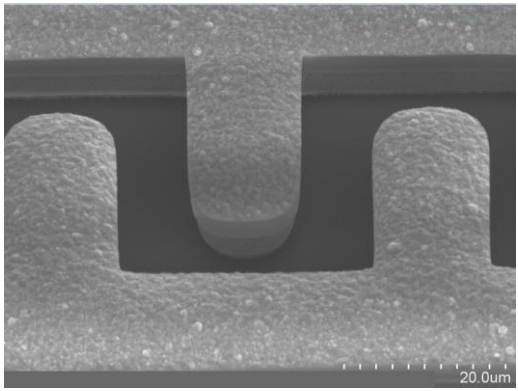
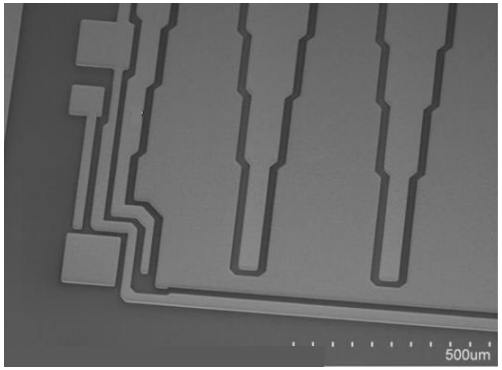
RDL Etch – Pattern Density Challenges

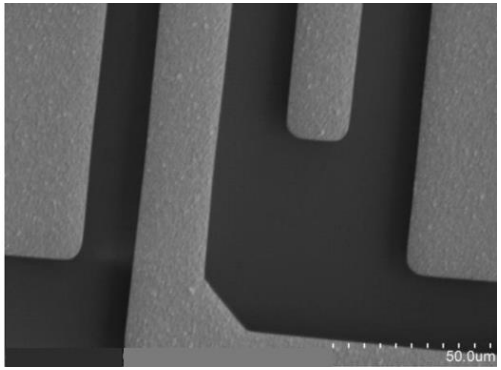


Isolated and Dense Features









Embedded structures

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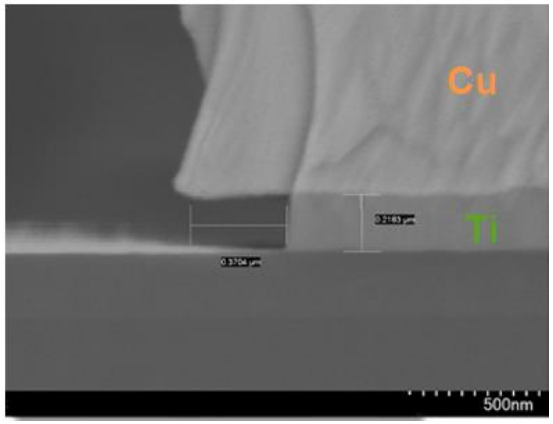
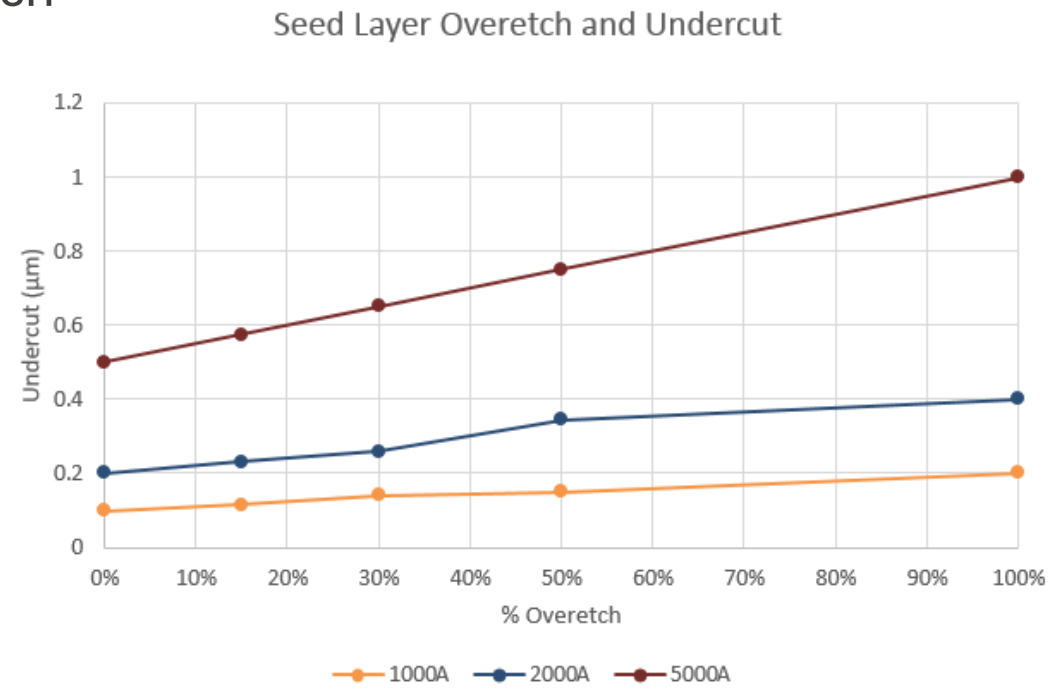
Undercut and Overetch

- Isotropic etch results in undercut equal to thickness of film if etch stopped at endpoint
- For narrow Line/Space dimensions undercut must be minimized
  - Reduce Thickness of seed layer
  - Eliminate / Reduce overetch





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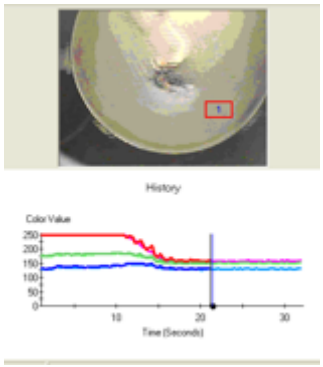
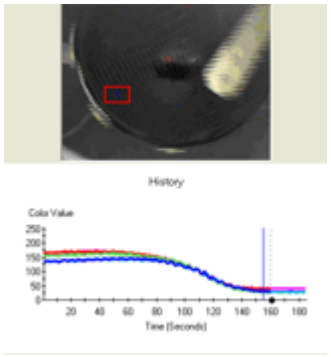
WaferChek® In-Situ Process Control for Endpoint Detection

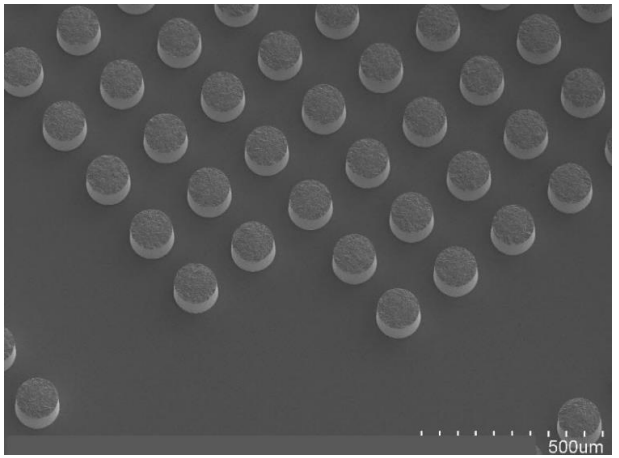
UBM Etch : Cu Over TiW



Cu Etch

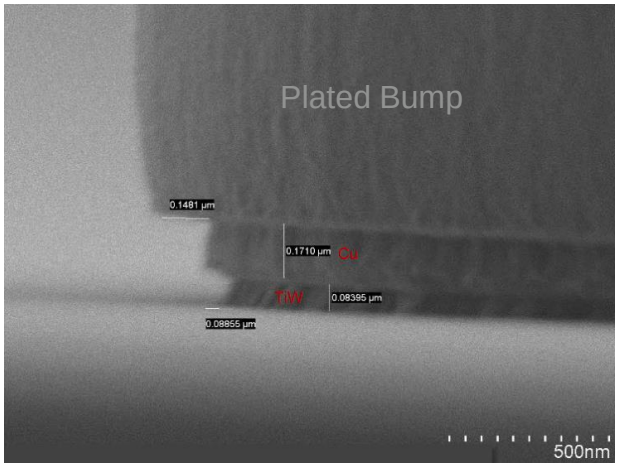


TiW Etch



Process Requirements

- Completely etch away field metal (barrier and seed metals)
- Keep overetch to a minimum for bump integrity, electrical performance and throughput
- No substrate attack
- Low Cost - $/wafer processed



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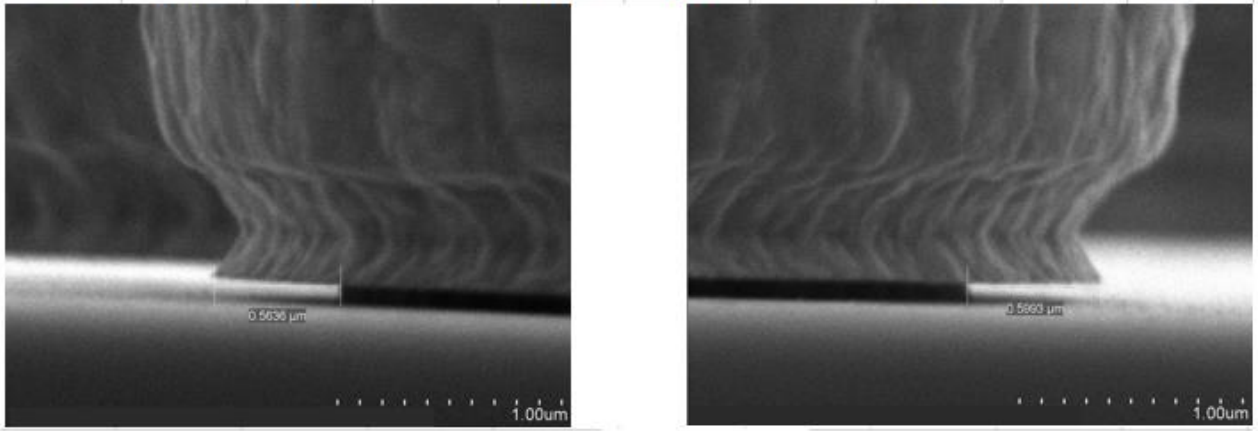
Undercut and Etchant Selection

HF

Ti undercut - HF Etched

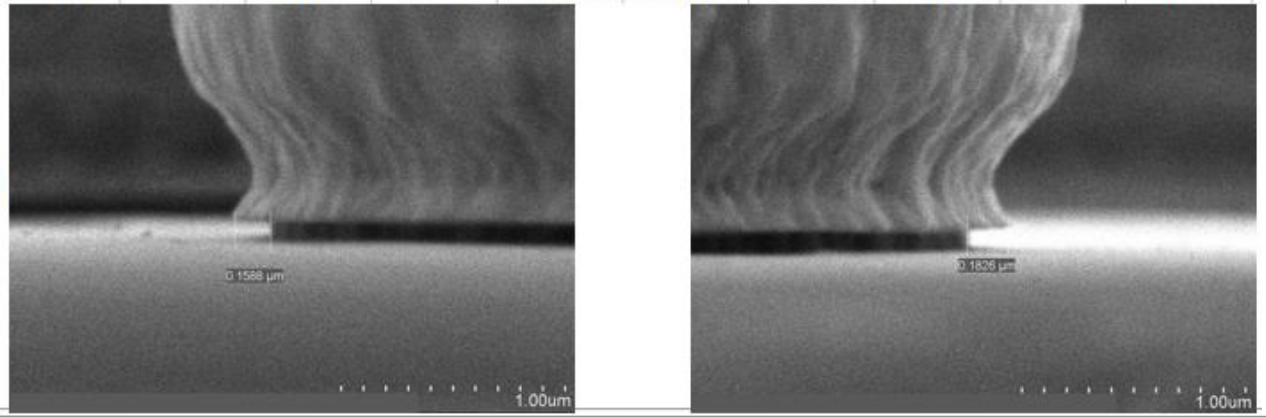
1		2		3		4		5	
center L	center R	left	right	mid left	mid right	left	right	edge left	edge right
0.56	0.59	0.59	0.59	0.59	0.61	0.60	0.57	0.50	0.55



TiE-100

Ti undercut - TiE-100 Etchant

1		2		3		4		5	
center L	center R	left	right	mid left	mid right	left	right	edge left	edge right
0.17	0.18	0.17	0.16	0.16	0.17	0.16	0.16	0.16	0.15



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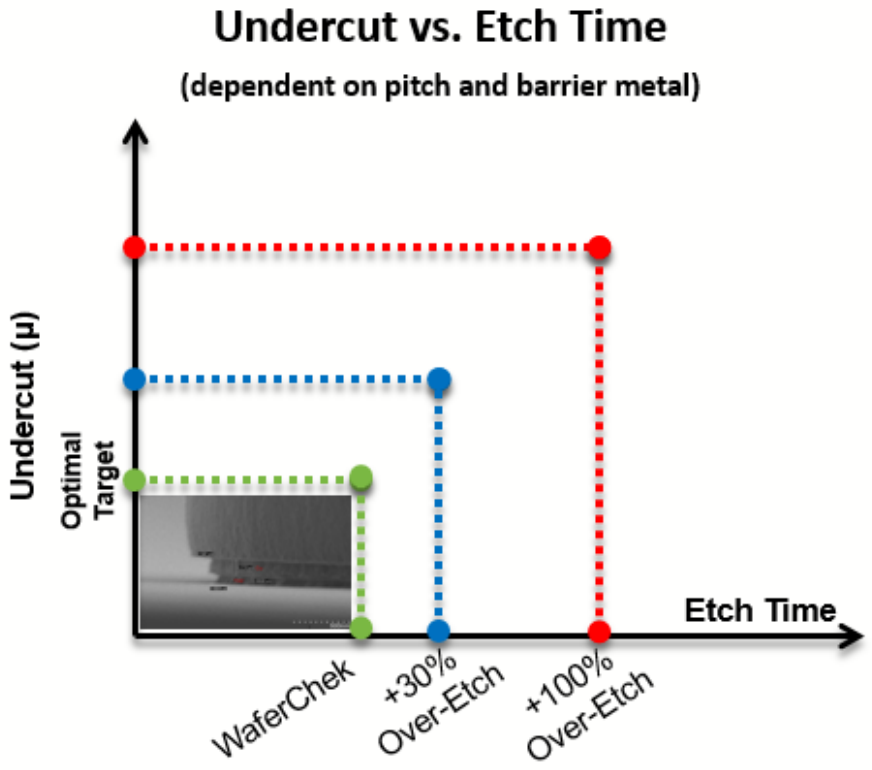
Quantifying the Impact of Over-Etch on WPY

Under Bump Metallization (UBM) Etch Example



Example: Over-Etch Impact on T/P

Etch Example*	Cu or Ti Etch	Production Loss
Etch Time (sec)	60	
SRD Time	60	
Overall Process Time (chambers in Parallel)	**120**	
Handling (wafers in/ out)	24	
Number of Chambers	1	
Throughput (wph) with WaferChek	**25**	**Baseline**
Impact of 30% over-etch (wph)	22	11%
Impact of 100% over-etch (wph)	18	29%
Available Production Hours	7,862	
Wafers Per Year with WaferChek	**196,560**	**Baseline**
Wafers Per Year at 30% over-etch	174,720	11%
Wafers Per Year at 100% over-etch	138,748	29%

**** Process times will vary depending on feature dimensions, barrier metals, thickness, etchant***

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Substrate Handling Example: Cleaning on Film Frame

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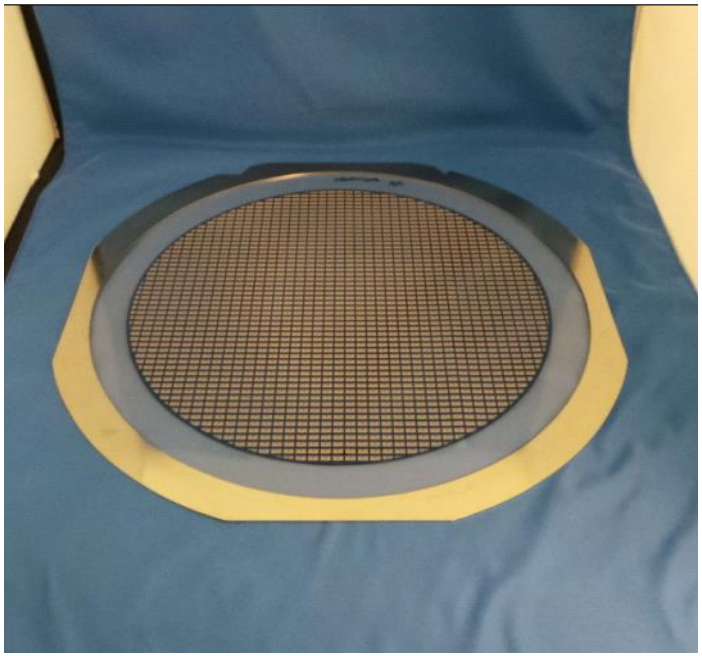
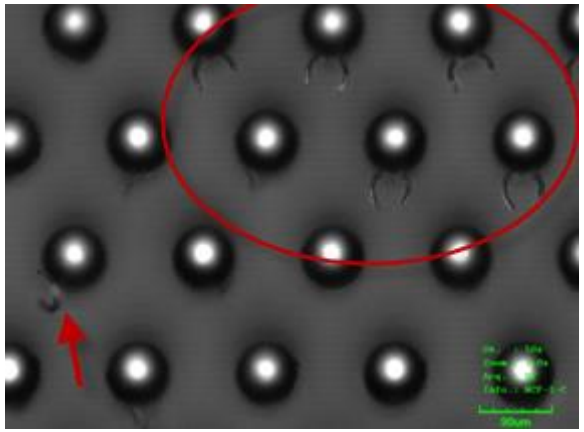
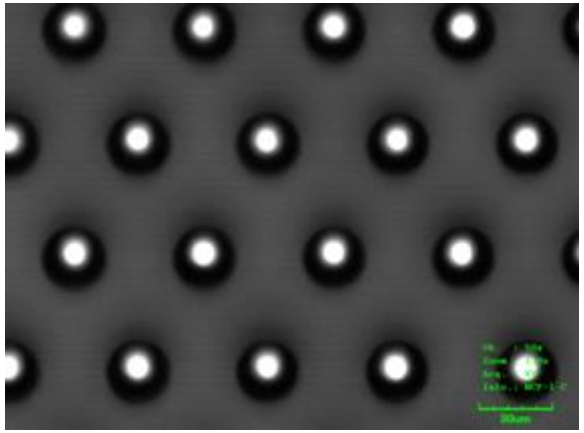
Cleaning Wafers on Film Frames – post debond from carrier







Larger than 300mm wafer ~380mm

Removing residual adhesive without affecting tape film frame
→ combination of appropriate chemistry and physical force

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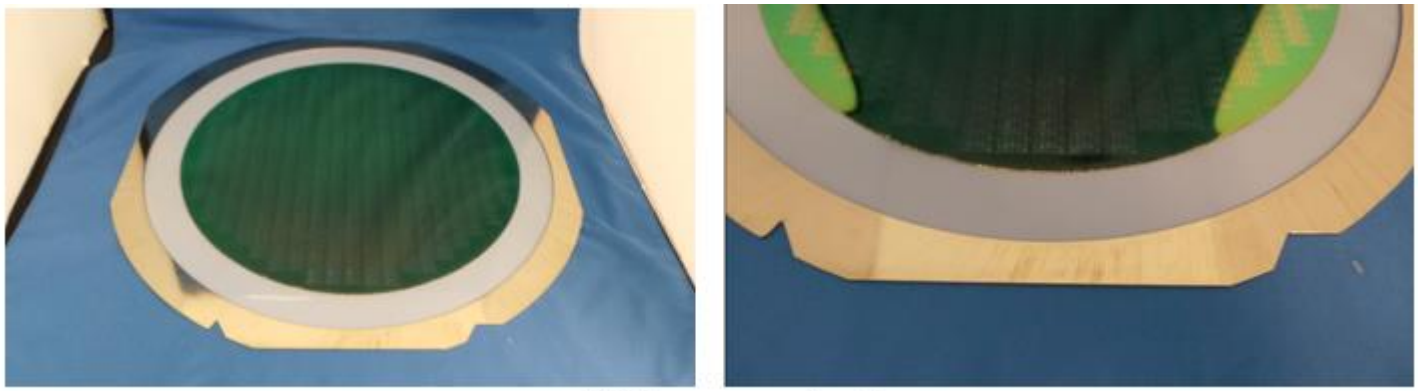
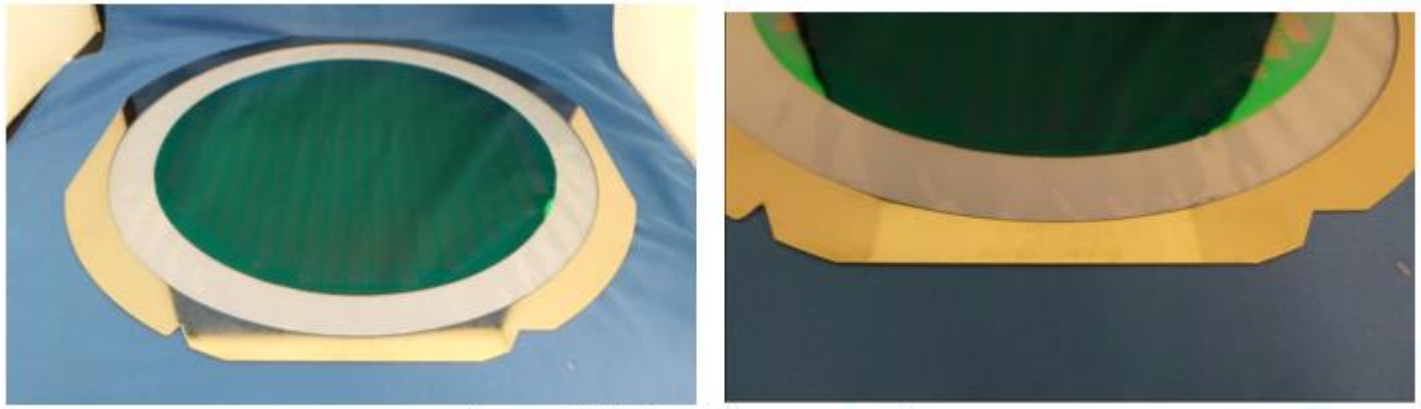
Removing thick layer of adhesive without damage



PRE – as received



Immediately after processing

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Cleaning post debond on film frames

- Fixturing to handle and support wafer on film frame
- Chemistry for cleaning/stripping residual and compatible with tape
- Use of physical force (high pressure spray / high velocity spray) to assist in cleaning

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Summary

- No single road being followed for Advanced Packaging
- Many different types of packages depending upon application requirements
- Equipment flexibility and versatility will be needed to address
  - Substrate size and form factor
  - Shrinking dimensions
  - Materials
- Process solutions combine equipment and chemistry

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Thank you

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