BEOL Interconnect Innovations for Improving Performance

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Market Needs Drive Requirements and Technology Innovations

- Power, performance, cost/area (PPA) are driving our industry
- Customers demand the highest performing processors

Power | Performance | Cost/Area
--- | --- | ---
Android | Navigation | 32nm HKMG
| Imaging | 28nm HKMG
| Video | 20nm HKMG
| | 14nm FinFET

Slide from Paul Besser, Semicon Korea 2014
Innovations in Silicon Manufacturing

New materials enable innovation by
- Improving performance,
- Enabling dimensional scaling, and
- Improving reliability

Slide from Paul Besser, Semicon Korea 2014
MOL and BEOL Materials Innovations Roadmap

- Improving performance (data access speed, battery life, etc.) is much more than just shrinking the dimensions of the processor.
- Novel materials innovations drive contact and BEOL RC improvement (reduction).
  - $\text{RC Delay} \propto \text{Resistance} \times \text{Capacitance}$
# BEOL — How Important Are Resistance and Capacitance?

<table>
<thead>
<tr>
<th>Technology</th>
<th>14nm</th>
<th>10nm</th>
<th>7nm</th>
<th>5nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{CONTACT}}$ + EPI, per side</td>
<td>Ω-μm</td>
<td>Ω-μm</td>
<td>Ω-μm</td>
<td>Ω-μm</td>
</tr>
<tr>
<td>Back end R</td>
<td>aF/μm</td>
<td>aF/μm</td>
<td>aF/μm</td>
<td>aF/μm</td>
</tr>
<tr>
<td>Back end C</td>
<td>aF/μm</td>
<td>aF/μm</td>
<td>aF/μm</td>
<td>aF/μm</td>
</tr>
</tbody>
</table>

- **Key issue at 5 nm:** non-scaling parasitics
  - Line Rs dominates but at 5 nm
  - Via Rs will affect design
  - More power is required when design adds a buffer to compensate for R

- Unidirectional patterning has made via Rs more critical since it requires routing changes; standard cell routes must go through multiple vias

- Back-end interconnect resistance will dominate product performance at 5nm
- BEOL capacitance scaling slows, beyond 10nm

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*Greg Yeric, ARM (IEDM 2014)*

*James Hsueh-Chung Chen (IITC 2014)*

*February 23, 2017*  
*Paul Besser, NCCAVS Symposium in San Jose, CA*

*Besser, ECS Prime, October 2016*
BEOL RC Reduction Innovations for Future Generations

- **How to reduce C**
  - New lower K dielectrics, even dielectric replacement
  - Air gaps
  - Lower K ESL

- **How to reduce R**
  - New metals
  - Reduce barrier thickness
  - Reduce barrier metal resistivity

RC Delay $\propto$ Resistance x Capacitance
Capacitance Reduction Opportunities
Challenges with Lowering Capacitance

• Capacitance (C) can be reduced by lowering the dielectric constant (k) of the material, but at a cost!
  • Dielectric constant is lowered by changing the chemical composition of the dielectric or by introducing porosity (pULK)**
  • $k \rightarrow$ elastic modulus ($E$) $\rightarrow$ reliability, integration, and packaging issues
• Process-induced damage to trench sidewall and top interface is a major integration challenge**
  • Higher K, moisture uptake, increased capacitance, TDDB failure

P.R. Besser, ECS Trans 2(6), 3 (2007)
TDDB Lifetime and Interconnect Scaling

• Capacitance reduction by increasing porosity is high risk with little benefit
• TDDB is a critical hurdle for BEOL scaling, suffering an order of magnitude degradation for each generation @ ULK2.4
• Reducing ULK dielectric constant further degrades dielectric reliability
• Poor LER and misaligned vias can further degrade TDDB

“Progress in lowering k, or even maintaining it at present levels, with continued technology progression requires integration of (novel) non-porous materials or changes in interconnect architecture to include air-gaps.”

* A. Oates (TSMC) IEDM 2014
New Dielectrics Can Help Reduce RC, but Have Challenges

- Porous low k were introduced as part of the 32/28 nm technology
  - ↑ porosity ↓ k value, but dielectrics have ↑ process-induced damage and ↓ mechanical strength
  - Damage ↑ the effective k and can erase the capacitance benefit

- As a result, at tight pitch interconnects, industry options are **
  - Higher K, non-porous, dense LK dielectrics (less susceptible to damage)
  - Single precursor formulations (dense LK) with a lower K, and/or
  - Low porosity ULK with higher C content

- Industry is spending much resource and has a huge risk exposure for a little gain in C
  - Is there a better way?

** E Todd Ryan et al, IITC-MAM (2015)

Rama Divakaruni (IBM) SOI Technology Summit, Shanghai (2013)
Technology Elements of Air Gaps (AG) in Integrated Circuits

- Air gap insertion has been demonstrated to reduce capacitance and lower the effective dielectric constant
  - Logic had AG >20 years ago: Al technology, pre-unlanded vias
  - Memory AG in production for years: NAND BL-BL + WL-WL, DRAM BL-BL
- AG for capacitance reduction reemerging **
  - Implemented by Intel 14 nm in performance critical layers
  - Two metal levels, with one level without air gap between AG layers
  - Huge RC gain was realized – 14 and 17% at 80 and 160nm pitch.

February 23, 2017
Paul Besser, NCCAVS Symposium in San Jose, CA

G Schindler et al., AMC (2006)
Fischer et al., IITC/MAM (2015)

** Intel, IEDM (2014)
Air Gap Structure and Integration Flow

1. Diffusion barrier open in select AG regions
2. Low-k etch process
3. Post-etch strip/clean
4. Conformal dielectric barrier deposition
5. Non-conformal low-k deposition to create AG

Every process step is critical for reliability, but conformal DB dep affects design.
Reliability Considerations: Short Lines are Integrated in Products!

• Under normal electromigration (EM) testing,
  • As atoms diffuse along the line length, compressive and tensile stresses develop at opposite ends of the line

• Line length:
  • If the line is long, then a void develops in the line = failure
  • If the line is short enough (< $L_{\text{crit}}$), there is a balance between electromigration- and stress-induced atomic diffusion

• Short-line effect:
  • Short lines will never fail (< $L_{\text{crit}}$ = Blech Length)
  • Short-line effect will depend on dielectric material**

Designers utilize and rely on short line effects in their designs for tight pitch interconnects; however, Blech Length is also considered at all metal layers, for deciding current density design rules

Thickness of DB, Post Air Gap Formation, Affects Reliability

- Air gaps have to be designed into the chip
  - Air gaps are selectively introduced, avoiding vias and placing air gaps at critical layers with high current densities for maximum benefit
- Process-oriented simulations reveal affect of Air Gaps on circuit design:
  - As expected, the tensile stress in Cu lines increases linearly DB thickness
  - $J_{lcrit}$ (Blech Length) in an air-gapped interconnect depends on SiCN (DB) thickness and increasing the DB thickness degrades $J_{lcrit}$
  - Airgapped interconnects with 5 nm conformal SiCN have a $J_{lcrit}$ comparable to non-airgapped interconnects (with ULK 2.5 ILD)
  - DB must be thick enough to be hermetic, but if too thick, $J_{lcrit}$ will be degraded, affecting circuit design

Houman, Besser, Wilson and Croes, JAP 120, 095103 (2016)
Dielectric Barrier/Etch Stop Layer Requirements

- Requirements for dielectric barrier/ESL
  - Cu diffusion barrier
  - Hermetic barrier for moisture and O$_2$
  - High etch selectivity
  - Excellent adhesion to metal and ULK
  - High breakdown voltage and low leakage
  - Low dielectric constant

- A combination of high etch selectivity ESL and thin hermetic Cu barrier enables DB scaling
  - A high selectivity ESL can provide better control of unlanded via over etch and enable TiN wet removal with protected via bottom
    - Replacing SiCN with AlN + SiCO offers a highly conformal stack with high etch selectivity, $k_{eff}$ reduction, and excellent diffusion barrier;
    - Film is hermetic at 3 nm thick.
Dielectric Barrier (DB)/Etch Stop Layer (ESL) Scaling to the Rescue

• Modelling suggest thinning or scaling the DB to 5 nm NDC thickness provides 7% $k_{eff}$ reduction, which is more than one generation of low k dielectric progress.

• Can DB/ESL continue to scale with all the DB/ESL requirements and increasing complex patterning?
Dielectric Barrier (DB)/Etch Stop Layer (ESL) Scaling to the Rescue

- DB/ESL remains as the key process for capacitance reduction
- Co-optimization of etch and ESL is needed to enable robust via patterning and capacitance improvement

- Integrating AlN + SiCO stacks as a replacement for SiCN provides an integration advantage:
  - Scaling enabled
  - High etch selectivity
  - Significant $k_{\text{eff}}$ reduction
  - Excellent diffusion barrier
Resistance Reduction Opportunities

How far can Cu extend? And what replaces Cu?
Understanding Copper Resistance Increase in Narrow Features

- Resistance increase with decreasing linewidth, due to scattering
  - Electrons are scattered by grain boundaries, interfaces, surfaces, and defects (Cu electron mfp = 36 nm)
  - Scattering events lead to Cu resistivity ↑ with ↓ linewidth
  - How to compensate?
    - Increase aspect ratio of the Cu line? Void-free fill is a challenge.

G. Schindler, Sematech workshop on Cu resistivity (2005)  
P.R. Besser, ECS Trans 2(6), 3 (2007)
Why Line Resistance Increases as Linewidth Decreases

• Cu extendibility is challenged by fill, barrier integrity, conductive metal area, and scattering; Cu current carrying cross-section i with i linewidth

• A calculation of conductive metal area and Cu line Rs as a function of linewidth reveals
  • Barrier thicknesses has not scaled below 2.5 nm, but must scale for Cu to scale below 20 nm linewidth, and
  • Area for conductive metal is small, leading to a high Rs in narrow features
BEOL Scaling Simulations: Cu can Extend to 7 nm, Maybe to 5 nm

- Coventor™ simulations (to scale) reveal the challenge with extending PVD barrier/liner/seed: PVD overhang and can lead to voids in narrow features
  - Cu extendibility is a function of design rules
  - Cu seed extendibility to 5nm is questionable

- Migrating to PVD TaN/CVD liner (Co or Ru) is likely at 7 nm to enable extendibility of Cu
At 10 and 7nm, Cu Extendibility is Possible

- Co liner provides an improvement for Cu scaling; however, only to 12 nm linewidth
- Scaling the liner thickness (with alternative liners) can extend Cu, but with a net resistance line resistance increase

van der Veen, IITC AMC (2016)
What Is Beyond Cu?
 Resistivity in Narrow Features (Intel, 2015)

• At the 5 nm node, not scaling the PVD liner thickness reduces the electrical area by a factor of 2 while increasing the Rs by an order of magnitude

• Based on modeling, resistivity in a 12 nm line (AR=1.5, 3 nm liner) is dominated by surface scattering:
  • Surface scattering (54%), bulk resistivity/phonon(15%) and GB scattering (31%)

• Options to reduce line Rs:
  • Subtractive patterning
  • Scale liner thickness → barrierless
  • Smaller EMFP metals

Chawla et al, (AMC 2015)
Another Perspective: EMFP and Resistivity

- In the case of thin wires and/or small grain sizes, the wire resistivity is proportional to the product of EMFP ($\lambda$) and bulk resistivity ($\rho_0$), for a fixed grain size distribution and linewidth.

- With this metric, options to consider as Cu replacements are:
  - Rh cost
  - Ir cost
  - Al cost and thermal excursion
  - Co
  - Ni options to consider...
  - Ru

<table>
<thead>
<tr>
<th>Element</th>
<th>Crystal structures</th>
<th>$\lambda_n$ (nm)</th>
<th>$\lambda \times \rho_0$ ($10^{-16} \Omega \cdot m^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver (Ag)</td>
<td>fcc</td>
<td>53.3</td>
<td>8.46</td>
</tr>
<tr>
<td>Copper (Cu)</td>
<td>fcc</td>
<td>39.9</td>
<td>6.70</td>
</tr>
<tr>
<td>Gold (Au)</td>
<td>fcc</td>
<td>37.7</td>
<td>8.35</td>
</tr>
<tr>
<td>Aluminum (Al)</td>
<td>fcc</td>
<td>18.9</td>
<td>5.01</td>
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<tr>
<td>Calcium (Ca)</td>
<td>fcc</td>
<td>35.4</td>
<td>11.9</td>
</tr>
<tr>
<td>Beryllium (Be)</td>
<td>hcp</td>
<td>48.0/68.2</td>
<td>17.1/24.3</td>
</tr>
<tr>
<td>Magnesium (Mg)</td>
<td>hcp</td>
<td>22.3/20.0</td>
<td>9.81/8.80</td>
</tr>
<tr>
<td>Rhodium (Rh)</td>
<td>fcc</td>
<td>6.88</td>
<td>3.23</td>
</tr>
<tr>
<td>Sodium (Na)</td>
<td>bcc</td>
<td>30.9</td>
<td>14.7</td>
</tr>
<tr>
<td>Iridium (Ir)</td>
<td>fcc</td>
<td>7.09</td>
<td>3.69</td>
</tr>
<tr>
<td>Tungsten (W)</td>
<td>bcc</td>
<td>15.5</td>
<td>8.20</td>
</tr>
<tr>
<td>Molybdenum (Mo)</td>
<td>bcc</td>
<td>11.2</td>
<td>5.99</td>
</tr>
<tr>
<td>Zinc (Zn)</td>
<td>hcp</td>
<td>17.4/13.7</td>
<td>10.3/8.1</td>
</tr>
<tr>
<td>Cobalt (Co)</td>
<td>hcp</td>
<td>11.8/7.77</td>
<td>7.31/4.82</td>
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<tr>
<td>Nickel (Ni)</td>
<td>fcc</td>
<td>5.87</td>
<td>4.07</td>
</tr>
<tr>
<td>Potassium (K)</td>
<td>bcc</td>
<td>31.5</td>
<td>22.7</td>
</tr>
<tr>
<td>Cadmium (Cd)</td>
<td>hcp</td>
<td>16.8/15.1</td>
<td>12.6/11.3</td>
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<tr>
<td>Ruthenium (Ru)</td>
<td>hcp</td>
<td>6.59/4.88</td>
<td>5.14/3.81</td>
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<td>Indium (In)</td>
<td>bcc</td>
<td>8.65/8.16</td>
<td>7.62/7.18</td>
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<tr>
<td>Osmium (Os)</td>
<td>hcp</td>
<td>7.20/4.87</td>
<td>6.41/4.33</td>
</tr>
</tbody>
</table>

D. Gall, JAP 119, 085101 (2016)
## Metal Options: Choosing a Good Metal Conductor to Replace Cu

<table>
<thead>
<tr>
<th></th>
<th>Cu</th>
<th>Co</th>
<th>Ru</th>
<th>Ni</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Barrier/Liner Needed</strong></td>
<td>Barrier</td>
<td>Thin liner</td>
<td>Thin liner</td>
<td>TBD</td>
</tr>
<tr>
<td><strong>Bulk Resistivity</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EMFP (nm)</strong></td>
<td>39</td>
<td>6</td>
<td>10</td>
<td>18</td>
</tr>
<tr>
<td><strong>Melting Point (°C)</strong></td>
<td>1083</td>
<td>1495</td>
<td>2250</td>
<td>1453</td>
</tr>
<tr>
<td><strong>Deposition processes</strong></td>
<td>ECD, PVD</td>
<td>ECD, ELD, CVD, PVD</td>
<td>CVD, PVD</td>
<td>PVD, CVD, ELD</td>
</tr>
<tr>
<td><strong>Gap Fill of Narrow Features</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td></td>
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</tr>
</tbody>
</table>

Co exhibits short EMFP, high melting point, and can be deposited with various techniques at low cost

P.R. Besser, ECS Trans 2(6), 3 (2007)
Why Cobalt for Interconnects?

- Co is already integrated in IC processing as a liner and a cap layer.
- The shorter mean free path of electrons in Co and the reduced requirement for a barrier reduce the resistivity disadvantage of Co (vs. Cu) in the 15-20 nm line dimension range.
- Co electromigration (EM) is better than Cu, based on melting point and publications.
- Electroplating allows bottom-up Co fill at a low cost, but CVD/PVD also fills features.
- IMEC simulations suggest barrierless vias filled with Co have a resistance benefit for N7 and beyond.

Melting Point vs. Interconnect Metal

![Melting Point vs. Interconnect Metal](image)

- Al
- Cu
- Ni
- Co
- Ru
- W

M. H. van der Veen et al., IITC (2015)
M. H. van der Veen, IITC/MAM (2015)
Enabling Void-Free Metallization with Co Electrochemical Dep

- Co electroplating on CVD Co liner alleviates PVD Cu seed “pinch off”
- Co liner oxidizes when exposed to air and leads to resistivity increase and potential interfacial integrity degradation
- Pre-treatment of Co liner results in substantial conductivity increase and allows for improved nucleation of ECP Co film
- Temperature/time/chemistry can be used to control the sheet resistance drop and Co agglomeration

Natalia Doubina et al., CSTIC 2016, Shanghai
Hui-Jung Wu et al., Semicon West (2016)
Other Alternatives to Cu

• Resistance and Electromigration Performance of 6 nm Wires (Intel)
  • Line Rs and EM were measured for 6 nm CD wires; interconnect performance was measured down to 60 nm² wire cross-sectional area.

• Ruthenium is an option to replace Cu at 5nm (imec, GLOBALFOUNDRIES, IBM)
  • Ru refloows at a low temperature; resistivity is 18 µΩ-cm at 7 nm LW is better than Cu (with a 2 nm barrier); via Rs was comparable to Cu; a thin adhesion layer is required (TiN), but TDDB and EM are good
  • The challenges with Ru are cost, CMP, and immaturity
How to Reduce Interconnect Rs Further?

- The solutions shown thus far are incremental improvements in via/line Rs: the industry needs still lower via and line Rs!

Contributions to line resistance

A  intrinsic resistance of metal = f(material)
B  increase in Rs due to scattering = f(interfaces, grains, impurities, etc)
C  increase in Rs due to resistive barriers or geometry

Low or no barrier/liner offers an opportunity to eliminate the increase in Rs due to barriers (C)

NOT drawn to scale
How to Reduce Interconnect Rs Further?

- The solutions shown thus far are incremental improvements in via/line Rs: the industry needs still lower via and line Rs!

- **One option: directly platable, conductive liner**
  - Co-Ti (University of Tokyo). Resistivity is ~130 $\mu\Omega$-cm
  - Co-Mo (Fudan University). Resistivity is 100-150 $\mu\Omega$-cm
  - Co-W (Tokyo University). Resistivity of CoW films (200 nm) with 10 and 20%W were 80 and 200 $\mu\Omega$-cm. Adding Cp$_2$WH$_3$ into source gas in an ALD cycle -> CoW alloy film with 5%W without including WO$_3$ or C reduced resistivity to 25 $\mu\Omega$-cm (15 nm thick)
  - Co-Si (Literature). Resistivity is 10-40 $\mu\Omega$-cm, depending on the phase of CoSix formed

<table>
<thead>
<tr>
<th>Co-Ti</th>
<th>Co-Mo</th>
<th>Co-W</th>
<th>Co-Si</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Graph" /></td>
<td><img src="image2.png" alt="Graph" /></td>
<td><img src="image3.png" alt="Graph" /></td>
<td><img src="image4.png" alt="Graph" /></td>
</tr>
</tbody>
</table>

Figure 4 Sheet resistance variation with annealing time of sandwich structure after thermal process in air at (a) 200°C, (b) 250°C, (c) 300°C.

M. Hosseini et al., IITC/AMC 2016  
Li-Ao Cao et al, IITC/AMC 2016  
Murarka et al, JAP (1984)  
Modelling of Barrier Resistivity Affects Line Resistance

Calculations of line resistance as a function of barrier resistivity (25 vs. 1000 µOhm-cm) reveal barrier line Rs reduces ~40% as a function of barrier resistance (at 12 nm linewidth)

Barrier resistance matters

Circuit performance simulations confirm a performance gain with conductive liner

Assumptions
- Co Line Rs based was measured to 18nm. Extrapolated to 12nm LW
- 70% linewidth scaling node to node
- aspect ratio is constant at 2
- Metal resistivity changes with linewidth (LW)
- Barrier thickness is constant at 2.5 nm
- Barrier resistivity changes from 25-1000 µOhm-cm
Summary

• Materials innovations drive performance improvements in the microelectronics industry, creating faster and smaller devices

• Leading-edge nodes are seeing an explosion of new innovations to drive BEOL RC reduction

• For capacitance (C)
  • Capacitance scaling has slowed
  • Dielectric barrier scaling (i.e. AlN + SiCO) offers the best opportunity to reduce capacitance

• For resistance (R)
  • Line and via resistance are the dominant source of interconnect delay at 7 and 5 nm
  • Cu line and via resistance are increasing with each technology node, due to electron scattering, but also due unidirectional patterning and a lack of barrier scaling
  • Conductive liner/barriers offer promise to lower line and via resistance
  • Co interconnects show great promise to replace Cu, either by
    • Electroless Co via prefill or
    • Co electroplating
Thank you