2017 CMPUG/TFUG JOINT MEETING

Topic: 3D Packaging Technology

Meeting Date: June 7, 2017

Time: 12:30 pm - 4:30 pm

Location: **SEMI Headquarters (NEW LOCATION!!)**
673 South Milpitas Blvd.
Milpitas, CA 95035

****

FREE TO ATTEND, JUST SHOW UP!

****

Co-Chairs:
Robert L. Rhoades, Entrepix, Inc., rrhoades@entrepix.com
Sing-Pin Tay, sing-pin_tay@avs.org

This meeting focuses on technologies and applications related to 3D Packaging. The purpose of this meeting is to bring together leading researchers in academia, government, and industry with innovative technologies to nurture a free exchange of triumphs and challenges in the advances in 3D Packaging applications.

SPEAKERS/AGENDA

12:30 pm – Meeting Start and Lunch, **FREE LUNCH – Sponsored by Kurt J. Lesker Company**

1:15 pm – Welcome

1:20 pm – **Monolithic 3D Integration Using Standard Fab and Standard Transistors, Zvi Or-Bach, Monolithic 3D Inc.**

Abstract: The challenge for Monolithic 3D IC is how to provide high quality transistor on top and tightly connected to prefabricated transistors and interconnection, without impairing the underlying structure by the high temperature process steps which are usually associated with the formation of high quality transistor. This talk will give some general background and then detail a breakthrough flow which would allow using standard fab and standard transistors. The talk will illustrate such a flow for a specific application enabling 1,000x better computers.

Bio: *Zvi Or-Bach is the founder President and CEO of MonolithIC 3D™ Inc. Or-Bach has more than 30 years of innovative development including the breakthroughs of monolithic 3D ICs and fast-turn ASICs. Prior to MonolithIC 3D, Or-Bach founded eASIC in 1999 and served as the company's CEO for six years. Earlier, Or-Bach founded Chip Express in 1989 (recently acquired by Gigoptix) and served as the company's President and CEO for almost 10 years, bringing the company to $40M revenue, He holds over 100 issued patents, primarily in the field of 3D integrated circuits and semi-custom chip architectures. He is the Chairman of the Board for Zeno Semiconductors, Bioaxial and VisuMenu.*

2:00 pm – Coffee Break and Networking - **Sponsored by UC Components**

2:30 pm – **Reliability of ultra-fine RDL Structures in Advanced Packaging Patterned by Excimer Laser Ablation, Markus Arendt, SUSS MicroTec Photonic Systems, Inc.**

Abstract: Fan out wafer level packaging (FOWLP) continues to be the main driver for advanced packaging. Multi-chip integrated Fan-Out packages and high I/O CSPs demands for higher routing density on wafer level. However, there is a continuing need for low cost packaging. While traditional organic flip-chip substrates using semi-additive processes (SAP) have not been able to scale to ultra-fine RDL pitches and via opening below 10um, photo-sensitive spin-on dielectrics and RDL processes used for wafer level packaging do not sufficiently address the cost reduction need, and continue to cause reliability issues.

The latest results from creating ultra-fine RDL and micro-via structures using excimer laser ablation are discussed. Various materials like low cure temperature polyimide and dry-film ABF material are structured using an excimer laser stepper with a reticle mask to pattern feature size below 4 um with a high throughput. Micro-vias with a diameter below 5 um are realized with high aspect ratio which overcomes the photolithographic limitations of the common used photosensitive thin-film polymers. The laser structuring provides access to innovative dielectric materials for WLP with optimized mechanical and electrical parameters for example inorganic filled polymers like dry-film ABF materials, which do not have to be photosensitive.

Electrical data of daisy chain is presented, formed by micro via and ultra-fine RDL traces patterned by Excimer laser in both photo and non photo materials. The reliability of two ultra-fine RDL layers patterned by excimer laser will be discussed. The commercial benefits of the new laser based patterning process as compared to the current process of record (POR) will be highlighted.

Bio: *Dr. Markus Arendt is President of SUSS MicroTec Photonic Systems, an equipment supplier for lithography solutions for Advanced Packaging, 3D Integration, and MEMS industries. Throughout his 10 years with SUSS MicroTec, he has held a range of senior-level positions, from Division Head for the Photomask Equipment Division to VP of Operations. Previously, he was General Manager of ANKA Synchrotron Radiation Source, and responsible for the commercialization of products and services with Synchrotron Radiation. Markus holds a Diploma in Engineering from the University of Karlsruhe/Germany, and a Ph.D. in Economics from the University of Heidelberg/Germany.*

3:10 pm – **CMP and Current Trends Related to Advanced Packaging, Robert L. Rhoades, Entrepix, Inc.**

Abstract: Advanced packaging technology is evolving quickly. Modules based on 3D packaging with thru silicon vias (TSV's) are now available in the market for a few applications and many more are being developed. The design goals often include reducing parasitic losses, shrinking form factors, enabling combinations of different chip technologies, and lowering costs – all at the same time and without sacrificing reliability. This is an extremely difficult set of goals and CMP is a key process at one or more steps in many of these integrations.

Many aspects of packaging applications represent challenges for CMP, including removal rates, throughput, rapidly changing design rules, overall yield, and one of the biggest challenges of all - cost. This presentation will provide an overview of CMP for packaging, provide a few examples of issues arising during development, and highlight a few trends currently impacting the technology.

Bio: *Dr. Robert Rhoades is the Chief Technology Officer for Entrepix, Inc.. He has been a recognized industry leader in CMP for over 22 years. In 2002, he joined Entrepix to launch a process foundry to provide CMP services for R&D prototypes through volume production on virtually any material and any wafer size. Dr. Rhoades earned B.S., M.S. and Ph.D. degrees in Electrical Engineering from the University of Illinois. He is a named inventor on roughly a dozen patents and has authored more than 100 technical publications and conference presentations.*

3:40 pm – **Open Forum Discussions – Moderator: Robert L. Rhoades, Entrepix, Inc.**

4:30 pm – **End Meeting**

****

All presentations will be requested to be posted on the CMPUG & TFUG Proceedings webpage approximately 1-2 weeks following the meeting.

If you would like to sponsor this meeting please check out our "NCCAVS Marketing/ Sponsorship" opportunities at: NCCAVS_marketing_opportunities