CMP and Current Trends Related to Advanced Packaging

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NCCAVS TFUG-CMPUG Joint Meeting
June 7, 2017
• Industry Trends
• Trends in Packaging
• Where is CMP used in next generation packaging?
• Summary
Question: Is anyone out there confident in the next 3 years?

**Global Economic Conditions**

**WORLD ECONOMIC OUTLOOK (WEO) UPDATE**

**A Shifting Global Economic Landscape**

January 2017

*India economy sees 7.6% annual growth*

India's economy grew by 7.6% in 2015-16 as the nation retained its place as the world's fastest-growing major economy.

*Fed, China fears force investors to check out of Asia*

Beppe Grillo, founder of Italy's Movimento 5 Stelle (Five Star Movement), speaks during a public rally. Pacific Press LightRocket via Getty Images

*A businessman walks in Tokyo's business district, Japan. January 26, 2016. REUTERS/Toru Hanai*
According to S&P:

- Alphabet (Google)
- Amazon
- Apple
- Facebook
- Microsoft
What Drives Growth in Semiconductors?

- **Historical Growth Segments**
  - Computers and PC’s
  - Cell phones
  - High bandwidth infrastructure
  - Tablets

- **Recent or Emerging Growth Segments**
  - Smartphones
  - Internet of Things (IoT)
  - Power management and remote control
  - Medical applications
Semiconductor Revenue by Year

- PC Wars
- Internet Bubble
- Cell phones & Tablets
- Global Financial Crisis
- Stable??

Source: WSTS, PwC analysis
• What drives decisions in the semiconductors? SPEED and COST!
  – New products must be ready on time for market launch
  – Long term efficiency improves competitive strength
• Moore’s Law dominated the CMOS industry for >40 years
  – Not interrupted by cycles, markets, analysts, or the economy
• Photolithography and CMP are two critical process technologies to contributed both cost and performance improvements
  – Photolithography enables SHRINKS
  – CMP enables more complex STACKS
• Recent evidence shows very few companies still trying to hold to Moore’s Law … most are choosing to pursue alternatives rather than continue to pursue 2D shrinks

Source: Intel Corporation
Moore’s Law Is Dead. Now What?

Shrinking transistors have powered 50 years of advances in computing—but now other ways must be found to make computers more capable.

Source: MIT Technology Review, 2016

**TECHNOLOGY QUARTERLY AFTER MOORE’S LAW**

Double, double, toil and trouble

Microprocessor Transistor Counts 1971-2011 & Moore’s Law

Source: Fortune.com “Intel Insisting Moore’s Law Isn’t Dead” May2017

**LOGIC TRANSISTOR DENSITY**

Source: Fortune.com “Intel Insisting Moore’s Law Isn’t Dead” May2017

IBM proves Moore's Law is not dead by squeezing 30 billion transistors into a fingernail-sized chip

By Rob Hogan

1 day ago

Source: pcr-online.com/news posted 5June2017
Trends in Scaling and Integration

Beyond CMOS

Baseline CMOS
CPU, Memory, Logic

More Moore: Scalingen

More than Moore:
Functional Diversification

Information Processing
Digital content System-on-Chip (SOC)

Combine SOC & SiP:
Higher Value System

Interacting with people
and environment
Non-digital content System-in-Package (SiP)

Unlike retail or other types of packaging, the performance and reliability of an electronic component are closely tied to the proper design of the package.

Electronic packages are more than just a protective cover.

Source: Clemson Technical Report: CVEL-07-001
Packaging Design Considerations

Source: Clemson Technical Report: CVEL-07-001
Some Definitions

- **DIP** = Dual In-line Package
- **BGA** = Ball Grid Array
- **WLP** = Wafer Level Packaging
- **SoC** = System on Chip
  - Increase functional integration by including sub-systems on a single chip.
  - Includes more than just digital functions, e.g. analog-to-digital converter, RF radio, power isolation, amplifiers, etc. built into the same die.
- **SiP** = System in Package
  - Combines multiple active electronic components of different functionality assembled into a single packaged unit.
  - SiP may integrate passives, MEMS, optical components, and other types of devices and may include multiple types of packaging technology.

*Source: Wolter - Bio and Nano Packaging Techniques for Electron Devices*
Traditional IC Packages

Source: Clemson Technical Report: CVEL-07-001

Thru-Hole Mounted

Surface Mounted
## Types of Packages

<table>
<thead>
<tr>
<th>Type of Package</th>
<th>Primary Use and Advantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard (DIP, BGA, etc.)</td>
<td>Cheap / Simple / Well established CMP or planarization not normally needed</td>
</tr>
<tr>
<td>Ceramic</td>
<td>Tolerates high temperature and mechanical force Greensheet + fill + sinter → No planarization need</td>
</tr>
<tr>
<td>WLP</td>
<td>Higher pinout density, thin RDL layers, thin wafers Leverages device fabrication process steps First layers of “packaging” done before singulation</td>
</tr>
<tr>
<td>2.5D (Interposers)</td>
<td>Material can be Si, polymer, or other Typical integration has 3 RDL layers Planarization required, esp. for TSV fabrication</td>
</tr>
<tr>
<td>3D</td>
<td>Dense functionality, but mating connections require careful design and planarization Thermal management is very difficult</td>
</tr>
<tr>
<td>Thin / Flexible Systems</td>
<td>Fast growing niche Requires ultrathin devices to flex w/o cracking Planarization of mating surfaces is essential</td>
</tr>
</tbody>
</table>
2.5D vs 3D Integration

2.5D: Side-by-side die stacked on a passive interposer that includes TSVs

2.5 or 3D: Interposer with top and bottom connection

3D + Interposer: Mix of side-by-side and stacked implementations on an interposer

3D Memory on Logic: One or more DRAM die stacked directly on logic die
Sometimes called 2.5D integration

Allows mixture of device types, pinout spacing, and component thicknesses

Common versions are Si, glass, or polymer

Frequently include at least 3 wiring levels (RDL) and may include thru vias as well

Source: Hopkins, University of Buffalo (2009)
Pulling Technologies Together

Well over 50% of device content does not require leading edge fab capability

Digital CMOS, MEMS, RF, power, and analog are combined through advanced packaging technology to meet a desired form factor
The number of sensors is currently 60-100 per car ... and is projected to more than double in the next 8-10 years.

Source: Semiengineering.com (Bernard Murphy, Sept 2015)
What is the Internet of Things (IoT)

• Google Definition
  • A proposed development of the Internet in which everyday objects have network connectivity, allowing them to send and receive data.

• TechTarget.com Explanation
  • The Internet of Things (IoT) is a system of interrelated computing devices, mechanical and digital machines, objects, animals or people that are provided with unique identifiers and the ability to transfer data over a network without requiring human-to-human or human-to-computer interaction.
  • IoT has evolved from the convergence of wireless technologies, microelectromechanical systems (MEMS), microservices and the Internet. The convergence has helped tear down the silo walls between operational technology (OT) and information technology (IT), allowing unstructured machine-generated data to be analyzed and drive system improvements.
Strong growth predicted in IoT for next 5 years

Many applications are enabled by MEMS sensors


Source: Semico (Oct 2015)
Some Sensor Data Analytics Applications

- **Keg Data**: My Bud in Mud Room
  - Temperature: 32.7°F
  - Contents: 533 oz
  - Percent: 50%
  - 16 oz pours: 33
  - 12 oz pours: 44
  - Remaining Amount:
  - Date of Pours: Dec 06, 2014 8:55:38 pm
  - Source: Freescale FTF 2015

- **Horsesenseshoes**: Wearables that Save Lives
  - Multi-sensors measure weight variations and patterns as informational indicators.
  - Detect joint problems, laminitis, or lameness early.

- **Freescale FTF 2015**: Never boil over again. Vibration detection using an accelerometer helps your stove autonomously adjust the temperature.

- **BAM Labs**: Wake up rested and energized. Sleep cycle monitoring helps optimize when your alarm should wake you. Vitalis monitored by sensor data included to start your day.

Source: Freescale presentation at Semi Industry Forum on IoT (Oct 2015)
• Expansion of IoT/IoE means an increased number of sensors, but also more connectivity, signal processing, and data storage
• Primary device requirements are low power and low cost
• No single package format
  – Many applications may adopt system-in-package (SiP)
  – Many just SMT modules on FR-4 board, not counted as SiP but as system-in-module (SiM)
• One main reason IoT/IoE is expanding rapidly is the low cost of sensors and multi-die packages and modules
What Factors Will Influence IoT Growth Rate?

- **Security and Privacy Control**
  - Especially important for health care, retail, and critical systems data

- **Interoperability**
  - Must have a manageable number of standards
  - Software apps may hold key to cross-platform integration

- **Reduced Cost**
  - Initial focus is on IC components and sensors
  - Lower packaging, assembly and distribution costs are also critical

- **Low Power**

- **Embedded Processing**
  - Can add distributed intelligence to system (local interpretation / faster decisions)
  - Reduces load on communication bandwidth

*Source: Semico Research (Oct 2015)*
CMP Supplier Complexity

**Process Applications:**

<table>
<thead>
<tr>
<th>Year</th>
<th>Qty ≤ 2</th>
<th>Qty ≤ 5</th>
<th>Qty ≥ 40</th>
</tr>
</thead>
<tbody>
<tr>
<td>1995</td>
<td>CMOS</td>
<td>Oxide</td>
<td>Tungsten</td>
</tr>
<tr>
<td>2001</td>
<td>CMOS</td>
<td>Oxide</td>
<td>Tungsten</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Oxide</td>
<td>Tungsten</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cu (Ta barrier)</td>
<td>Shallow Trench</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Polysilicon</td>
<td>Low k</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capped Ultra Low k</td>
<td>Ultra Thin Wafers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Metal Gates</td>
<td>NiFe &amp; NiFeCo</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Gate Insulators</td>
<td>Al &amp; Stainless</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High k Dielectrics</td>
<td>Detector Arrays</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ir &amp; Pt Electrodes</td>
<td>Polymers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Novel barrier metals</td>
<td>Magnetics</td>
</tr>
</tbody>
</table>

**Consumables and Controls**

- **PADS**
- **SLURRIES**
- **ABRASIVES**
- **CONDITIONING DISCS**
- **BRUSHES & CLEAN CHEMISTRIES**
- **COMPONENTS**
CMP is typically used in a damascene manner to planarize and isolate the vias after conductor deposition from one side.

TSV’s can be filled with any of several conductive materials.

- Most common options are copper and polysilicon.
- Final choice depends on dimensions, operating voltage and current, frequency, temperature requirements, plus other integration factors.

CMP is used again after thinning to help expose and planarize the original “bottom” of the TSV’s – called TSV Reveal.
Example #1: TSV Formation

Background

• Large via needed for design (75-100um diameter)
• Via last with extremely thick Cu plating (about 45 um)
• Previous CMP using standard stock removal slurries resulted in very long polish times (45 mins to 1 hour)

Goals for CMP optimization phase

• Test new high-rate Cu slurry for much shorter clear times
• Verify reasonable selectivity to nitride after barrier clear
• Dishing <1 µm across 80 µm via
• Good surface finish on both Cu and dielectric
Example #1: Results after CMP

Via Diameter = 80 microns
Field area = nitride and via liner = oxide

Optical Microscope

SEM

Source: RTI International, Inc.
Example #2 – TSV with 6um Cu layer

Cu TSV’s up to 8 micron diameter

• Entrepix worked with slurry mfg to develop a more aggressive Cu slurry to cut through the residues

• Result was successful and became the POR slurry for this customer

• Qual data confirms stability across >10 batches over ~12 months time

Initial batches had Cu thickness variation and random small areas on some wafers that were extremely difficult to clear

Customer believed that issues were caused by Cu plating bath

Long polish times turned into unacceptably long (>20 mins) trying to clear these spots
Process module following completion of device layers on front side

TSV must be exposed to make contact and/or continue patterning next layers (RDL) from wafer backside.

Various integrations are viable with combinations of backgrind, etch, selective CMP, or non-selective CMP.

- Some approaches require 2 or 3 steps of CMP

Examples from two alternative integrations

- Reveal Using Non-selective CMP
- Reveal CMP Following Si Etch
Process flow for Si interposer with TSVs: (a) TSV etch, isolation layer, plating, and via CMP, (b) Frontside multi-level metallization, (c) Wafer thinning and TSV reveal, (d) Backside metallization.

Source: RTI International, Inc.
Backgrind for Substrate Thinning

**Carrier Mount**
- TSV wafers mounted face down on carrier wafers

**Backgrind**
- TSV wafers thinned using backgrind to stop roughly 3-15um before hitting TSVs
- Reveal CMP performs dual function of removing grind damage layer and remaining bulk Si then exposing center conductor of TSV’s

Backgrind stops in Si before reaching TSV’s
Expose & Planarize TSVs

Several exposed materials
• Single crystal silicon
• Oxide (or other liner)
• Barrier metal
• Copper

Carrier Wafer
Need to polish far enough into TSVs to remove rounded profile at base of vias

Source: RTI International, Inc.
Cu TSV Reveal

Customized CMP process was used to planarize final surface comprised of Si+Ox+barrier+Cu

Source: RTI International, Inc.
Completed interposer test structure: large via diameter, 100um thickness.

Structure has 2 frontside metal layers (4um Cu) and 1 backside metal.

Bottom surface received TSV reveal polish

Source: RTI International, Inc.
After backgrind, bulk Si removed by an etch process

- Can be dry etch or wet etch, but must be highly selective to oxide
- Installed equipment already available
- Proceeds until 2-5um of encased via “bumps” protrude

Layer of dielectric is usually deposited to protect field areas

Primary goal of CMP is to planarize bumps and expose the Cu cores

One benefit of this approach is to reduce total CMP polish time

- Less sensitive to uniformity issues
- Faster throughput and lower CMP process cost
CMP becomes relatively short “kiss” polish

Pre-CMP Step Height
22,000 Ang

Post-CMP Step Height
60 Ang
• CMP Requirements Related to Packaging
  • High stock removal rates are often needed for acceptable throughput
  • Topography demands are usually less stringent than CMOS interconnect
  • Defectivity is defined at a different level
  • Lower cost is a MUST
  • Wafer thinning is necessary and TTV control is critical
  • New slurries may be needed for new materials, esp. for interposers and flexible electronics
  • Advanced packaging and TSV applications have huge volume potential, but still struggling to define preferred integration that can meet cost expectations
• Miniaturization
  • Form factor and functionality density (package height, footprint)
• Heterogeneous technology integration
  • Digital, RF, analog, power, and sensor integration
• System performance
  • Noise reduction and higher speed
• Flexibility, features, and configurability
• Total system cost reduction
  • Unit cost
  • Development cost
  • Time to market
• Advanced packaging applications have huge potential, but are still struggling to define preferred integrations that can meet cost expectations

Adapted from source: Techsearch International
Many thanks to the following people:

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Customers, colleagues and analysts for various contributions

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