Between 2D and 3D: WLFO Packaging Technologies and Applications

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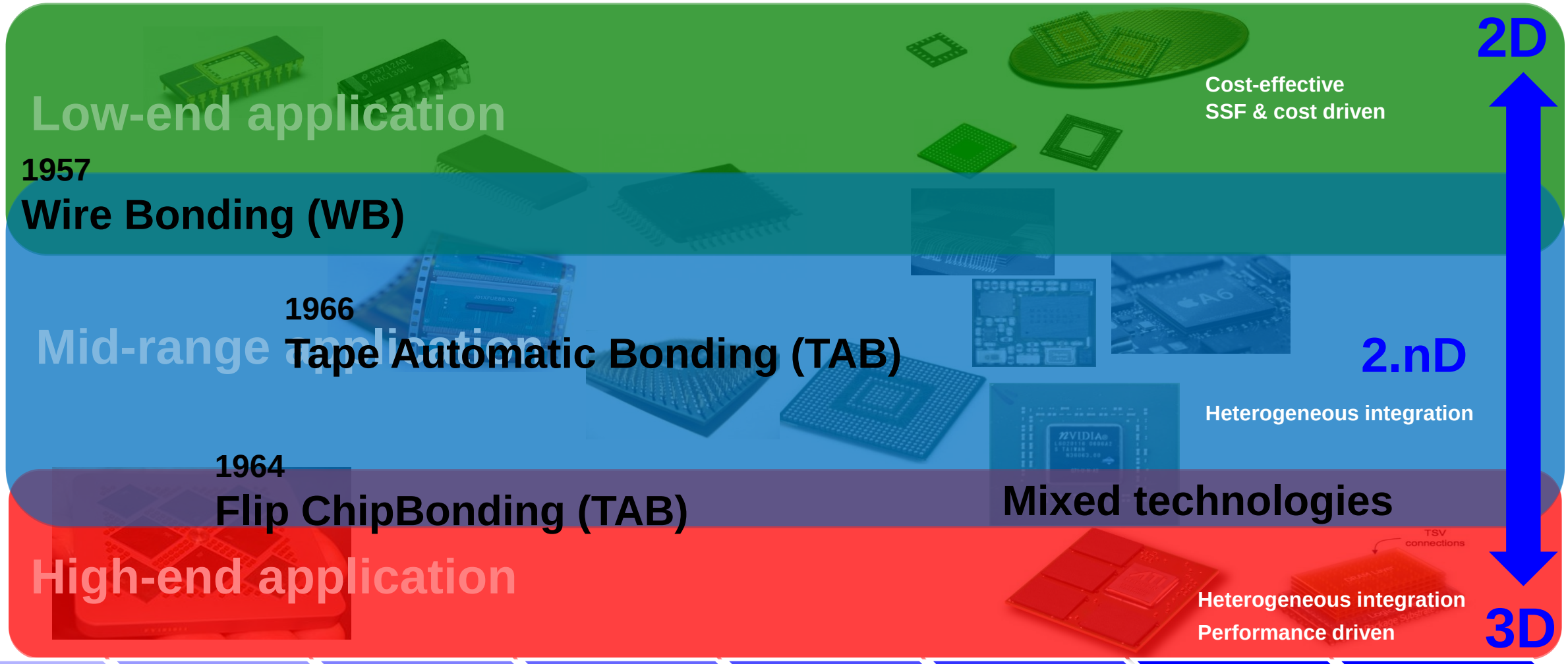
June 9th, 2016

Outline

- The 2.n D
- WLFO technologies
  - Process and architect options
  - Feature comparison
- WLFO's application for Si – Interposer – Substrate co-architecture
  - Introduction
  - <10um pitch bumping
- Summary

Chip-to-Package Interconnect Technology



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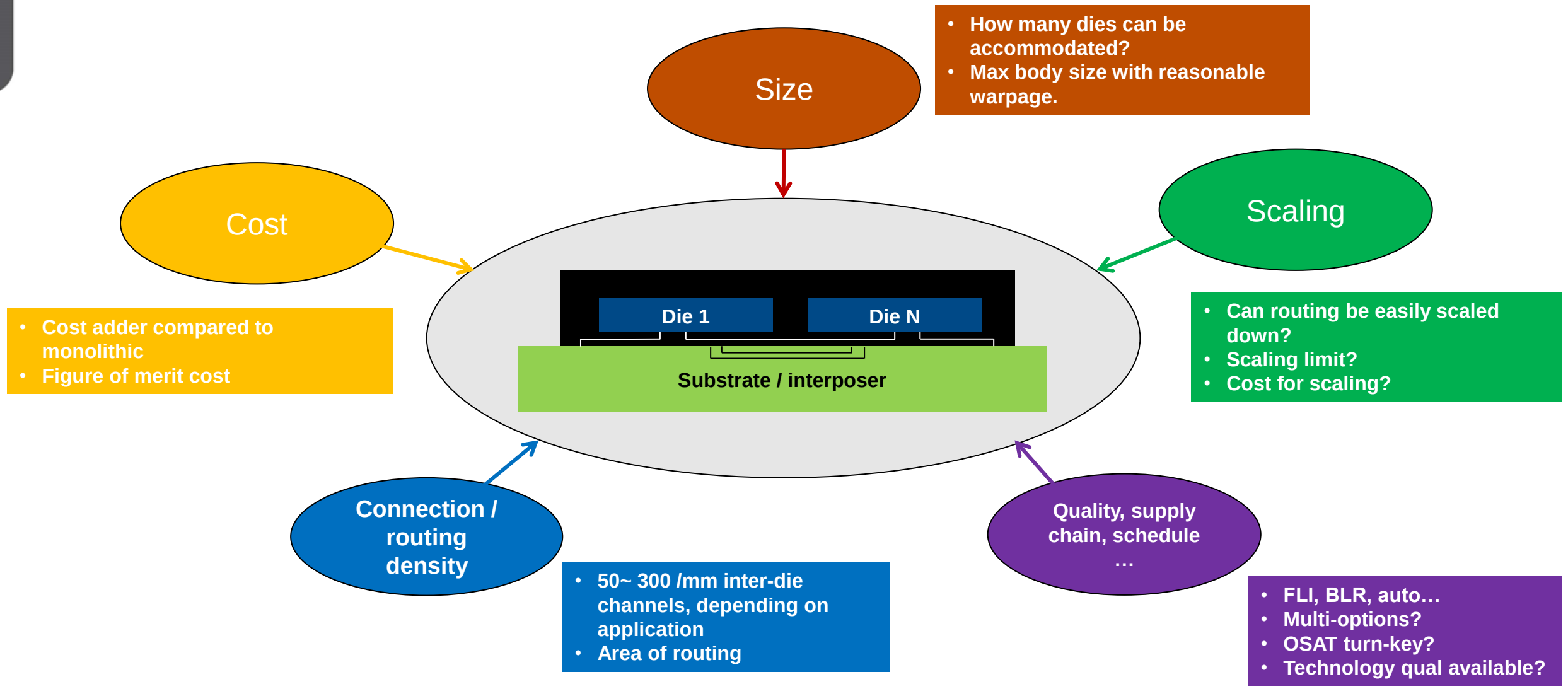
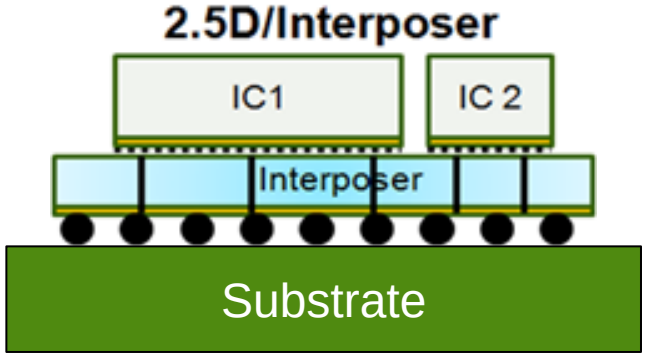
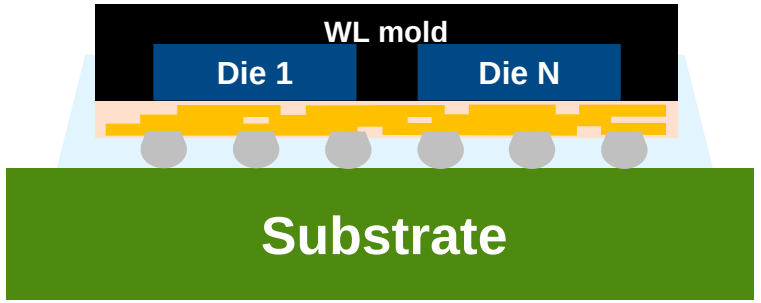
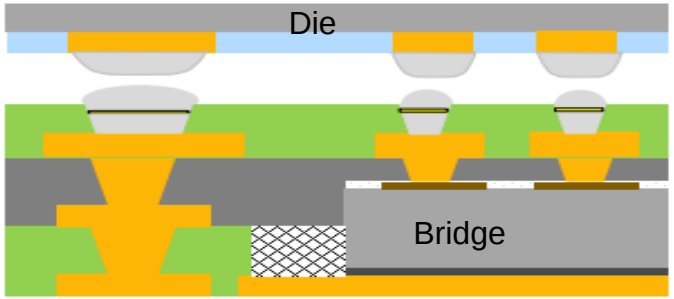
Multi-die Integration Key Factors



The 2.n D : CoWoS – WLFO – EMIB





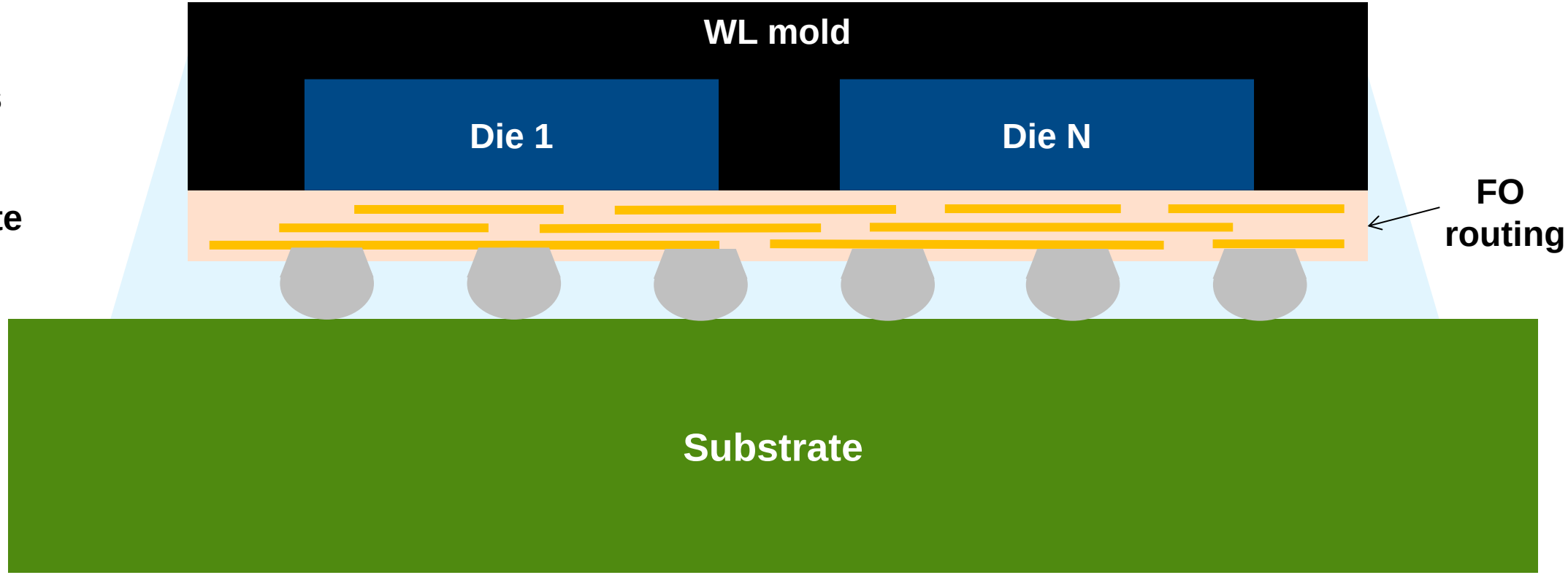


	CoWoS	WLFO	EMIB
TSV	Yes	No	No
Interposer size	Covers all dies, reticle limit, or high cost reticle stitching	Covers all dies, reticle limit, or high cost reticle stitching	Only at the die interface. No area limitation
Connection / routing density	4 layers of full area routing, <4um pitch	>=4 layers of full area routing. ~4 - 20um pitch	Only inter-die routing. Others go through looser PKG routing
Substrate layer count	Same or add 2 layers wrt. monolithic	Partially absorbed in interposer. Possible to reduce substrate 2 layers without PTH or no substrate at all.	Add min. 2 layers wrt. monolithic.

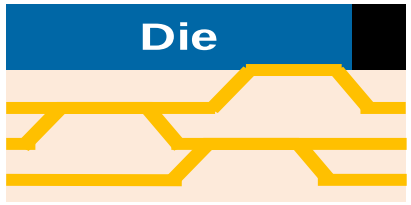
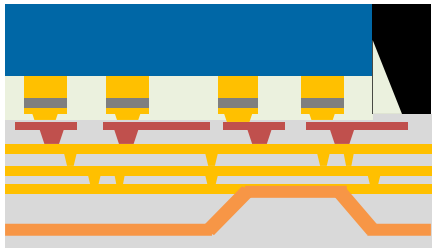
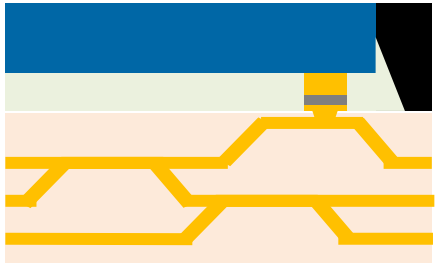
WLFO Schematics

Substrate-less

On substrate



WLFO Technology Overview

	Die First (eWLB like)	Die Last	
		Si based	RDL based
			
Description	1. 2~3 layers of stacked RLD. 2. 2~3um minimal line width RDL	1. upto 4 layers of <=2/2um routing 2. Si interposer w/o TSV, sacrificial Si removed 3. Die to interposer join by ubump.	1. upto 3 layers of 2~3um minimal line width RDL 2. Die to interposer join by ubump.
Example	InFO, eWLB, Deca*	SLIM, SLIT	SWIFT
Pro.	1. Simpler process, no bumping involved. 2. No Si interposer	**1. High routing density, can support HBM and XCVR** 2. Die last --> known good die and known good interposer 3. High routing process yield (matural FEOL Cu damascene process 4. No technical limitation on routing layer count	1. Die last --> known good die and known good routing 2. No Si interposer
Con.	1. Low routing density 2. Die committed prior to low yield stacked RDL process 3. Limited routing layer count	1. Si interposer --> cost adder 2. ubump --> Cost adder	1. ubump --> Cost adder 2. Low routing density 3. Limited routing layer count

Pick the right 2.n Package

- No one-solution fits all 2.n package technology
  - Size, cost, performance, and other factors…
- Small body size, low connection density applications favor die-first WLFO, due to its simplicity, and lower cost
- Super large body size applications are more suitable for EMIB technology due to less limitation on the die box size.
- In between…
  - TSV based interposer solution and die-last TSV-less interposer solutions
  - With the advance of fine pitch and multi-stack of Cu RDL, die-first WLFO may take some advantages away from die-last WLFO
  - Deca panel-like WLFO…
  - And more…

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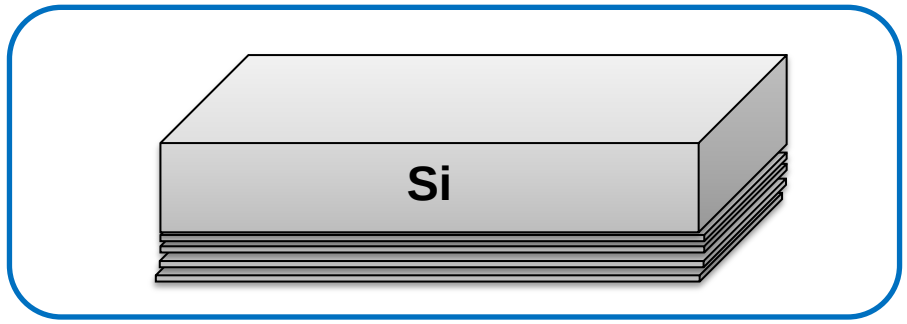
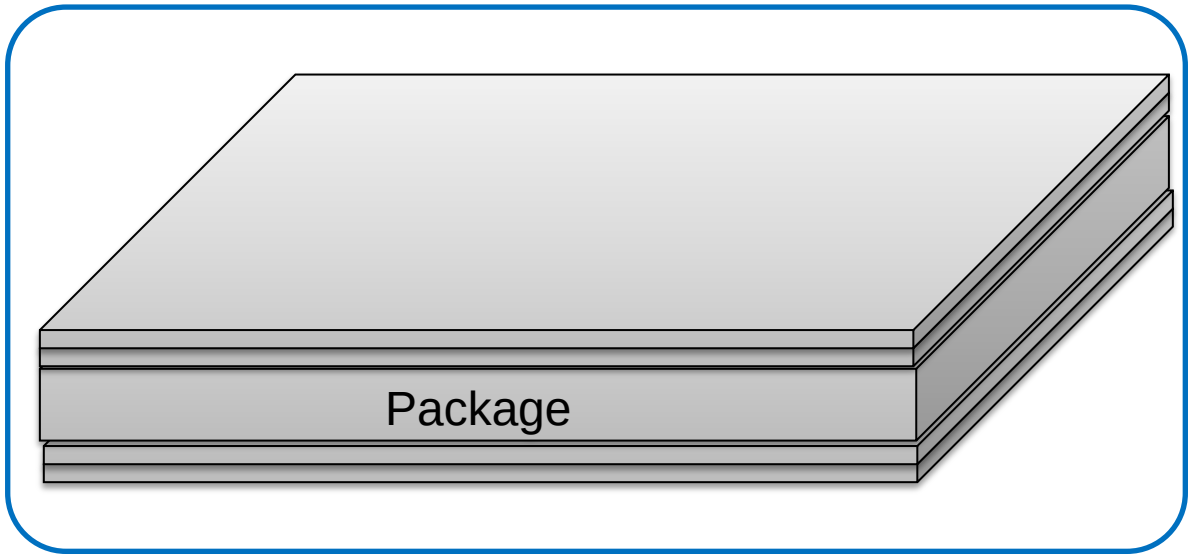
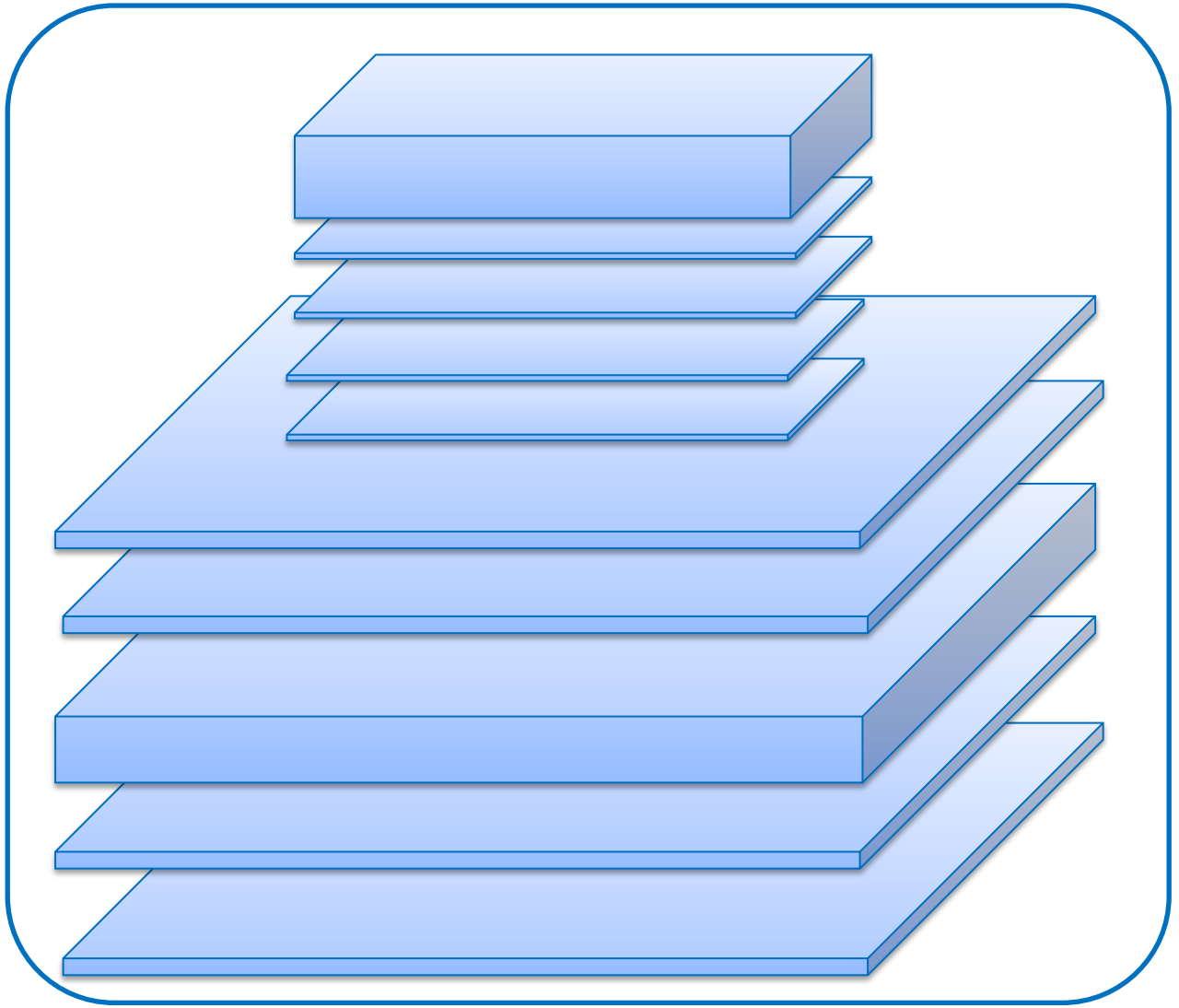
From Interface Co-Design to Co-Architecture



Design 1

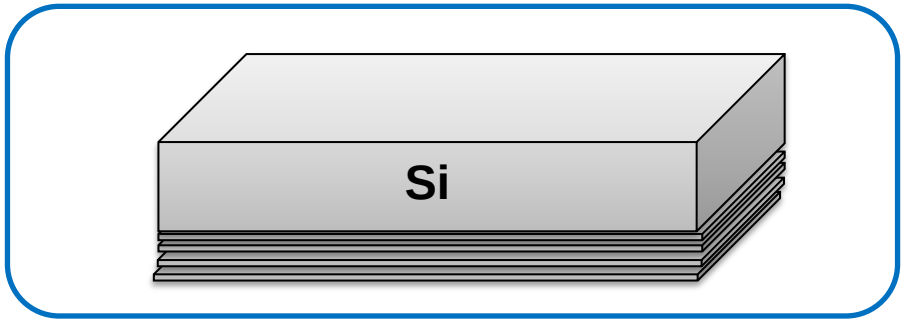


Design 2



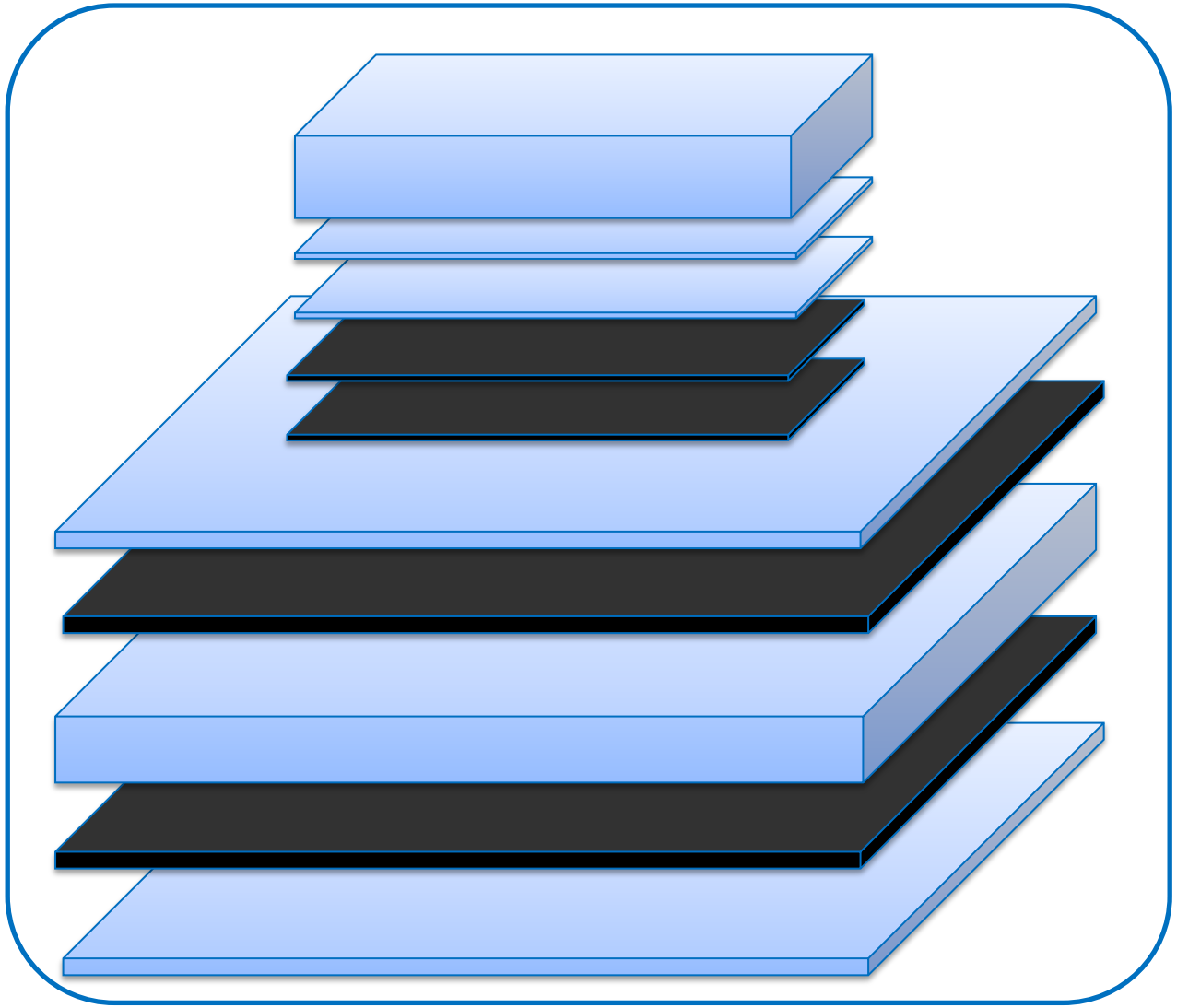
The Design

From Interface Co-Design to Co-Architecture



Design 1

Design 2



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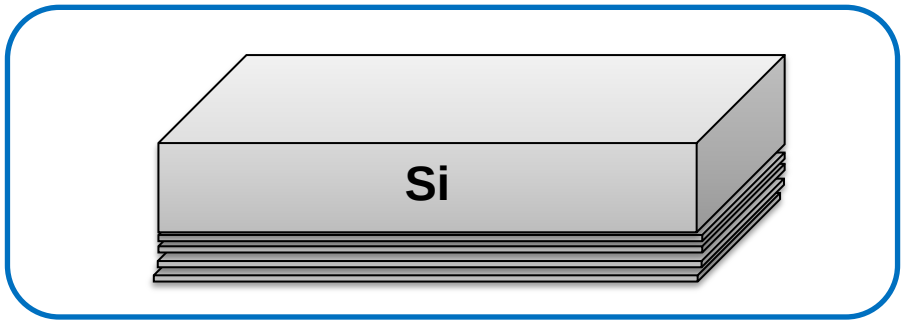

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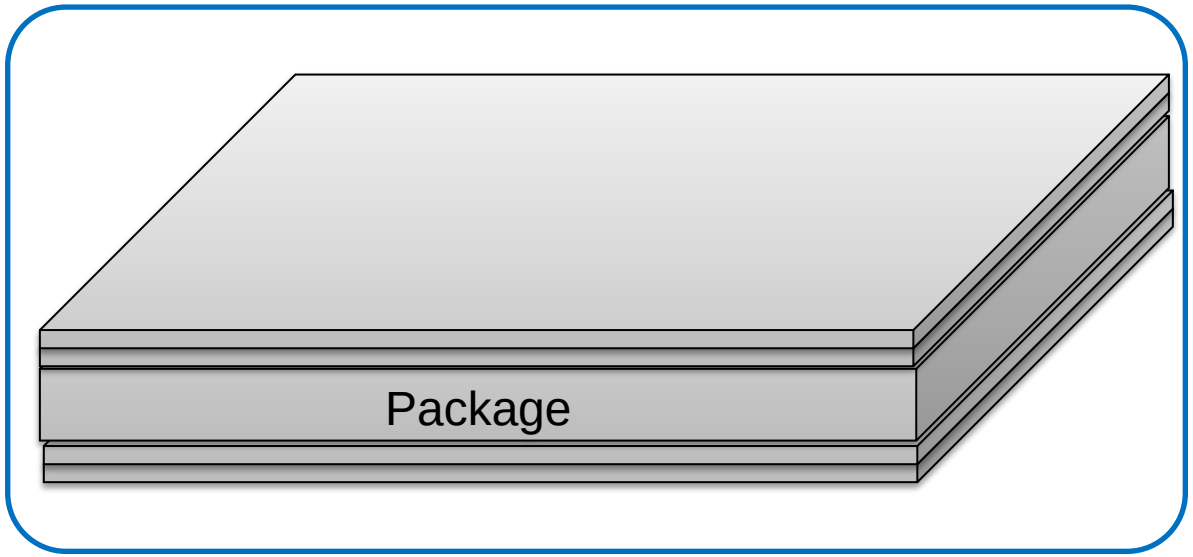

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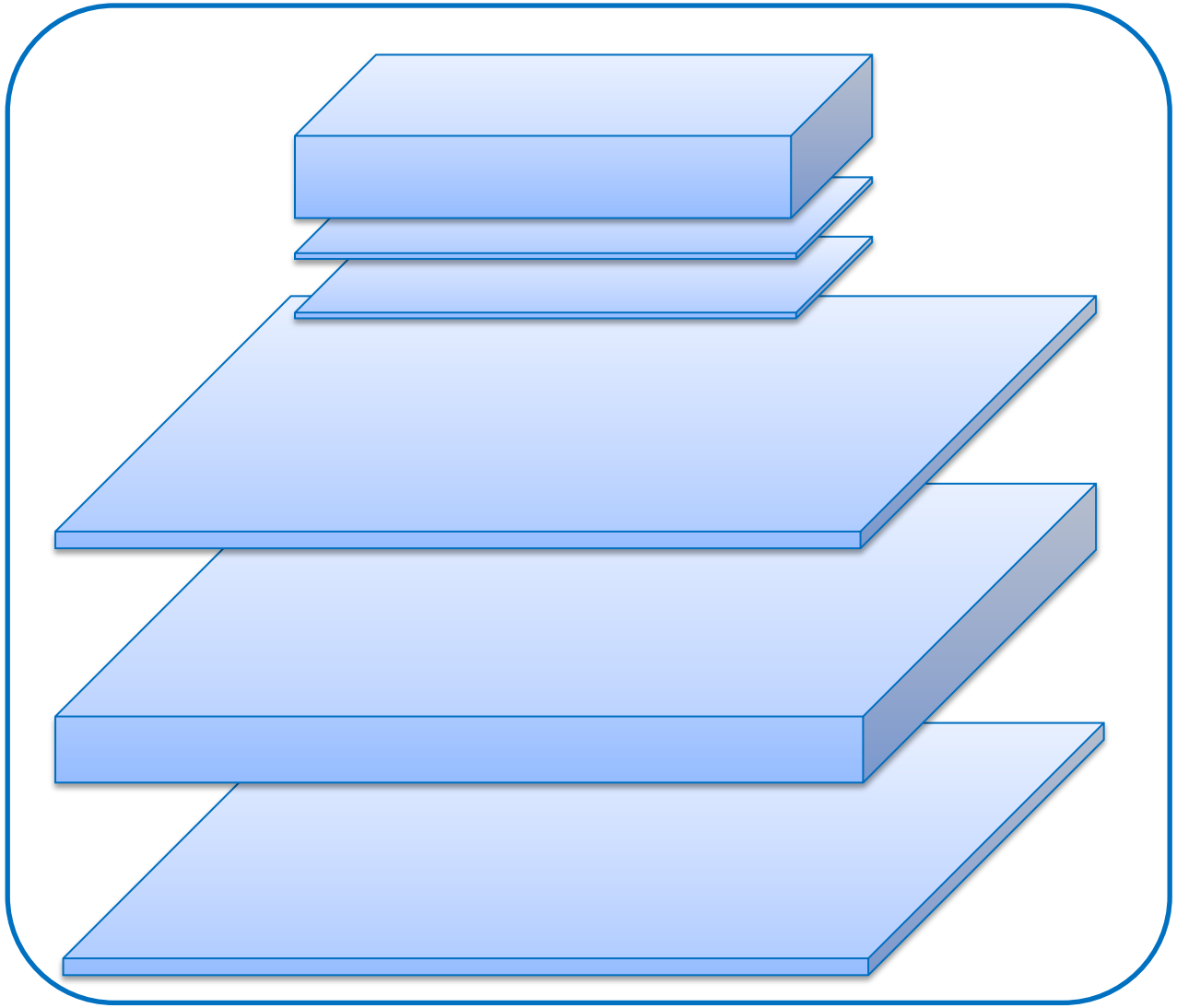

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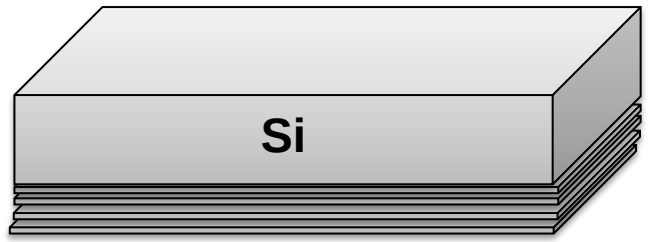

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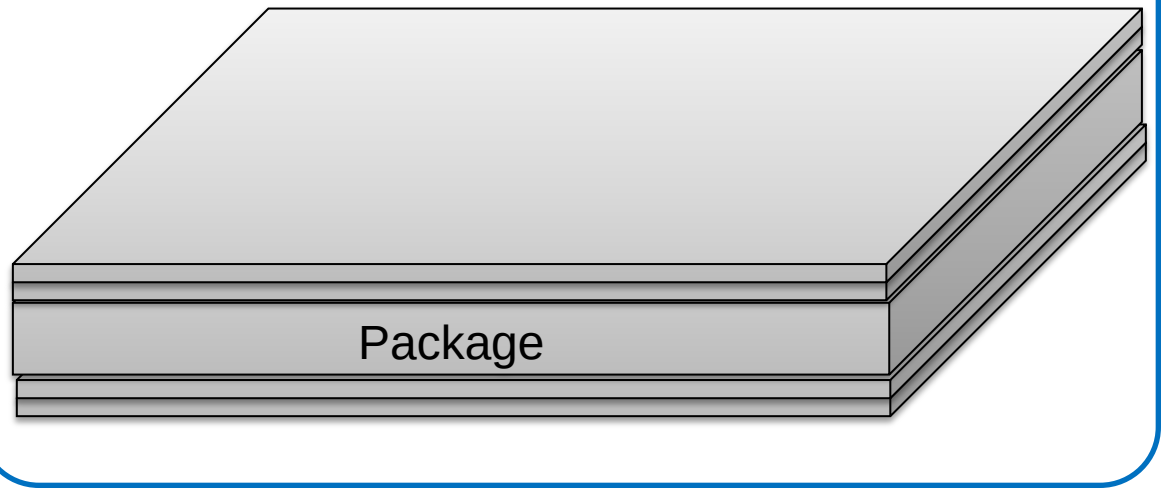
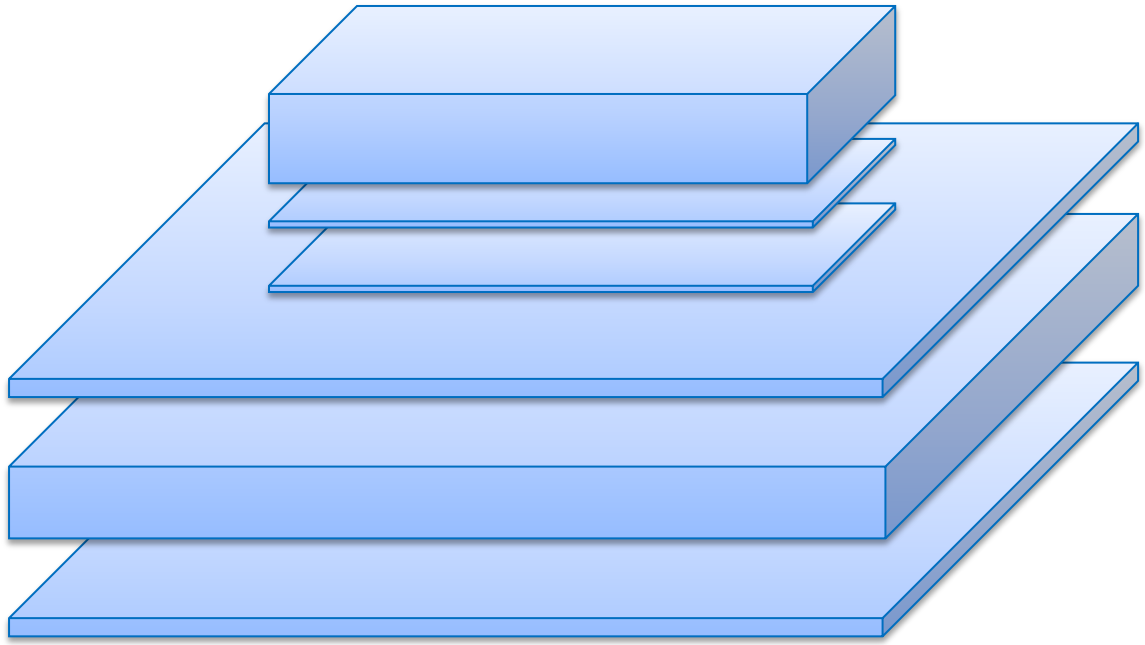
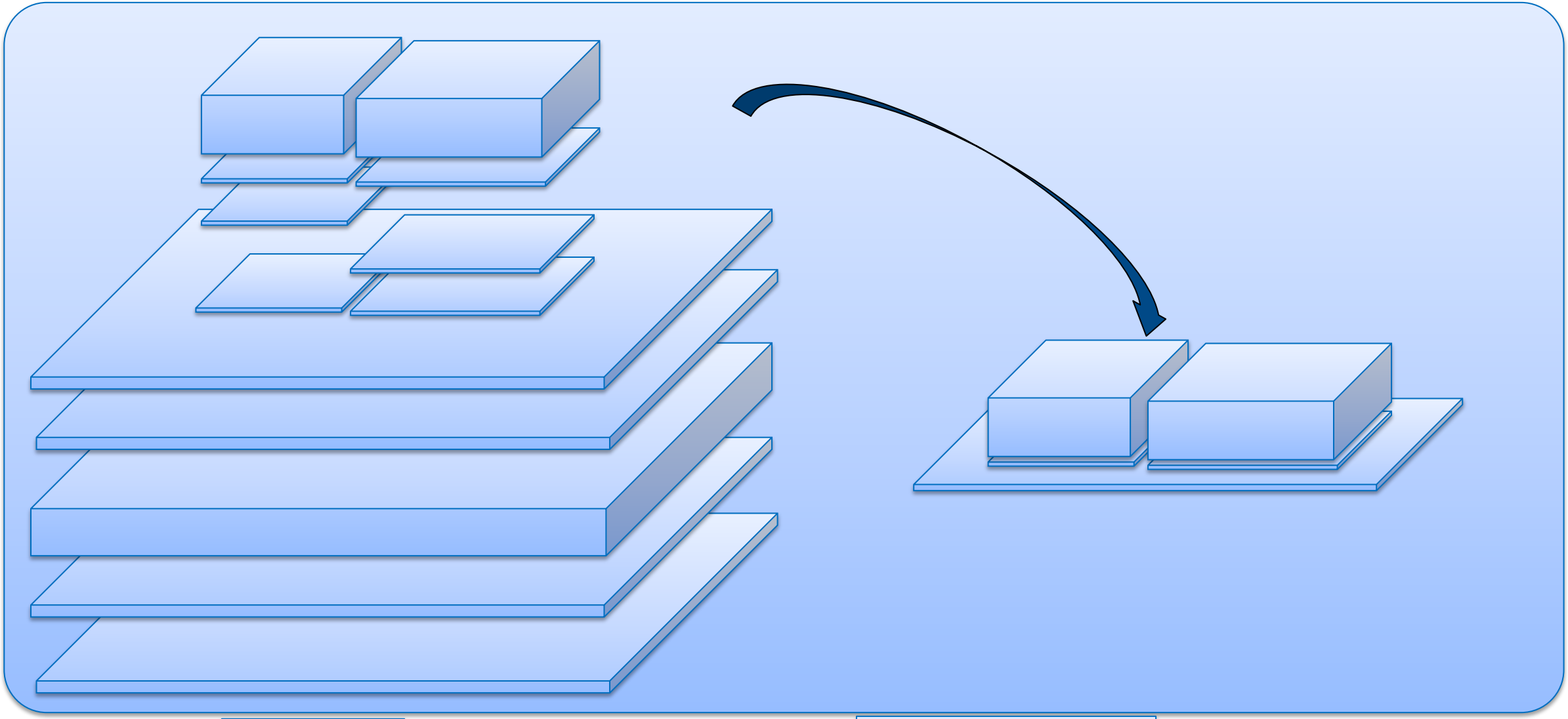


Design 2



The Design

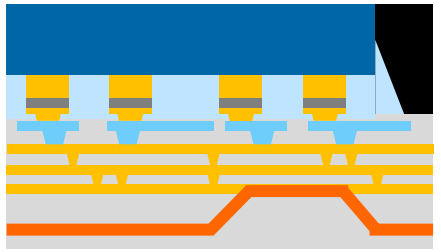
From Component Co-Design to System Co-Architecture



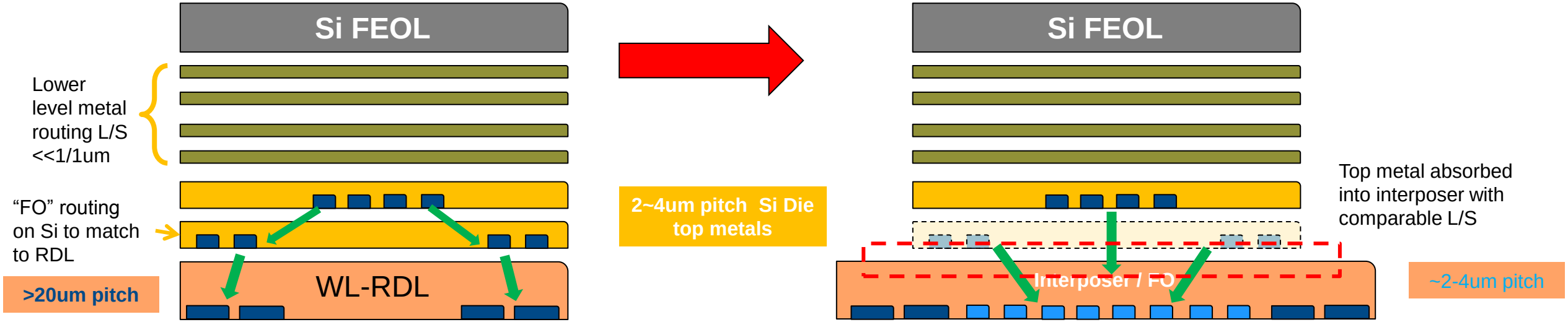
Baby 2.XD

Baby WLFO/PLFO

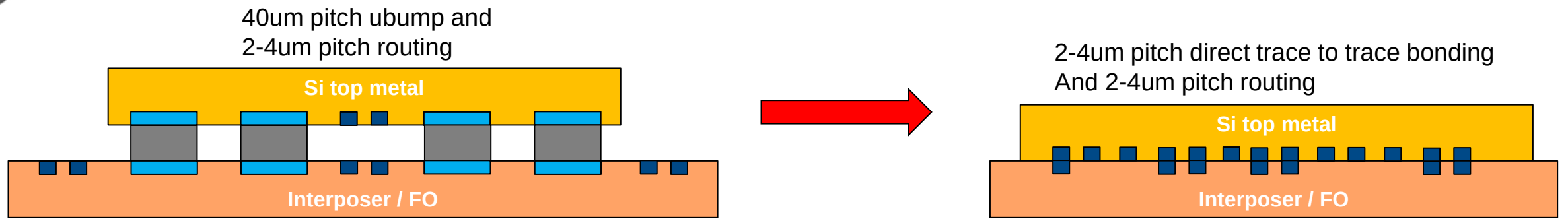
The Si ↔ Interposer Co-architecture



- Interposer L/S <= Si top metal and Substrate L/S
- Interposer area > Si area
- ➔ Interposer absorbs some layers from Si and substrate to reduce total layer count



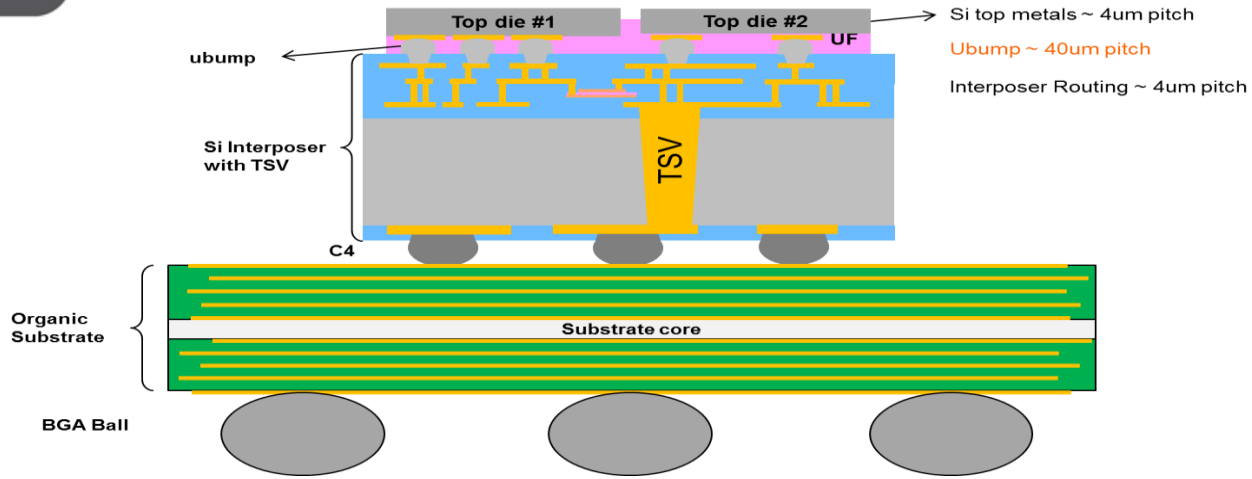
The REAL Si ↔ Interposer Co-architecture

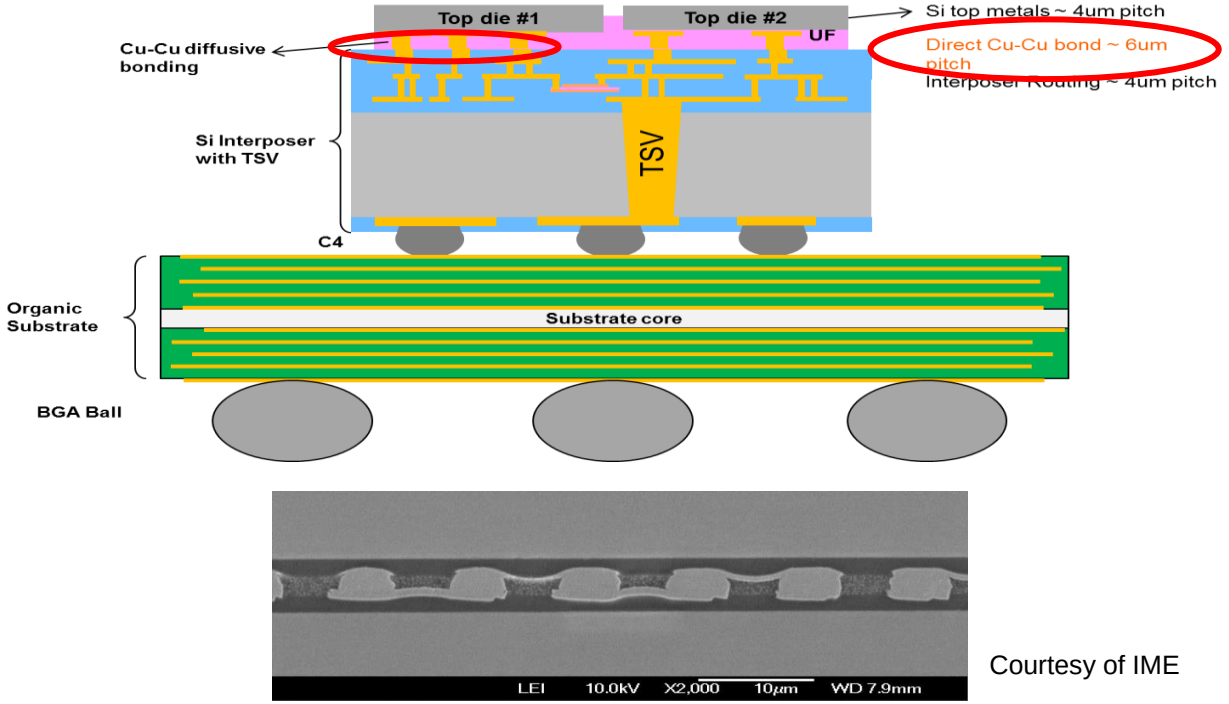


- Ubump bonded interposer structure is **NOT REAL** Si ↔ interposer co-design
- Si top metal still needs to FO to provide large pitch ubump pads
  - Large routing area taken by ubumps.
  - "FO" design is needed to redistribute the routing given the constrains.

- Bonding pitch ≅ routing pitch **IS REAL** Si ↔ interposer co-design

First Step: Direct Cu-Cu diffusive bonding technology

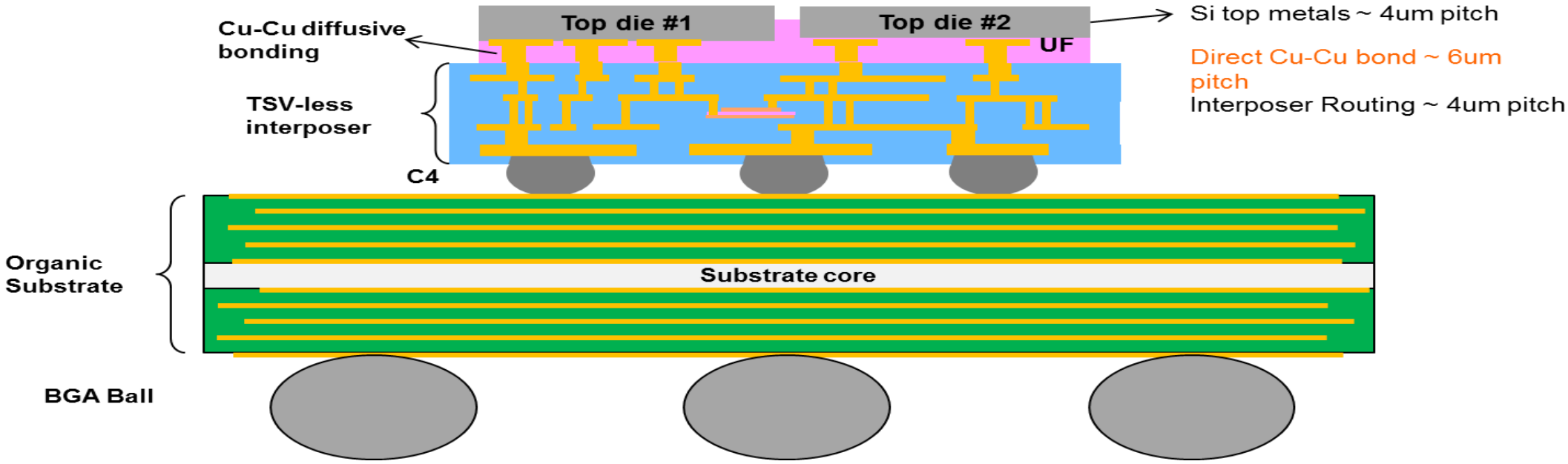




Courtesy of IME

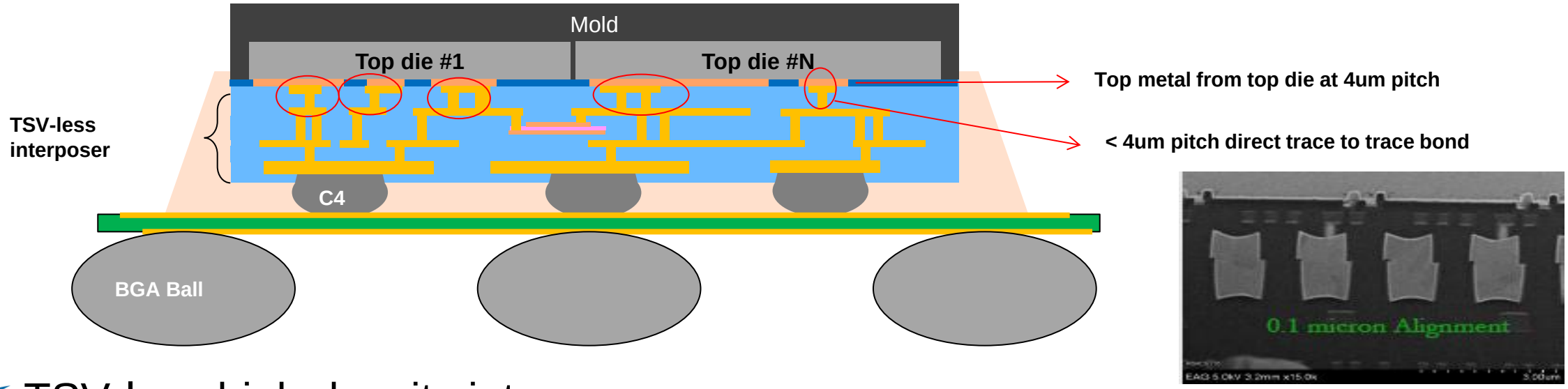
- Direct Cu-Cu bond
  - Cu bump to Cu bump diffusive bonding under low pressure and relatively low temperature.
  - Small bump pitch of 6um, comparable to die top metal <=4um pitch.
  - ➔Reduce the unnecessary FO from die to interposer.
  - ➔Move top metals to interposer
  - ➔Reduce total layer count and cost

Second Step : Direct Cu-Cu diffusive bond TSV-less WLFO



- Remove TSV for further cost reduction

Third Step : Bumpless TSV-less WLFO

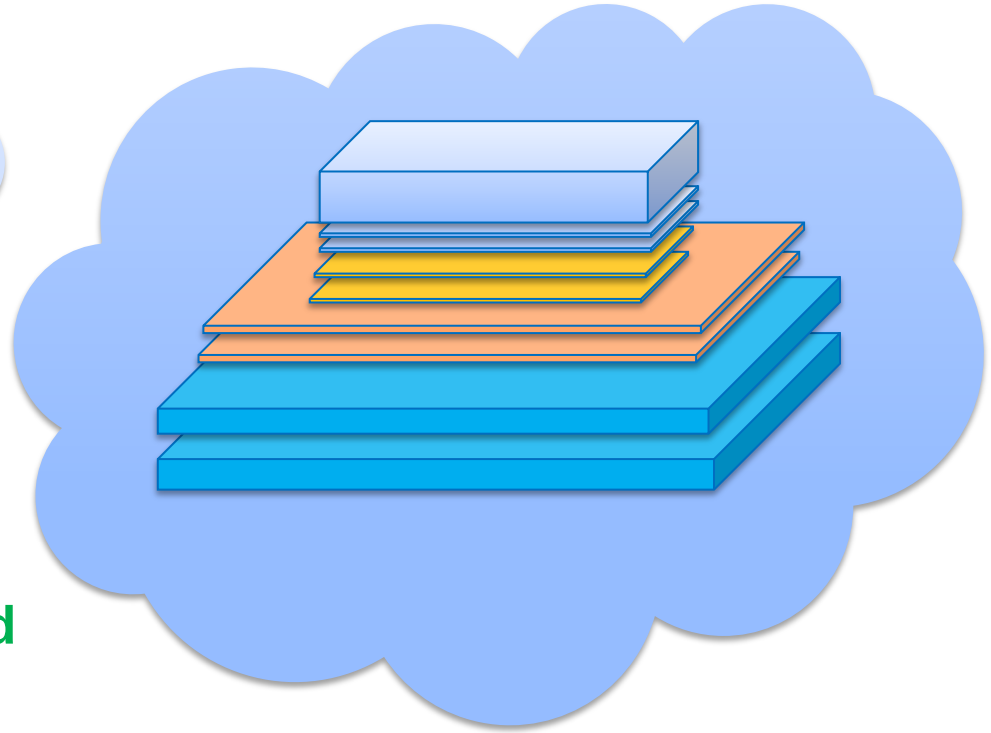


Courtesy of Ziptronix

- TSV-less high density interposer
- Direct die trace to die trace bonding < 4um pitch
  - No Die to interposer FO at all → easily exchange die top metals with interposer metals.
  - Remove bumping process → lower cost
  - Low temperature, low pressure, high throughput process → lower cost
- Reduced layer low cost coreless substrate

Summary: Co-architecture

- Co-development is a more advanced co-design
- Co-architecture is a more advanced co-development
- Different interconnect levels use different type metal circuitries
- Different type of metal circuities can be substituted
- Thicker metal is more efficient for power supply
- Thinner metal is more efficient for IO
- Reduced form factor reduces discontinuity
- Reduced discontinuity reduces overhead on interconnect circuitry



CO-ARCHITECTURE = LOW COST

Thank You