CMP for Advanced Packaging

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NCCAVS TFUG-CMPUG Joint Meeting
June 9, 2016
• Industry Trends
• Trends in Packaging
• Where is CMP used in next generation packaging?
• Examples and Observations
• Summary
What Drives Growth in Semiconductors?

• **Historical Growth Segments**
  - Computers and PC’s
  - Cell phones
  - High bandwidth infrastructure
  - Tablets

• **Recent or Emerging Growth Segments**
  - Smartphones
  - Internet of Things (IoT)
  - Power management and remote control
  - Medical applications
Semiconductor Revenue by Year

Source: WSTS, PwC analysis.

PC Wars

Internet Bubble

Global Financial Crisis

Cell phones & Tablets

Next??

June 2016

NCCAVS TFUG/CMPUG
Consolidation Continues to Change Landscape

Lam Research + Novellus

TriQuint + RF Micro-Devices → Qorvo

Cabot Microelectronics + NexPlanar

Microchip + Atmel

NXP + Freescale

Who’s Next ???
Historical Trends

- What drives decisions in the semiconductors? SPEED and COST!
  - New products must be ready on time for market launch
  - Long term efficiency improves competitive strength
- Moore’s Law dominated the CMOS industry for >40 years
  - Not affected by cycles, markets, analysts, or the economy
- Photolithography and CMP are two critical process technologies to contributed both cost and performance improvements
  - Photolithography enables SHRINKS
  - CMP enables more complex STACKS
- Recent evidence shows very few companies still trying to hold to Moore’s Law … most are choosing to pursue alternatives rather than continue to pursue 2D shrinks

Source: Intel Corporation
Some Definitions

- DIP = Dual In-line Package
- BGA = Ball Grid Array
- WLP = Wafer Level Packaging
- SoC = System on Chip
  - Increase functional integration by including sub-systems on a single chip.
  - Includes more than just digital functions, e.g. analog-to-digital converter, RF radio, power isolation, amplifiers, etc. built into the same die.
- SiP = System in Package
  - Combines multiple active electronic components of different functionality assembled into a single packaged unit.
  - SiP may integrate passives, MEMS, optical components, and other types of devices and may include multiple types of packaging technology.

3D Packaging Prediction from 2010

Source: Yole Development
Unlike retail or other types of packaging, the performance and reliability of an electronic component are closely tied to the proper design of the package.

Functions of Electronic Package

- **Signal Distribution**
- **Power Distribution**
- **Heat Dissipation**
- **Circuit Support And Protection**

Electronic packages are more than just a protective cover.

Source: Clemson Technical Report: CVEL-07-001
<table>
<thead>
<tr>
<th>Type of Package</th>
<th>Primary Use and Advantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard (DIP, BGA, etc.)</td>
<td>Cheap / Simple / Well established CMP or planarization not normally needed</td>
</tr>
<tr>
<td>Ceramic</td>
<td>Tolerates high temperature and mechanical force Greensheet + fill + sinter → No planarization need</td>
</tr>
<tr>
<td>WLP</td>
<td>Higher pinout density, thin RDL layers, thin wafers Leverages device fabrication process steps First layers of “packaging” done before singulation</td>
</tr>
<tr>
<td>2.5D (Interposers)</td>
<td>Material can be Si, polymer, or other Typical integration has 3 RDL layers Planarization required, esp. for TSV fabrication</td>
</tr>
<tr>
<td>3D</td>
<td>Dense functionality, but mating connections require careful design and planarization Thermal management is very difficult</td>
</tr>
<tr>
<td>Thin / Flexible Systems</td>
<td>Fast growing niche Requires ultrathin devices to flex w/o cracking Planarization of mating surfaces is essential</td>
</tr>
</tbody>
</table>
• **Major applications for WLP**
  - Smartphones (highest volume application)
  - Digital cameras and camcorders
  - Laptops and tablets
  - Medical
  - Automotive
  - Wearable electronics such as watch

• **WLP meets system packaging needs**
  - Small form factor
  - Need for low profile packages
  - Lower cost (less material)

• **Form Factor is key**
  - Low profile
  - Limited space on PCB

*Source: Techsearch International (2015)*
Sometimes called 2.5D integration

Allows mixture of device types, pinout spacing, and component thicknesses

Common versions are Si, glass, or polymer

Frequently include at least 3 wiring levels (RDL) and may include thru vias as well

Source: Hopkins, University of Buffalo (2009)
<table>
<thead>
<tr>
<th>Relative Position</th>
<th>Planar Need</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral</td>
<td>None</td>
</tr>
<tr>
<td>Offset stack</td>
<td>Low</td>
</tr>
<tr>
<td>Stacked</td>
<td>High</td>
</tr>
<tr>
<td>Varies</td>
<td>Varies</td>
</tr>
<tr>
<td>Single layer</td>
<td>Low</td>
</tr>
<tr>
<td>Stacked</td>
<td>High</td>
</tr>
</tbody>
</table>

iPhone 6S

Well over 50% of device content does not require leading edge fab capability

Digital CMOS, MEMS, RF, power, and analog are combined through advanced packaging technology to meet a desired form factor.
Example: 3D Packaging in a Ceramic Module

Source: Hopkins, University of Buffalo (2009)
Semiconductor content in new automobiles continues to increase for sensors, control systems, and more.

The number of sensors is currently 60-100 per car ... and is projected to more than double in the next 8-10 years.

Source: Semiengineering.com (Bernard Murphy, Sept 2015)
Internet of Things
IoT

Source: WSTS, PwC analysis.

SEMICONDUCTOR DRIVER – INTERNET OF THINGS

June 2016
What is the Internet of Things (IoT)

• Google Definition
  • A proposed development of the Internet in which everyday objects have network connectivity, allowing them to send and receive data.

• TechTarget.com Explanation
  • The Internet of Things (IoT) is a system of interrelated computing devices, mechanical and digital machines, objects, animals or people that are provided with unique identifiers and the ability to transfer data over a network without requiring human-to-human or human-to-computer interaction.
  • IoT has evolved from the convergence of wireless technologies, micro-electromechanical systems (MEMS), microservices and the Internet. The convergence has helped tear down the silo walls between operational technology (OT) and information technology (IT), allowing unstructured machine-generated data to be analyzed and drive system improvements.
Strong growth predicted in IoT for next 5 years

Many applications are enabled by MEMS sensors

Other Examples of IoT

Some Sensor Data Analytics Applications

- **Keg Data**: Track the temperature and remaining amount of beer in a keg. (Source: Freescale FTF 2015)
- **HorsesenseShoes**: Wearables that save lives by detecting joint problems like laminitis early. (Source: Freescale presentation at Semi Industry Forum on IoT (Oct 2015))
- **Freescale FTF 2015**: Never boil over again. Vibration detection using an accelerometer helps adjust the temperature.
- **BAM Labs**: Wake up rested and energized. Sleep cycle monitoring helps optimize when your alarms should wake you.

Source: Freescale presentation at Semi Industry Forum on IoT (Oct 2015)
IoT benefits from packaging innovation

- Expansion of IoT/IIoT means an increased number of sensors, but also more connectivity, signal processing, and data storage
- Primary device requirements are low power and low cost
- No single package format
  - Many applications may adopt system-in-package (SiP)
  - Many just SMT modules on FR-4 board, not counted as SiP but as system-in-module (SiM)
- One main reason IoT/IIoT is expanding rapidly is the low cost of sensors and multi-die packages and modules

Source: SPIL.
What Factors Will Influence IoT Growth Rate?

- **Security and Privacy Control**
  - Especially important for health care, retail, and critical systems data

- **Interoperability**
  - Must have a manageable number of standards
  - Software apps may hold key to cross-platform integration

- **Reduced Cost**
  - Initial focus is on IC components and sensors
  - Lower packaging, assembly and distribution costs are also critical

- **Low Power**

- **Embedded Processing**
  - Can add distributed intelligence to system (local interpretation / faster decisions)
  - Reduces load on communication bandwidth

*Source: Semico Research (Oct 2015)*
### CMP Supplier Complexity

#### Process Applications:

<table>
<thead>
<tr>
<th>Year</th>
<th>Qty</th>
<th>CMOS</th>
<th>New Apps</th>
<th>Substrate/Epi</th>
</tr>
</thead>
<tbody>
<tr>
<td>1995</td>
<td>Qty ≤ 2</td>
<td>Oxide</td>
<td>MEMS</td>
<td>GaAs &amp; AlGaAs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tungsten</td>
<td>Nanodevices</td>
<td>poly-AlN &amp; GaN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cu (Ta barrier)</td>
<td>Direct Wafer Bond</td>
<td>InP &amp; InGaP</td>
</tr>
<tr>
<td>2001</td>
<td>Qty ≤ 5</td>
<td>Oxide</td>
<td>Noble Metals</td>
<td>CdTe &amp; HgCdTe</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tungsten</td>
<td>Shallow Trench</td>
<td>Ge &amp; SiGe</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cu (Ta barrier)</td>
<td>Poly silicon</td>
<td>3D Packaging</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Shallow Trench</td>
<td>Low k</td>
<td>SiC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Polysilicon</td>
<td>Through Si Vias</td>
<td>Capped Ultra Low k</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tungsten</td>
<td>Ultra Thin Wafers</td>
<td>Diamond &amp; DLC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Shallow Trench</td>
<td>Metal Gates</td>
<td>NiFe &amp; NiFeCo</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Polysilicon</td>
<td>Gate Insulators</td>
<td>Al &amp; Stainless</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tungsten</td>
<td>High k Dielectrics</td>
<td>Lithium Niobate</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Polysilicon</td>
<td>Ir &amp; Pt Electrodes</td>
<td>Quartz &amp; Glass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tungsten</td>
<td>Novel barrier metals</td>
<td>Polymers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tungsten</td>
<td>Integrated Optics</td>
<td>Titanium</td>
</tr>
<tr>
<td></td>
<td>Qty ≥ 40</td>
<td>Tungsten</td>
<td>Magnetics</td>
<td>Sapphire</td>
</tr>
</tbody>
</table>

#### Consumables and Controls

- **PADS**
- **SLURRIES**
- **ABRASIVES**
- **CONDITIONING DISCS**
- **BRUSHES & CLEAN CHEMISTRIES**
- **COMPONENTS**
CMP is typically used in a damascene manner to planarize and isolate the vias after conductor deposition from one side.

TSV’s can be filled with any of several conductive materials.

- Most common options are copper and polysilicon.
- Final choice depends on dimensions, operating voltage and current, frequency, temperature requirements, plus other integration factors.

CMP is used again after thinning to help expose and planarize the original “bottom” of the TSV’s – called TSV Reveal.
Example: Large Cu TSV for Interposer

Background

- Large via needed for design (75-100um diameter)
- Via last with extremely thick Cu plating (about 45 um)
- Previous CMP using standard stock removal slurries resulted in very long polish times (45 mins to 1 hour)

Goals for CMP optimization phase

- Test new high-rate Cu slurry for much shorter clear times
- Verify reasonable selectivity to nitride after barrier clear
- Dishing <1 µm across 80 µm via
- Good surface finish on both Cu and dielectric
Typical Results after CMP

Via Diameter = 80 microns
Field area = nitride and via liner = oxide

Source: RTI International, Inc.
Process module following completion of device layers on front side

TSV must be exposed to make contact and/or continue patterning next layers (RDL) from wafer backside.

Various integrations are viable with combinations of backgrind, etch, selective CMP, or non-selective CMP.

- Some approaches require 2 or 3 steps of CMP

Examples from two alternative integrations

- Reveal Using Non-selective CMP
- Reveal CMP Following Si Etch
Process flow for Si interposer with TSVs: (a) TSV etch, isolation layer, plating, and via CMP, (b) Frontside multi-level metallization, (c) Wafer thinning and TSV reveal, (d) Backside metallization.

Source: RTI International, Inc.
Backgrind for Substrate Thinning

Carrier Mount
- TSV wafers mounted face down on carrier wafers

Backgrind
- TSV wafers thinned using backgrind stopping approx 3-15um before hitting TSVs
- Reveal CMP performs dual function of removing grind damage layer and remaining bulk Si then exposing center conductor of TSV’s

Backgrind stops in Si before reaching TSV’s
Expose & Planarize TSVs

Several exposed materials
- Single crystal silicon
- Oxide (or other liner)
- Barrier metal
- Copper

Carrier Wafer
Need to polish far enough into TSVs to remove rounded profile at base of vias

Source: RTI International, Inc.
Customized CMP process was used to planarize final surface comprised of Si+Ox+barrier+Cu.

Source: RTI International, Inc.
Completed interposer test structure: large via diameter, 100um thickness.

Structure has 2 frontside metal layers (4um Cu) and 1 backside metal.

Source: RTI International, Inc.
After backgrind, bulk Si removed by an etch process

- Can be dry etch or wet etch, but must be highly selective to oxide
- Installed equipment already available
- Proceeds until 2-5um of encased via “bumps” protrude

Layer of dielectric is usually deposited to protect field areas

Primary goal of CMP is to planarize bumps and expose the Cu cores

One benefit of this approach is to reduce total CMP polish time

- Less sensitive to uniformity issues
- Faster throughput and lower CMP process cost
CMP becomes relatively short “kiss” polish

Pre-CMP Step Height
22,000 Ang

Post-CMP Step Height
60 Ang
CMP Requirements Related to Packaging

- High stock removal rates are often needed for acceptable throughput
- Topography demands are much less stringent than CMOS interconnect
- Defectivity is defined at a different level
- Lower cost is a MUST
- Wafer thinning and TTV control are alternate types of planarization
- New slurries may be needed for new materials, esp. for interposers and flexible electronics
- Advanced packaging and TSV applications have huge volume potential, but still struggling to define preferred integration that can meet cost expectations
2016 Drivers for SiP Adoption

- Miniaturization
  - Form factor and functionality density (package height, footprint)
- Heterogeneous technology integration
  - Digital, RF, analog, power, and sensor integration
- Mixed process technology
- System performance
  - Noise reduction and higher speed
- System flexibility, features, and configurability
- Total system cost reduction
  - Package/device cost
  - Development cost
  - Time to market

Adapted from source: Techsearch International
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