

CMP for Advanced Packaging

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NCCAUS TFUG-CMPUG Joint Meeting
June 9, 2016



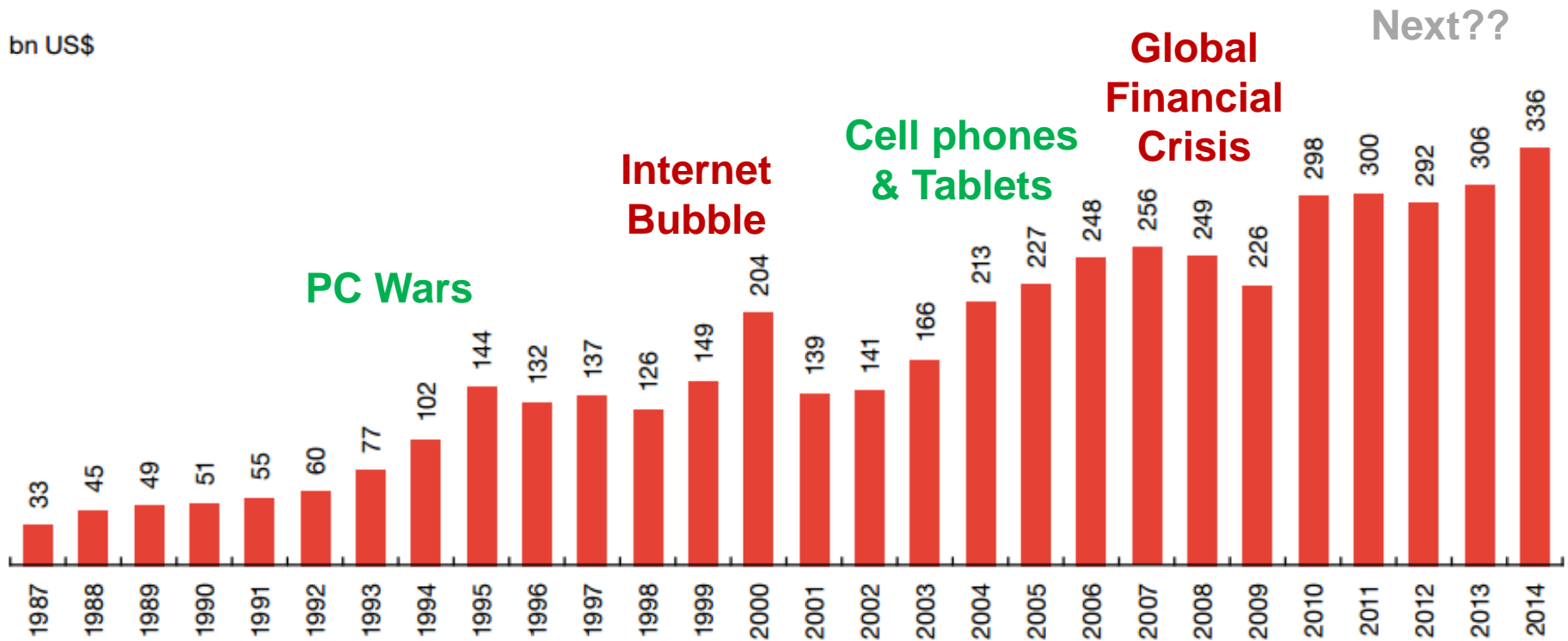
Semiconductor Equipment

Spare Parts and Service

Foundry

- Industry Trends
- Trends in Packaging
- Where is CMP used in next generation packaging?
- Examples and Observations
- Summary

- Historical Growth Segments
 - Computers and PC's
 - Cell phones
 - High bandwidth infrastructure
 - Tablets
- Recent or Emerging Growth Segments
 - Smartphones
 - Internet of Things (IoT)
 - Power management and remote control
 - Medical applications

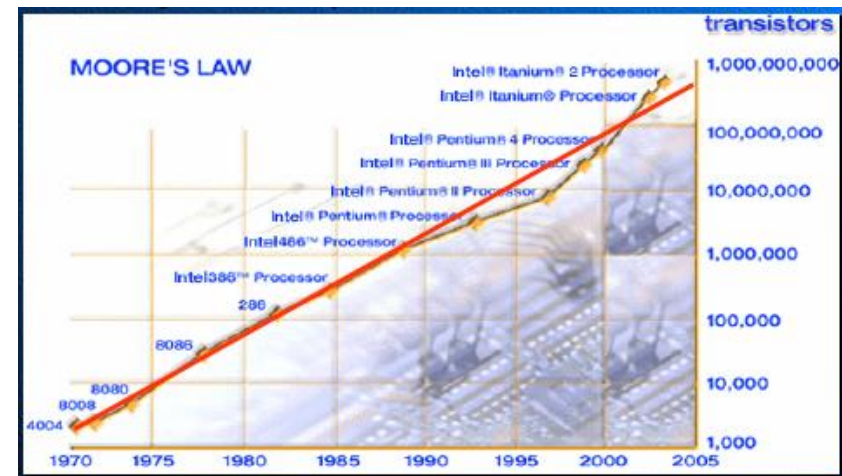


Source: WSTS, PwC analysis.

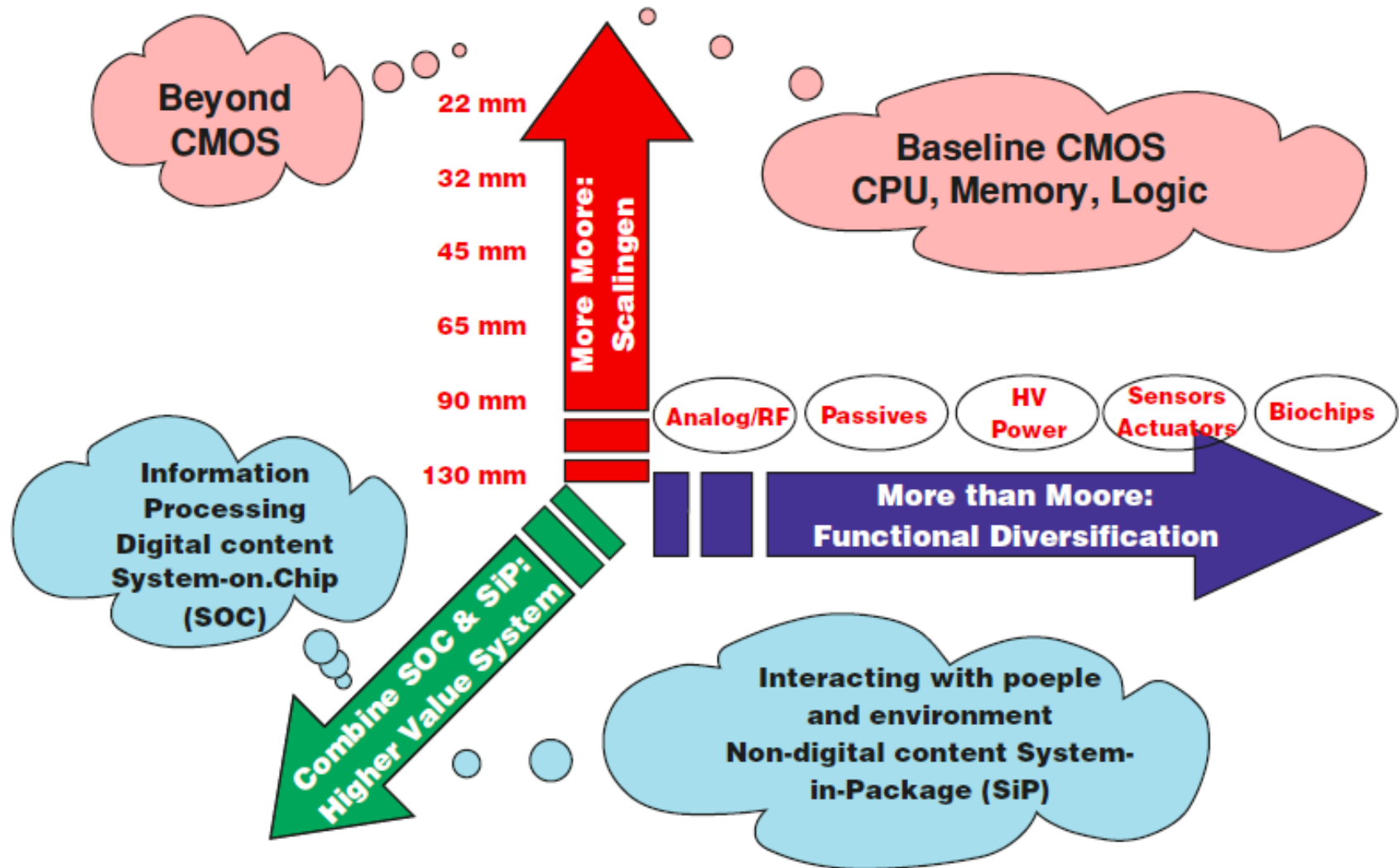


Who's Next ???

- What drives decisions in the semiconductors? **SPEED and COST!**
 - New products must be ready on time for market launch
 - Long term efficiency improves competitive strength
- Moore's Law dominated the CMOS industry for >40 years
 - Not affected by cycles, markets, analysts, or the economy
- Photolithography and CMP are two critical process technologies to contributed both cost and performance improvements
 - Photolithography enables SHRINKS
 - CMP enables more complex STACKS
- Recent evidence shows very few companies still trying to hold to Moore's Law ... most are choosing to pursue alternatives rather than continue to pursue 2D shrinks



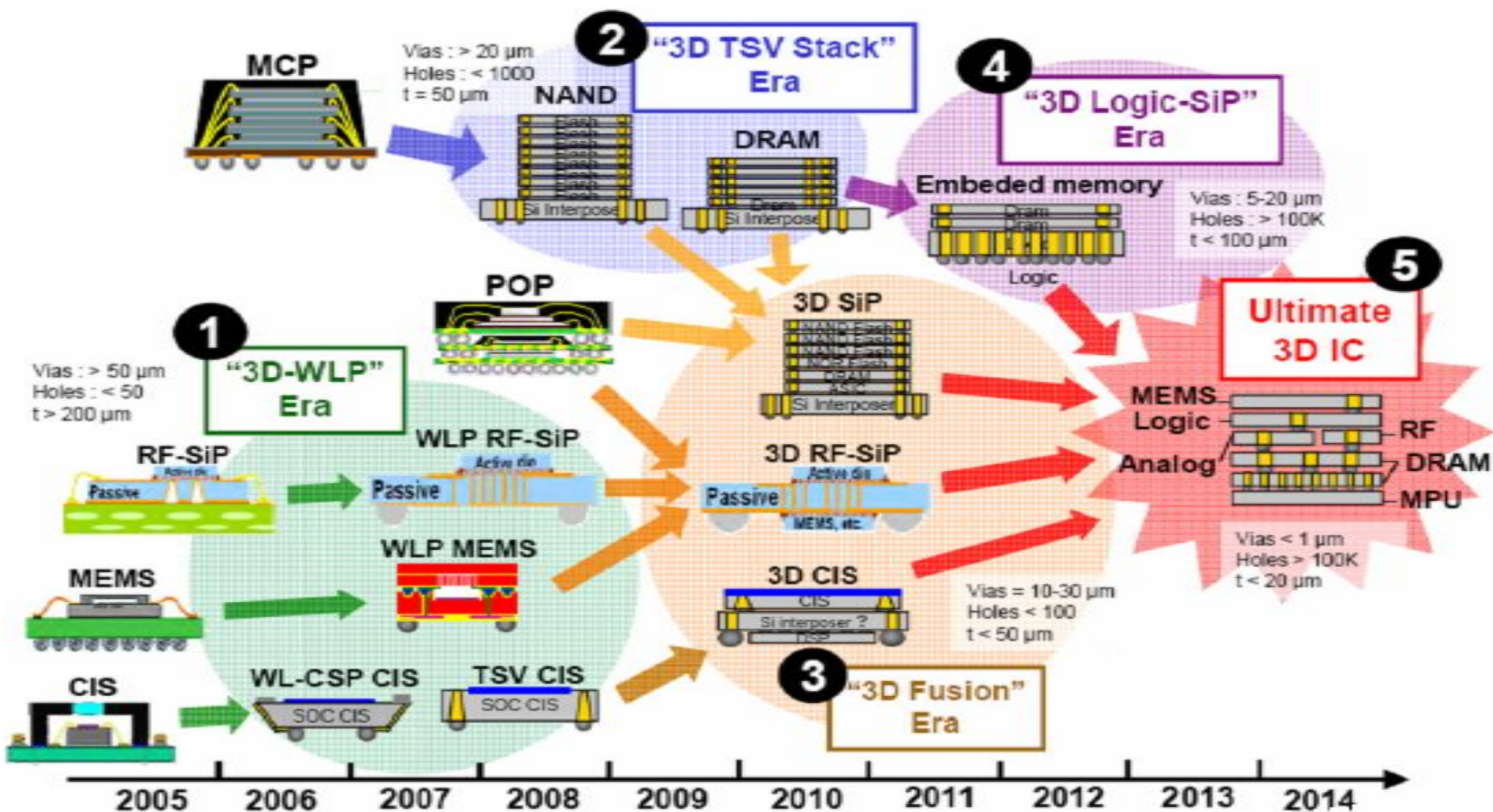
Source: Intel Corporation



Source: Wolter - Bio and Nano Packaging Techniques for Electron Devices

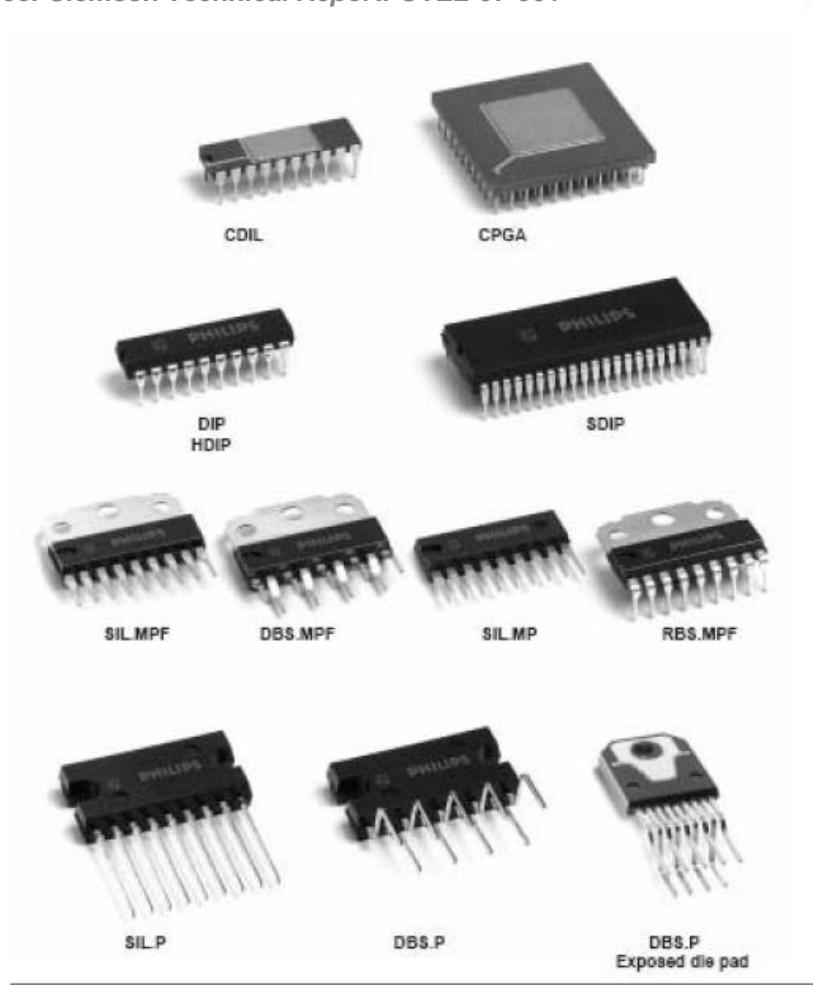
- DIP = Dual In-line Package
- BGA = Ball Grid Array
- WLP = Wafer Level Packaging
- SoC = System on Chip
 - Increase functional integration by including sub-systems on a single chip.
 - Includes more than just digital functions, e.g. analog-to-digital converter, RF radio, power isolation, amplifiers, etc. built into the same die.
- SiP = System in Package
 - Combines multiple active electronic components of different functionality assembled into a single packaged unit.
 - SiP may integrate passives, MEMS, optical components, and other types of devices and may include multiple types of packaging technology.

Source: Wolter - Bio and Nano Packaging Techniques for Electron Devices

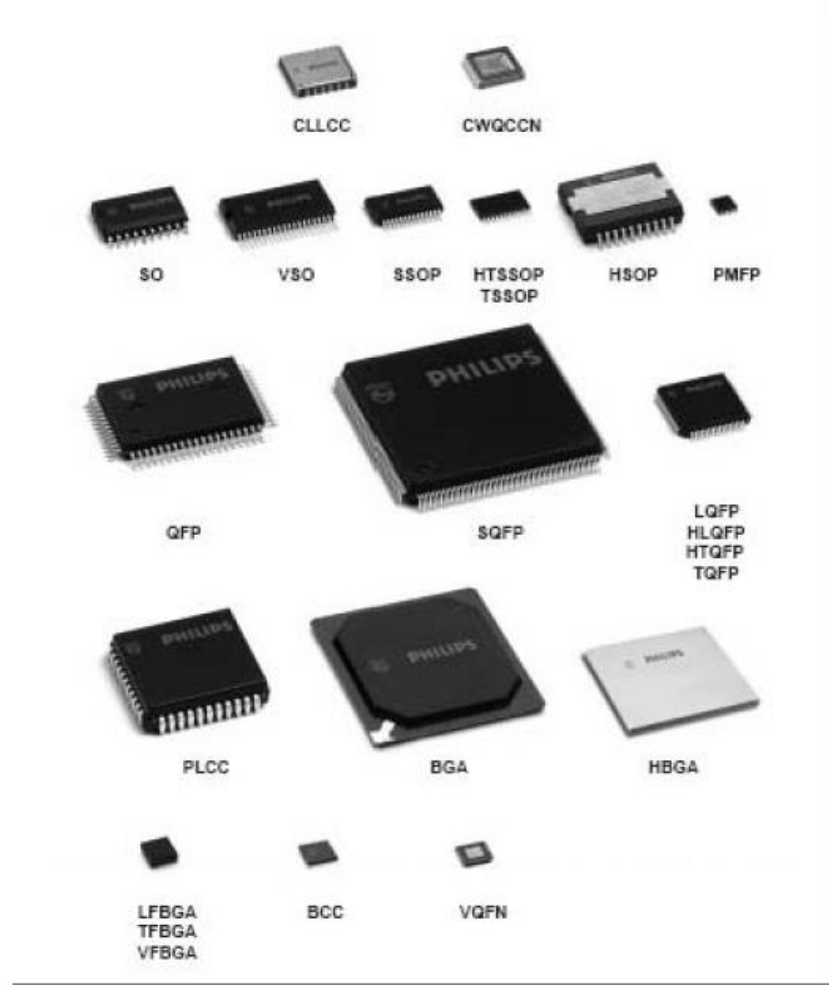


Source: Yole Development

Source: Clemson Technical Report: CVEL-07-001

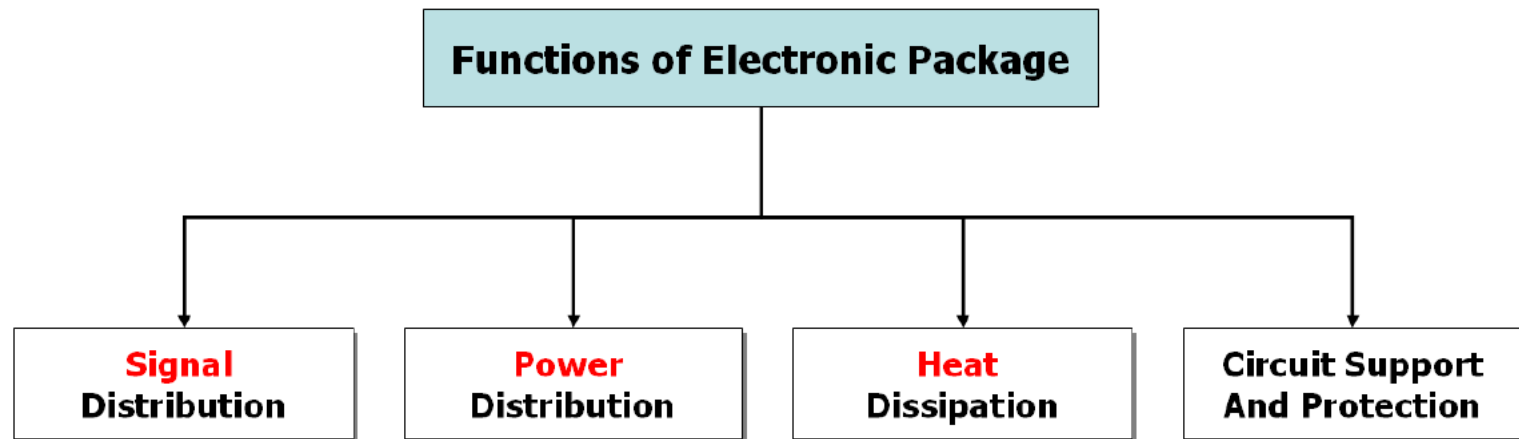


Thru-Hole Mounted



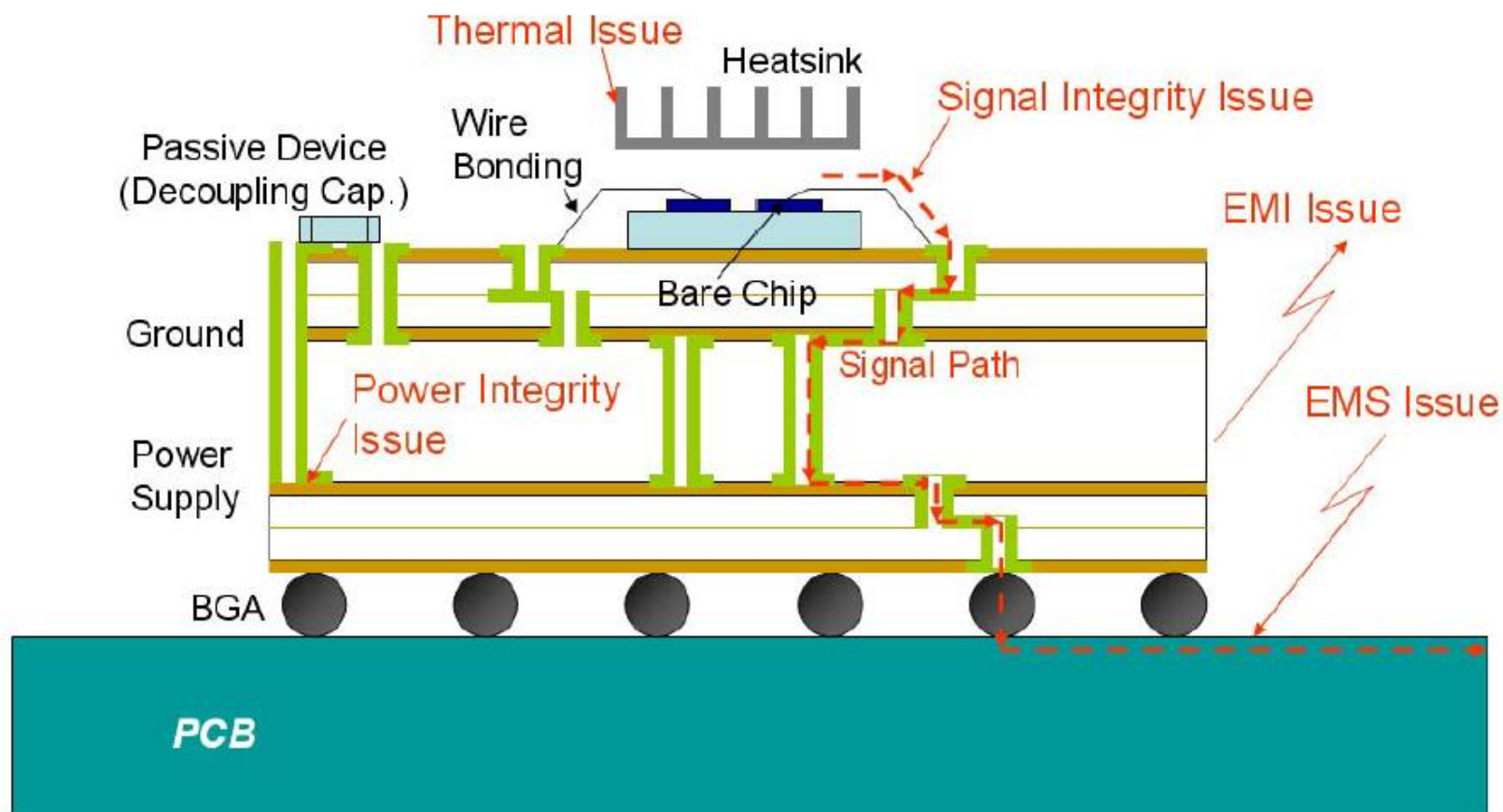
Surface Mounted

Unlike retail or other types of packaging, the performance and reliability of an electronic component are closely tied to the proper design of the package.



Electronic packages are more than just a protective cover.

Source: Clemson Technical Report: CVEL-07-001



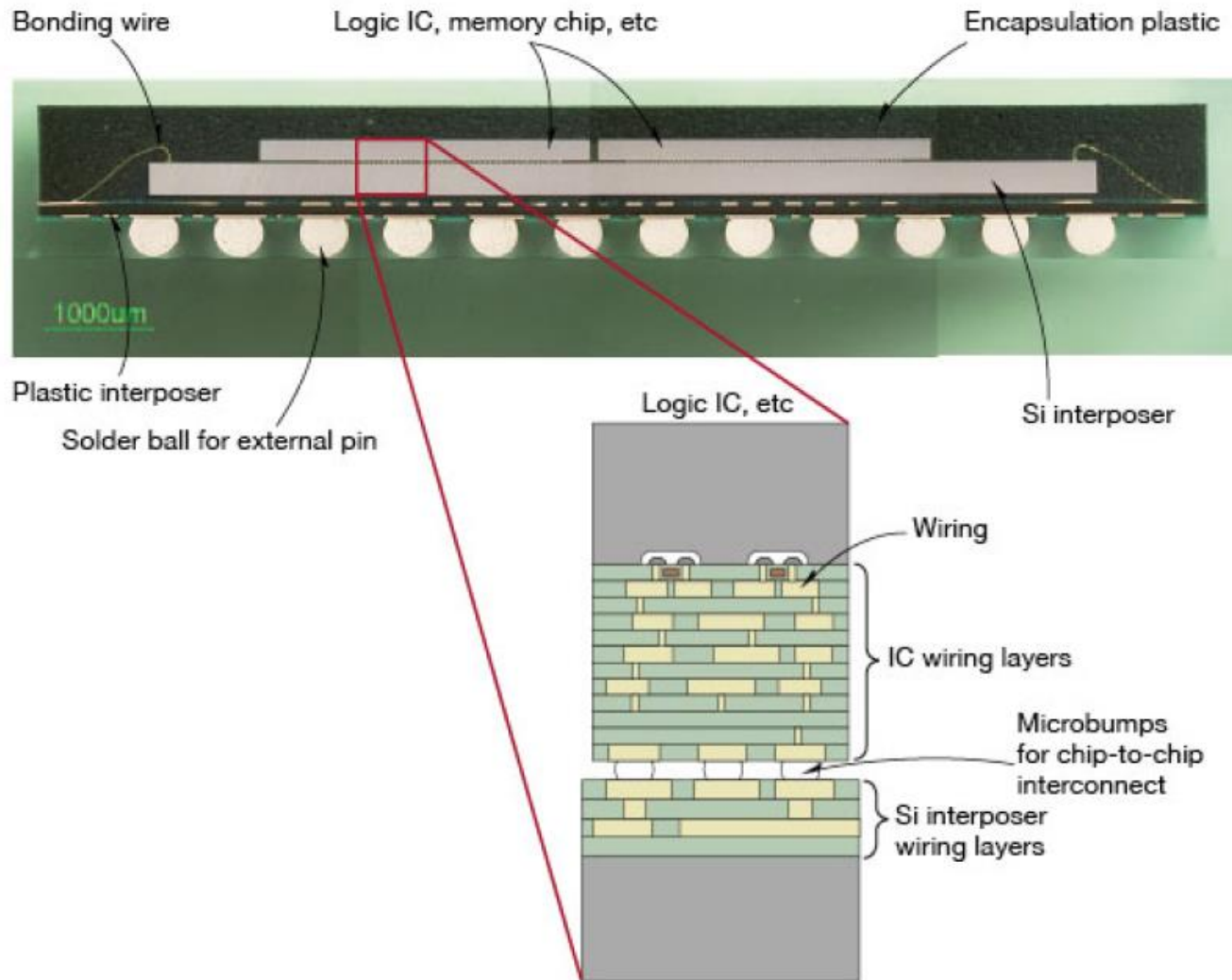
Source: Clemson Technical Report: CVEL-07-001

Type of Package	Primary Use and Advantages
Standard (DIP, BGA, etc.)	Cheap / Simple / Well established CMP or planarization not normally needed
Ceramic	Tolerates high temperature and mechanical force Greensheet + fill + sinter → No planarization need
WLP	Higher pinout density, thin RDL layers, thin wafers Leverages device fabrication process steps First layers of “packaging” done before singulation
2.5D (Interposers)	Material can be Si, polymer, or other Typical integration has 3 RDL layers Planarization required, esp. for TSV fabrication
3D	Dense functionality, but mating connections require careful design and planarization Thermal management is very difficult
Thin / Flexible Systems	Fast growing niche Requires ultrathin devices to flex w/o cracking Planarization of mating surfaces is essential

- **Major applications for WLP.....**
 - Smartphones (highest volume application)
 - Digital cameras and camcorders
 - Laptops and tablets
 - Medical
 - Automotive
 - Wearable electronics such as watch
- **WLP meets system packaging needs**
 - Small form factor
 - Need for low profile packages
 - Lower cost (less material)
- **Form Factor is key**
 - Low profile
 - Limited space on PCB



Source: Techsearch International (2015)



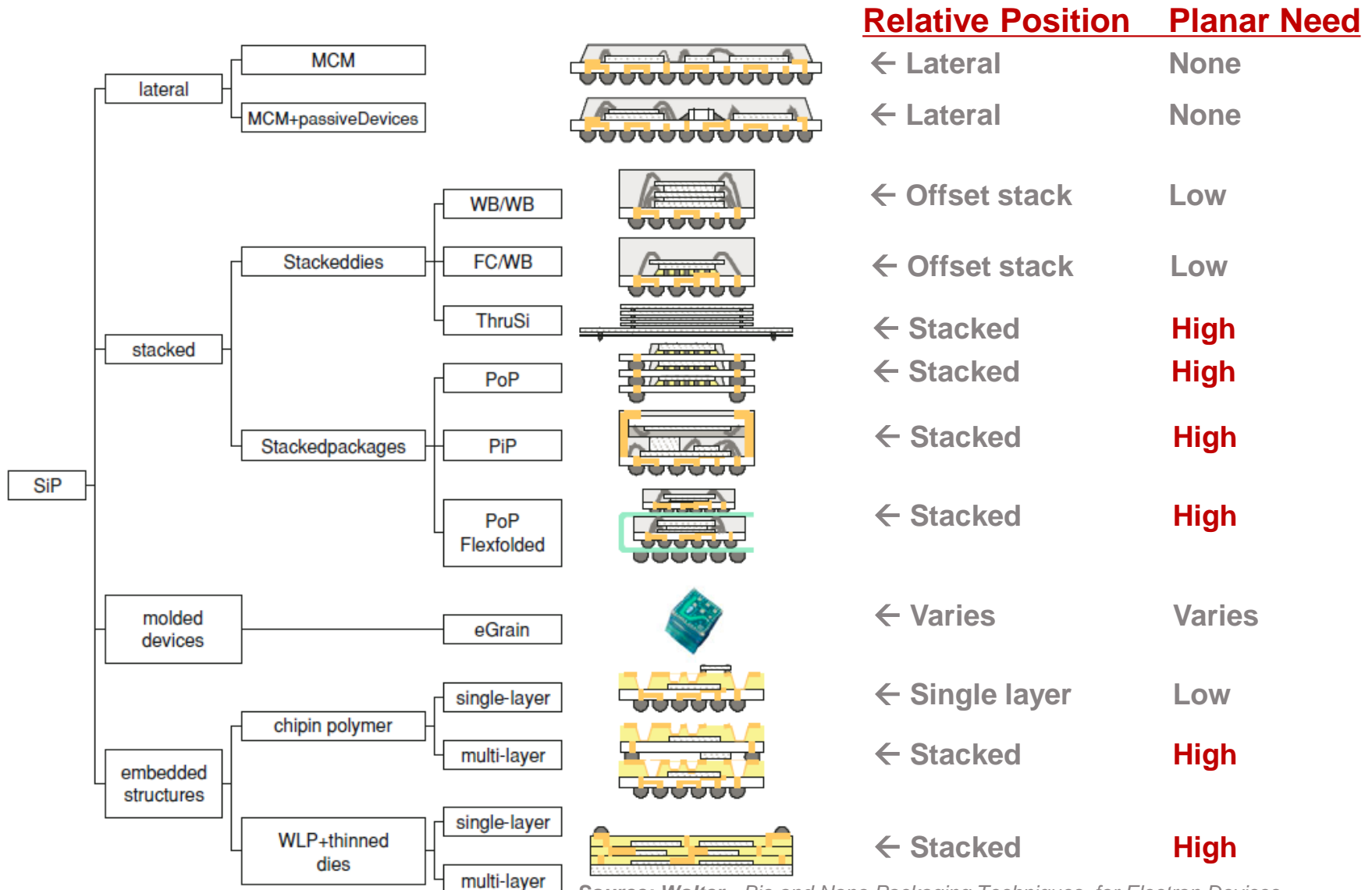
Sometimes called
2.5D integration

Allows mixture of
device types,
pinout spacing,
and component
thicknesses

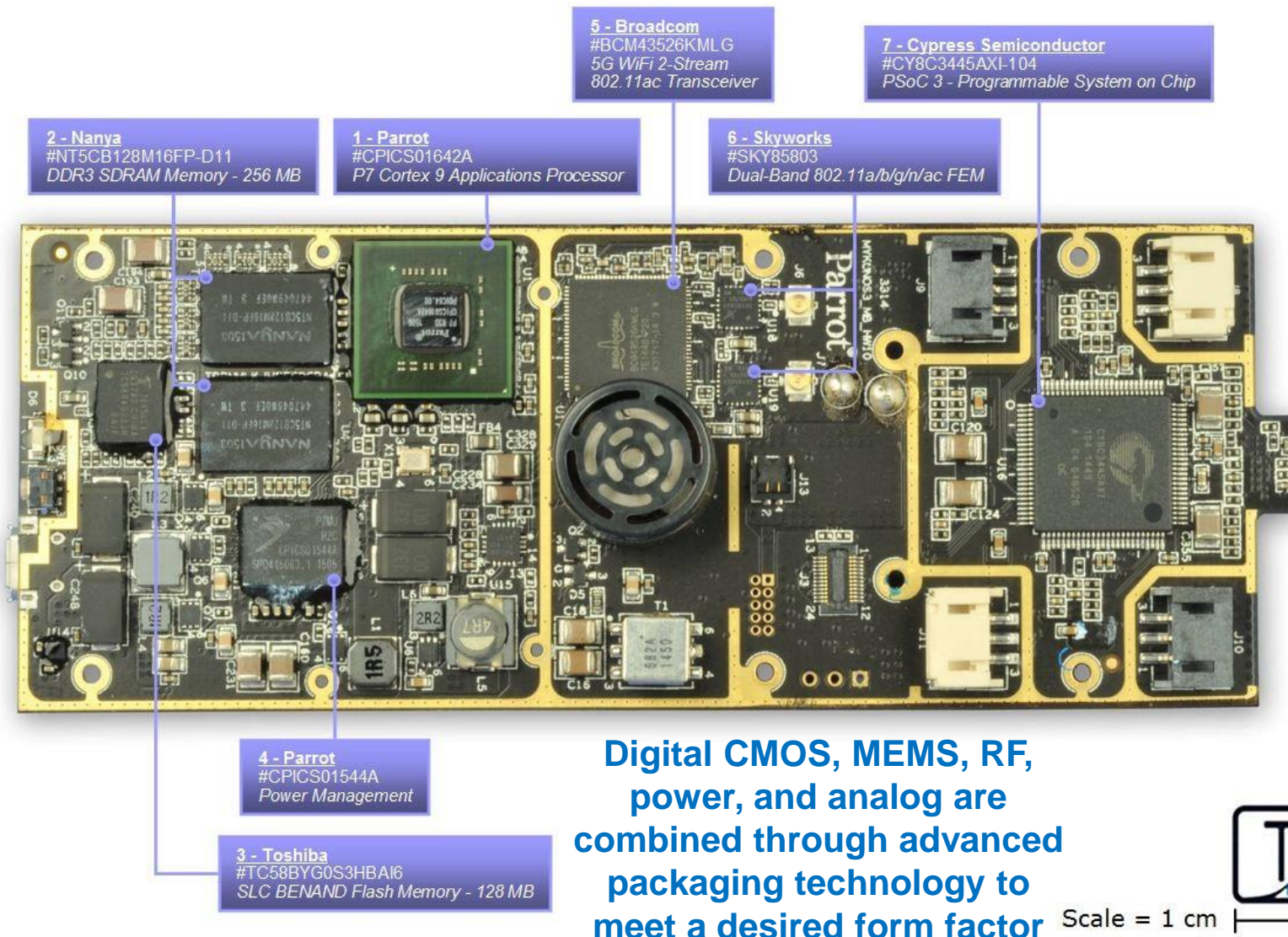
Common versions
are Si, glass, or
polymer

Frequently include
at least 3 wiring
levels (RDL) and
may include thru
vias as well

Source: Hopkins, University of Buffalo (2009)



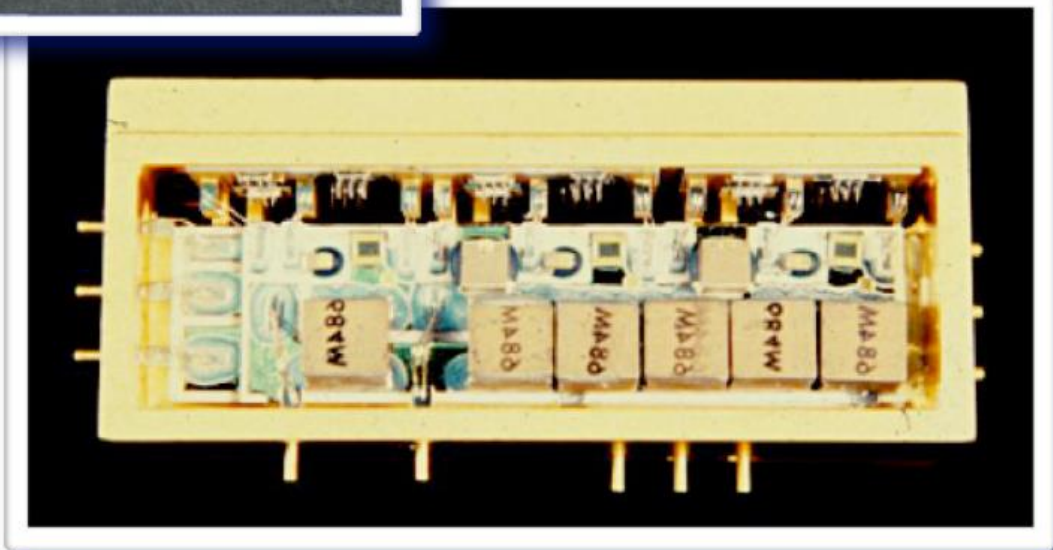
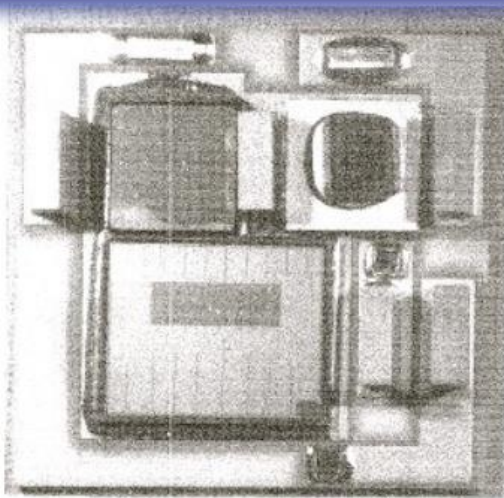
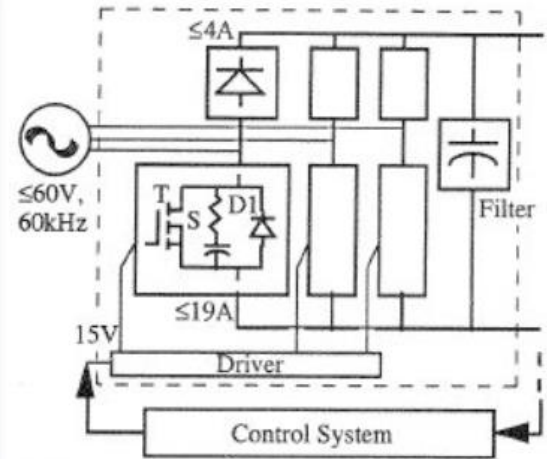
Source: Wolter - Bio and Nano Packaging Techniques for Electron Devices



iPhone 6S

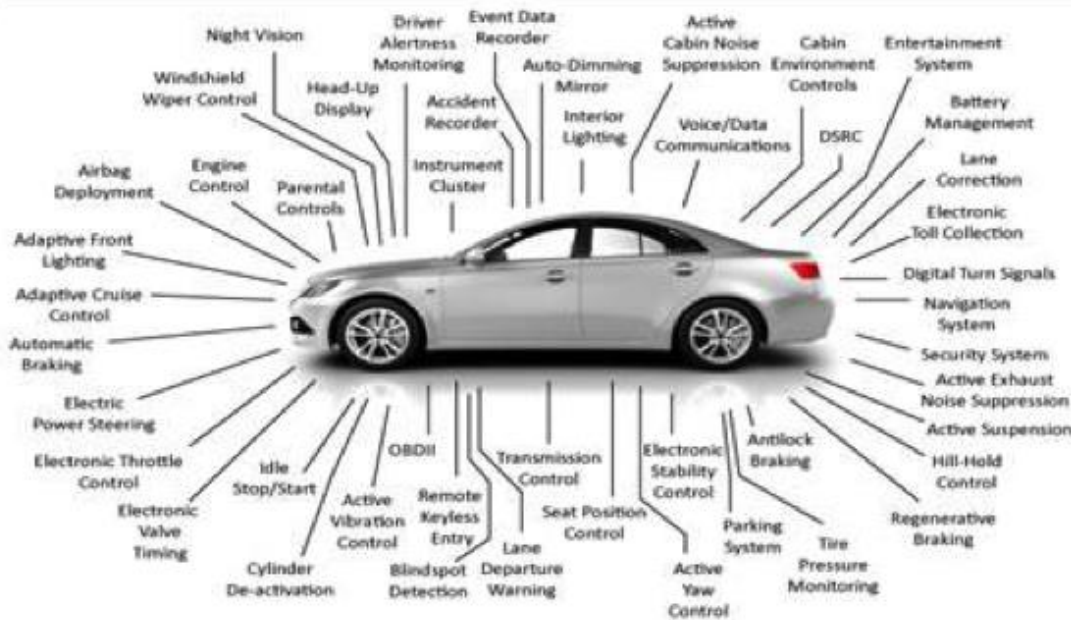
Well over
50% of
device
content
does not
require
leading
edge fab
capability





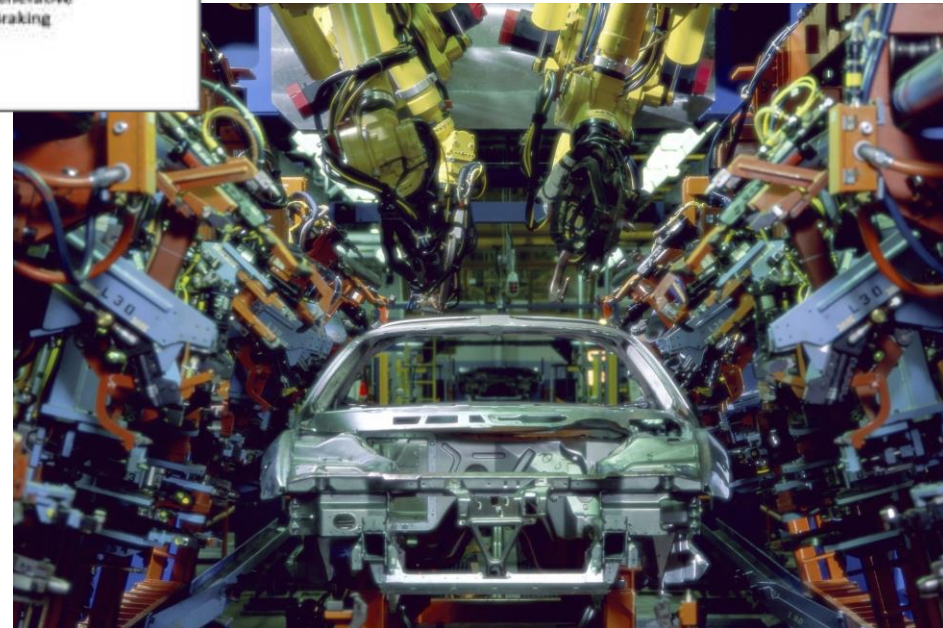
Source: Hopkins, University of Buffalo (2009)

Semiconductor content in new automobiles continues to increase for sensors, control systems, and more

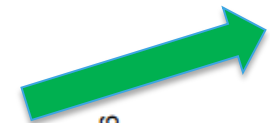


Source: Semiengineering.com (Bernard Murphy, Sept 2015)

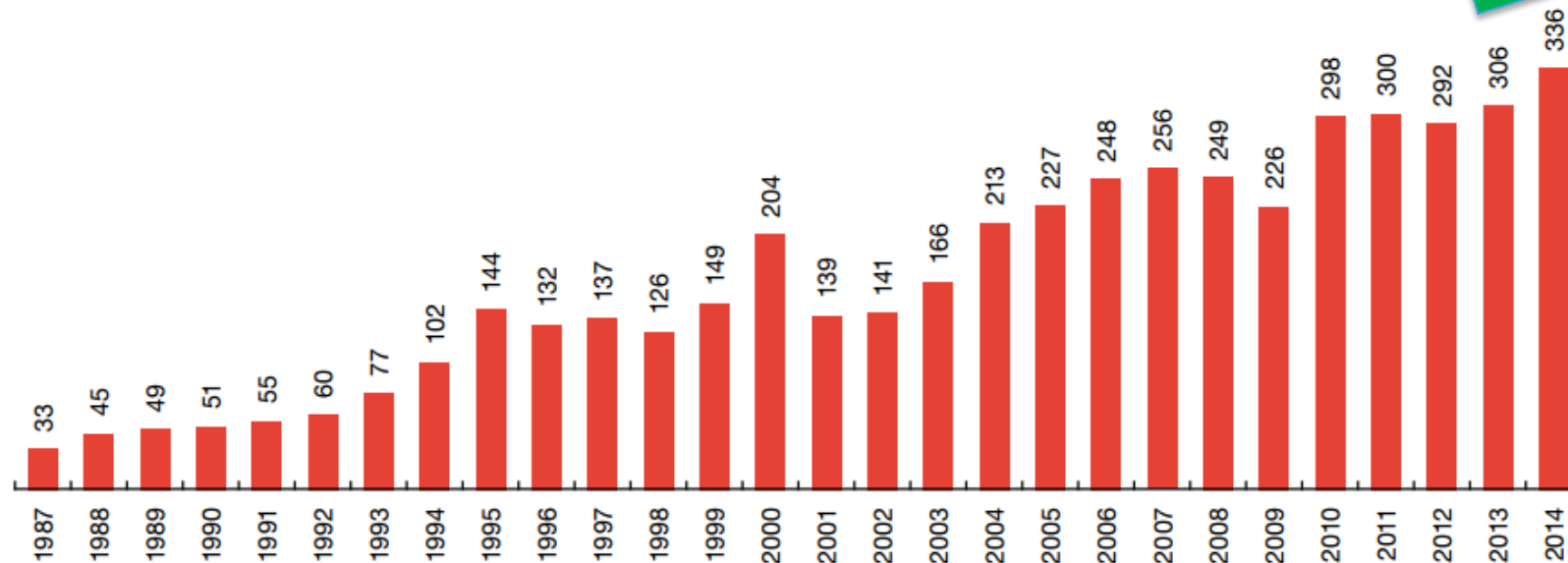
The number of sensors is currently 60-100 per car ... and is projected to more than double in the next 8-10 years.



Internet of Things
IoT



bn US\$



Source: WSTS, PwC analysis.

- Google Definition

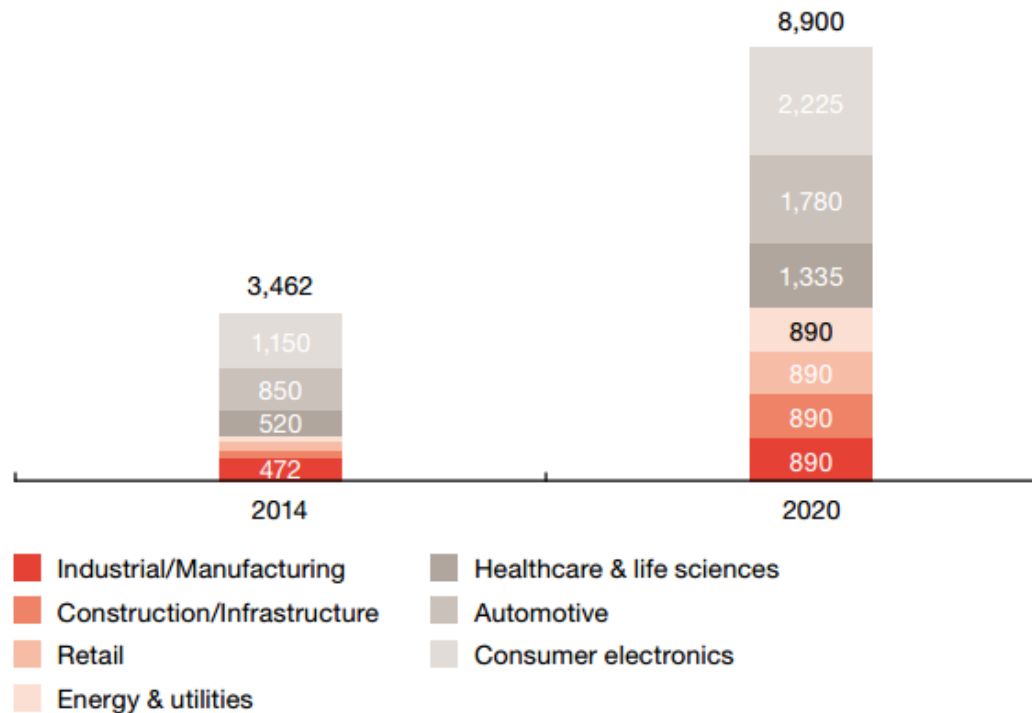
- A proposed development of the Internet in which everyday objects have network connectivity, allowing them to send and receive data.

- TechTarget.com Explanation

- The Internet of Things (IoT) is a system of interrelated computing devices, mechanical and digital machines, objects, animals or people that are provided with unique identifiers and the ability to transfer data over a network without requiring human-to-human or human-to-computer interaction.
- IoT has evolved from the convergence of wireless technologies, micro-electromechanical systems (MEMS), microservices and the Internet. The convergence has helped tear down the silo walls between operational technology (OT) and information technology (IT), allowing unstructured machine-generated data to be analyzed and drive system improvements.

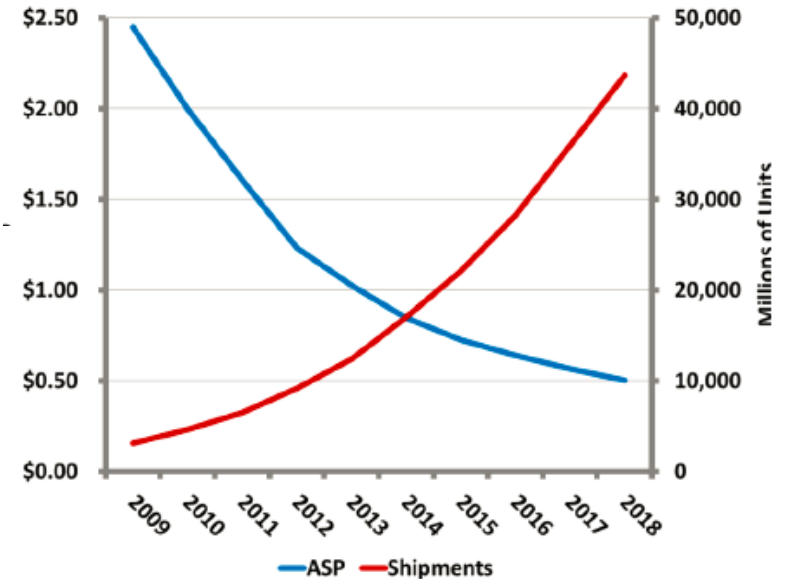
Strong growth predicted in IoT for next 5 years

bn US\$



Source: Industry Forecasts Compilation, 2020 forecast from IDC, PwC analysis.

Total MEMS Market



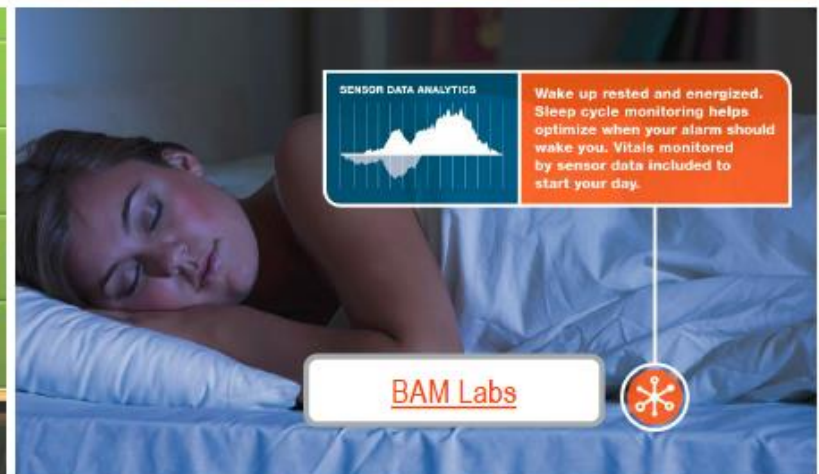
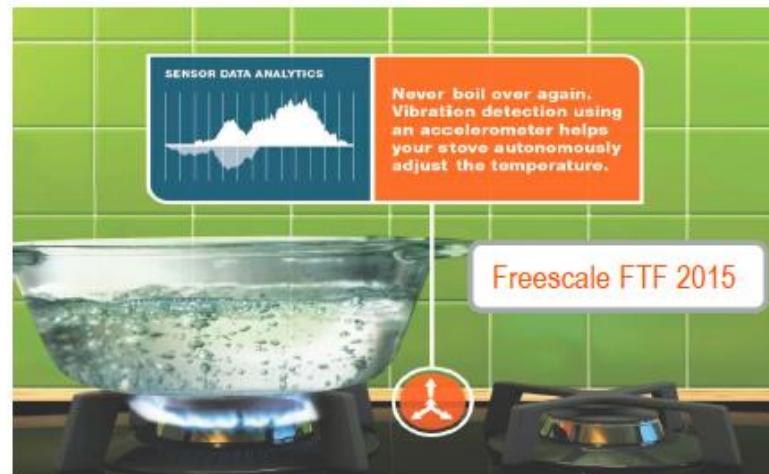
Source: Semico (Oct 2015)

Many applications are enabled by MEMS sensors

Some Sensor Data Analytics Applications

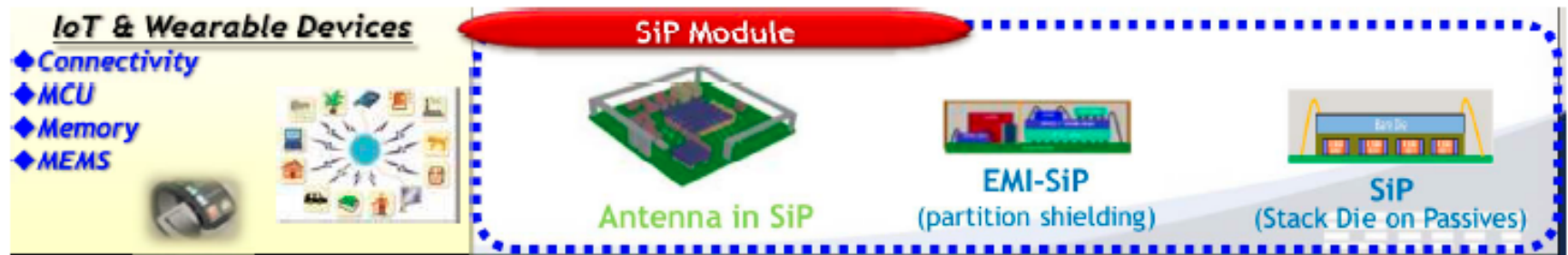


Keg Data



Source: Freescale presentation at Semi Industry Forum on IoT (Oct 2015)

- Expansion of IoT/IoE means an increased number of sensors, but also more connectivity, signal processing, and data storage
- Primary device requirements are low power and low cost
- No single package format
 - Many applications may adopt system-in-package (SiP)
 - Many just SMT modules on FR-4 board, not counted as SiP but as system-in-module (SiM)
- One main reason IoT/IoE is expanding rapidly is the low cost of sensors and multi-die packages and modules

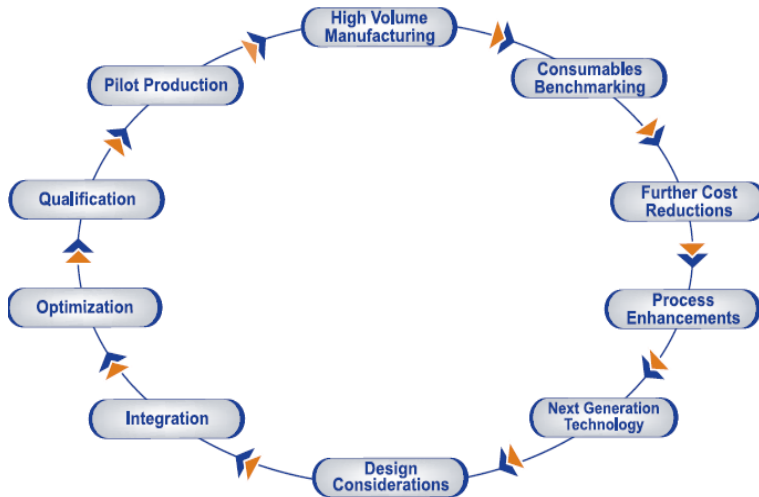


Source: SPIL.

- Security and Privacy Control
 - Especially important for health care, retail, and critical systems data
- Interoperability
 - Must have a manageable number of standards
 - Software apps may hold key to cross-platform integration
- Reduced Cost
 - Initial focus is on IC components and sensors
 - Lower packaging, assembly and distribution costs are also critical
- Low Power
- Embedded Processing
 - Can add distributed intelligence to system (local interpretation / faster decisions)
 - Reduces load on communication bandwidth

Source: Semico Research (Oct 2015)

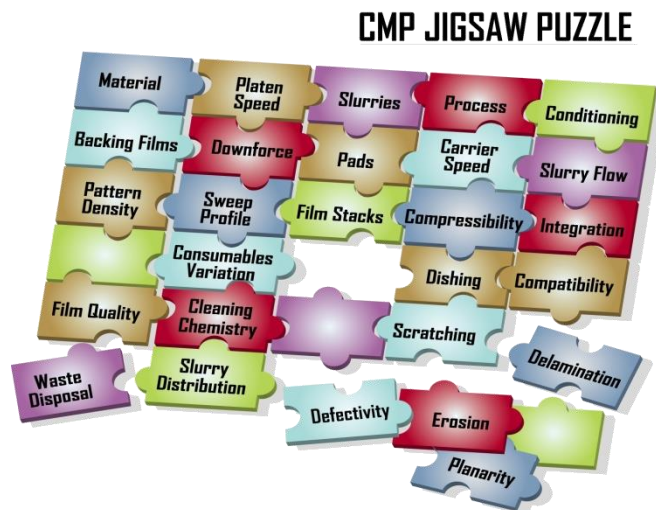
CMP FastForward™



Process Applications:

1995 - Qty ≤ 2 CMOS	2001 - Qty ≤ 5 CMOS	2016 Qty ≥ 40		
		CMOS	New Apps	Substrate/Epi
Oxide	Oxide	Oxide	MEMS	GaAs & AlGaAs
Tungsten	Tungsten	Tungsten	Nanodevices	poly-AlN & GaN
	Cu (Ta barrier)	Cu (Ta barrier)	Direct Wafer Bond	InP & InGaP
	Shallow Trench	Shallow Trench	Noble Metals	CdTe & HgCdTe
	Polysilicon	Polysilicon	Through Si Vias	Ge & SiGe
		Low k	3D Packaging	SiC
		Capped Ultra Low k	Ultra Thin Wafers	Diamond & DLC
		Metal Gates	NiFe & NiFeCo	Si and SOI
		Gate Insulators	Al & Stainless	Lithium Niobate
		High k Dielectrics	Detector Arrays	Quartz & Glass
		Ir & Pt Electrodes	Polymers	Titanium
		Novel barrier metals	Magnetics	Sapphire
			Integrated Optics	

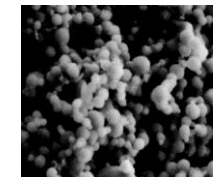
Consumables and Controls



PADS



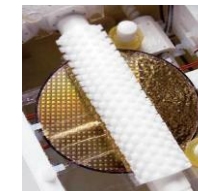
SLURRIES



ABRASIVES



CONDITIONING DISCS



BRUSHES & CLEAN CHEMISTRIES



COMPONENTS

CMP is typically used in a damascene manner to planarize and isolate the vias after conductor deposition from one side.

TSV's can be filled with any of several conductive materials.

- Most common options are copper and polysilicon.
- Final choice depends on dimensions, operating voltage and current, frequency, temperature requirements, plus other integration factors.

CMP is used again after thinning to help expose and planarize the original “bottom” of the TSV's – called TSV Reveal.

Background

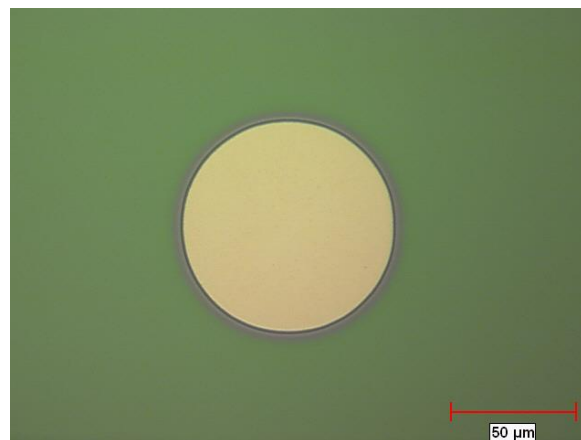
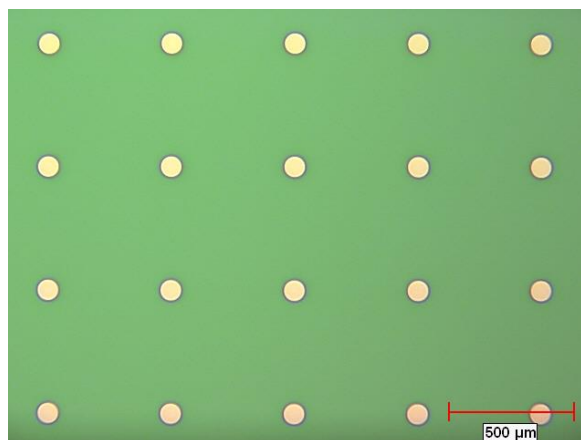
- Large via needed for design (75-100um diameter)
- Via last with extremely thick Cu plating (about 45 um)
- Previous CMP using standard stock removal slurries resulted in very long polish times (45 mins to 1 hour)

Goals for CMP optimization phase

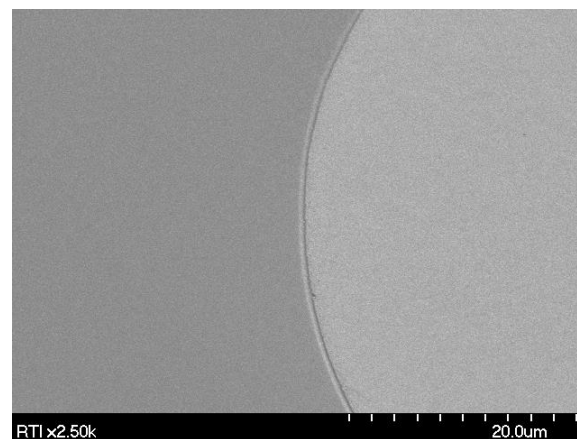
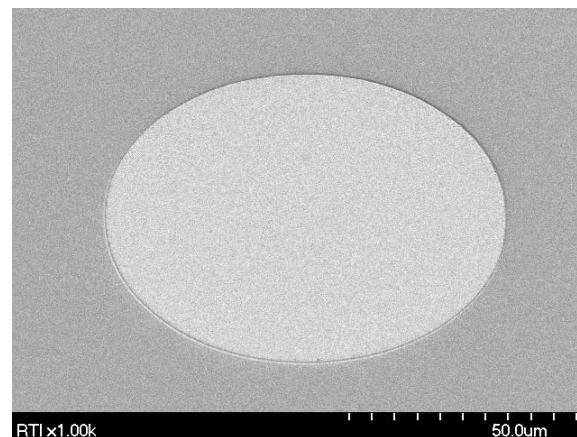
- Test new high-rate Cu slurry for much shorter clear times
- Verify reasonable selectivity to nitride after barrier clear
- Dishing <1 μm across 80 μm via
- Good surface finish on both Cu and dielectric

Via Diameter = 80 microns
Field area = nitride and via liner = oxide

Optical Microscope



SEM



Source: RTI International, Inc.

Process module following completion of device layers on front side

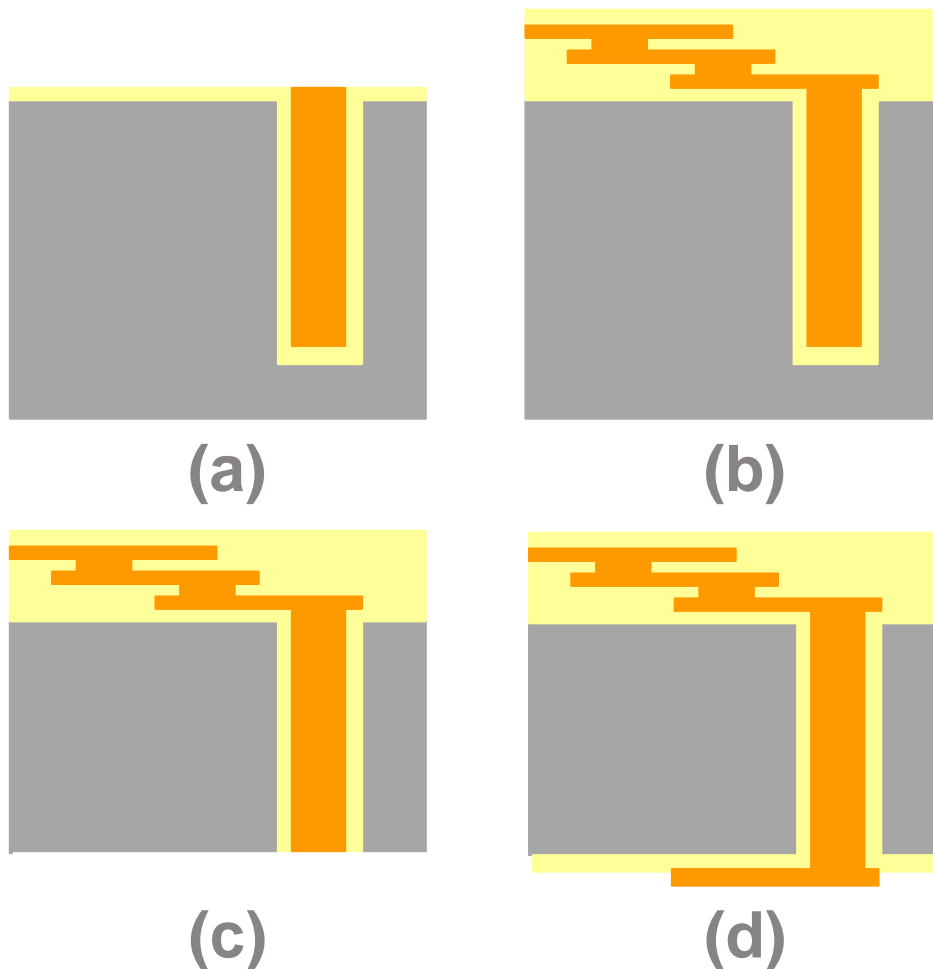
TSV must be exposed to make contact and/or continue patterning next layers (RDL) from wafer backside.

Various integrations are viable with combinations of backgrind, etch, selective CMP, or non-selective CMP.

- Some approaches require 2 or 3 steps of CMP

Examples from two alternative integrations

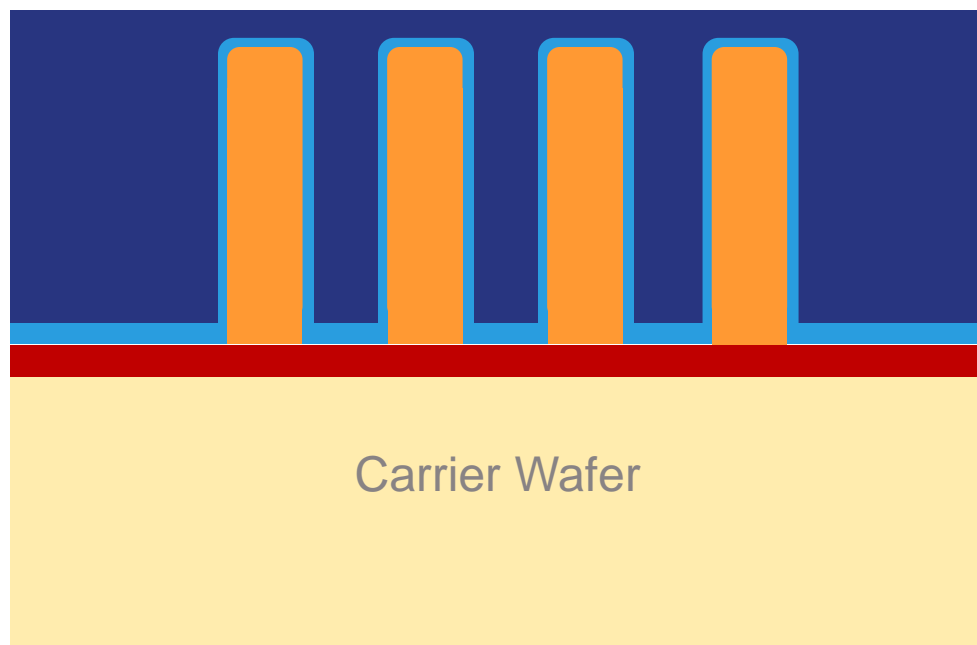
- Reveal Using Non-selective CMP
- Reveal CMP Following Si Etch



Process flow for Si interposer with TSVs: (a) TSV etch, isolation layer, plating, and via CMP, (b) Frontside multi-level metallization, (c) Wafer thinning and TSV reveal, (d) Backside metallization.

Source: RTI International, Inc.

Backgrind stops in Si before reaching TSV's



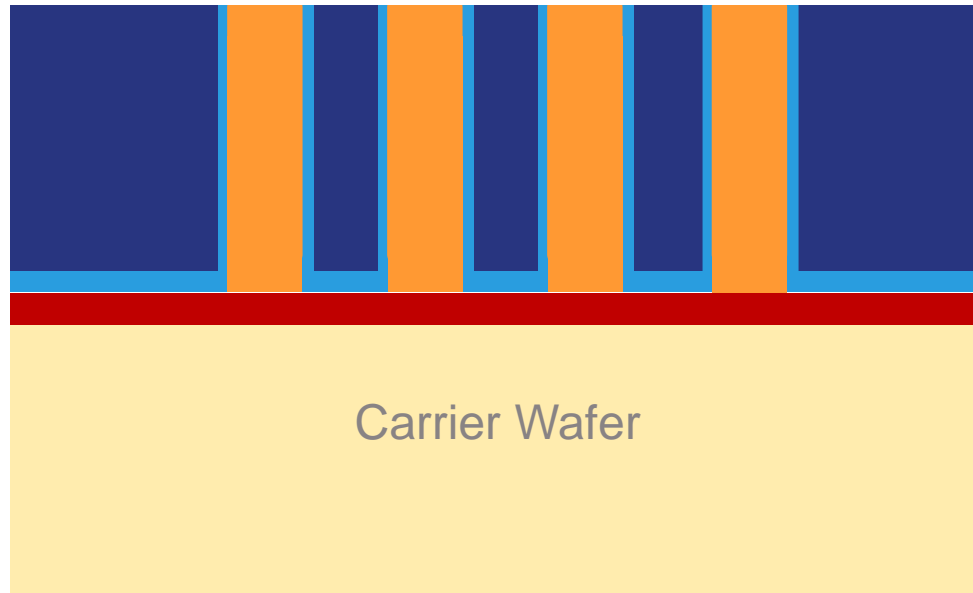
Carrier Mount

- TSV wafers mounted face down on carrier wafers

Backgrind

- TSV wafers thinned using backgrind stopping approx 3-15um before hitting TSVs
- Reveal CMP performs dual function of removing grind damage layer and remaining bulk Si then exposing center conductor of TSV's

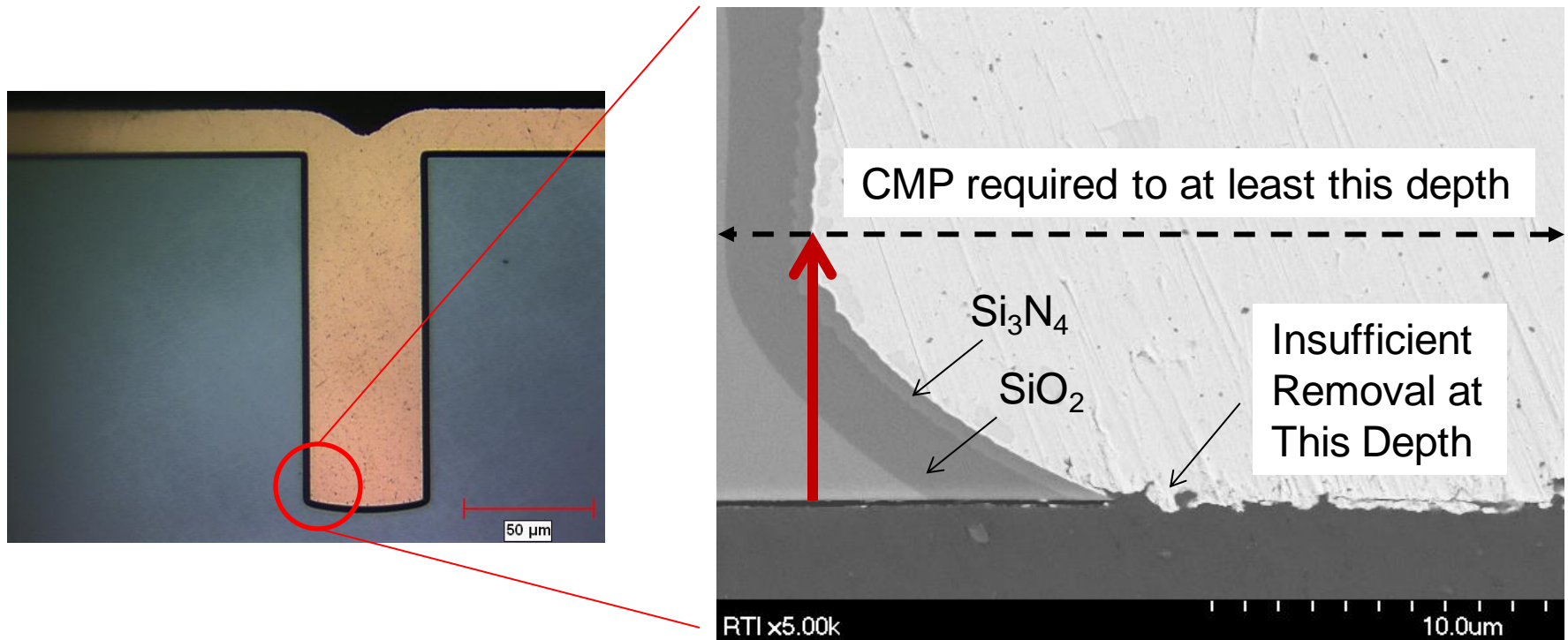
Expose & Planarize TSVs



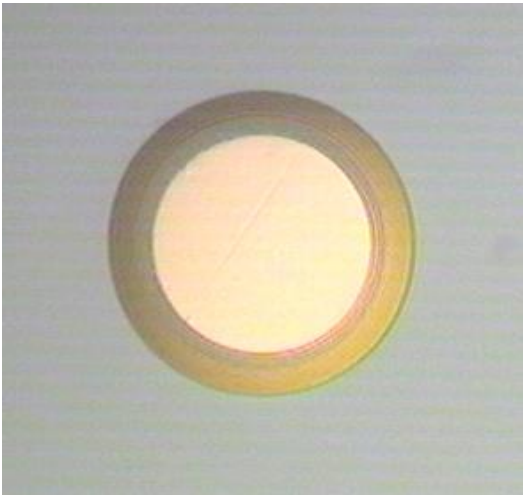
Several exposed materials

- Single crystal silicon
- Oxide (or other liner)
- Barrier metal
- Copper

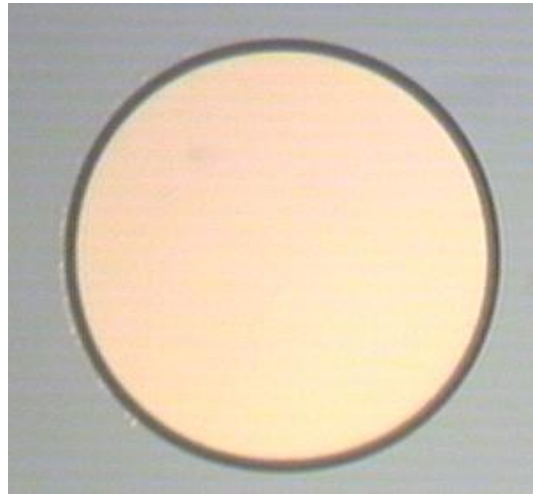
Need to polish far enough into TSVs to remove rounded profile at base of vias



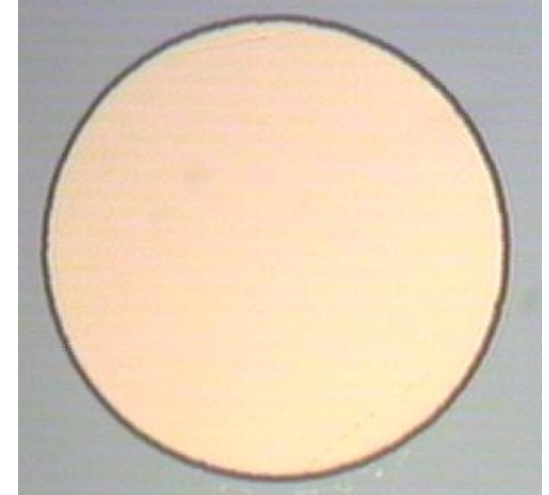
Source: RTI International, Inc.



Starting to clear

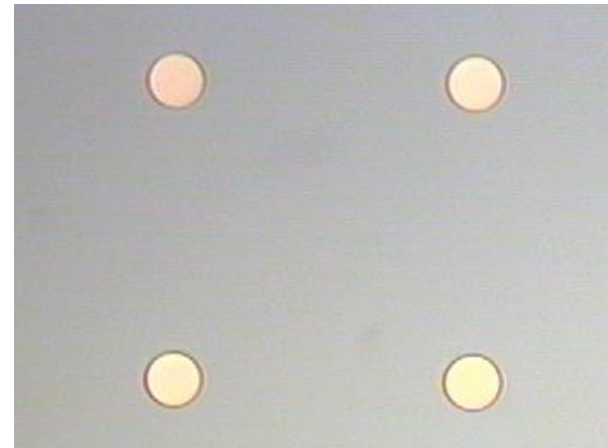


Mostly clear



Finished

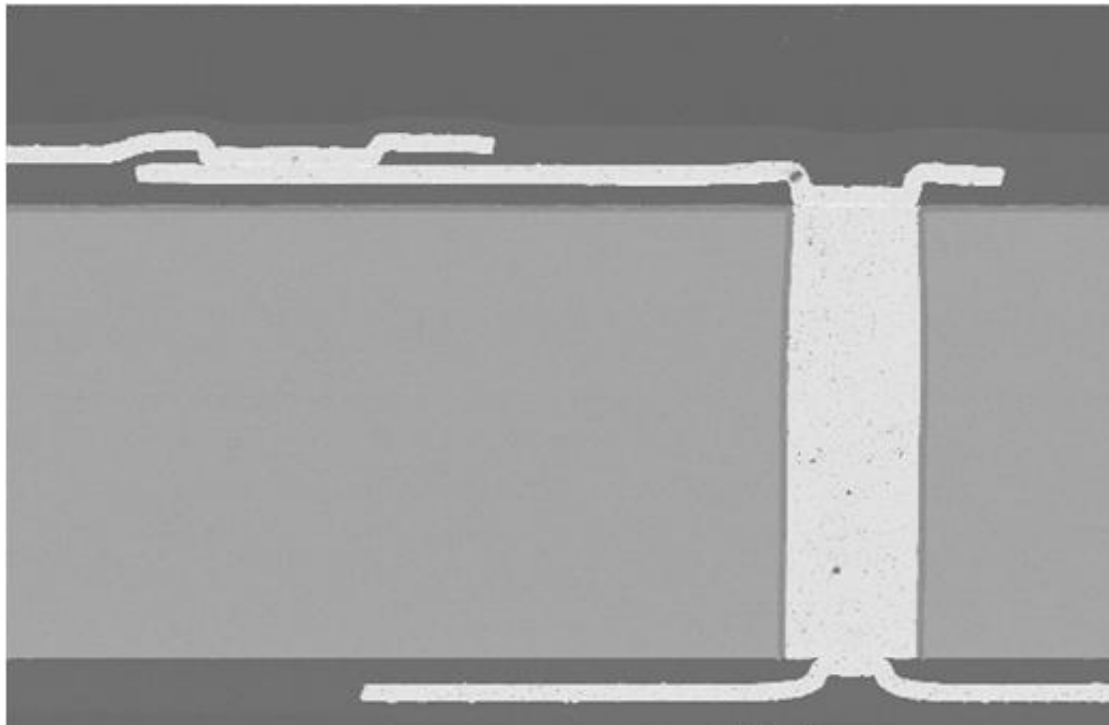
**Customized CMP process was
used to planarize final surface
comprised of Si+Ox+barrier+Cu**



Source: RTI International, Inc.

Completed interposer test structure: large via diameter, 100um thickness.

Structure has 2 frontside metal layers (4um Cu) and 1 backside metal.

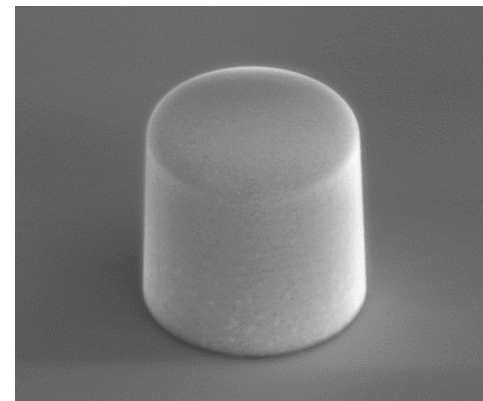


Bottom surface received
TSV reveal polish

Source: RTI International, Inc.

After backgrind, bulk Si removed by an etch process

- Can be dry etch or wet etch, but must be highly selective to oxide
- Installed equipment already available
- Proceeds until 2-5um of encased via “bumps” protrude



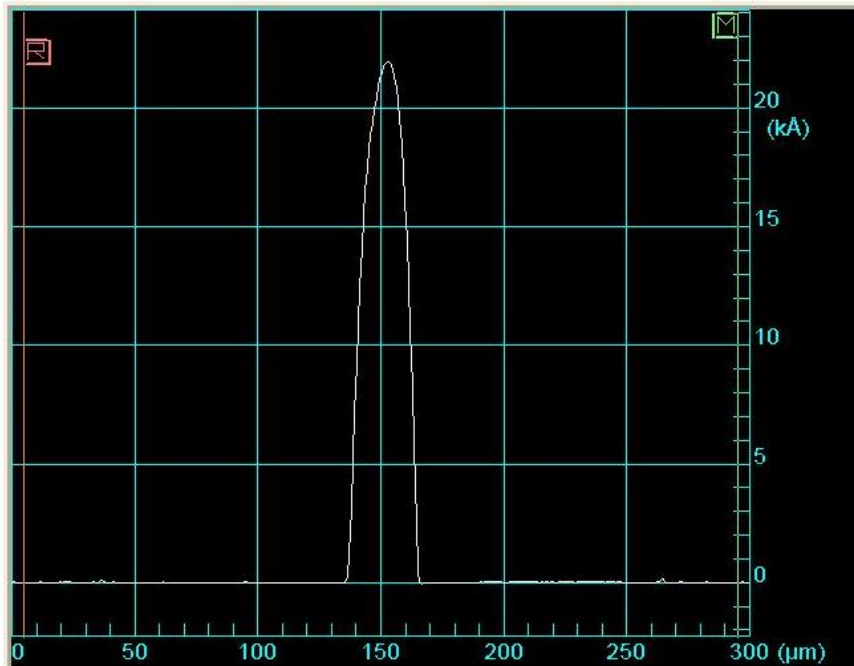
Layer of dielectric is usually deposited to protect field areas

Primary goal of CMP is to planarize bumps and expose the Cu cores

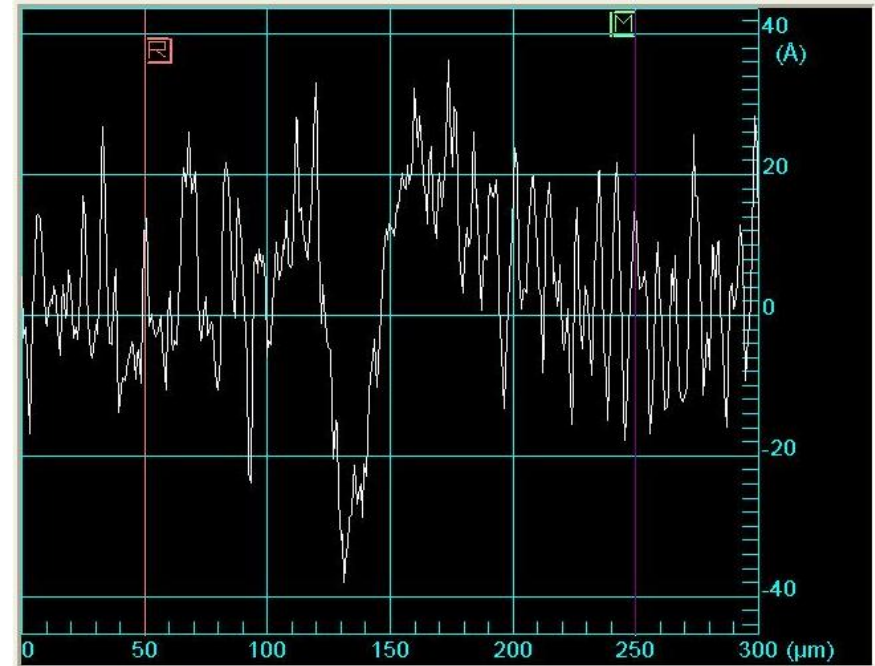
One benefit of this approach is to reduce total CMP polish time

- Less sensitive to uniformity issues
- Faster throughput and lower CMP process cost

CMP becomes relatively short “kiss” polish



Pre-CMP Step Height
22,000 Ang



Post-CMP Step Height
60 Ang

- CMP Requirements Related to Packaging
 - High stock removal rates are often needed for acceptable throughput
 - Topography demands are much less stringent than CMOS interconnect
 - Defectivity is defined at a different level
 - Lower cost is a MUST
 - Wafer thinning and TTV control are alternate types of planarization
 - New slurries may be needed for new materials, esp. for interposers and flexible electronics
 - Advanced packaging and TSV applications have huge volume potential, but still struggling to define preferred integration that can meet cost expectations

- Miniaturization
 - Form factor and functionality density (package height, footprint)
- Heterogeneous technology integration
 - Digital, RF, analog, power, and sensor integration
- Mixed process technology
- System performance
 - Noise reduction and higher speed
- System flexibility, features, and configurability
- Total system cost reduction
 - Package/device cost
 - Development cost
 - Time to market

Adapted from source: Techsearch International

Many thanks to the following people:

Paul Feeney, Terry Pfau, Paul Lenkersdorfer, Donna Grannis (Entrepix)

Customers, colleagues and analysts for various contributions

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