Limitations and Challenges to Meet Moore's *Law*

Advanced Product and Technology Development
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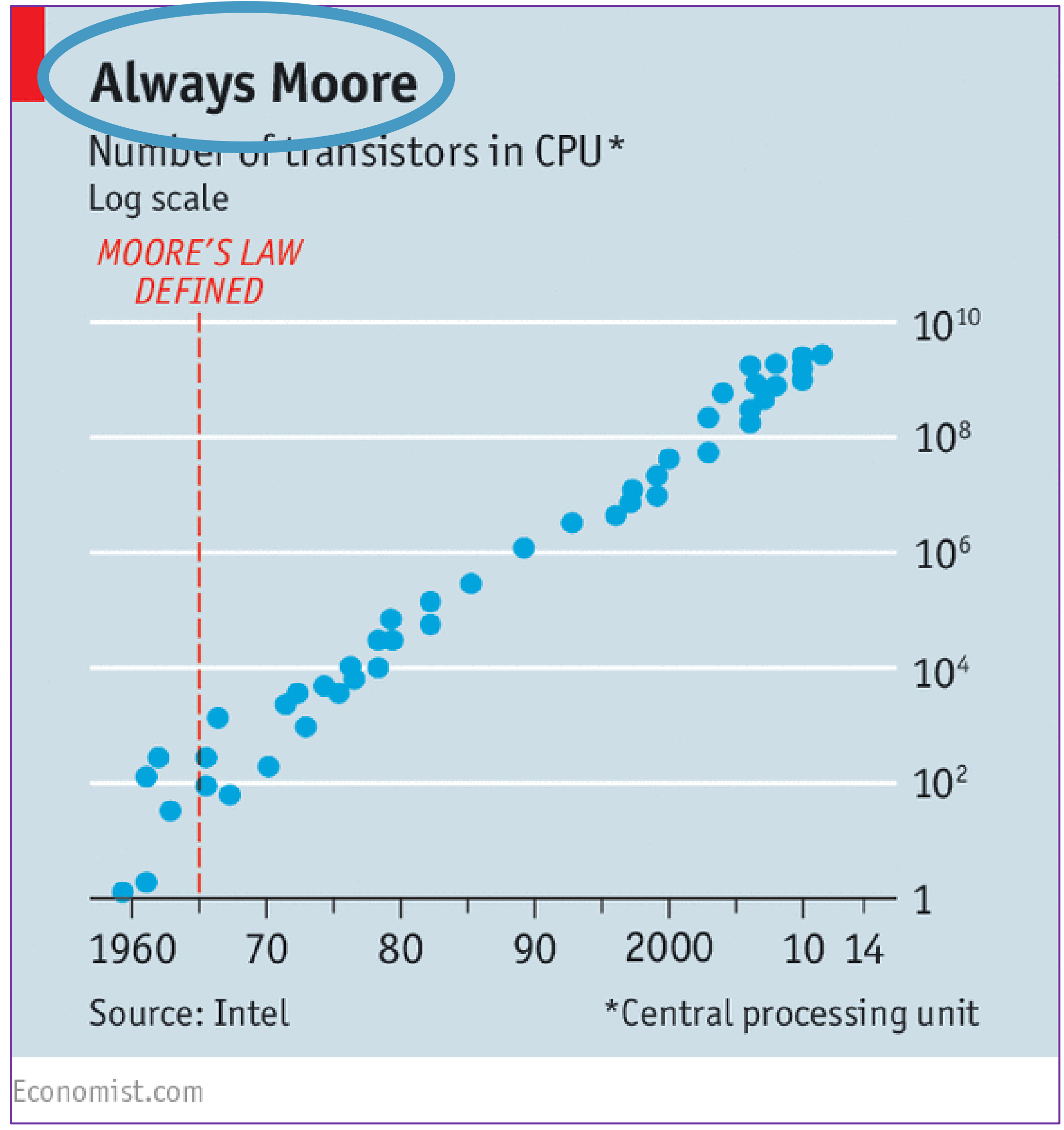
State of the art:

- cleanroom
- toolsets
- metrology
- analysis
- module development
- test & reliability

- Introduction
- Why do we scale?
- Limitations and Challenges:
  - Transistor
  - Patterning

External Use

5nm is the end of Moore?



Faith no Moore

Selected predictions for the end of Moore's Law

Cited reason: Economic limits / Technical limits

Prediction issued — Predicted end date

1995 2000 2005 2010 2015 2020 2025 2030

Gordon Moore, Intel: 1995 – 2005

G. Dan Hutcheson, VLSI Research: 1996 – 2003

Isaac Chuang, IBM Research: 2000 – 2020

Paolo Gargani, Intel: 2003 – 2021

Lawrence Krauss, Case Western, and **Glenn Starkman**, CERN: 2004 – approx. 2600

Gordon Moore, Intel: 2005 – 2015–25

Michio Kaku, City College of NY: 2011 – 2021–22

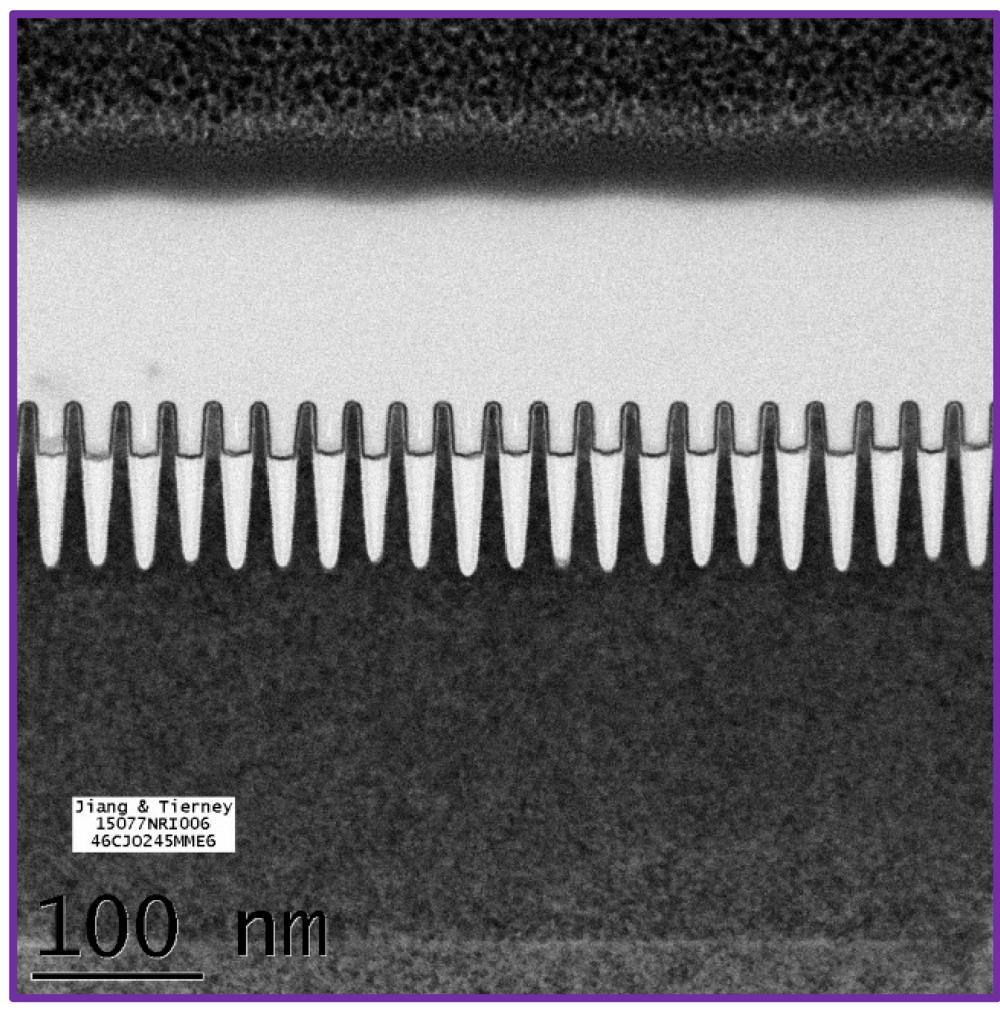
Robert Colwell, DARPA; (fmr) Intel: 2013 – 2020–22

Gordon Moore, Intel: 2015 – 2025

Sources: Press reports; *The Economist*

Economist.com

Feasible down to 5nm?



- Press Release Albany New York: IBM, Samsung & Globalfoundries; working 7nm transistors.
- ISSC conference early 2015:
  - Head of Samsung R&D keynote: ‘no fundamental difficulties until 5nm’
- Intel conference call: 10nm pushed out another year (3 year cadence vs. 2 year) due to:
  - "The lithography is continuing to get more difficult as you try and scale, and the number of multi-pattern steps you have to do is increasing," - Brian Krzanich
  - Looking at another round of 14nm and ‘other means’ to improve performance.
  - ‘other means’ : Skylake vs. Broadwell

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Scaling by node

Scaling by Year

Calendar Year

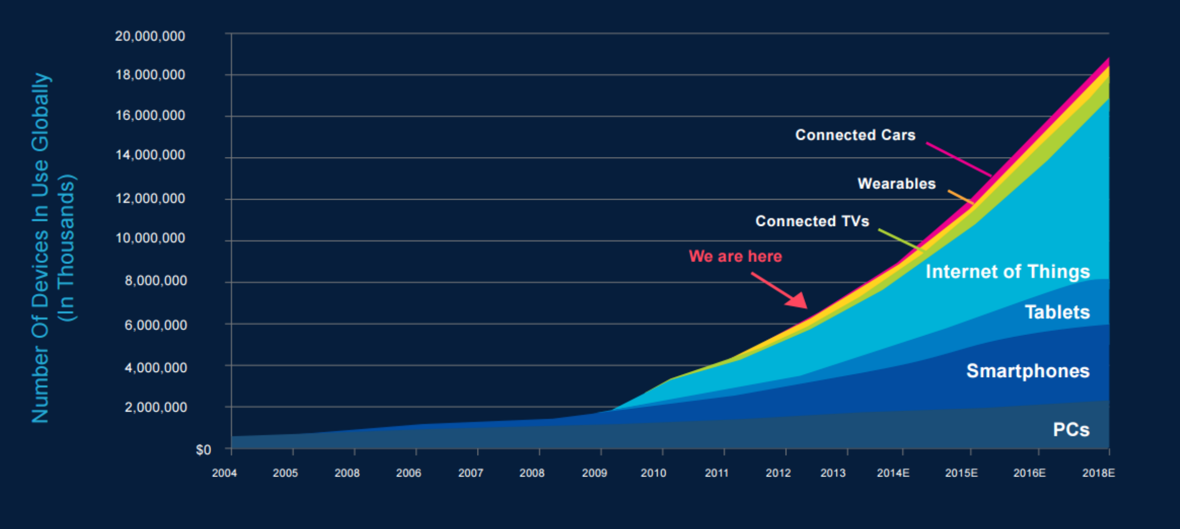
Logic Area (k nm²)

Series	Node	Approx. year	Logic Area (k nm²)
Foundry	14nm	2015	
Foundry	10nm	2017	
Foundry	7nm	2018	
Foundry	5nm	2020	
Logic	14nm	2013	
Logic	10nm	2016	
Logic	7nm	2019	
Logic	5nm	2022	

Y axis: 0, 1, 2, 3, 4, 5, 6

X axis: 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021, 2022

10nm logic area equivalent to foundry 7nm



Source: Business Intelligence, The Internet of Everything: 2014

Industry Technology Scaling Trend

- Logic ahead by one gen (2 years - 10nm ~ foundry 7nm)

Notable Speculation on Timing

- 10nm for next gen phone in 2017.
- Earliest possible EUV insertion: 7nm (to what extent?)
- Next earliest transistor architectural change (GAA?): 7nm.

Why do we scale?

- **Performance**
  - **Speed**
    - **– though physical area is shrinking**
- **Power**
  - **Heat & Battery Life:**
    - **– though features per area is increasing**
- **Cost**

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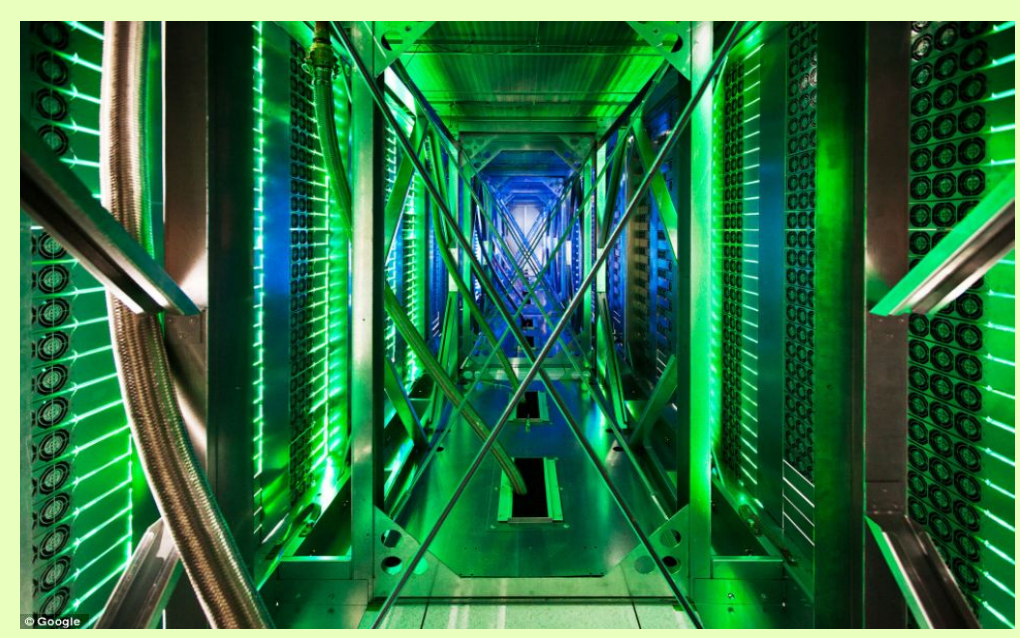
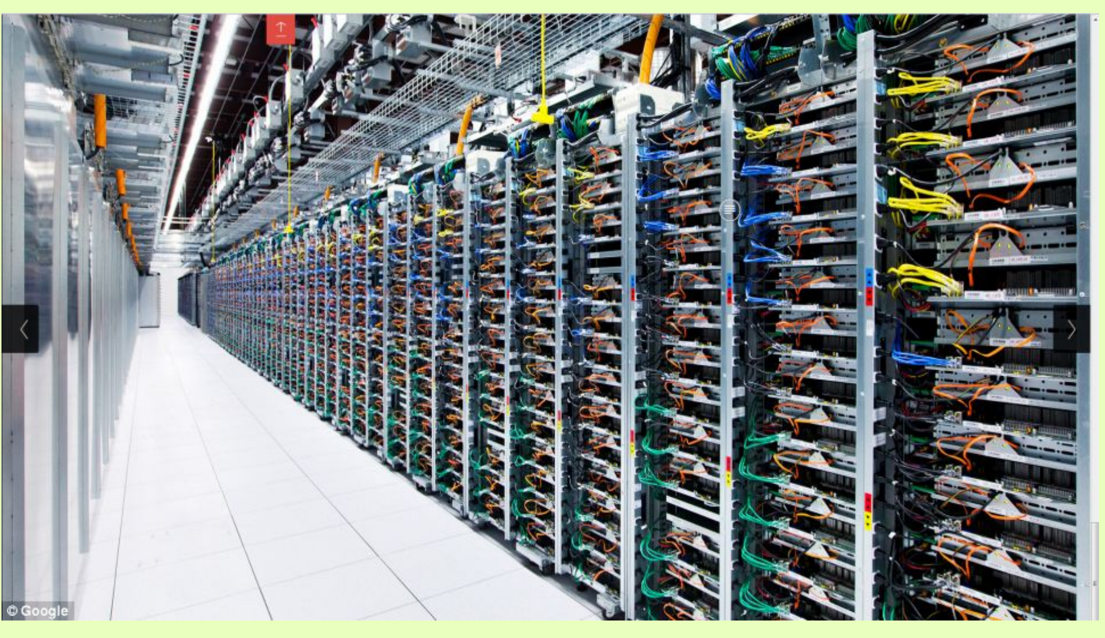
What are we scaling for?





Notable players:

- Apple
- Amazon
- Google
- Microsoft
- Facebook

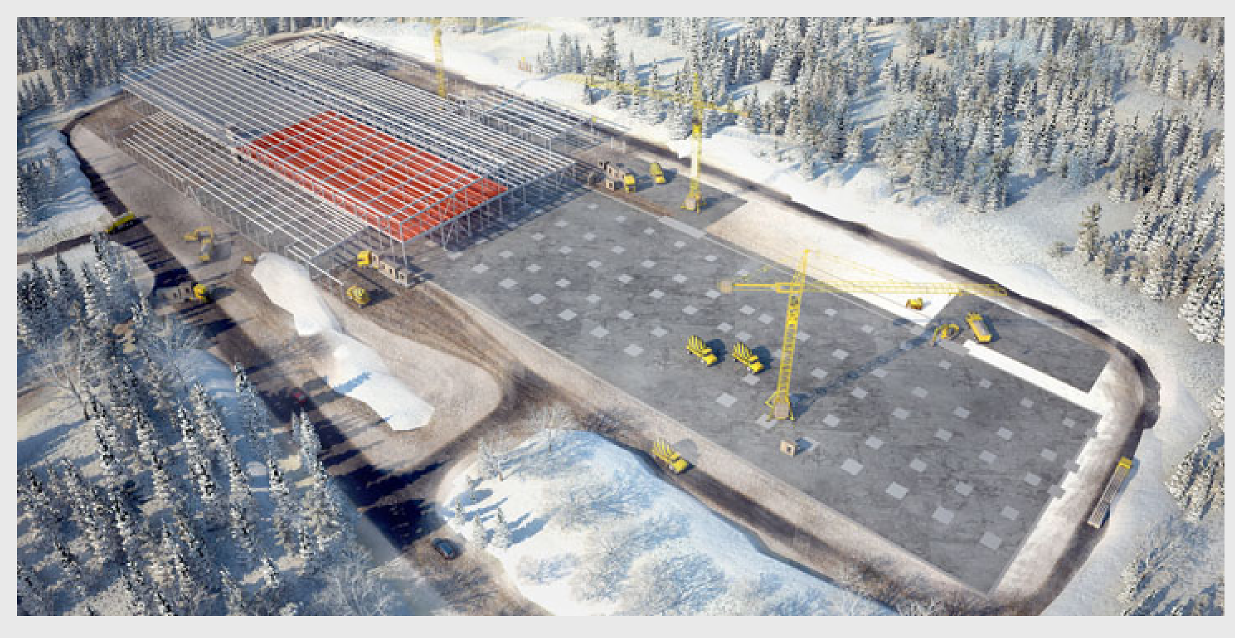
Interesting Factoids:

- Huge carbon footprint / large % electrical consumption
- over 38% of large companies expected to exceed IT capacity within 18 months - IoT
- the average life of a data center is 9 years

Scaling on a macro level?

Challenges:

Performance:	Switching /transmission; speed, data integrity/back up; security.
Power :	For every 100 watts 10% of world's electrical demand?
Cost:	Scaling requirements



What's Inside.

- less about internal server speed
- More about applications
- And external challenges

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The current tool of choice for data collection:

- From PC to mobility – getting smaller
- And now…
- And next ➡ Internet of Things.

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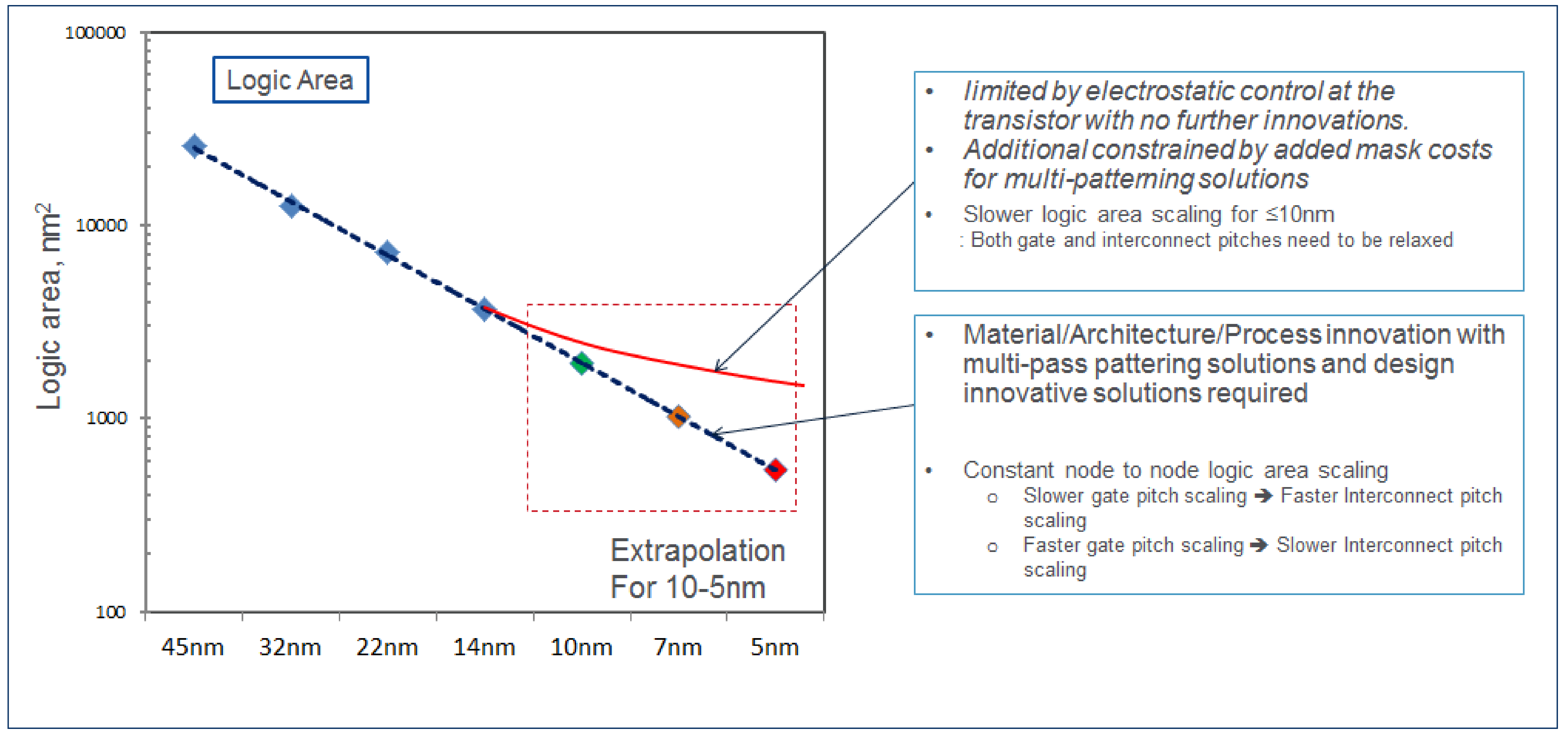
Scaling challenges for next nodes



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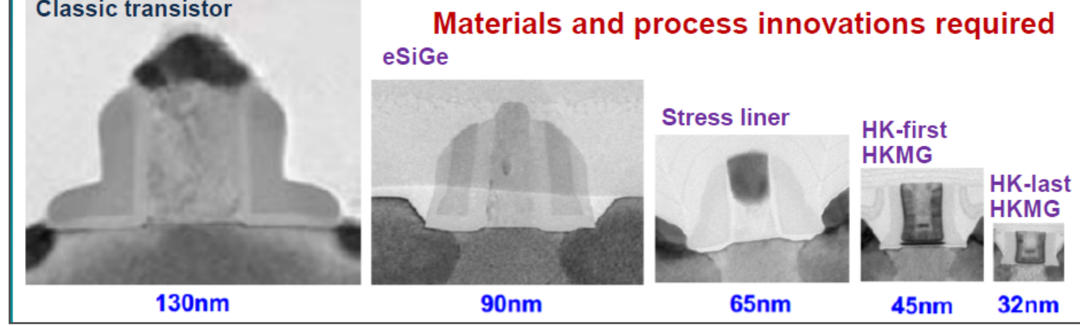
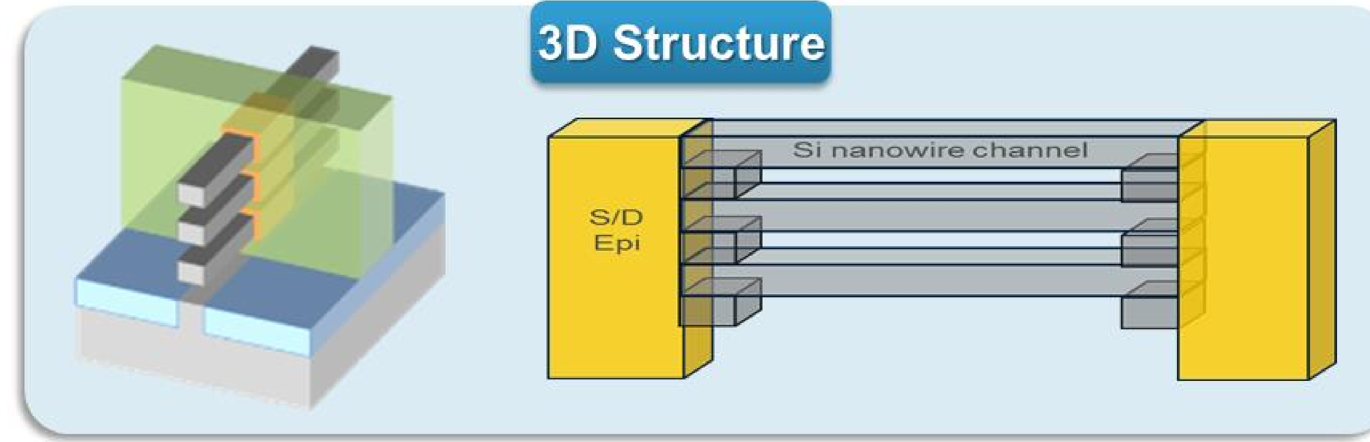
Scaling challenges for next nodes



Source: Kuhn SSDM Japan 2009

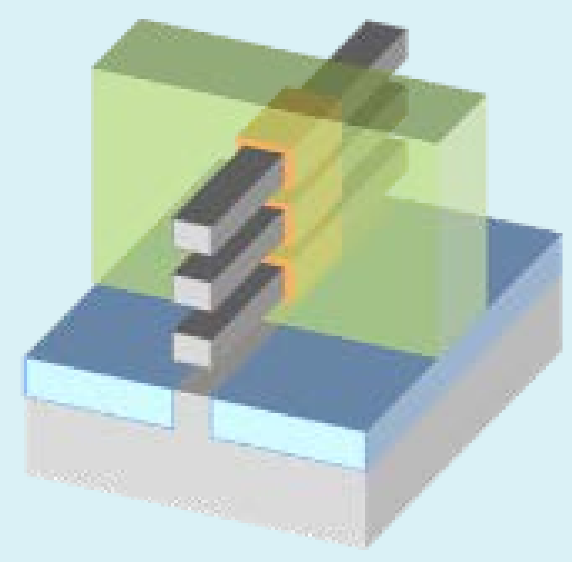
Source: Applied Materials Investor Day 2014



External Use

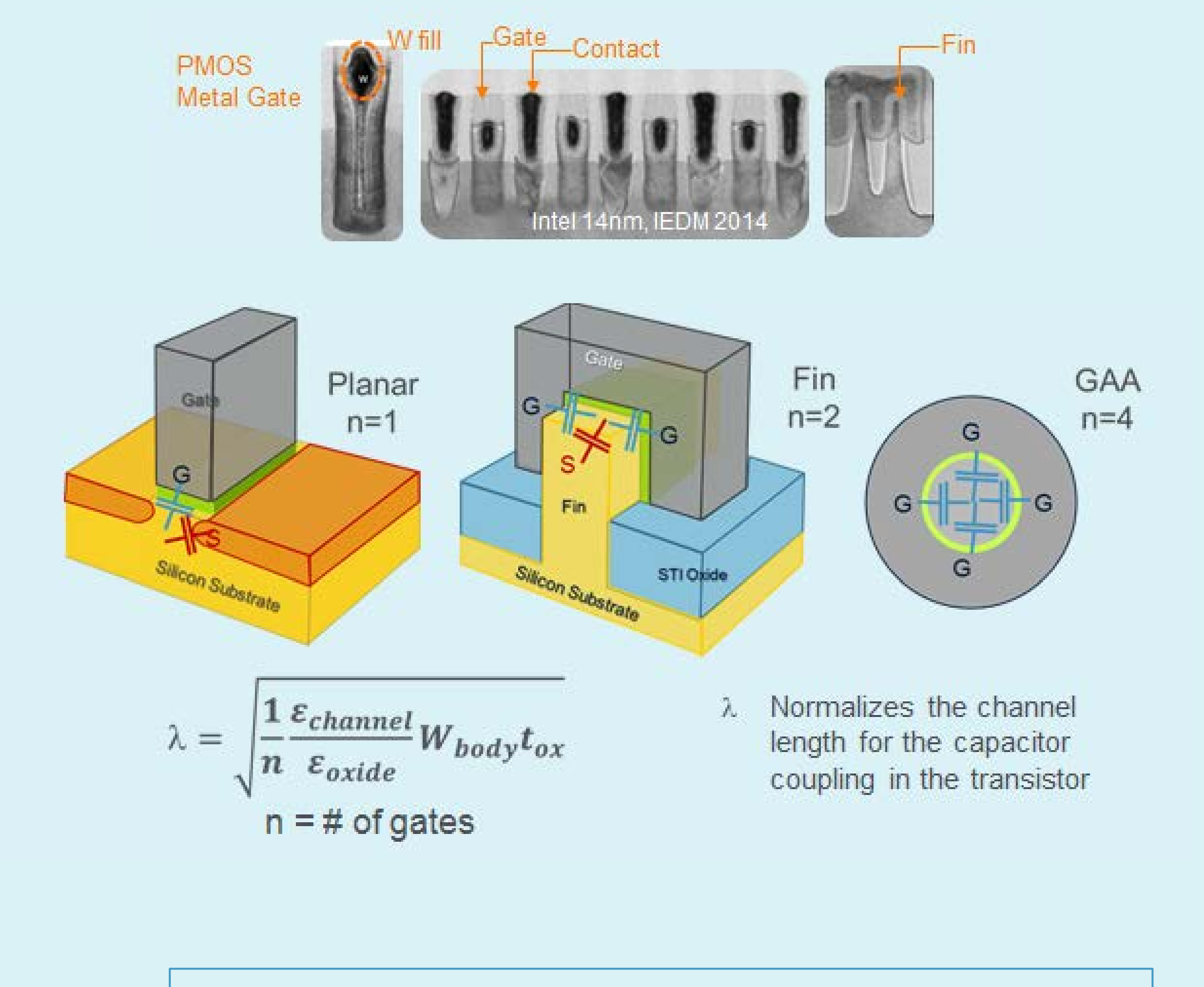
Superior Electrostatic Control to Enable Gate Scaling

Improving Gate Control



Key Challenges

- Nanowire formation
- Bottom isolation
- Nanowire spacer
- Stressor material
- High k metal gate formation
- S/D & Extension doping



$$\lambda = \sqrt{\frac{1}{n}\frac{\varepsilon_{channel}}{\varepsilon_{oxide}} W_{body} t_{ox}}$$

n = # of gates

λ Normalizes the channel length for the capacitor coupling in the transistor

Reducing body width and increasing number of gates enables gate length scaling

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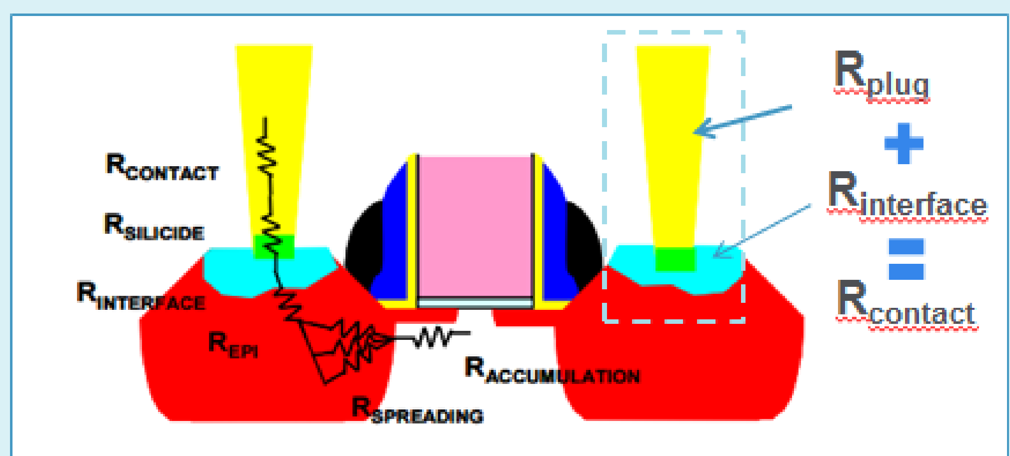
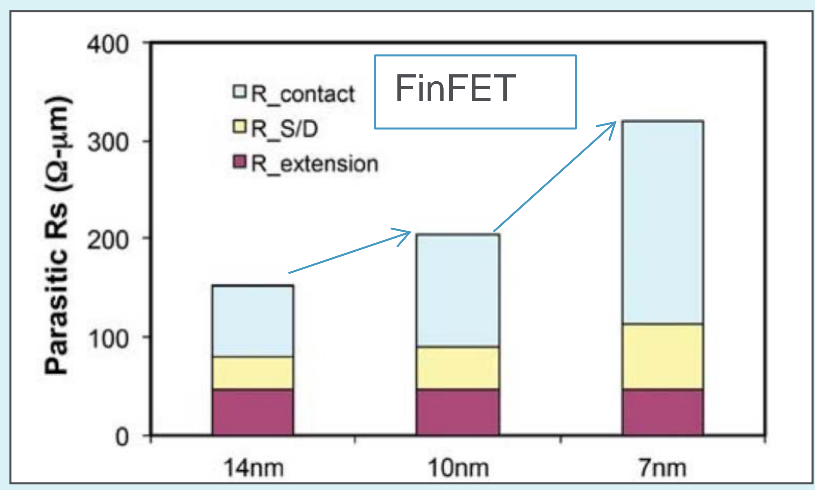
Parasitic Resistance: Increasing Contribution of $R_{contact}$

Contact resistance reduction

Challenges:

- Increasing parasitic resistance comes from $R_{contact}$.
- R_{plug} dominant resistance at ≤10nm CD with conventional W





Parasitic resistance components of FinFET.
Source: Synopsis Simulation

Technology Solutions

- Interface Engineering
- Schotky Barrier Height reduction (III-V)
- Silicidation
- Low Resistivity Contact Fill
- Contact Area Scaling

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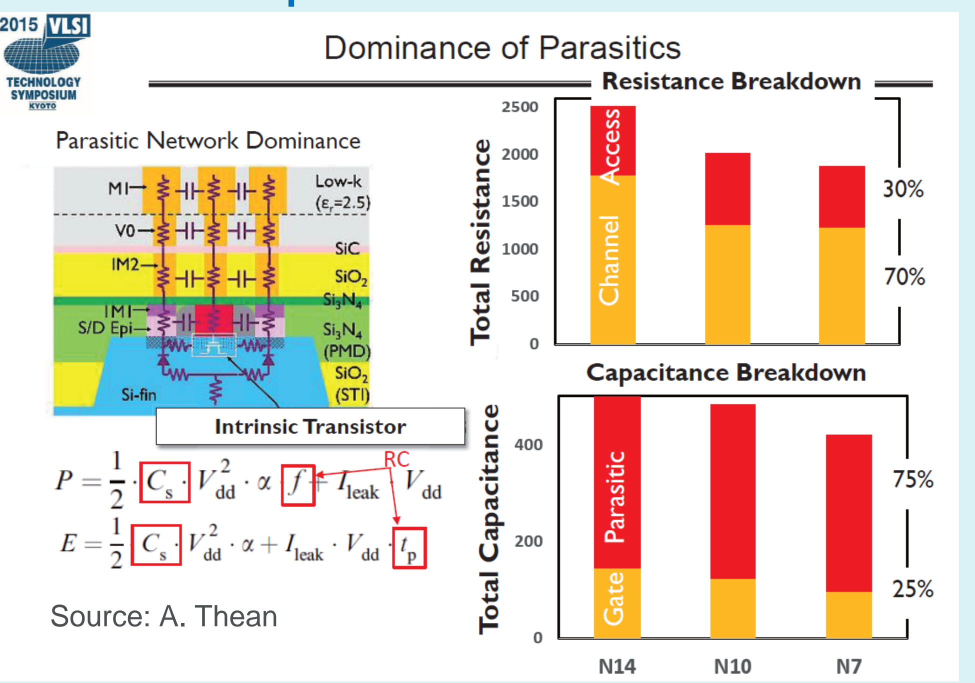
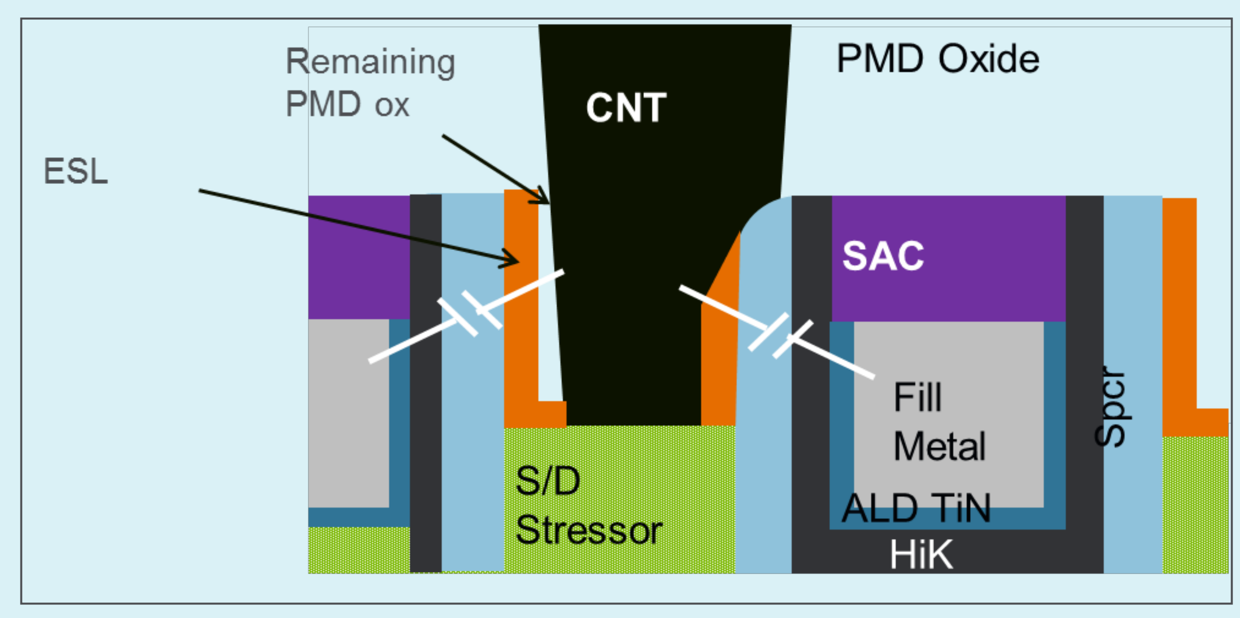
Parasitic Capacitance Fix solutions for Power Reduction

Parasitic capacitance reduction





Scaling Challenges:

- Gate to drain capacitance increases with Lg scaling
- Parasitic RC for scaled device increases

Technology challenges:

- Lower k ~ 4 for spacer and ESL
- Selectivity for removal of ESL
- Narrow contact, narrow stressor

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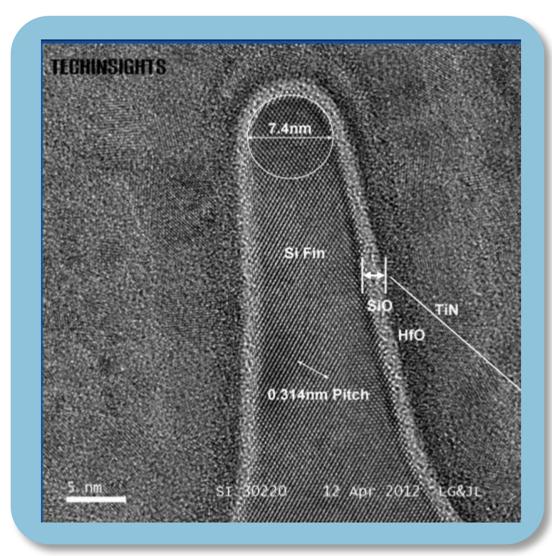
Transistor Challenges

Year	2014	2016	2018	2020
Node (nm)	14	10	7	5
Lg (nm)	20	16	12	9

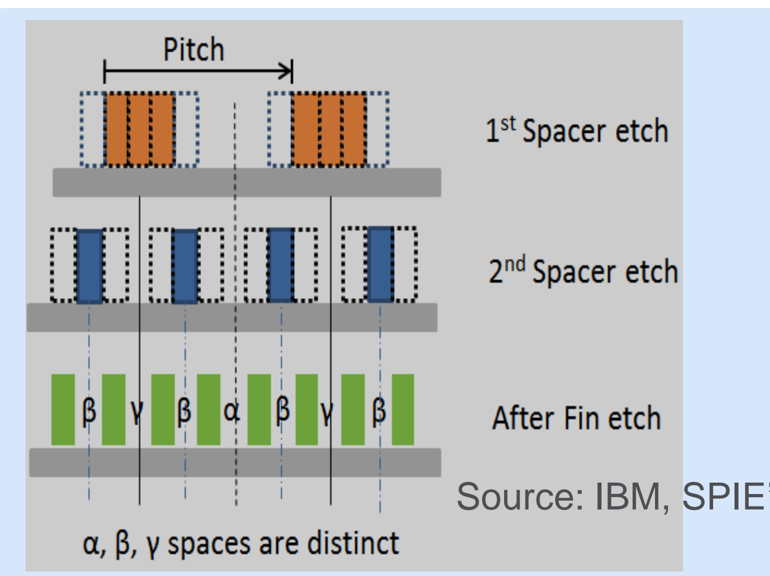
Architecture	FinFET → Gate All Around (GAA)
S/D Stressor	SiCP (n) / SiGe (p) → Higher doping (n) / Ge-rich SiGe (p)
Metal Gate	ALD Metal, W fill → Multi VT by MG → Material Change

- Solve ***Transistor Technology Challenges***
  - Gate control improvement – 3D scaling
  - Contact Rc – materials engineering for $R_{contact}$
  - Parasitic capacitance reduction – materials engineering

*With continued scaling: electro static resistance and parasitic capacitance control

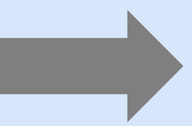


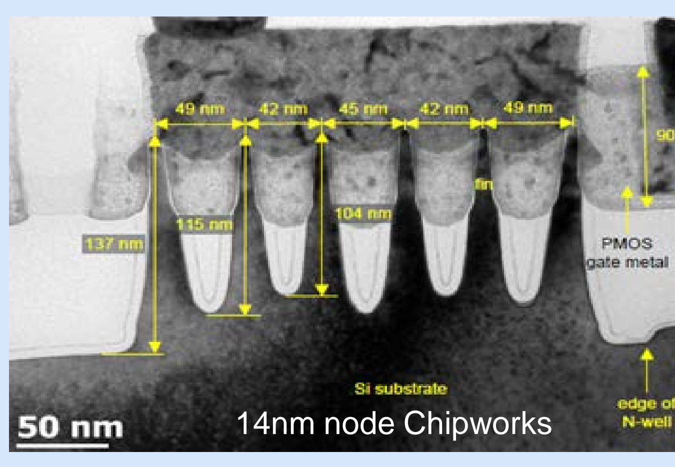
Multi-patterning vs. EUV



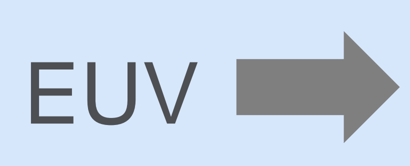
Source: IBM, SPIE'15

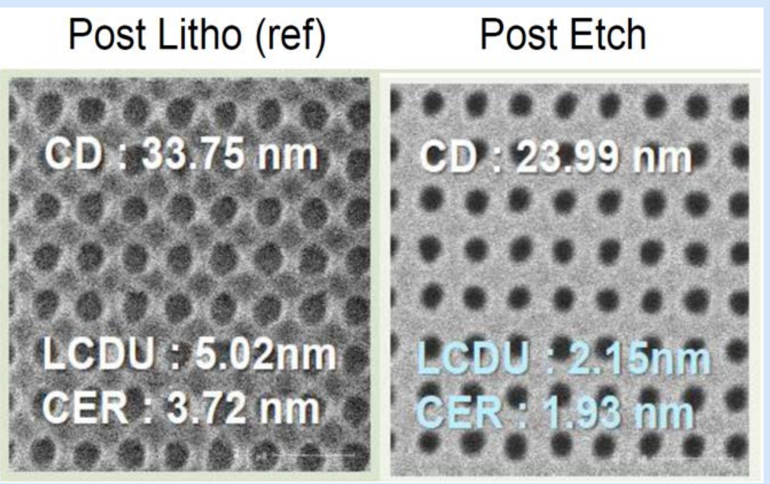
Process impacts on CD Variability





EUV





Source: P. Naulleau, Berkeley Lab

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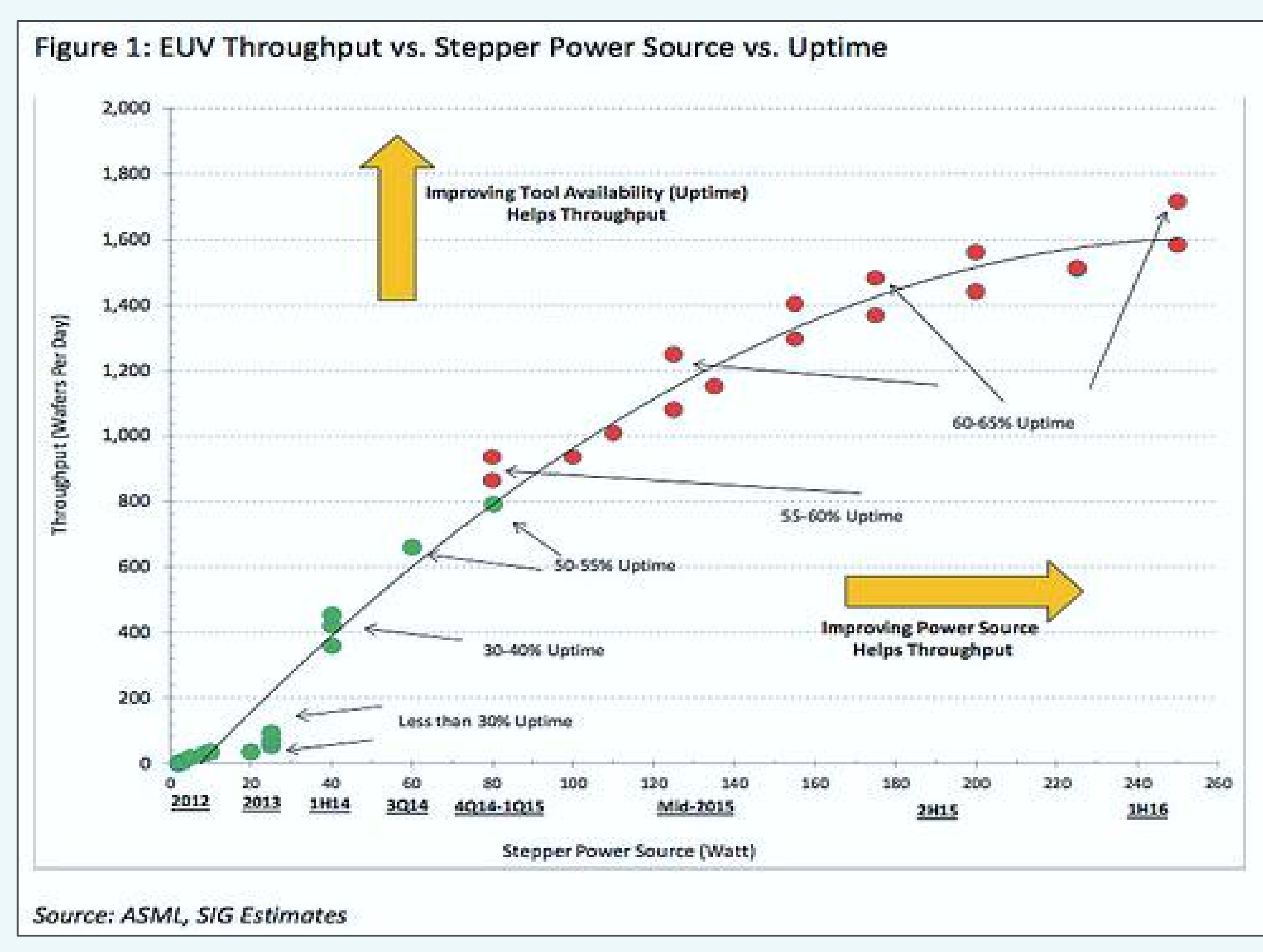
Patterning



EUV challenges:

- Potential (imaging) is good
- Source power:
  - wafers per hour
  - Cost of Ownership
- Mask technology:
  - Manufacturing cost & short lifetime
  - High consumable cost:
    - Pellicle
    - Blanks
  - Ability to inspect
- Photo-chemicals…
- Infrastructure

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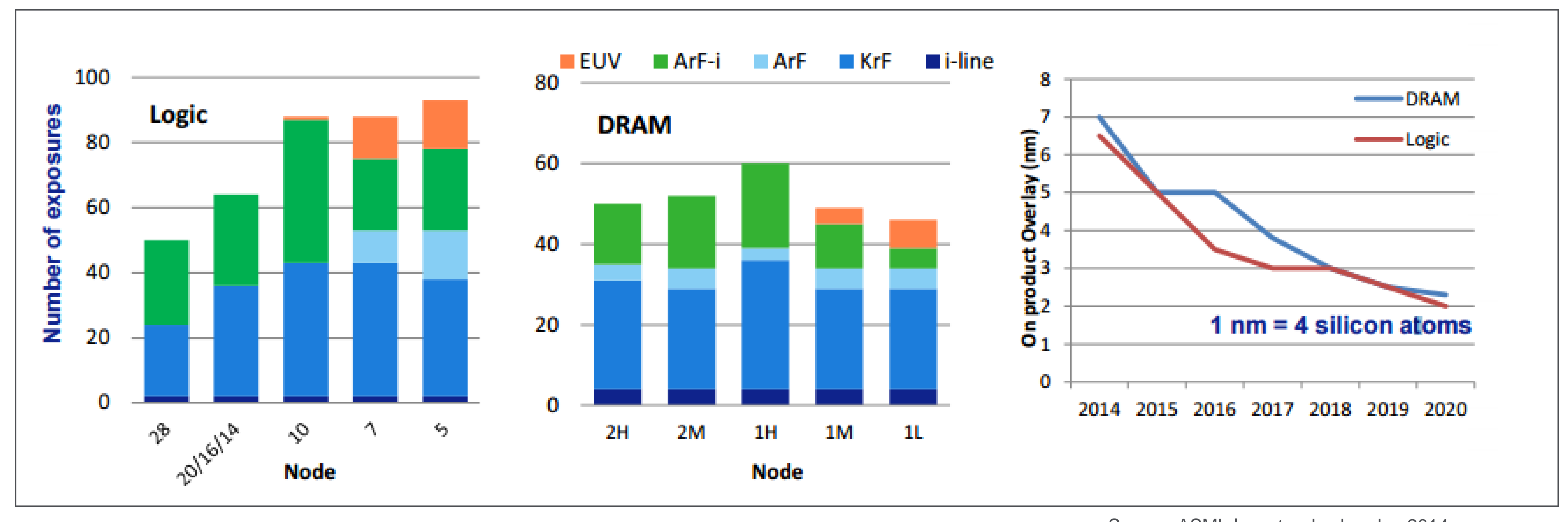
Patterning:

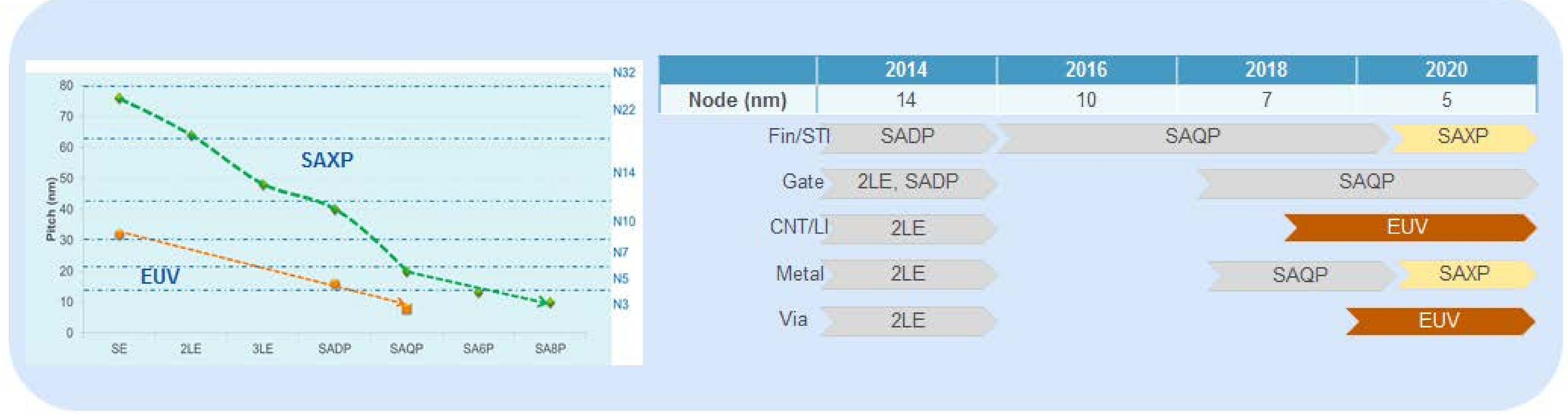


Source: ASML Investor day London 2014

Challenges:

- Number of mask counts doubled from 28nm to 14nm node
- Multi patterning continues
- Overlay specifications now are the challenge

Patterning Technology Roadmap



EUV Patterning technology readiness?

- Multi-Patterning enables Scaling but…
- SAXP brings it's set of challenges: cost & complexity
- Overlay / Patterning: technical challenges

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Summary

- Scaling:
  - After FinFET transition Logic continues to scale faster than Foundry/Mobile
  - Even with new node cadence from 2 to 2.5~3 years (10nm intro).
  - Vertical integration/ architectural changes – like GAA & 3DNand
  - With Materials engineering
- Transistor:
  - Electrostatic challenges while integrating vertical 3D structures
  - Parasitic Capacitance
- Patterning:
  - Multi-pass patterning being used due to the uncertainty of EUV introduction.
  - EUV: economics & infrastructure obstacles – earliest 7nm timing
  - SAXP: cost & materials/architectural engineering challenges