Limitations and Challenges to Meet Moore's Law

Advanced Product and Technology Development
Maydan Technology Center

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State of the art:
• cleanroom
• toolsets
• metrology
• analysis
• module development
• test & reliability
Introduction

Why do we scale?

Limitations and Challenges:
- Transistor
- Patterning
5nm is the end of Moore?

**Always Moore**
Number of transistors in CPU*
Log scale

**MOORE’S LAW DEFINED**

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**Faith no Moore**
Selected predictions for the end of Moore’s Law

<table>
<thead>
<tr>
<th>Cited reason:</th>
<th>Economic limits</th>
<th>Technical limits</th>
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<tbody>
<tr>
<td>Gordon Moore, Intel</td>
<td>1995</td>
<td>2005</td>
</tr>
<tr>
<td>G. Dan Hutcheson, VLSI Research</td>
<td>1996</td>
<td>2003</td>
</tr>
<tr>
<td>Isaac Chuang, IBM Research</td>
<td>2000</td>
<td>2020</td>
</tr>
<tr>
<td>Paolo Gargani, Intel</td>
<td>2003</td>
<td>2021</td>
</tr>
<tr>
<td>Lawrence Krauss, Case Western, and Glenn Starkman, CERN</td>
<td>2004</td>
<td>approx. 2060</td>
</tr>
<tr>
<td>Gordon Moore, Intel</td>
<td>2005</td>
<td>2015-25</td>
</tr>
<tr>
<td>Michio Kaku, City College of NY</td>
<td>2011</td>
<td>2021-22</td>
</tr>
<tr>
<td>Robert Colwell, DARPA; (fmr) Intel</td>
<td>2013</td>
<td>2020-22</td>
</tr>
<tr>
<td>Gordon Moore, Intel</td>
<td>2015</td>
<td>2025</td>
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Sources: Press reports; The Economist, Economist.com
Feasible down to 5nm?

- Press Release Albany New York: IBM, Samsung & Globalfoundries; working 7nm transistors.

- ISSC conference early 2015:
  - Head of Samsung R&D keynote: ‘no fundamental difficulties until 5nm’

- Intel conference call: 10nm pushed out another year (3 year cadence vs. 2 year) due to:
  - "The lithography is continuing to get more difficult as you try and scale, and the number of multi-pattern steps you have to do is increasing," - Brian Krzanich
  - Looking at another round of 14nm and ‘other means’ to improve performance.
  - ‘other means’: Skylake vs. Broadwell
Scaling by node

Industry Technology Scaling Trend
- Logic ahead by one gen (2 years - 10nm ~ foundry 7nm)

Notable Speculation on Timing
- 10nm for next gen phone in 2017.
- Earliest possible EUV insertion: 7nm (to what extent?)
- Next earliest transistor architectural change (GAA?): 7nm.
Why do we scale?

- **Performance**
  - Speed
    - though physical area is shrinking

- **Power**
  - Heat & Battery Life:
    - though features per area is increasing

- **Cost**
What are we scaling for?

Notable players:
Apple
Amazon
Google
Microsoft
Facebook

Interesting Factoids:
• Huge carbon footprint / large % electrical consumption
• over 38% of large companies expected to exceed IT capacity within 18 months - IoT
• the average life of a data center is 9 years
Scaling on a macro level?

Challenges:
Performance: Switching /transmission; speed, data integrity/back up; security.
Power: For every 100 watts 10% of world’s electrical demand?
Cost: Scaling requirements

What’s Inside.
- less about internal server speed
- More about applications
- And external challenges
The current tool of choice for data collection:

- From PC to mobility – getting smaller
- And now…
- And next → Internet of Things.
Scaling challenges for next nodes

- Limited by electrostatic control at the transistor with no further innovations.
- Additional constrained by added mask costs for multi-patterning solutions.
- Slower logic area scaling for ≤10nm. Both gate and interconnect pitches need to be relaxed.

- Material/Architecture/Process innovation with multi-pass pattering solutions and design innovative solutions required.

- Constant node to node logic area scaling:
  - Slower gate pitch scaling ➔ Faster interconnect pitch scaling
  - Faster gate pitch scaling ➔ Slower interconnect pitch scaling
Scaling challenges for next nodes

### Changes in Scaling

**THEN**
- Scaling drove down cost
- Scaling drove performance
- Performance constrained
- Active power dominates
- Independent design-process

**NOW**
- Scaling drives down cost
- **Materials** drive performance
- **Power** constrained
- **Standby power** dominates
- **Collaborative design-process**

> 45nm Materials
> Additional Materials at <45nm

Source: Kuhn SSDM Japan 2009

Materials and process innovations required

Source: Kuhn SSDM Japan 2009

Source: Applied Materials Investor Day 2014

### 3D Structure

- Si nanowire channel

Source: Applied Materials
Superior Electrostatic Control to Enable Gate Scaling

Improving Gate Control

Key Challenges
- Nanowire formation
- Bottom isolation
- Nanowire spacer
- Stressor material
- High k metal gate formation
- S/D & Extension doping

Reducing body width and increasing number of gates enables gate length scaling

\[ \lambda = \frac{1}{n \cdot \varepsilon_{oxide}} \sqrt{\frac{e_{channel}}{W_{body} t_{ox}}} \]

\( n = \# \text{ of gates} \)

\( \lambda \) Normalizes the channel length for the capacitor coupling in the transistor.
Parasitic Resistance: Increasing Contribution of $R_{\text{contact}}$

**Contact resistance reduction**

**Challenges:**
- Increasing parasitic resistance comes from $R_{\text{contact}}$.
- $R_{\text{plug}}$ dominant resistance at $\leq 10$nm CD with conventional W

**Technology Solutions**
- Interface Engineering
- Schotky Barrier Height reduction (III-V)
- Silicidation
- Low Resistivity Contact Fill
- Contact Area Scaling

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**Parasitic resistance components of FinFET. Source: Synopsis Simulation**
Parasitic Capacitance Fix solutions for Power Reduction

Parasitic capacitance reduction

Scaling Challenges:
- Gate to drain capacitance increases with Lg scaling
- Parasitic RC for scaled device increases

Technology challenges:
- Lower k ~ 4 for spacer and ESL
- Selectivity for removal of ESL
- Narrow contact, narrow stressor
# Transistor Challenges

<table>
<thead>
<tr>
<th>Year</th>
<th>2014</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
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<tbody>
<tr>
<td>Node (nm)</td>
<td>14</td>
<td>10</td>
<td>7</td>
<td>5</td>
</tr>
<tr>
<td>Lg (nm)</td>
<td>20</td>
<td>16</td>
<td>12</td>
<td>9</td>
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- **Architecture**: FinFET
- **S/D Stresor**: SiCP (n) / SiGe (p)
- **Metal Gate**: ALD Metal, W fill

**Gate All Around (GAA)**

- Higher doping (n) / Ge-rich SiGe (p)
- Multi VT by MG

- **Solve Transistor Technology Challenges**
  - Gate control improvement – 3D scaling
  - Contact Rc – materials engineering for $R_{\text{contact}}$
  - Parasitic capacitance reduction – materials engineering

*With continued scaling: electro static resistance and parasitic capacitance control*
Multi-patterning vs. EUV

Process impacts on CD Variability

Source: IBM, SPIE’15

EUV

Source: P. Naulleau, Berkeley Lab
Patterning

**EUV challenges:**

- Potential (imaging) is good
- Source power:
  - wafers per hour
  - Cost of Ownership
- Mask technology:
  - Manufacturing cost & short lifetime
  - High consumable cost:
    - Pellice
    - Blanks
  - Ability to inspect
- Photo-chemicals…
- Infrastructure
Patterning:

Challenges:
- Number of mask counts doubled from 28nm to 14nm node
- Multi patterning continues
- Overlay specifications now are the challenge

Source: ASML Investor day London 2014
EUV Patterning technology readiness?

- Multi-Patterning enables Scaling but…
- SAXP brings it’s set of challenges: cost & complexity
- Overlay / Patterning: technical challenges
Summary

- **Scaling:**
  - After FinFET transition Logic continues to scale faster than Foundry/Mobile
  - Even with new node cadence from 2 to 2.5~3 years (10nm intro).
  - Vertical integration/ architectural changes – like GAA & 3DNand
  - With Materials engineering

- **Transistor:**
  - Electrostatic challenges while integrating vertical 3D structures
  - Parasitic Capacitance

- **Patterning:**
  - Multi-pass patterning being used due to the uncertainty of EUV introduction.
  - EUV: economics & infrastructure obstacles – earliest 7nm timing
  - SAXP: cost & materials/architectural engineering challenges