

Electromigration Simulation Flow For Chip-Scale Parametric Failure Analysis

Valeriy Sukharev¹, Jun-Ho Choy¹, Armen Kteyan², and Xin Huang³

¹Mentor Graphics, Fremont, CA, USA ²Mentor Graphics, Armenia ³UCR, Riverside, CA, USA



Outline

- Introduction and motivations
- A role of residual stress and temperature in EM-induced degradation
- Methodology of across-interconnect residual stress assessment
- Methodology of across-interconnect temperature assessment
- Voiding-induced IR-drop degradation parametric failure
- Characterization techniques for models/methodology validation



Electromigration

- Material depletion and accumulation occurring at the sites of atomic flux divergence results the localized tensile and compressive stresses.
- Resulting stress gradient creates a backflow atomic flux.
- Immortality: the interconnect segment will be immortal, if the electron-wind and back-stress forces balance each other before the critical stresses needed for void nucleation or metal extrusion are developed.





General Physical Model

If atom flux diverges somewhere inside metal line then accumulation or depletion of atoms is happening there: $\partial N = \overline{\sigma} = \partial \sigma_{\rm ext} - \partial \sigma_{\rm ext}$



© 2010 Mentor Graphics Corp. www.mentor.com



Black's equation based MTTF





A set of calculated MTTF obtained for different T_{accel} and j_{accel} is used for extraction of the current density exponent *n* and apparent activation energy *E* used in the Black's equation:

$$MTTF = \frac{A}{j^n} \exp\left\{\frac{E}{kT}\right\}$$

• Assuming an "universal" character of the extracted *n* and *E*, the MTTF at the used conditions is:

$$MTTF_{use} = MTTF_{accel} (j_{accel} / j_{use})^n \exp\left\{\frac{E}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{accel}}\right)\right\}$$

Experiments demonstrates that **n** and **E** by themselves are the functions of both **j** and **T**



M. Hauschildt, C. Hennesthal, G. Talut, et al. (GF & Fraunhofer), 2C.1.1, IRPS 2013



EM Assessment – PROBLEM!

- Stress and temperature dependency of the current density exponent,
- Current density and temperature dependency of the activation energy
- Across-interconnect temperature and residual stress variation

ALL THESE FACTORS MAKE **QUESTIONABLE** USING BLACK EQUATION and BLECH LIMIT (CRITICAL PRODUCT) FOR ACCURATE EM ASSESSMENT!



$$t_{nuc} = \frac{A(\vec{r}, \sigma_{res})}{j^{n(T)}} \exp\left\{\frac{E(j, T)}{kT}\right\}$$
$$(j \times L)_{crit} = \frac{\Omega(\sigma_{EM} \pm \sigma_{res}(\vec{r}, T))}{eZ\rho}$$



EM Assessment requires

- Current density assessment
- Temperature assessment
- Residual stress assessment



STRESS ASSESSMENT

3D TSS (Through Si Stacking) Technology

CDMA Technologies

Die Integration Technology

- using Through Si Vias
- electrical connection from front to back (on die or interposer)
- Value Proposition

uBumps

Tier 1

- Small form factor (in X-Y &Z)
- Improved Performance
- Heterogeneous Integration
- Typical Implementation
- e.g. WIO Memory-on-Logic
 - stacking orientation: F2B
 - TSV via diameter ~ 5u
 - wafer thickness ~ 50
- e.g. Die on (Active) Interposer
 - stacking orientation: F2F
 - TSV via diameter $\sim 10u$
 - wafer thickness ~ 100 u

Fraunhofer



© 2010 Mentor Graphics Corp. www.mentor.com



Multiscale methodology for calculation of device-todevice variation of stress: Stress Exchange Format



Effective mechanical properties of BEoL, BRDL interconnects and Si/TSV bulk layer

- Theory of the mechanical properties of anisotropic composites is employed.
- Required input: (a) Thermo-mechanical properties of each material metal, dielectric: CTE, Young's moduli, Poisson factors; (b) fraction of dispersed phase; (c) routing direction of the metal layer.
- For each bin of each layer of interconnect, depending on routing direction: for example the Young's modulus:

$$E_{\parallel}^{i,j} = E_{M} \rho_{M}^{i,j} + E_{D} \left(1 - \rho_{M}^{i,j} \right)$$
$$E_{\perp}^{i,j} = \frac{E_{M} E_{D}}{E_{D} \rho_{M}^{i,j} + E_{M} \left(1 - \rho_{M}^{i,j} \right)}$$





Young's modulus components for M1 layer





Supported Compact Models

1. Package-scale: Warpage-Induced Stress





2. Compact Model for Bump-Induced Displacements



3. Effect of Non-Uniform Interconnect



Stress component distributions obtained with: "smeared" (dashed line) and non-uniform (solid line) interconnects.



4. Compact Model for TSV-Induced Stress:

Based on: S. Ryu, K. Lu, X., et Al., , "Impact of Near-Surface Thermal Stresses on Interfacial Reliability of Through-Silicon Vias for 3-D Interconnects", IEEE TDMR, VOL. 11, NO. 1, (2011) pp. 35-43



© 2010 Mentor Graphics Corp. www.mentor.com



Residual stress in on-chip interconnect

Interconnect tree is a elemental EM reliability unit representing a continuously connected, highly conductive metal (Cu) lines within one layer of metallization, terminated by diffusion barriers.





TEMPERATURE ASSESSMENT

Major components

- MGC's effective thermal properties extractor.
 - Each interconnect layer is considered as a composite: a mixture of metal fibers included in a dielectric matrix.
 - Calculates the effective thermal conductivity (k_i , i=x,y,z), specific heat of each interconnect layer as a function of local metal density (ρ_M).
- Lateral components $K_{x,y}$ inside each metal layer are determined by a routing direction:

 $k_{\mu} = \rho_{M} k_{M} + (1 - \rho_{M}) k_{\mu D}$

 $k_{z} = \rho_{M}k_{M} + (1 - \rho_{M})k_{HD}$

 $k_{\perp} = k_{ILD} \left| 1 + \frac{\rho_M}{k_{ILD} / (k_M - k_{ILD}) + (1 - \rho_{\perp}) / 2} \right|$

- Parallel to the routing direction:
- Normal to the routing direction:
- A vertical component:
 - Thermal Netlist Builder.
 - A die is represented by a 3D array of cuboidal thermal cells. Each cell contains a thermal node, and is characterized by local effective thermal properties(R_{th}, C_{th}).
 The array transforms into a thermal netlist.

SPICE simulator.

- Calculates transistor power consumption.
- Solves for temperature for each thermal node.

Effective thermal properties of a die





From effective thermal props to thermal netlist

- Construct an array of cuboidal cells of dimension, LxLxt : "L" is user-supplied binSize.
- For each cell, MGC's engine uses Calibre to extract local metal density, and calculates effective thermal properties.
- Thermal netlist builder transforms effective thermal properties into R_{th} and C_{th}.

$$\begin{split} R_{top/bottomi} &= \frac{1}{k_{z,i}} \frac{t_{M6}/2}{L^2}; \ R_{north/southi} = \frac{1}{k_{y,i}} \frac{L/2}{t_{M6}L}; \ R_{east/west,i} = \frac{1}{k_{x,i}} \frac{L/2}{t_{M6}L} \\ C_{cell,i} &= S_i \cdot (L \cdot L \cdot t_{M6}) \end{split}$$

- The array transforms into a thermal netlist.
- Consideration on boundaries
 - Fixed T with V source & R=0; Insulation with large R.



Power map



Temperature across M1

 t_{M6}

t_{v5√}





Cell i: $(\rho_{Mi}, k_{xi}, k_{yi}, k_{zi}, S_i)$

z // top

y // north

x // east

z // topy // northx // east

STEP1: Obtain thermal properties of each bin

- Run **mPower** to obtain power dissipation map.
- Run MGC thermal properties extractor to obtain per layer effective thermal properties of each layer.
- Run a script to obtain per bin thermal properties.

STEP2: Generate thermal netlist

- Input :
 - Thermal properties of each bin (rawBin.txt)
 - Location
 - Thermal conductance in 6 directions
 - Power consumption
 - Boundary condition
 - etc.
 - Chip size, bin size, #layers
- Output:
 - Thermal netlist (.spef)
 - Control file (Tamb (V), Power Sources (Is))

STEP3: PERC calcd solver (static analysis): Obtain temperature distribution

- Input:
 - Thermal netlist, control file
- Output:
 - temperature distribution -> Used in EM analysis



i j k: {gx gy gz} Cap U Tinit : x1 y1 z1 x2 y2 z2

0.0148702 0.00238877755511} 3.27732222e-08 0 320 8.078e-05 1.8e-05 0

{2.98e-05 2.98e-05 1.192} 6.56778e-11 0.0230466 320 8.078e-05 1.8e-05 4.99e-05 0.00010078 3.8e-05 5e-05

INTERCONNECT SCALE EM MODELING

Chip-scale EM assessment

Interconnect functionality

- interconnectivity for signal propagation
 bidirectional pulsed currents
- voltage delivery
 -unidirectional current
 - power grids, more susceptible to EM effect

Traditional segment-based EM assessment

- single segment based stress analysis
 - assume individual segment is confined by diffusion barriers
 - however, in power grids, atoms can diffuse in the interconnect tree, stress redistribution
- EM induced failure rate of the individual segment

EM induced degradation in power grids

- high level of redundancy
- Failure: loss of performance, parametric failure
 - cannot deliver needed voltage to any point of the circuitry

New methodology for EM assessment:

- IR drop based assessment
- physics based models for void initiation and evolution



Interconnect tree



Interconnect tree

Follow Carl Thompson we consider interconnect trees, which are the continuously connected conductor metals within one layer of metallization confined by the diffusion barrier liners, as segments where EM assessment should be done.



Interconnect tree; sidewalls and bottoms of the lines and exit vias are covered by metal diffusion liners (Ta/TaN).

20





Dielectric (SiN) diffusion barrier layers covering tops of the metal lines.





Interconnect segment vs. wire





Closed-form analytical solution for stress evolution in the multi-branched interconnect tree



with shown directions of

the electron flows.



Evolution of the stress distribution along the segment of the shown T-shaped tree; (a) line 1, (b) line 2, and (c) line 3.

If we disassemble these brunches a standard stress evolution will take place in each of them:



V. Sukharev, X. Huang, H.-B. Chen, and S. X.-D. Tan, Proc. ACCAD, October 2014.

© 2010 Mentor Graphics Corp. www.mentor.com



Voiding

When void is nucleated the stress at the void surface is zero. The solution of the stress kinetics equation with the zero-flux condition at the downstream (anode) end of the line is [J. He and Z. Suo, AIP Conf. Proceedings, vol. 741, 2004]: $(t \ge t_{nuc})$

$$\sigma(x,t) = -\frac{eZ\rho jL}{\Omega} \left(\frac{x}{L} + \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n-1)^2} \sin\left[\frac{(2n-1)\pi x}{2L}\right] \exp\left\{-\left(\frac{2n-1}{2}\pi\right)^2 \frac{t}{\tau}\right\}$$

Once void is nucleated and the stress field ^{Void} is solved, the void volume is calculated from the volume of atoms drifted into the line:

Llava

 $\tau = \frac{L^2}{L} = \frac{L^2 k_B T}{L^2 k_B T}$

$$V = -A \int_{0}^{L} \Omega N_{PL} dx = -A \int_{0}^{L} \Omega \left(\frac{\sigma}{B} N_{A}\right) dx = -A \int_{0}^{L} \left(\frac{\sigma}{B}\right) dx = \frac{eZ\rho jL^{2}A}{2\Omega B} \left(1 + \frac{32}{\pi^{3}} \sum_{n=0}^{\infty} \frac{(-1)^{n}}{(2n-1)^{2}} \exp\left\{-\left(\frac{2n-1}{2}\pi\right)^{2} \frac{t}{\tau}\right\}\right)$$

There are two limiting cases for volume void: 1. Short time; stress in the line is small, so

$$\Gamma(\vec{r}) = \frac{D}{\Omega k_B T} e^{Z} \rho j \text{ and } V = \Omega \Gamma A t = \frac{e^{Z} \rho j D A t}{k_B T}$$

2. Steady state was reached; the atomic flux vanishes, void volume is saturated:

$$\sigma(x) = -\frac{eZ\rho jx}{\Omega}$$
 and $V_{sat} = -A \int_{0}^{L} \left(\frac{\sigma}{B}\right) dx = \frac{eZ\rho jL^{2}A}{2\Omega B}$



Void growth-induced line resistance change

Once V(t) is known the kinetics of line resistance can be easily calculated.

For a void volume at an instance in time t we have:

$$V_{void}(t) = \mathcal{G} * (t - t_{nuc}) HW \qquad \qquad \mathcal{G} = \frac{DeZ\rho j}{kT}$$

 $V_{void}(t) = HW \frac{DeZ\rho}{kT} \int_{t}^{t} j(t)dt$

Or, when current density depends on time:



For the corresponding change in the line resistance we can write:

Void

$$\begin{split} \Delta R &= R_{Ta}^{Void} - R_{Cu}^{Void} \\ \frac{1}{R_{Ta}^{Void}} &= \frac{1}{R_{Ta}^{void_wall}} + \frac{1}{R_{Ta}^{void_wall}} + \frac{1}{R_{Ta}^{void_bottom}} \\ R_{Ta}^{void_wall} &= \rho_{Ta} \frac{\mathcal{G} * (t - t_{nuc})}{hH}; \ R_{Ta}^{void_bottom} = \rho_{Ta} \frac{\mathcal{G} * (t - t_{nuc})}{hW}; \ R_{Cu}^{Void} = \rho_{Ta} \frac{\mathcal{G} * (t - t_{nuc})}{HW} \\ \Delta R(t) &= \mathcal{G} * (t - t_{nuc}) \left[\frac{\rho_{Ta}}{h(H+2W)} - \frac{\rho_{Cu}}{HW} \right] \approx \mathcal{G} * (t - t_{nuc}) \frac{\rho_{Ta}}{h(H+2W)} = \frac{V_{void}(t)\rho_{Ta}}{h(H+2W)HW} \end{split}$$



Steady state distribution of the hydrostatic stress inside interconnect tree in void-less regime

• Assume (just for a moment) that the void less steady state was achieved in the tree.

For the steady state: $\sigma_i^{cathod} - \sigma_j^{anode} = \Delta \sigma_{ij} = \frac{eZ\rho(j_{ij}L_{ij})}{\Omega}$

• Consider the redistribution of the atoms between sub-segments due to unblocked sub-segment ends:



along the considered tree



• Previously, we use uniform temperature distribution:

The shortest void nucleation time is characterized by the biggest steady state stress $\sigma_m(j_1, j_{2,...}, j_n)$,

$$t_{nuc}^{\rm m} \approx \frac{L_{\rm max/min}^2}{2D_0} e^{\frac{E_V + E_D}{kT}} \frac{kT}{\Omega B} \exp\left\{-\frac{f\Omega\sigma_{\rm m}\left(j_1, j_{2,\dots,j_n}\right)}{kT}\right\}$$
$$\cdot \ln\left\{\frac{\sigma_{\rm m}\left(j_1, j_{2,\dots,j_n}\right) - \sigma_{\rm Res}}{\sigma_{\rm m}\left(j_1, j_{2,\dots,j_n}\right) - \sigma_{\rm crit}}\right\}$$

With temperature variation: Void nucleation time is affected by both T and hydrostatic stress. Consider both factors to find the first nucleated void $(\min\{t_{nuc}^{i}\})$

© 2010 Mentor Graphics Corp. **www.mentor.com**



EM-induced supply voltage degradation





EM Assessment Results in IBM Benchmarks

14

12

Time to

380

6

4

2

250

X. Huang, T. Yu, V. Sukharev, and S. X.-D. Tan, Proc. IEEE/ACM Design Automation Conference (DAC'14), San Francisco, June, 2014.



TABLE: COMPARISON OF POWER GRID MTTF

Both Black's equation based series and Mesh models \diamond lead to pessimistic predictions

370

Temperature (K)

380

(vear)),

In(TTF,) 280 360

372

Temperature (K)

- TTF exponentially relates to temperature



In this work, the first failure is most likely to happen at \diamond the nodes where the initial hydrostatic stress is large



(the same as Black's equation) Reducing chip temperature/ temperature gradient could extend TTF \diamond

376

© 2010 Mentor Graphics Corp. www.mentor.com



27

 \diamond

100

Time to Failure (yrs) 7 09 08

20

360

364

368

EM effect is sensitive to temperature

EXAMPLE OF IR-DROP EM ASSESSMENT

CHIP-SCALE EM ASSESSMENT CONSIDERING THE IMPACT OF TEMPERATURE AND CPI STRESS VARIATIONS

Layout



- Design:
- 7-metal layer
- 32nm
- Dimension:184um ×184um

Layer number	Name
3	Contact
4	M1
5	V1
6	M2
7	V2
8	M3
9	V3
10	M4
11	V4
12	M5
13	YX(V5)
14	IA(M6 wide)
15	XA(V6)
16	IB(M7 wide)



Initial current density and initial IR-drop

-power net, M1 layer



30



Graphics

Temperature distribution



© 2010 Mentor Graphics Corp. www.mentor.com



EM induced IR drop change

- power net



© 2010 Mentor Graphics Corp. www.mentor.com

EM induced IR drop change

- power net

Branches with voids

- power net



Voids mainly locate in M1 layer, some voids locate in M3 layer



Chip fails when the maximum IR drop > threshold level



CALIBRATION/VALIDATION

How to calibrate/validate verification tools?

- Both types of tools predicting the effect of CPI on chip performance and chip reliability need as inputs:
 - Measured foundry and process dependent thermal-mechanical properties of the involved materials.
 - Calibrated compact models employed for calculation of the stresses and temperature across a device layer and across the whole chip.
 - Calibrated models for calculating effective thermal-mechanical properties of all composite layers (BEoL and RDL interconnects, underfill with C4 and u-bumps, silicon bulk with TSVs, etc.).
- Both types of tools need to be validated by a direct comparison between the predicted characteristics and measured:
 - Comparing the measured characteristics of individual transistors and predicted by verification tools is a validation of the CPI effect on chip performance.
 - What kind of test-structures should be used to validate the effect of CPI on chip reliability (EM as an example)?



Proof Electrical vs. Mechanical

H-Bar - TEM Lamella

Distance to TSV

CDMA Technologies

MECHANICAL DOMAIN



TEM CBED measurement of strain



ELECTRICAL DOMAIN





$$\Delta I^{simul} = -(\pi_x^I \sigma_x + \pi_y^I \sigma_y + \pi_z^I \sigma_z) I^{SPICE}$$

Good fit between simulated and measured electrical characteristics of transistors located at different distances from TSV allows to calibrate the developed tool with relatively easy accessible electrical data.

© 2010 Mentor Graphics Corp. Glacier Project www.mentor.com



Validation with the Foundry calibrated Model

Calibration was performed on ~100 gates Prediction was made for all (~4000) gates





Test-chip segment





Die Corner Array: Test-chip 28nm node

Schematics of the test structures used for model calibration: die corner









© 2010 Mentor Graphics Corp. www.mentor.com



Conclusions

- A novel methodology was developed for full-chip power/ground nets redundancy-aware EM assessment based on IR-drop analysis.
- Physics-based model was developed and implemented in the flow, for temperature- and residual stress-aware void nucleation and growth.
- A developed technique for calculating hydrostatic stress distribution inside a multi branch interconnect tree allows to avoid over optimistic prediction of the time to failure made with the Blech-Black analysis of individual branches of interconnect segment.



THANK YOU