Electromigration Simulation Flow For Chip-Scale Parametric Failure Analysis

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Outline

- Introduction and motivations
- A role of residual stress and temperature in EM-induced degradation
- Methodology of across-interconnect residual stress assessment
- Methodology of across-interconnect temperature assessment
- Voiding-induced IR-drop degradation – parametric failure
- Characterization techniques for models/methodology validation
Electromigration

- Material depletion and accumulation occurring at the sites of atomic flux divergence results the localized tensile and compressive stresses.
- Resulting stress gradient creates a backflow atomic flux.
- Immortality: the interconnect segment will be immortal, if the electron-wind and back-stress forces balance each other before the critical stresses needed for void nucleation or metal extrusion are developed.
General Physical Model

If atom flux diverges somewhere inside metal line then accumulation or depletion of atoms is happening there:

\[
\frac{\partial N_A}{\partial t} + \nabla \cdot \vec{J}_A = 0 \quad \Rightarrow \quad \frac{\partial \sigma_{\text{Hyd}}}{\partial t} = \frac{\partial}{\partial x} \left( \frac{eZj}{\Omega} + \frac{\partial \sigma_{\text{Hyd}}}{\partial x} \right)
\]

Solution of Korhonen’s equation:

\[
\sigma(x,t) = \sigma_{\text{res}} - \frac{eZj}{\Omega} \left( x + 4L \sum_{n=0}^{\infty} \frac{\cos(m_n(1/2 + x/L))}{m_n^2 \exp(m_n^2 \kappa/L^2)} \right)
\]

Condition for growing void formation:

\[
\sigma_{\text{crit}} = \sigma_{\text{res}} - \frac{eZj}{\Omega} \left( x + 4L \sum_{n=0}^{\infty} \frac{\cos(m_n(1/2 + x/L))}{m_n^2 \exp(m_n^2 \kappa \cdot t_{\text{nuc}}/L^2)} \right)
\]

Nucleation time for stable, growing void:

\[
t_{\text{nuc}} \approx \frac{L^2}{2D_0} \frac{k_B T}{\Omega B} e^{E_v + E_{\text{cl}} - \frac{\Omega \sigma_{\text{crit}} - eZjL/2}{k_B T}} \ln \left\{ \frac{eZjL}{2\Omega} \left( \frac{\sigma_{\text{res}} + eZjL/2}{2\Omega} - \sigma_{\text{crit}} \right) \right\}
\]

Evolution of the hydrostatic stress (a) along the metal line loaded with DC current, and at the cathode end of line, (b) \( j = 5 \times 10^9 A/m^2, T = 400K \).
Black’s equation based MTTF

EM accelerated test: $T_{\text{accel}}$ and $j_{\text{accel}}$

- TTF averaged with the accepted distribution function provides mean time to failure (MTTF).

- A set of calculated MTTF obtained for different $T_{\text{accel}}$ and $j_{\text{accel}}$ is used for extraction of the current density exponent $n$ and apparent activation energy $E$ used in the Black’s equation:

$$MTTF = \frac{A}{j^n} \exp \left\{ \frac{E}{kT} \right\}$$

- Assuming an “universal” character of the extracted $n$ and $E$, the MTTF at the used conditions is:

$$MTTF_{\text{use}} = MTTF_{\text{accel}} \left( \frac{j_{\text{accel}}}{j_{\text{use}}} \right)^n \exp \left\{ \frac{E}{k} \left( \frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{accel}}} \right) \right\}$$

Experiments demonstrates that $n$ and $E$ by themselves are the functions of both $j$ and $T$
EM Assessment – PROBLEM!

- Stress and temperature dependency of the current density exponent,
- Current density and temperature dependency of the activation energy
- Across-interconnect temperature and residual stress variation

ALL THESE FACTORS MAKE QUESTIONABLE USING BLACK EQUATION and BLECH LIMIT (CRITICAL PRODUCT) FOR ACCURATE EM ASSESSMENT!

\[
t_{\text{nuc}} = \frac{A(\vec{r}, \sigma_{\text{res}})}{j^n(T)} \exp \left\{ \frac{E(j, T)}{kT} \right\}
\]

\[
(j \times L)_{\text{crit}} = \frac{\Omega(\sigma_{\text{EM}} \pm \sigma_{\text{res}}(\vec{r}, T))}{eZ \rho}
\]
EM Assessment requires

- Current density assessment
- Temperature assessment
- Residual stress assessment
STRESS ASSESSMENT
Die Integration Technology
- using Through Si Vias
- electrical connection from front to back (on die or interposer)

Value Proposition
- Small form factor (in X-Y & Z)
- Improved Performance
- Heterogeneous Integration

Typical Implementation
- e.g. WIO Memory-on-Logic
  - stacking orientation: F2B
  - TSV via diameter ~ 5μ
  - wafer thickness ~ 50μ
- e.g. Die on (Active) Interposer
  - stacking orientation: F2F
  - TSV via diameter ~ 10μ
  - wafer thickness ~ 100μ
Multiscale methodology for calculation of device-to-device variation of stress: Stress Exchange Format

**Package-scale simulation (FEA)**
**Input:** geometry; material properties; smeared mechanical properties for RDLs, Silicon/TSV bulk, interconnect.
**Output:** field of displacement components on the die faces.

**Die-scale simulation (FEA)**
**Input:** geometry; field of displacements on the die faces; coordinate-dependent mechanical properties for RDLs, Silicon/TSV bulk, interconnect.
**Output:** Distribution of the strain components across device layer.

**Layout-scale with feature-scale resolution:**
**Input:** GDS.
**Output:** distribution of the stress components across interconnect metal layer.
Effective mechanical properties of BEoL, BRDL interconnects and Si/TSV bulk layer

- Theory of the mechanical properties of anisotropic composites is employed.
- Required input: (a) Thermo-mechanical properties of each material – metal, dielectric: CTE, Young’s moduli, Poisson factors; (b) fraction of dispersed phase; (c) routing direction of the metal layer.
- For each bin of each layer of interconnect, depending on routing direction: for example the Young’s modulus:

\[
E_{||}^{i,j} = E_M \rho_M^{i,j} + E_D \left(1 - \rho_M^{i,j}\right)
\]

\[
E_{\perp}^{i,j} = \frac{E_M E_D}{E_D \rho_M^{i,j} + E_M \left(1 - \rho_M^{i,j}\right)}
\]

Young’s modulus components for M1 layer
Supported Compact Models

1. Package-scale: Warpage-Induced Stress

2. Compact Model for Bump-Induced Displacements

3. Effect of Non-Uniform Interconnect

Stress component distributions obtained with: “smeared” (dashed line) and non-uniform (solid line) interconnects.

4. Compact Model for TSV-Induced Stress:
Residual stress in on-chip interconnect

Interconnect tree is an elemental EM reliability unit representing a continuously connected, highly conductive metal (Cu) lines within one layer of metallization, terminated by diffusion barriers.
TEMPERATURE ASSESSMENT
Major components

- **MGC’s effective thermal properties extractor.**
  - Each interconnect layer is considered as a composite: a mixture of metal fibers included in a dielectric matrix.
  - Calculates the effective thermal conductivity \(k_i, i=x,y,z\), specific heat of each interconnect layer as a function of local metal density \(\rho_M\).
  - Lateral components \(K_{x,y}\) inside each metal layer are determined by a routing direction:
    - Parallel to the routing direction: \(k_{ll} = \rho_M k_M + (1 - \rho_M) k_{ILD}\)
    - Normal to the routing direction: \(k_{l} = k_{ILD} \left[1 + \rho_M \frac{k_{ILD}}{k_M - k_{ILD}} + (1 - \rho_M)/2\right]\)
    - A vertical component: \(k_z = \rho_M k_M + (1 - \rho_M) k_{ILD}\)

- **Thermal Netlist Builder.**
  - A die is represented by a 3D array of cuboidal thermal cells. Each cell contains a thermal node, and is characterized by local effective thermal properties \(R_{th}, C_{th}\).
  - The array transforms into a thermal netlist.

- **SPICE simulator.**
  - Calculates transistor power consumption.
  - Solves for temperature for each thermal node.
From effective thermal props to thermal netlist

- Construct an array of cuboidal cells of dimension, LxLxL: “L” is user-supplied binSize.
- For each cell, MGC’s engine uses Calibre to extract local metal density, and calculates effective thermal properties.
- Thermal netlist builder transforms effective thermal properties into $R_{th}$ and $C_{th}$.

$$
R_{top/bottom,i} = \frac{1}{k_{z,i}} \frac{t_{M6}/2}{L^2}; \quad R_{north/south,i} = \frac{1}{k_{y,i}} \frac{L/2}{t_{M6}L}; \quad R_{east/west,i} = \frac{1}{k_{x,i}} \frac{L/2}{t_{M6}L}
$$

$$
C_{cell,i} = S_i \cdot (L \cdot L \cdot t_{M6})
$$

- The array transforms into a thermal netlist.
- Consideration on boundaries
  - Fixed T with V source & R=0; Insulation with large R.

Design

Power map

Temperature across M1
Flow

**STEP1:** Obtain thermal properties of each bin
- Run **mPower** to obtain power dissipation map.
- Run MGC thermal properties extractor to obtain per layer effective thermal properties of each layer.
- Run a script to obtain per bin thermal properties.

**STEP2:** Generate thermal netlist
- **Input:**
  - Thermal properties of each bin (rawBin.txt)
    - Location
    - Thermal conductance in 6 directions
    - Power consumption
    - Boundary condition
    - etc.
  - Chip size, bin size, #layers
- **Output:**
  - Thermal netlist (.spef)
  - Control file (Tamb (V), Power Sources (Is))

**STEP3:** **PERC calcd solver** (static analysis): Obtain temperature distribution
- **Input:**
  - Thermal netlist, control file
- **Output:**
  - temperature distribution -> Used in EM analysis
INTERCONNECT SCALE EM MODELING
Chip-scale EM assessment

Interconnect functionality
• interconnectivity for signal propagation
  - bidirectional pulsed currents
• voltage delivery
  - unidirectional current
  - power grids, more susceptible to EM effect

Traditional segment-based EM assessment
• single segment based stress analysis
  - assume individual segment is confined by diffusion barriers
  - however, in power grids, atoms can diffuse in the interconnect tree, stress redistribution
• EM induced failure rate of the individual segment

EM induced degradation in power grids
• high level of redundancy
• Failure: loss of performance, parametric failure
  - cannot deliver needed voltage to any point of the circuitry

New methodology for EM assessment:
• IR drop based assessment
• physics based models for void initiation and evolution
Follow Carl Thompson we consider interconnect trees, which are the continuously connected conductor metals within one layer of metallization confined by the diffusion barrier liners, as segments where EM assessment should be done.

Interconnect tree; sidewalls and bottoms of the lines and exit vias are covered by metal diffusion liners (Ta/TaN).

Dielectric (SiN) diffusion barrier layers covering tops of the metal lines.

Electron flow inlets.

Electron flow exits.

C.V. Thompson, 11th International workshop on stress-induced phenomena in metallization, AIP, 2005
Interconnect segment vs. wire

Current density

Hydrostatic stress
Closed-form analytical solution for stress evolution in the multi-branched interconnect tree

Evolution of the stress distribution along the segment of the shown T-shaped tree; (a) line 1, (b) line 2, and (c) line 3.

If we disassemble these branches a standard stress evolution will take place in each of them:

Voiding

When void is nucleated the stress at the void surface is zero. The solution of the stress kinetics equation with the zero-flux condition at the downstream (anode) end of the line is [J. He and Z. Suo, AIP Conf. Proceedings, vol. 741, 2004]: \( t \geq t_{nuc} \)

\[
\sigma(x,t) = -\frac{eZ\rho jL}{\Omega} \left( \frac{x}{L} + \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n-1)^2} \exp \left\{ -\left( \frac{2n-1}{2} \pi \right)^2 \frac{t}{\tau} \right\} \right)
\]

Here,

\[
\tau = \frac{L^2}{\kappa} = \frac{L^2 k_B T}{DB \Omega}
\]

Once void is nucleated and the stress field is solved, the void volume is calculated from the volume of atoms drifted into the line:

\[
V = -A \int_0^L \Omega N_A dx = -A \int_0^L \left( \frac{\sigma}{B} N_A \right) dx = -A \int_0^L \left( \frac{\sigma}{B} \right) dx = \frac{eZ\rho jL^2 A}{2\Omega B} \left( 1 + 32 \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n-1)^2} \exp \left\{ -\left( \frac{2n-1}{2} \pi \right)^2 \frac{t}{\tau} \right\} \right)
\]

There are two limiting cases for volume void:

1. Short time; stress in the line is small, so

\[
\Gamma(\tilde{r}) = \frac{D}{\Omega k_B T} eZ\rho j \quad \text{and} \quad V = \Omega \Gamma t = \frac{eZ\rho j DAt}{k_B T}
\]

2. Steady state was reached; the atomic flux vanishes, void volume is saturated:

\[
\sigma(x) = -\frac{eZ\rho j x}{\Omega} \quad \text{and} \quad V_{\text{sat}} = -A \int_0^L \left( \frac{\sigma}{B} \right) dx = \frac{eZ\rho j L^2 A}{2\Omega B}
\]

There is an associated graph showing the relationship between L (\( \mu \text{m} \)), J (mA/\mu m^2), and the void volume density (V/\Omega B \text{cm}^2). The graph includes data points at L = 15, 30, and 70 \( \mu \text{m} \), with corresponding J values of 23.6 mA/\mu m^2. The relationship is expressed by Eq (1).
Void growth-induced line resistance change

Once \( V(t) \) is known the kinetics of line resistance can be easily calculated. For a void volume at an instance in time \( t \) we have:

\[
V_{\text{void}}(t) = \vartheta \ast (t - t_{\text{nuc}})HW
\]

\[
\vartheta = \frac{DeZ\rho j}{kT}
\]

Or, when current density depends on time:

\[
V_{\text{void}}(t) = HW \frac{DeZ\rho}{kT} \int_{t_{\text{nuc}}}^{t} j(t) dt
\]

For the corresponding change in the line resistance we can write:

\[
\Delta R = R_{\text{Ta}}^{\text{Void}} - R_{\text{Cu}}^{\text{Void}}
\]

\[
\frac{1}{R_{\text{Ta}}^{\text{Void}}} = \frac{1}{R_{\text{Ta}}^{\text{void - wall}}} + \frac{1}{R_{\text{Ta}}^{\text{void - wall}}} + \frac{1}{R_{\text{Ta}}^{\text{void - bottom}}}
\]

\[
R_{\text{Ta}}^{\text{void - wall}} = \rho_{\text{Ta}} \frac{\vartheta \ast (t - t_{\text{nuc}})}{hH}; \quad R_{\text{Ta}}^{\text{void - bottom}} = \rho_{\text{Ta}} \frac{\vartheta \ast (t - t_{\text{nuc}})}{hW}; \quad R_{\text{Cu}}^{\text{Void}} = \rho_{\text{Ta}} \frac{\vartheta \ast (t - t_{\text{nuc}})}{HW}
\]

\[
\Delta R(t) = \vartheta \ast (t - t_{\text{nuc}}) \left[ \frac{\rho_{\text{Ta}}}{h(H + 2W)} - \frac{\rho_{\text{Cu}}}{HW} \right] \approx \vartheta \ast (t - t_{\text{nuc}}) \frac{\rho_{\text{Ta}}}{h(H + 2W)} = \frac{V_{\text{void}}(t)\rho_{\text{Ta}}}{h(H + 2W)HW}
\]
Steady state distribution of the hydrostatic stress inside interconnect tree in void-less regime

• Assume (just for a moment) that the void less steady state was achieved in the tree.

For the steady state: \( \sigma_i^{\text{cathod}} - \sigma_j^{\text{anode}} = \Delta \sigma_{ij} = \frac{eZ\rho(j_{ij}L_{ij})}{\Omega} \)

• Consider the redistribution of the atoms between sub-segments due to unblocked sub-segment ends:

\[
\sum_{i=1}^{n} \left( \sigma_i - \frac{\sigma_T + \frac{B}{3} \left( \frac{R_i}{\delta} \right) e^{-\frac{E_{ij}}{kT}} + \frac{eZ\rho(j_{ij}L_{ij})}{2\Omega} \right) L_{ij} = 0
\]

If \( \sigma_i \geq \sigma_{\text{crit}} \), this sub-segment is suspicious to EM failure.

Distribution of the steady state hydrostatic stress along the considered tree

• Previously, we use uniform temperature distribution:

The shortest void nucleation time is characterized by the biggest steady state stress \( \sigma_m(j_1, j_2, ..., j_n) \)

\[
t_{\text{nuc}}^m \approx \frac{L_i^2}{2D_0} \frac{E_i + E_2}{kT} \frac{kT}{\Omega B} \exp \left\{ -\frac{f\Omega \sigma_m(j_1, j_2, ..., j_n)}{kT} \right\} \cdot \ln \left\{ \frac{\sigma_m(j_1, j_2, ..., j_n) - \sigma_{\text{Res}}}{\sigma_m(j_1, j_2, ..., j_n) - \sigma_{\text{crit}}} \right\}
\]

• With temperature variation: Void nucleation time is affected by both T and hydrostatic stress. Consider both factors to find the first nucleated void (\( \min\{t_{\text{nuc}}^i\} \))
EM-induced supply voltage degradation

- Nucleated void
- Growing void
- Saturated void
EM Assessment Results in IBM Benchmarks

Both Black’s equation based series and Mesh models lead to pessimistic predictions.

EM effect is sensitive to temperature
- TTF exponentially relates to temperature (the same as Black’s equation)

Reducing chip temperature/ temperature gradient could extend TTF

TABLE: COMPARISON OF POWER GRID MTTF USING BLACK’S EQUATION AND PROPOSED MODEL

<table>
<thead>
<tr>
<th>Power Grid</th>
<th>Time to Failure (yrs)</th>
<th>CPU time of Our Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Black’s Equation</td>
<td>Proposed model</td>
</tr>
<tr>
<td>Nodes</td>
<td>Series</td>
<td>Mesh</td>
</tr>
<tr>
<td>IBMPG2</td>
<td>61797</td>
<td>7.82</td>
</tr>
<tr>
<td>IBMPG3</td>
<td>407279</td>
<td>15.77</td>
</tr>
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<td>IBMPG4</td>
<td>474836</td>
<td>12.58</td>
</tr>
<tr>
<td>IBMPG5</td>
<td>497658</td>
<td>6.34</td>
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<tr>
<td>IBMPG6</td>
<td>807825</td>
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<td>IBMPGNEW1</td>
<td>715022</td>
<td>13.64</td>
</tr>
<tr>
<td>IBMPGNEW2</td>
<td>715022</td>
<td>12.44</td>
</tr>
</tbody>
</table>

(a) Voltage drop (V) distribution and (b) Initial steady state hydrostatic stress (Pa) distribution predicted by initial current density in IBMPG2.

In this work, the first failure is most likely to happen at the nodes where the initial hydrostatic stress is large.

EXAMPLE OF IR-DROP EM ASSESSMENT
CHIP-SCALE EM ASSESSMENT CONSIDERING THE IMPACT OF TEMPERATURE AND CPI STRESS VARIATIONS
Layout

- Design:
  - 7-metal layer
  - 32nm
  - Dimension: 184μm × 184μm

<table>
<thead>
<tr>
<th>Layer number</th>
<th>Name</th>
</tr>
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<tbody>
<tr>
<td>3</td>
<td>Contact</td>
</tr>
<tr>
<td>4</td>
<td>M1</td>
</tr>
<tr>
<td>5</td>
<td>V1</td>
</tr>
<tr>
<td>6</td>
<td>M2</td>
</tr>
<tr>
<td>7</td>
<td>V2</td>
</tr>
<tr>
<td>8</td>
<td>M3</td>
</tr>
<tr>
<td>9</td>
<td>V3</td>
</tr>
<tr>
<td>10</td>
<td>M4</td>
</tr>
<tr>
<td>11</td>
<td>V4</td>
</tr>
<tr>
<td>12</td>
<td>M5</td>
</tr>
<tr>
<td>13</td>
<td>YX(V5)</td>
</tr>
<tr>
<td>14</td>
<td>IA(M6 wide)</td>
</tr>
<tr>
<td>15</td>
<td>XA(V6)</td>
</tr>
<tr>
<td>16</td>
<td>IB(M7 wide)</td>
</tr>
</tbody>
</table>
Initial current density and initial IR-drop
-power net, M1 layer
Initial hydrostatic stress
-power net, M1 layer

\[ \sigma_{\text{crit}} = 500 \text{Mpa} \]
Temperature distribution

Metal 1 layer

Temperature variation

<table>
<thead>
<tr>
<th>Layer</th>
<th>Layer number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
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</tr>
<tr>
<td>Si_device</td>
<td>2</td>
</tr>
<tr>
<td>Contact</td>
<td>3</td>
</tr>
<tr>
<td>M1</td>
<td>4</td>
</tr>
<tr>
<td>V1</td>
<td>5</td>
</tr>
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<td>M2</td>
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<td>V2</td>
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<tr>
<td>V3</td>
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<td>M4</td>
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<td>V4</td>
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</tr>
<tr>
<td>M5</td>
<td>12</td>
</tr>
<tr>
<td>YX</td>
<td>13</td>
</tr>
<tr>
<td>I[A(Bx)]</td>
<td>14</td>
</tr>
<tr>
<td>XA</td>
<td>15</td>
</tr>
<tr>
<td>I[B(Bx)]</td>
<td>16</td>
</tr>
</tbody>
</table>
EM induced IR drop change
- power net

Initial IR drop distribution

- Significant IR drop changes in M1 layer

Final IR drop distribution (at lifetime_{th})
EM induced IR drop change
- power net

Branches with voids
- power net

Voids mainly locate in M1 layer, some voids locate in M3 layer

Chip fails when the maximum IR drop > threshold level
CALIBRATION/VALIDATION
How to calibrate/validate verification tools?

- **Both types of tools predicting the effect of CPI on chip performance and chip reliability need as inputs:**
  - Measured foundry and process dependent thermal-mechanical properties of the involved materials.
  - Calibrated compact models employed for calculation of the stresses and temperature across a device layer and across the whole chip.
  - Calibrated models for calculating effective thermal-mechanical properties of all composite layers (BEoL and RDL interconnects, underfill with C4 and u-bumps, silicon bulk with TSVs, etc.).

- **Both types of tools need to be validated by a direct comparison between the predicted characteristics and measured:**
  - Comparing the measured characteristics of individual transistors and predicted by verification tools is a validation of the CPI effect on chip performance.
  - **What kind of test-structures should be used to validate the effect of CPI on chip reliability (EM as an example)?**
Proof Electrical vs. Mechanical

**MECHANICAL DOMAIN**

TEM CBED measurement of strain

Calibrating $\varepsilon_{th}$:

$$\sigma_x = -\sigma_y = \frac{E_S E_{th} D_{TSV}^2}{1 - 2v_S} \cos 2\theta$$

**ELECTRICAL DOMAIN**

Reconstructive FEA simulation

After FIB processing

Before FIB processing

Strain distribution in lamella

(• after FIB, — before FIB)

Good fit between simulated and measured electrical characteristics of transistors located at different distances from TSV allows to calibrate the developed tool with relatively easy accessible electrical data.

$\Delta I^{\text{simul}} = -\left(\pi_x' \varepsilon_x + \pi_y' \varepsilon_y + \pi_z' \varepsilon_z\right)^{\text{SPICE}}$
Validation with the Foundry calibrated Model

Calibration was performed on ~100 gates
Prediction was made for all (~4000) gates

Test-chip segment

Calibration Equations:
- n-ch Id_lin: $y = 0.9504x + 0.1289$, $R^2 = 0.9492$
- p-ch Id_lin: $y = 0.8711x + 0.2115$, $R^2 = 0.8514$
- n-ch Vt: $y = 0.941x - 0.0011$, $R^2 = 0.9235$
- p-ch Vt: $y = 0.9001x - 0.0036$, $R^2 = 0.8881$
Die Corner Array: Test-chip 28nm node

Schematics of the test structures used for model calibration: die corner

ΔId for pMOS

ΔId for pMOS, uA
Conclusions

• A novel methodology was developed for full-chip power/ground nets redundancy-aware EM assessment based on IR-drop analysis.

• Physics-based model was developed and implemented in the flow, for temperature- and residual stress-aware void nucleation and growth.

• A developed technique for calculating hydrostatic stress distribution inside a multi branch interconnect tree allows to avoid over optimistic prediction of the time to failure made with the Blech-Black analysis of individual branches of interconnect segment.
THANK YOU