New Applications of Chemical Mechanical Planarization

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Semiconductor Equipment | Spare Parts and Service | CMP Foundry

AVS Joint Meeting
San Jose, CA
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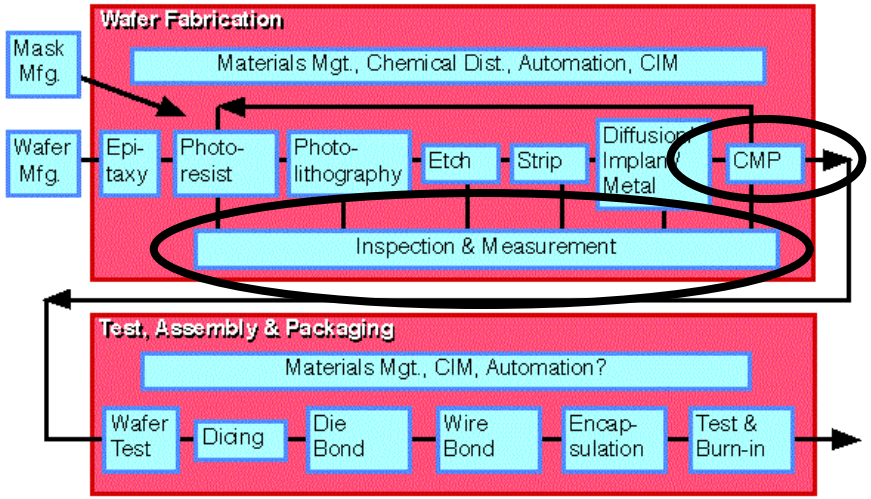
Welcome to Entrepix

infrastructure

The Chip Making Process



Copyright 1999 Infrastructure

1998	Company founded on value-add refurbishing & services
2002	Launched first of its kind CMP foundry operation
2003	New facility with sub-class 100 cleanroom
2005	Foundry ISO 9001 certification & top 5 IDM prod contracts
2007	Exclusive OEM partnership agreements
2008	Capital raise & first acquisition (Ascentec)
2009	Launched ETPX Asia (Singapore, China, Taiwan)
2012	Product expansions and Rite Track Partnership

Remanufactured Equipment

On-Site Field Services

Parts Support

Technology Upgrades

Personnel Training

Process Development

Polishing Services

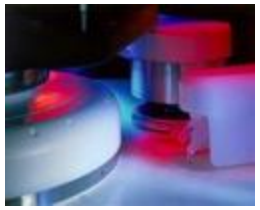
OEM Eco-Partnerships:

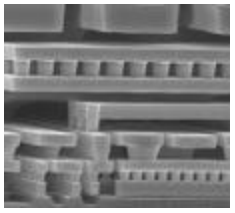
APPLIED MATERIALS. RUDOLPH TECHNOLOGIES Lam RESEARCH

Technology Renewal Partnership:

RITE TRACK www.ritetrack.com

Foundry Processing:





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Outline

CMP Intro

Process Development

Polymer CMP

SiGe Transfer Layer CMP

Oxide Nanostructure CMP

TSV CMP

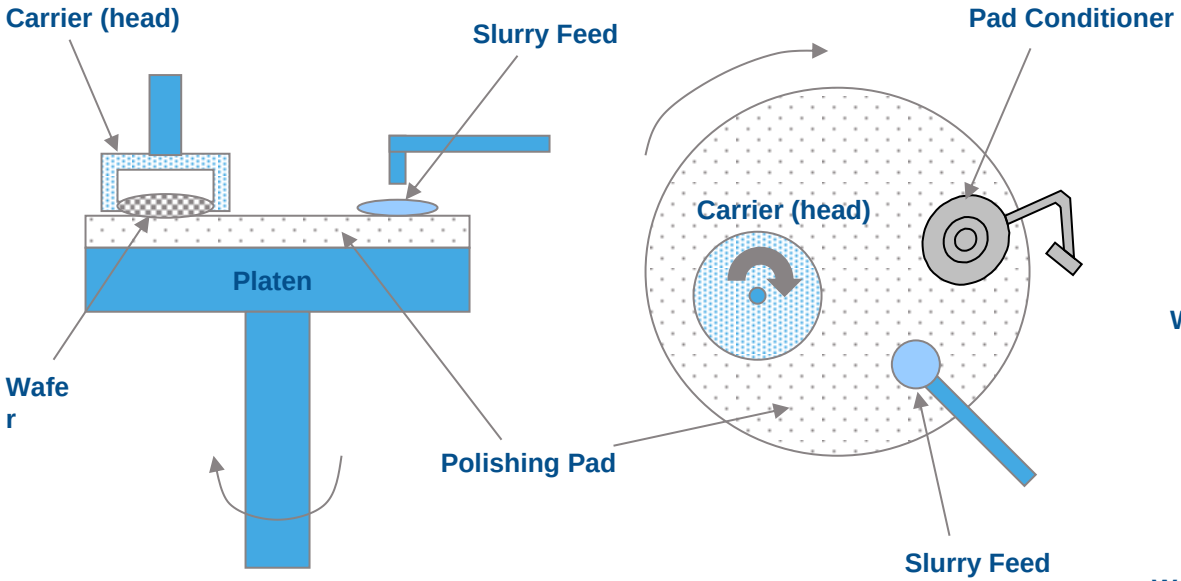
Summary

CMP = Chemical Mechanical Planarization

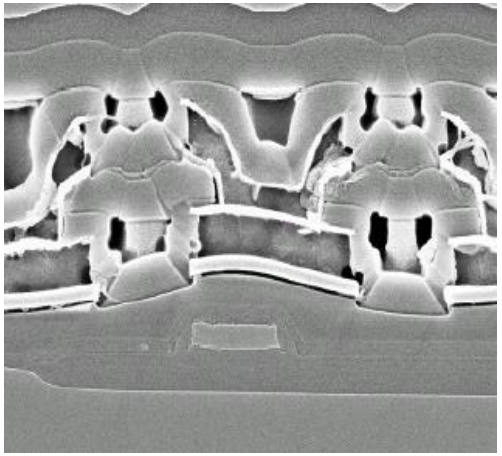
- Majority of equipment is based on rotational motion of pad and wafer (schematic representation below)
- Highest volume applications are oxide (ILD), tungsten and copper

(a) Side View

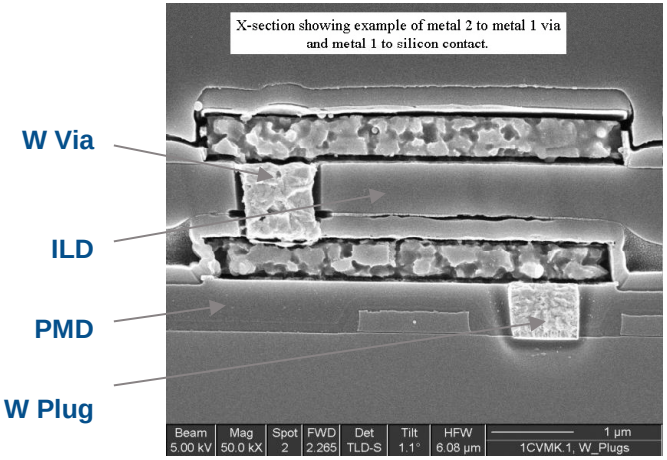
(b) Top View



No CMP – Traditional Device



4 Basic CMP Steps – Newer Device

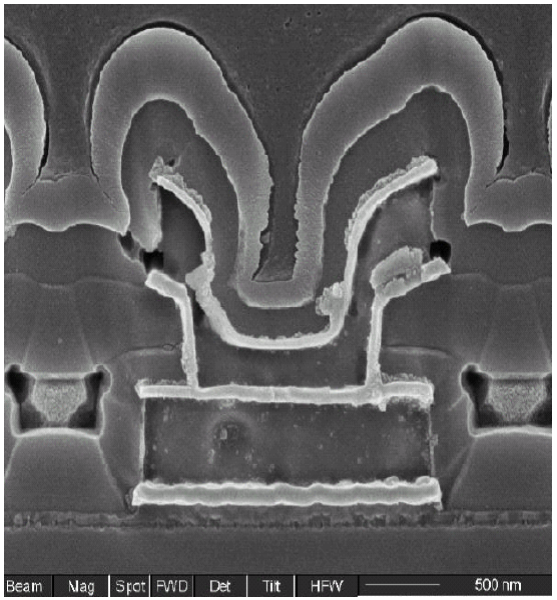


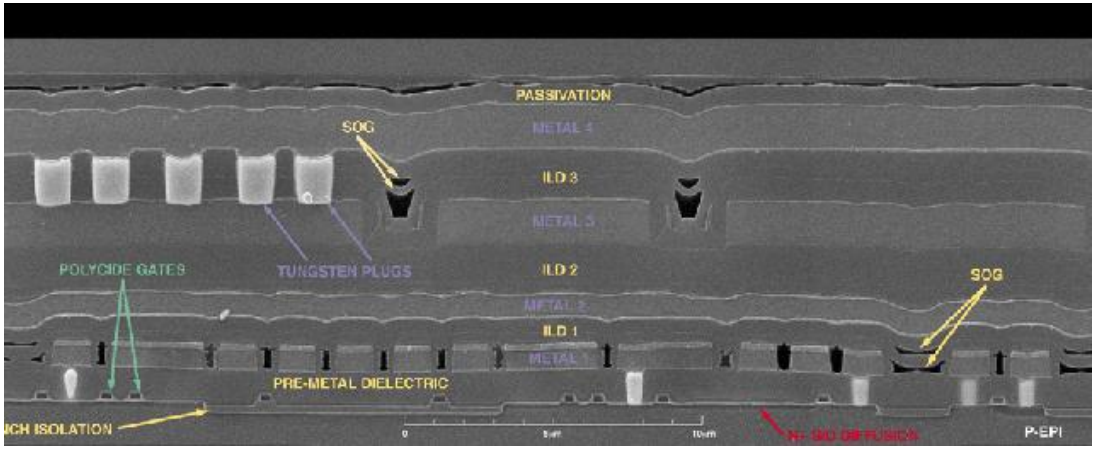
CMOS Life Before CMP

Topography at ILD levels (some severe)

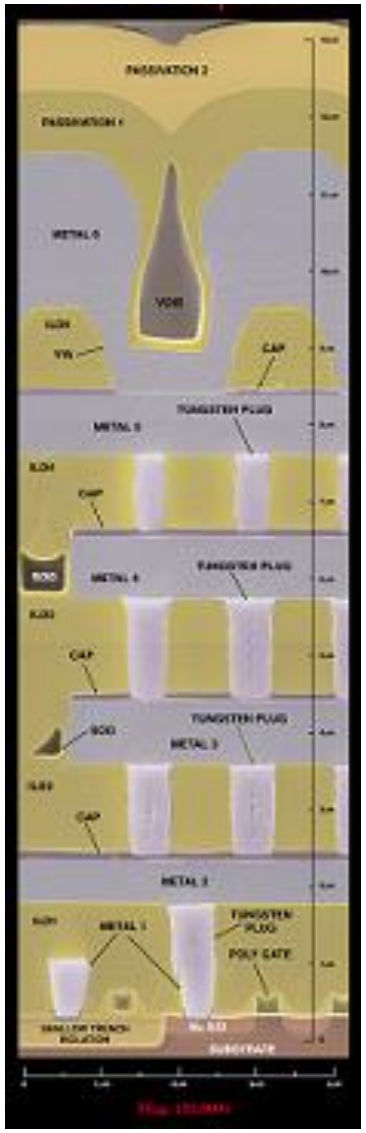
Sloped wall vias generally limited designers to only 2 or 3 levels of metal

Even for fabs that adopted tungsten plugs and SOG, stacked plugs were generally not allowed





CMOS Life After CMP



Topography under control

CMP enabled multiple levels of metal

Stacked plugs no longer an issue

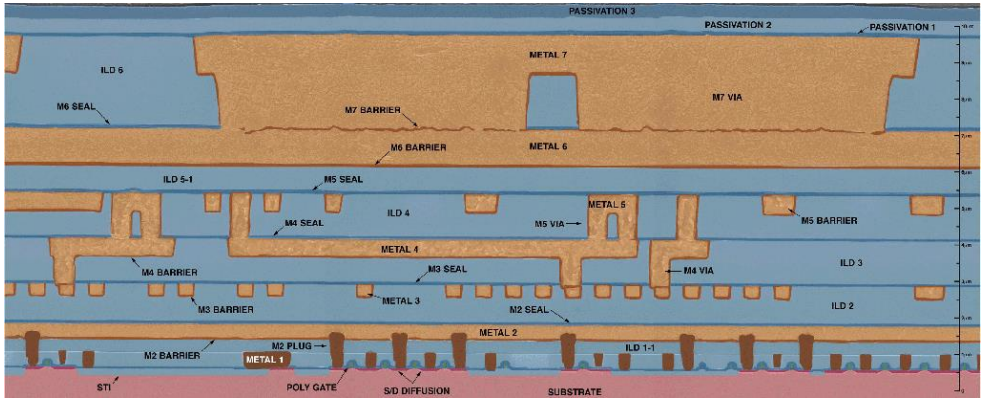
Shallow trench isolation widely adopted

Drove several generations of shrinks and more complicated stacks

However … this technology started to run out of steam for the most advanced CMOS devices

AMD K6 microprocessor (circa 1996)

Cu CMP



IBM PC603 microprocessor (circa 1998)

Dual damascene process integration for patterning Cu lines and vias

Primary process issues: Robust clear, defect density, dishing, erosion

Fastest growing CMP application for many years

New applications now starting to ramp into production

CMP Landscape

Process Applications:

1995 - Qty ≤ 2	2001 - Qty ≤ 5	2011 - Qty ≥ 40		
CMOS	CMOS	CMOS	New Apps	Substrate/Epi
Oxide	Oxide	Oxide	MEMS	GaAs & AlGaAs
Tungsten	Tungsten	Tungsten	Nanodevices	poly-AlN & GaN
	Cu (Ta barrier)	Cu (Ta barrier)	Direct Wafer Bond	InP & InGaP
	Shallow Trench	Shallow Trench	Noble Metals	CdTe & HgCdTe
	Polysilicon	Polysilicon	Through Si Vias	Ge & SiGe
		Low k	3D Packaging	SiC
		Capped Ultra Low k	Ultra Thin Wafers	Diamond & DLC
		Metal Gates	NiFe & NiFeCo	Si and SOI
		Gate Insulators	Al & Stainless	Lithium Niobate
		High k Dielectrics	Detector Arrays	Quartz & Glass
		Ir & Pt Electrodes	Polymers	Titanium
		Novel barrier metals	Magnetics	Sapphire
			Integrated Optics	entrepix

Intro to Example #1: Polymer CMP

The semiconductor industry is developing a range of advanced packaging technologies to help improve system performance. For some companies, this represents an alternative path to continued shrinks of 2D device architecture.

Design goals for many of these efforts include one or more of the following:

→ Improve signal routing flexibility
→ Reduce parasitic losses
→ Shrink final form factor of the system (particularly for mobile platforms)

One of the key technical challenges for advanced packaging is the ability to consistently form thru silicon vias (TSVs).

The goal of this particular project is to develop multi-layer interposers that include large Cu lines in stacked redistribution layers with large connecting vias. The project was led by Prof. Charles Ellis of Auburn University.

Dielectric Choice

Property	Measured Values		
	Polyimide HD2611	BCB	ALX 2010
Dielectric Constant	2.9 @ 1kHz	2.65 at 1-20 GHz	2.6 @ 1kHz-1GHz
Dissipation Factor	0.002	0.0008	0.003
Breakdown Voltage	> 2x 10^6 V/cm	5.3 x 10^6 V/cm	5.5 x 10^6 V/cm
Volume Resistivity	1 x 10^{16} Ω-cm	1 x 10^{19} Ω-cm	> 10^{16} Ω-cm
CTE	3 ppm/°C @ 25°C	42 ppm/°C @ 25°C	60 ppm/°C
Tensile Strength	350 MPa	87 ± 7 MPa	100 MPa
Tensile Modulus	8.5 GPa	2.9 ± 0.2 GPa	2.4 GPa
Elongation	100%	8 ± 2.5 %	30%
Residual Stress	2 MPa	28 ± 2 MPa at 25°C	32 MPa
Tg	360°C	> 350°C	230°C
Moisture Absorbtion	0.50%	< 0.2%	< 0.2%
Compatibility w/Copper	Poor	Good	Good
Metal Adhesion	Questionable	Good	Good
Cure Temperature	350°C	250°C	190°C

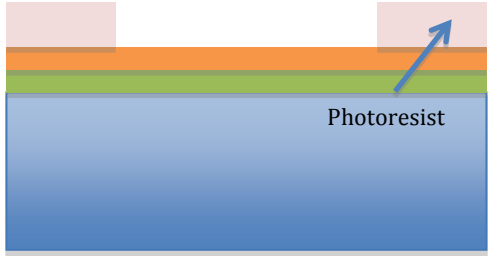
From 3 potentially viable alternatives, ALX2010 was chosen

Fabrication Sequence (part 1)

1. Grow oxide layer on bare Si

2. Deposit seed layer
(Ti / Cu / Ti)

3. Photolithography to define conductor plating areas

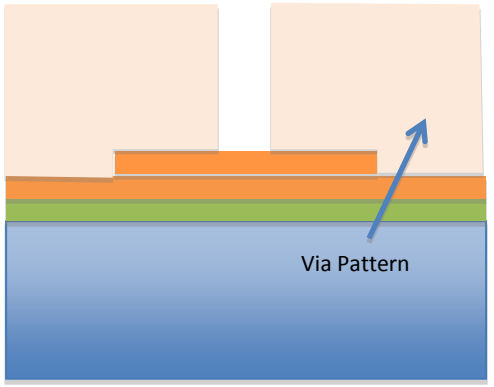


Courtesy of Auburn University

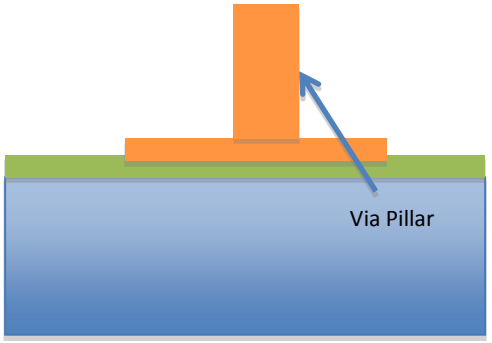
Fabrication Sequence (part 2)

4. Remove top Ti and plate conductors (3 um Cu)

5. Strip, recoat with thick resist, and pattern holes for via mold



6. Plate vias (13 um Cu), strip mold, and etch to remove seed layer.



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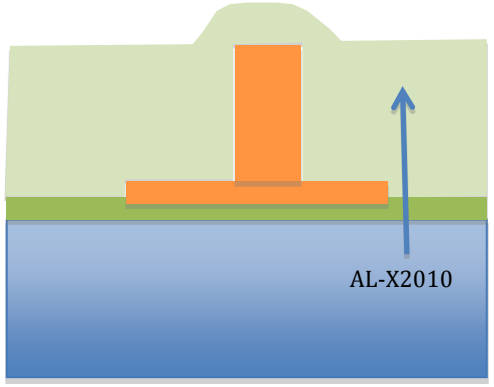
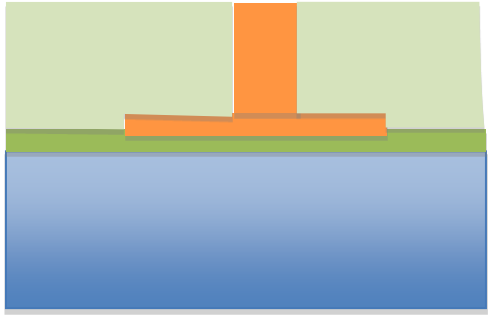
Fabrication Sequence (part 3)

7. Deposit ALX to a thickness slightly thicker (2-3 um) than via height



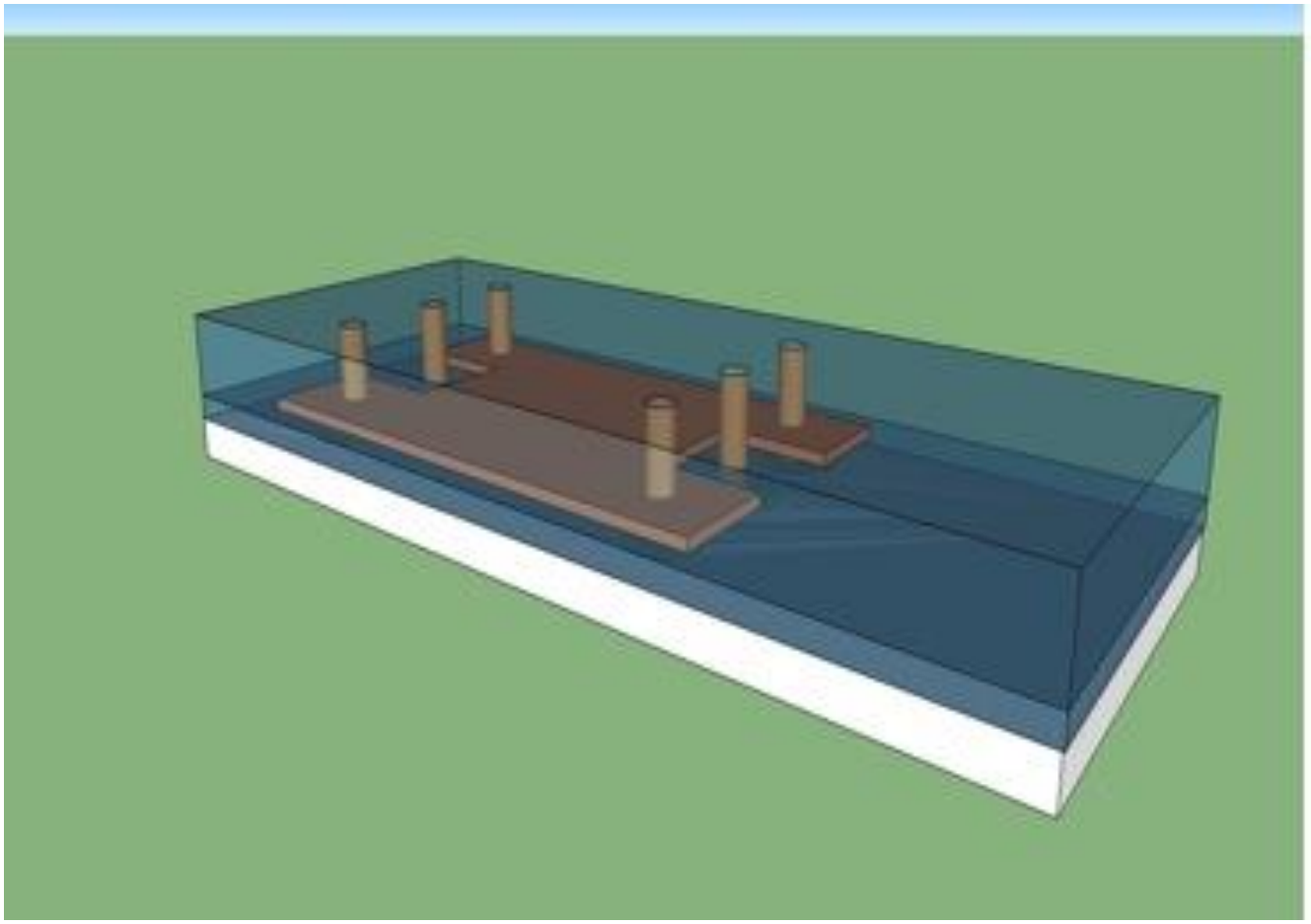
8. CMP to planarize ALX and expose tops of Cu vias



Courtesy of Auburn University

One Level Completed

Courtesy of Auburn University



First level conductor and vias completed.
Ready to repeat for next level.

SCREENING EXPERIMENTS

- Started with assortment of proven slurries used with other materials
- Same type of pad was used for all trials, but new pad installed for major changes in particle type
- Most slurries suffered one or both of 2 primary failure modes:

  1) low removal rate and/or

  2) severe scratching

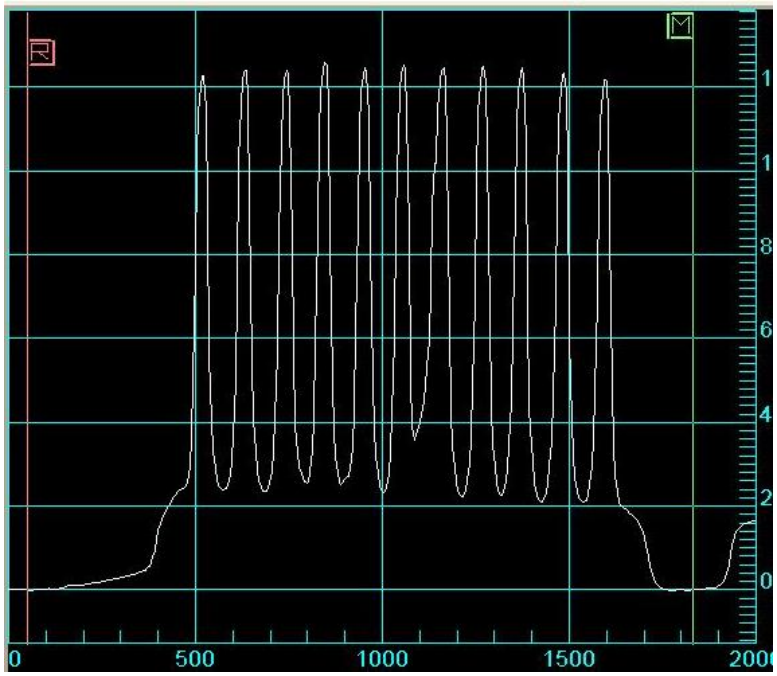
- Slurry with best performance on the ALX2010 in this test was a colloidal alumina
- Process summary at right →

CMP Process Summary	
Wafer size	100mm
Material	Polymer ALX2010
INPUTS	
Platform	IPEC 472 (later transferred to other platforms)
Primary Pad	IC1000 k-groove on SubaIV
Primary Slurry	colloidal alumina
Final Pad	Politex embossed
Final Slurry or Chemistry	None
Pad Conditioning	3M (4.25" standard)
Downforce	5 psi
Back Pressure	1 psi
Platen Speed	30 rpm
Carrier Speed	37 rpm
Slurry Flow	100 ml/min
CMP RESULTS	
Polymer Removal Rate	6000 - 7500 Ang/min
Planarization	Very good for this application Minimal dishing on Cu posts once exposed
Polymer surface finish	Excellent with no scratching
Cu surface finish	Good with no major scratching or pitting

Planarization Efficiency

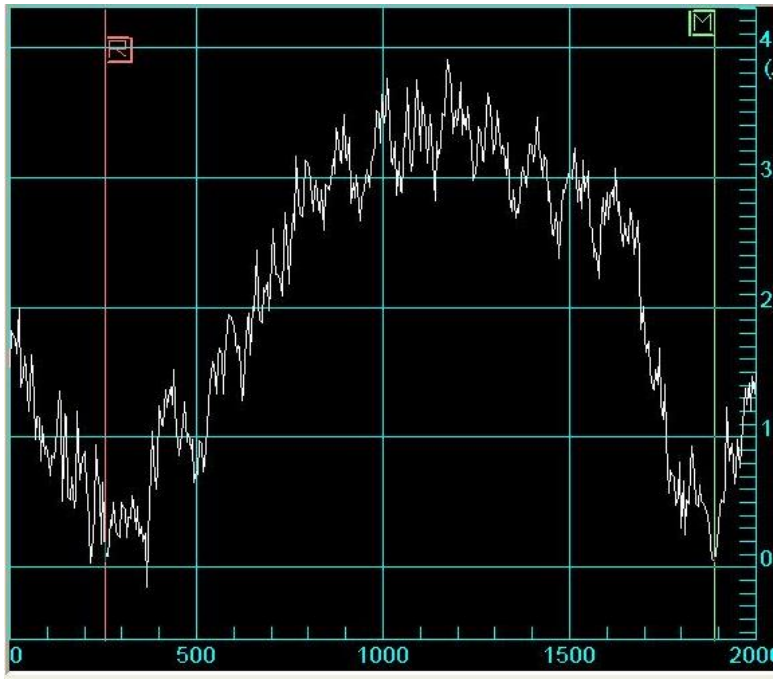
Pre-CMP

S.H. ~ 12.5 μm



Post-CMP

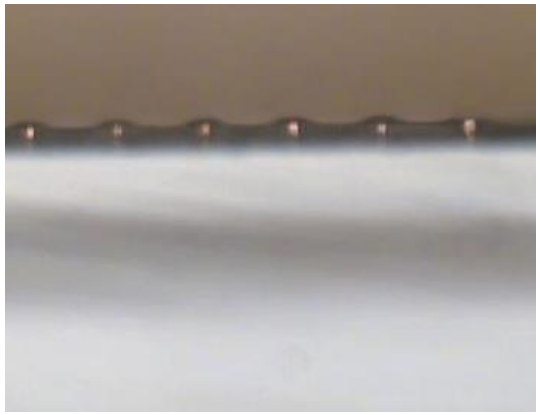
S.H. ~ 0.35 μm



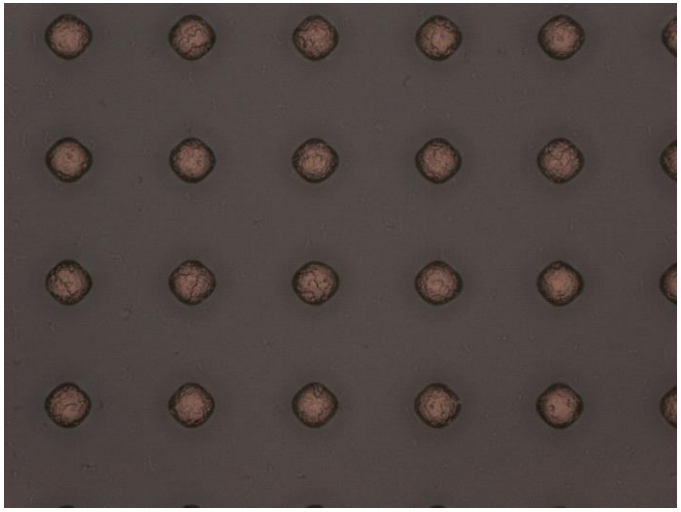
Planarization efficiency of roughly 97%

Images before/after CMP

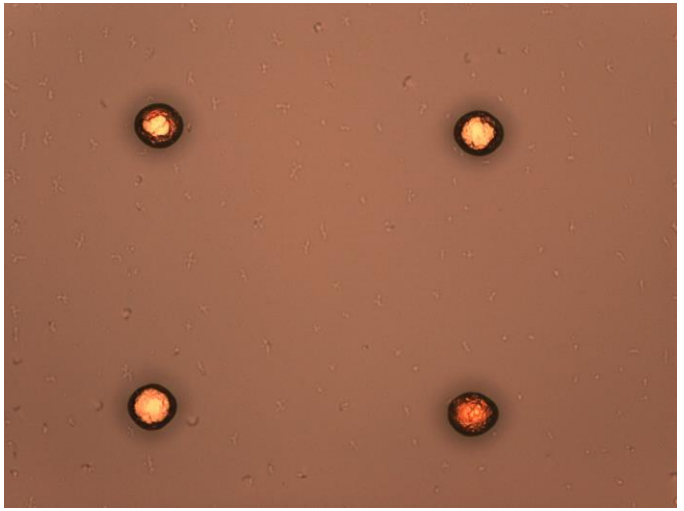
Cross section pre-CMP



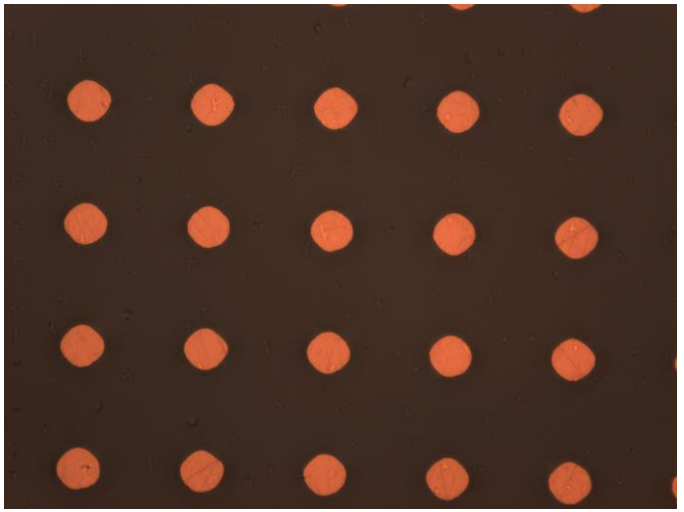
Top down view pre-CMP



Top down view at breakthrough

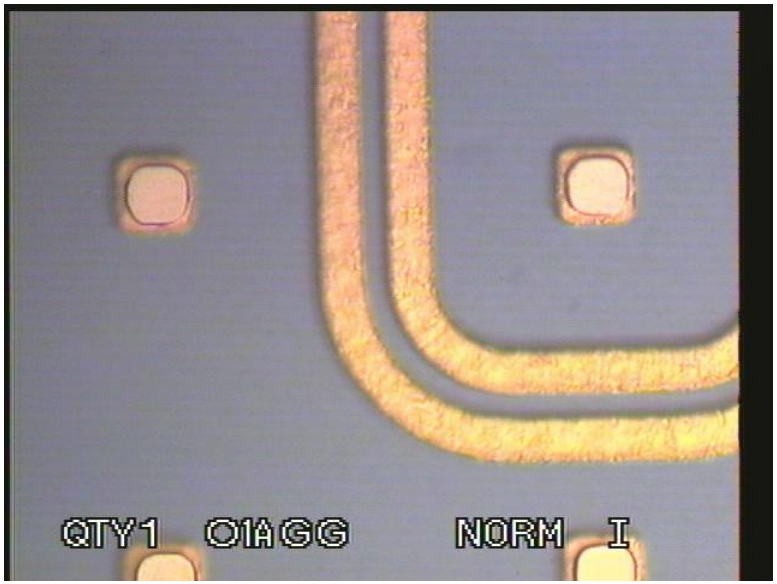


Top down view fully cleared



Top down view and xsection SEM

Buried conductor (thru polymer) and via posts with tops cleared after CMP →



←Cross section SEM of finished interposer with 3 levels of metal.

Courtesy of Auburn University

Advantages of Chosen Process Flow

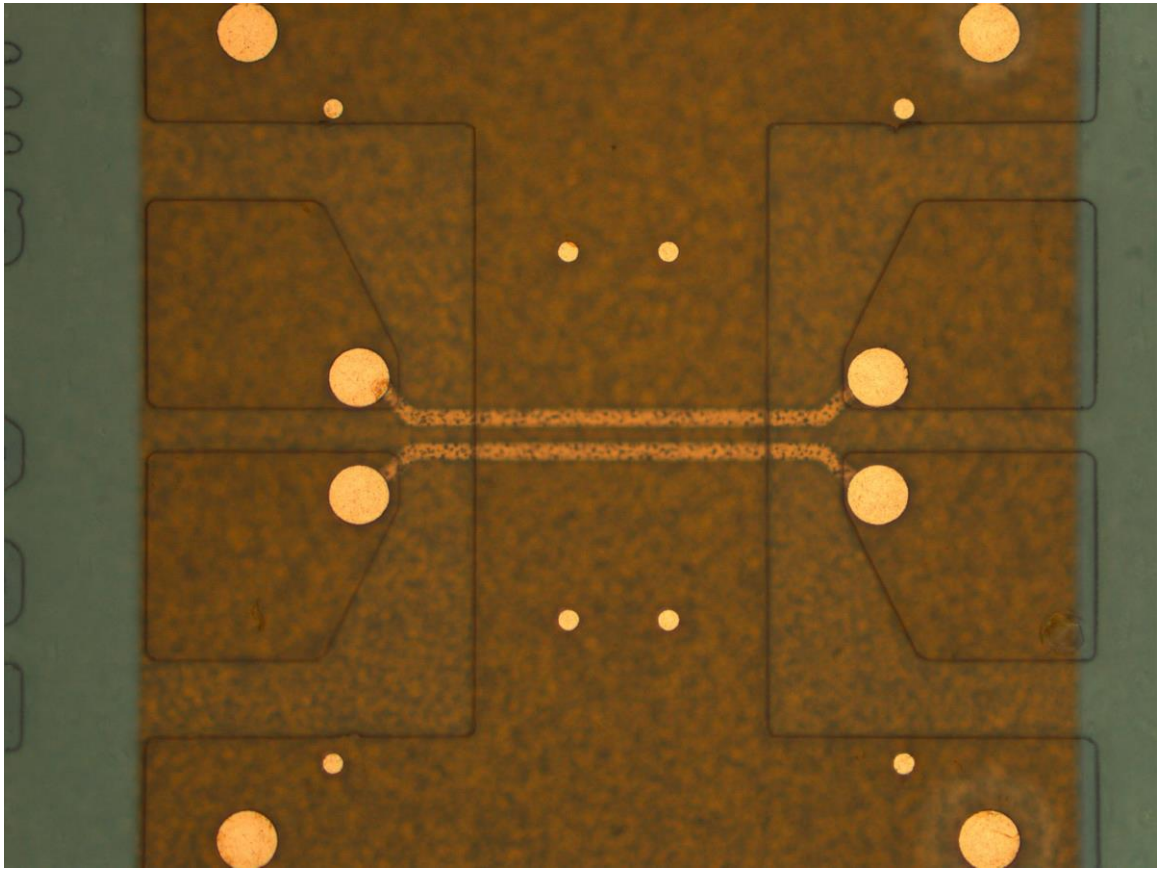
Filled (solid) Cu vias which have low resistance and are large enough to carry substantial current

No need to pattern dielectric
(can utilize any dielectric that can be polished)

High aspect ratio capability – depends on photoresist aspect ratio

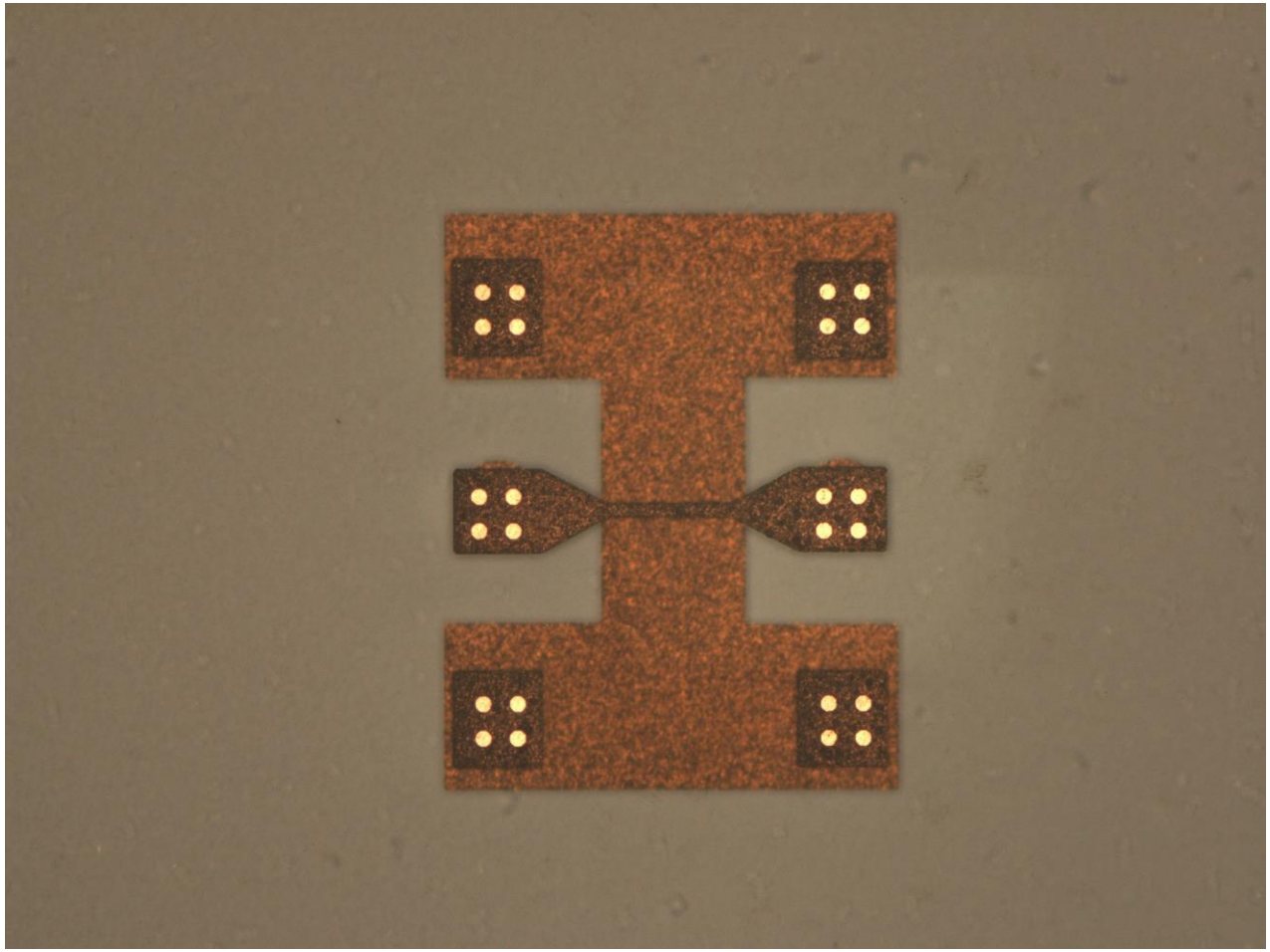
Very good planarization – easy to add multiple signal layers

Device pic #1



Courtesy of Auburn University

Device pic #2



Courtesy of Auburn University

Intro to Example #2: SiGe Transfer Layer

SiGe transferred from a donor substrate to an oxide layer on a Si wafer (similar to Smart-Cut SOI technique). Surface of SiGe after splitting is slightly rougher than desired.

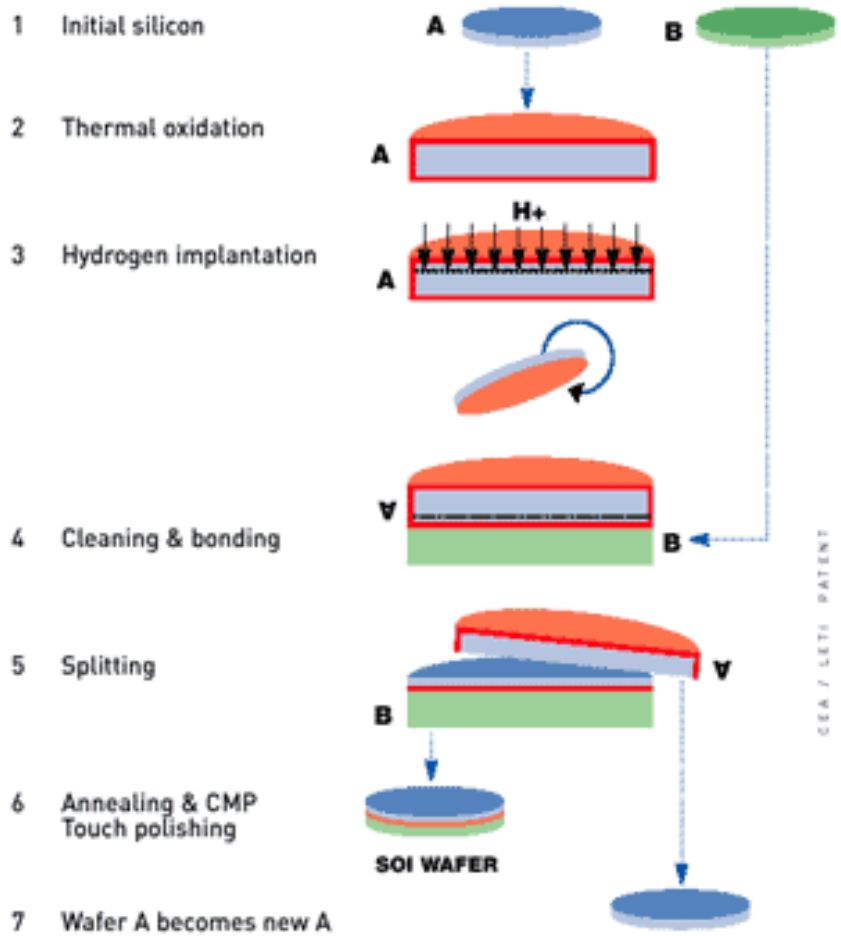
Process targets:

→ Reduce roughness of transferred SiGe layer to less than 5 Ang
→ Minimize amount of material removed to achieve above
→ Minimize all sources of added thickness variation

Most previous SiGe polishing processes removed too much material, or induced too much thickness variation, even when used for relatively short polish times. Success for this project required that a customized process be developed.

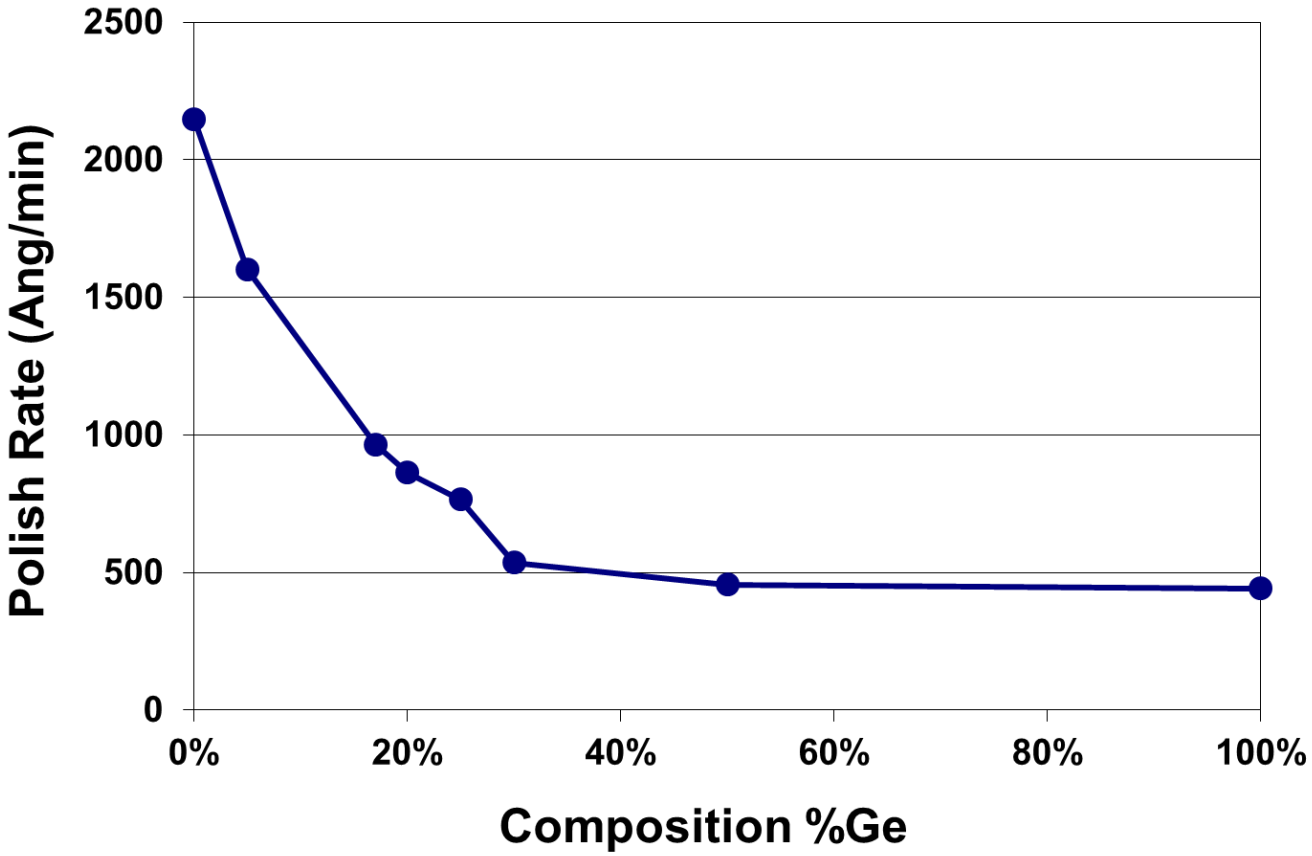
SOI Smart-Cut Flow

- Developed at CEA-Leti
- Six key steps
  - Oxidation
  - Hydrogen implantation
  - Direct wafer bonding
  - Splitting
  - Annealing
  - Touch or “Kiss” polishing
- Very flexible for thickness of buried oxide & top Si layers
- H+ damage relatively easy to anneal



Source: “SOI Technology” by Vishwas Jaju, 2004

SiGe Polish Rate vs Composition

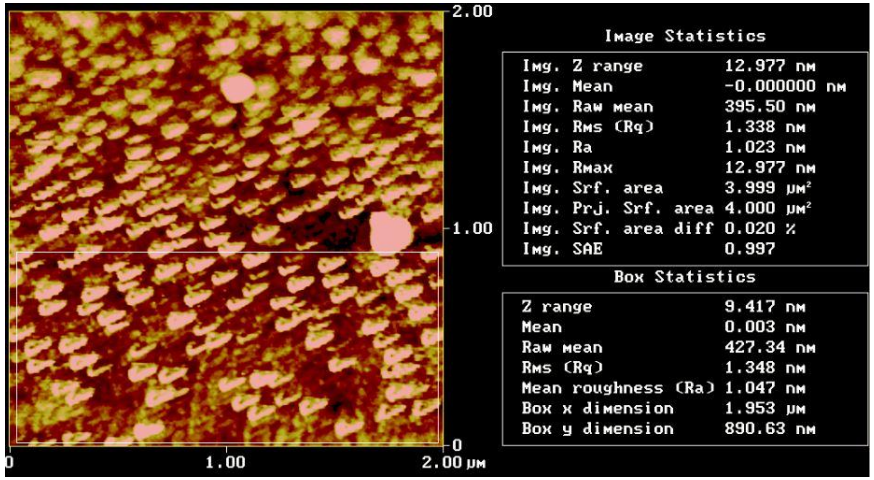


SiGe polish rate is a strong non-linear function of composition below 30% Ge.

This project was focused around 50% Ge layers, so rate was insensitive to small changes in composition.

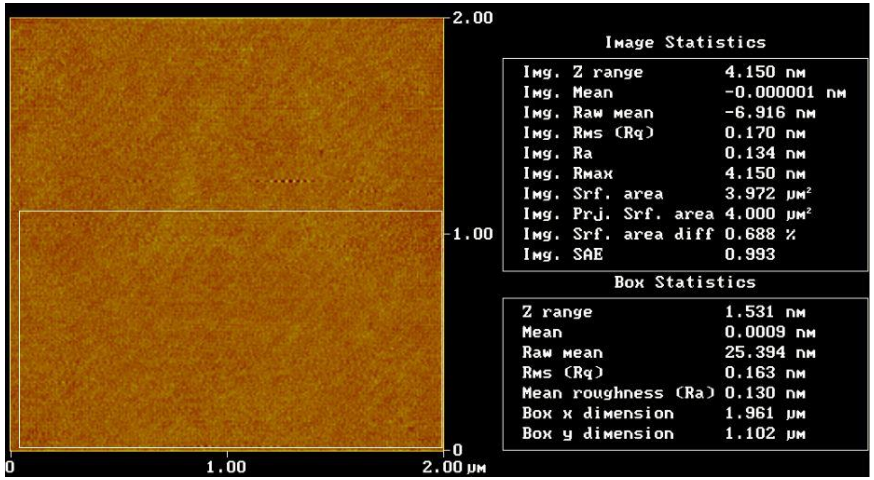
SiGe Transfer Layer

SiGe Layer Pre-CMP (after transfer)



RMS Roughness
13.5 Ang

SiGe Layer Post-CMP (device-ready)



RMS Roughness
1.6 Ang

Images courtesy of anonymous customer

The above result was achieved using a gentle CMP process with silica slurry and mild chemistry to only remove about 500-700 Ang of SiGe material.

Intro to Example #3: Oxide nanostructures

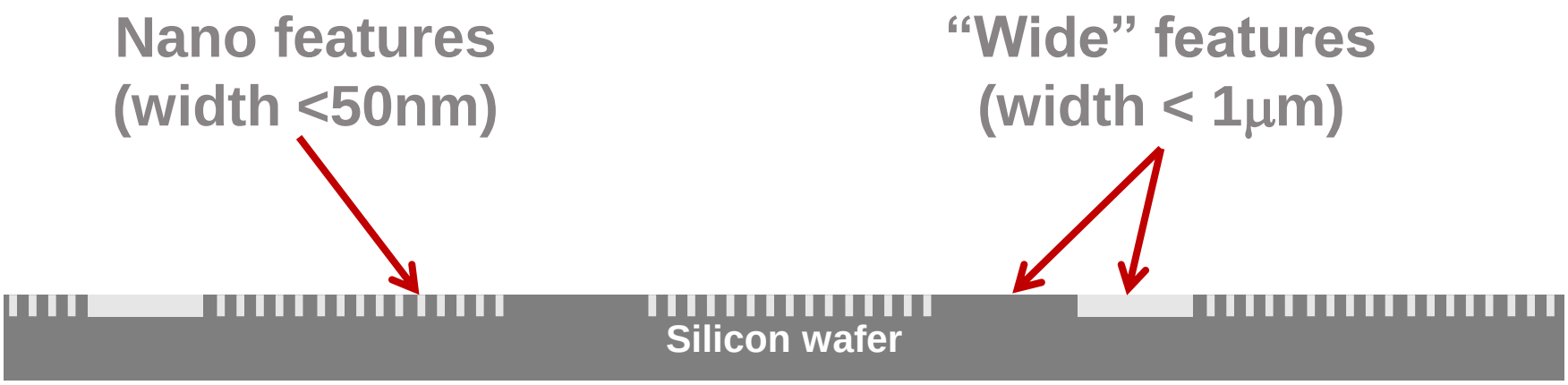
This project involves extremely repetitive inlaid nanostructures. After etching, recessed features of ~100nm depth are filled with densified CVD oxide then planarized using CMP.

Process targets:

→ Clear oxide over field areas as uniformly as possible
→ Minimize Si loss after breakthrough
→ Minimize topography after CMP to <1 nm if possible

CMP process approach:
- High selectivity STI slurry (ceria based)
- Standard planarizing pad
- Gentle conditioning
- Non-aggressive polishing recipe (about 2.5-3 psi and 70-90 rpm)

Inlaid Oxide Nanostructures



Courtesy of anonymous customer

Initial trench depth is 50-100 nm.

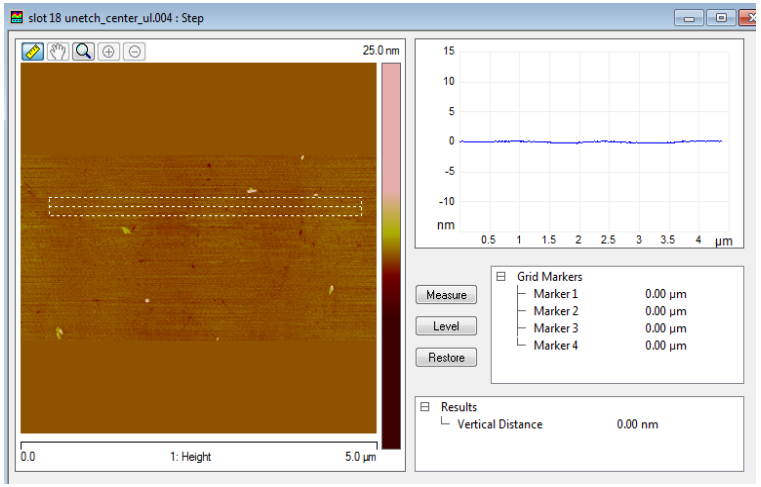
The desired final structure is isolated TEOS oxide filling the trenches with final surface topography <1nm.

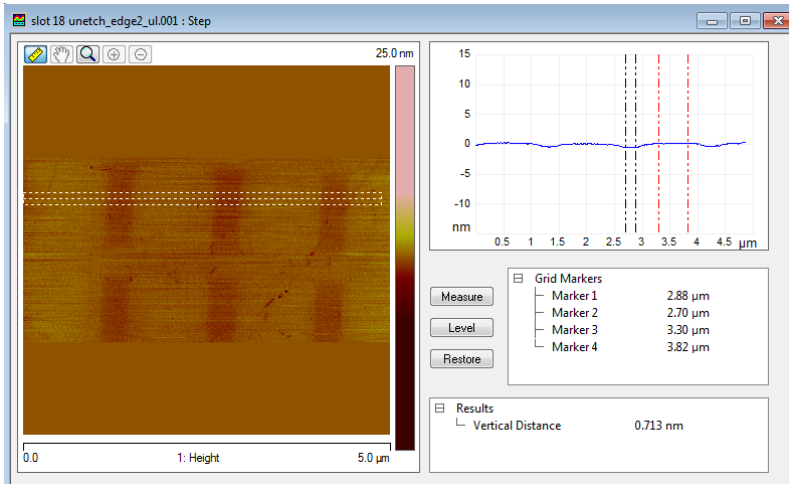
Post-CMP Topography <1nm

Wafer Center

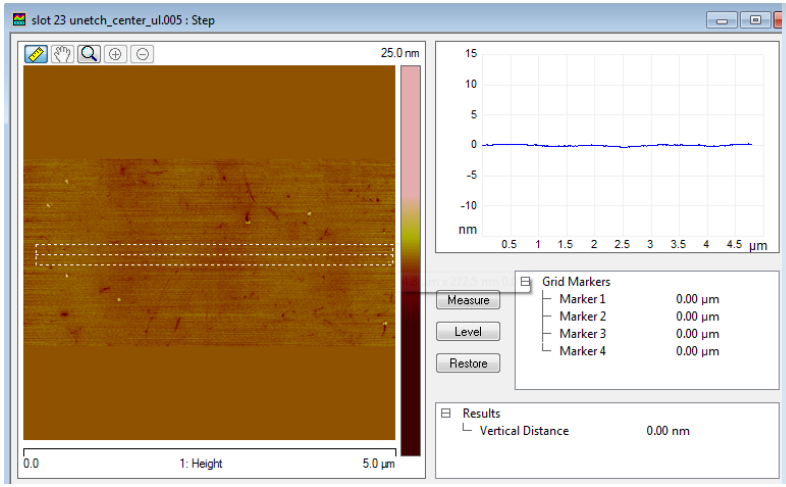
Wafer Edge

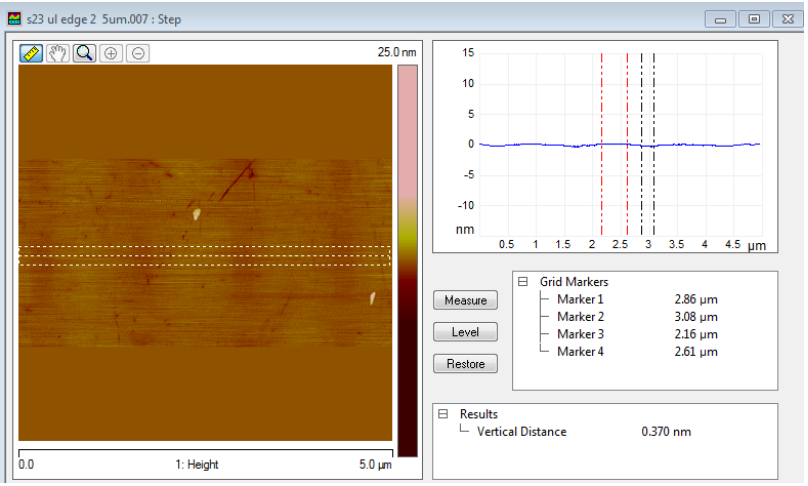
Slot 18:
105S POLISH





Slot 23:
120S POLISH



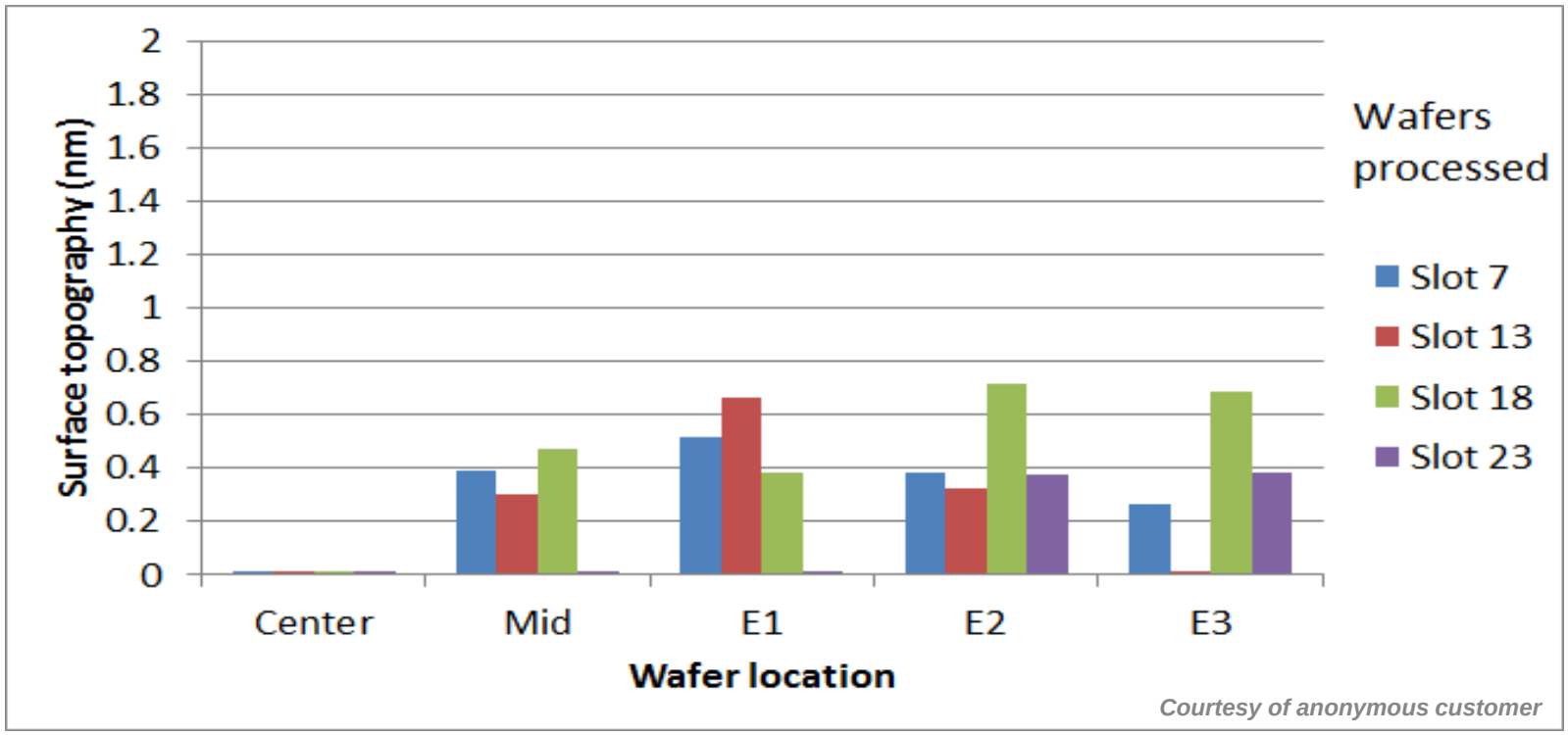


Images courtesy of anonymous customer

Topography Summary

CMP process was evaluated over a range of features

- Slots 7 and 13 were overpolished
- Slots 18 and 23 were polished to nominal target

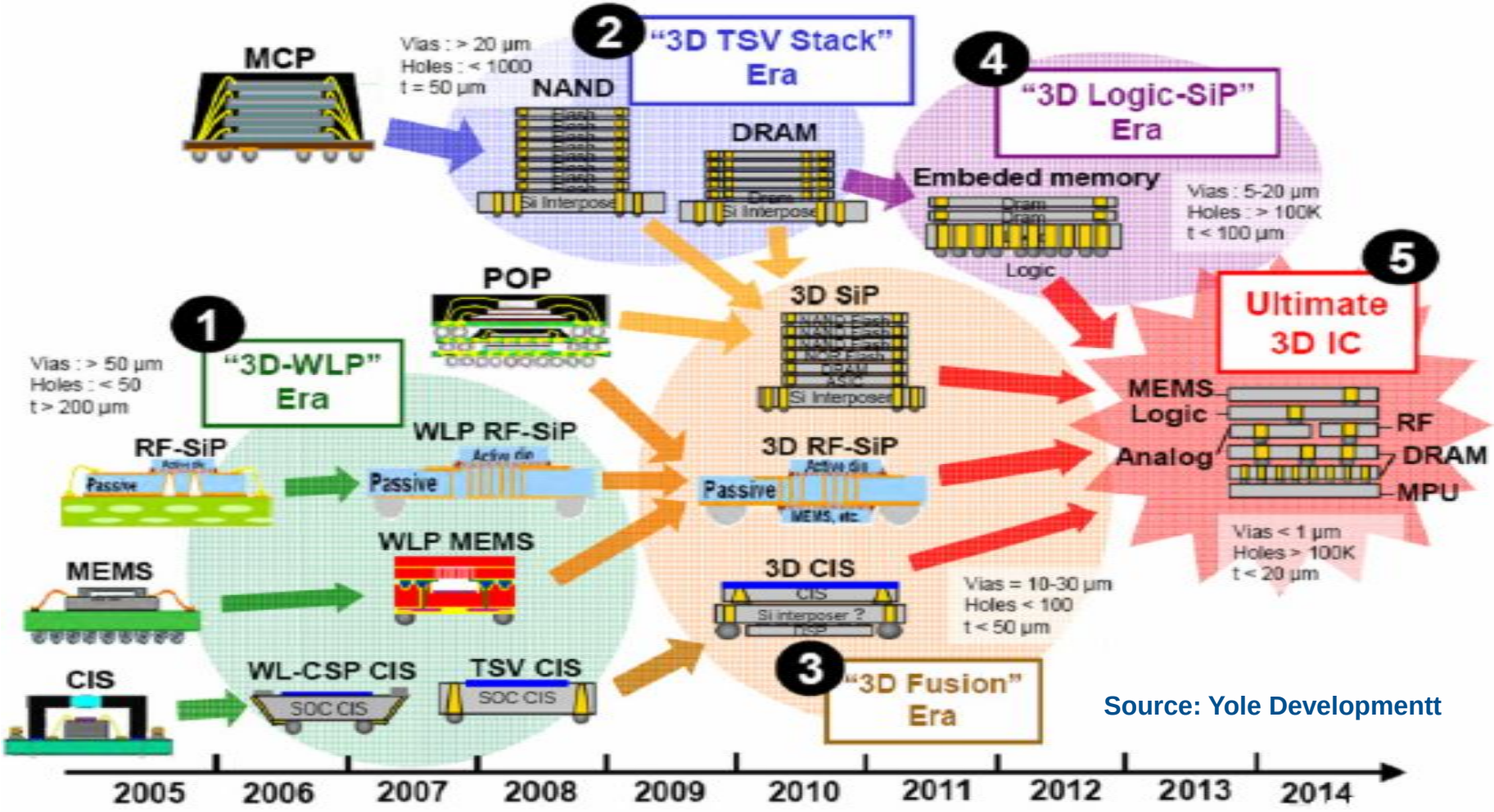


All sites measured well below target topography of <1nm

TSV Background

- Two-dimensional device scaling is increasingly difficult and fast approaching fundamental limits of physics (or balance sheets).
- 3D integration also faces substantial process and design issues, but various approaches are now gaining traction.
- Timing for mainstream adoption of 3D is now. Several products are already in the market and more are being launched.
- One of the key technologies to enable 3D structures is TSV's.

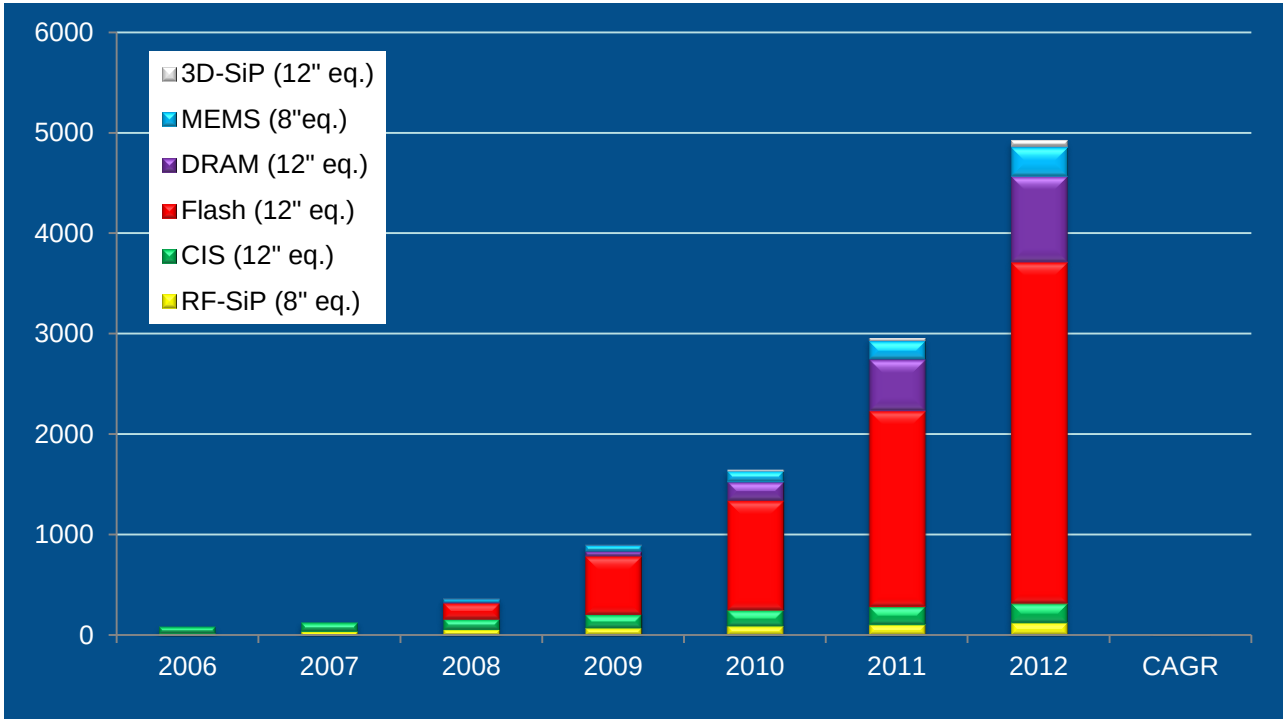
3D Packaging Apps



Source: Yole Developmentt

Source: Yole Development

- Growth rates for 3D integration
- Flash continues to drive the market
- DRAM leading new growth



Units (000)	2006	2007	2008	2009	2010	2011	2012	CAGR
RF-SiP (8" eq.)	19.77	37.58	54.38	71.19	88	104.81	121.62	35.4%
CIS (12" eq.)	68.06	92.63	106.53	136.15	164.45	182.13	194.92	19.2%
Flash (12" eq.)	0	0	164.94	583.73	1087.35	1946.4	3391.65	112.9%
DRAM (12" eq.)	0	0	6.04	46.01	189.44	513.34	857.07	245.2%
MEMS (8"eq.)	0	4.56	31.19	61.41	108.98	184.87	291.72	129.8%
3D-SiP (12" eq.)	0	0	0.42	3.02	10.63	28.16	64.26	251.3%

Role of CMP

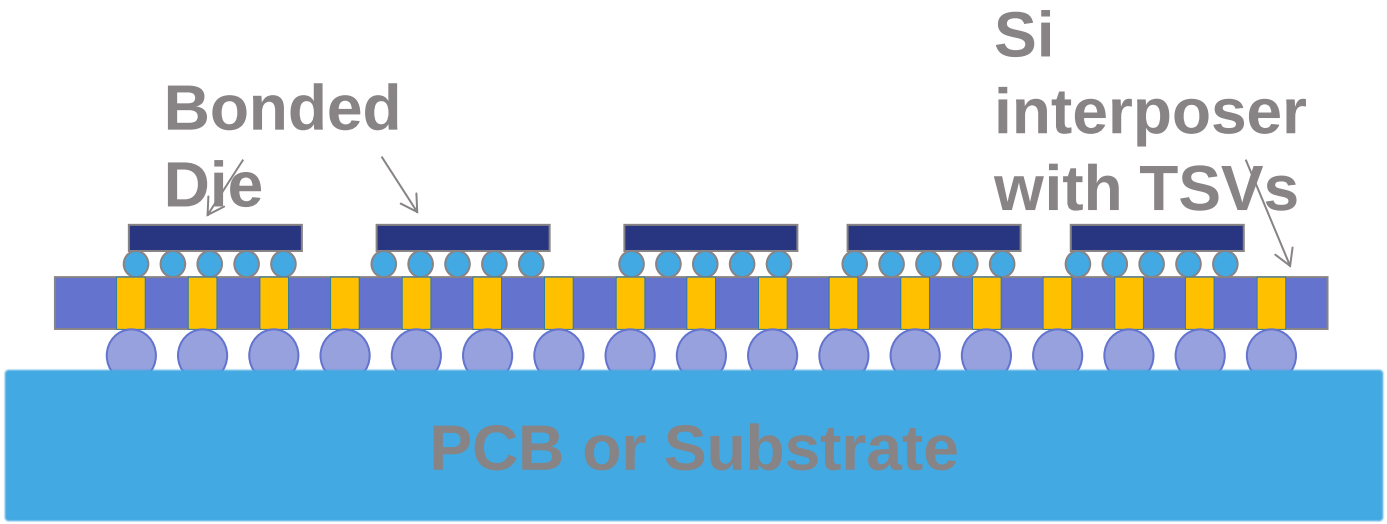
CMP is used in a damascene architecture to help form the via after the conductor deposition from one side.

TSV's can be filled with any of several conductive materials.

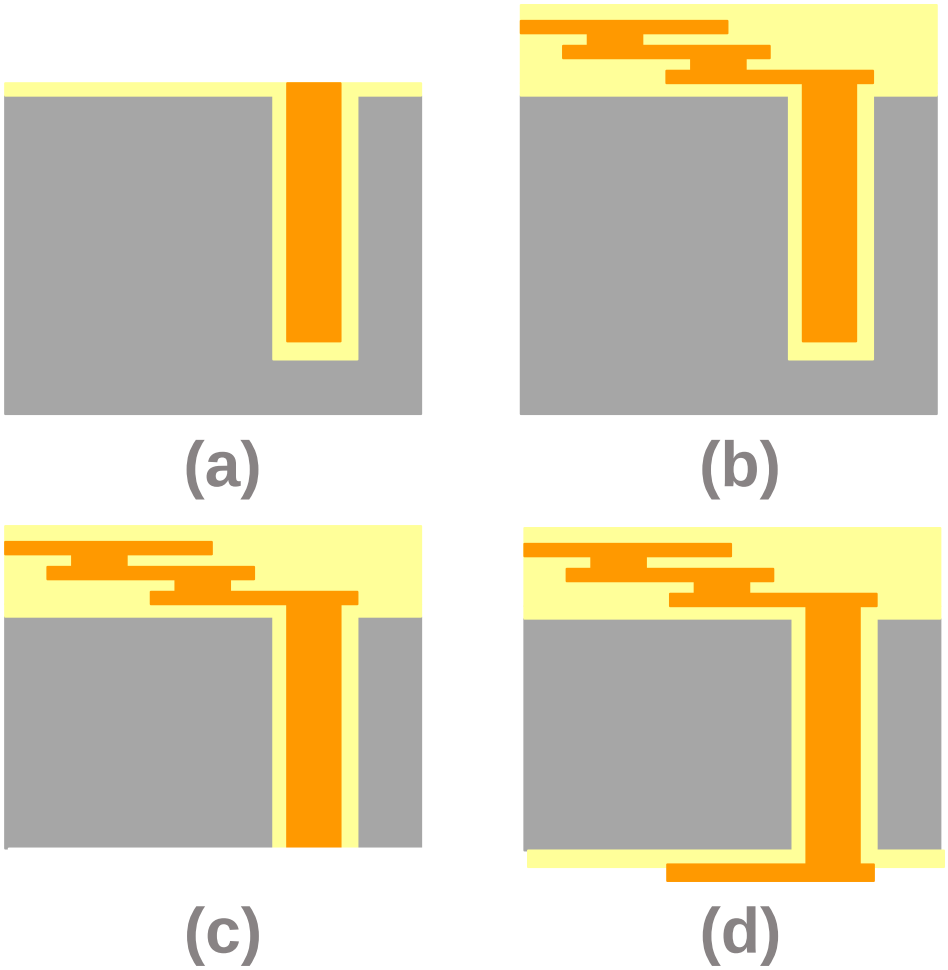
- Most common options are copper and polysilicon.
- Final choice depends on dimensions, operating voltage and current, frequency, plus other integration factors.

Layer thicknesses can be several microns (or more).

Topography requirements are generally much less demanding than CMOS



Source: RTI

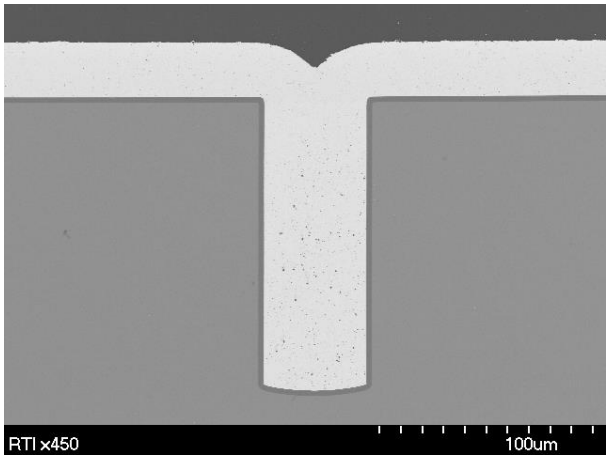


Process flow for Si interposer with TSVs: (a) TSV etch, insulation, plating, and CMP, (b) Frontside multi-level metallization, (c) Wafer thinning and TSV reveal, (d) Backside metallization.

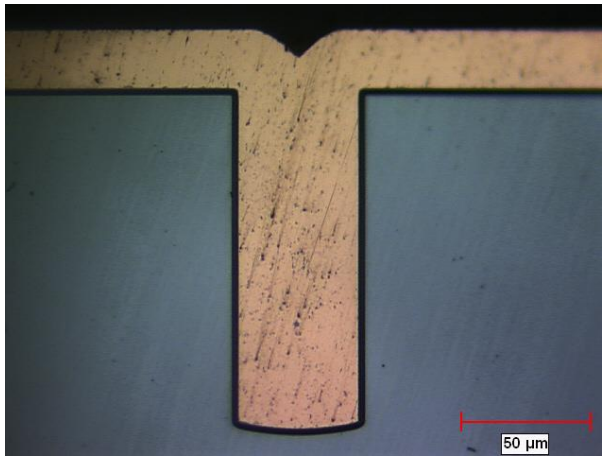
TSV Example 1: Front side Cu

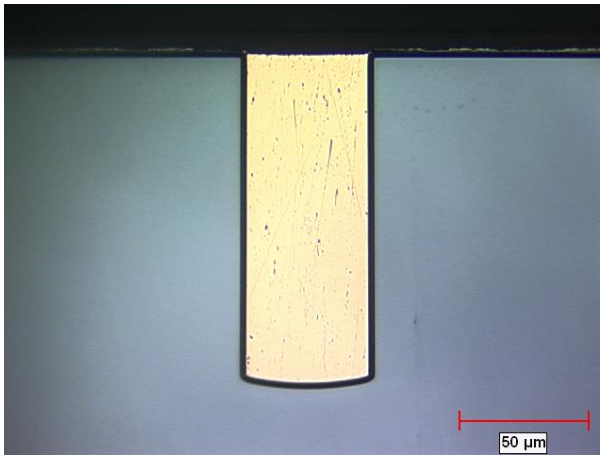
Representative Images of RTI TSVs for Si interposer applications showing large vias with thick Cu overburden

- TSVs shown are 50um diameter with 25um overburden.
- High rate Cu slurry was used to remove front-side overburden



TSVs and overburden, Pre-CMP



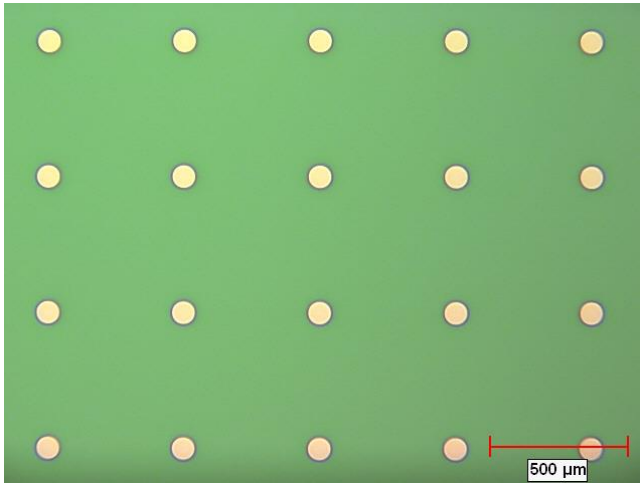


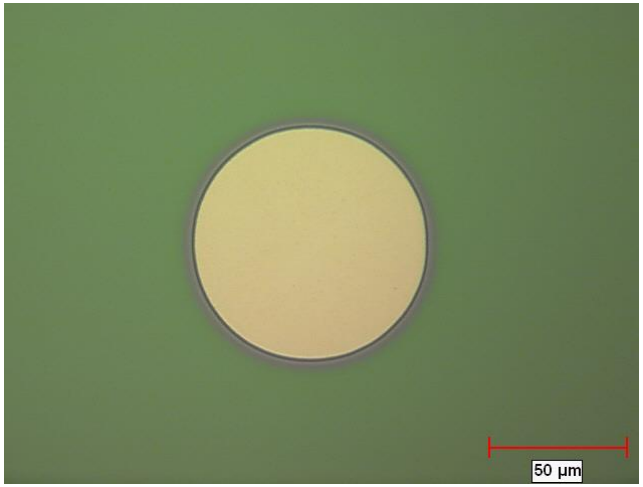
Post CMP (typical dishing ~0.5-1um)

High rate Cu CMP process using an AGC slurry

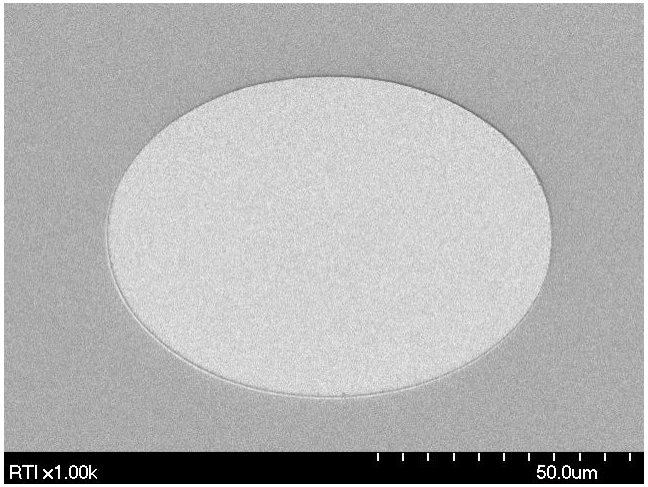
- Cu removal rates of >4 µm/min achieved
- Cu polishing times of reduced by 60-70% compared to standard CMOS-compatible Cu slurries
- Dishing ≤0.25um measured on multiple wafers (50 to 80um TSV diameter) even with up to 5 min overpolish
- Good surface finish on all exposed materials

Front side of TSVs





Optical Images post CMP- Cu TSVs polished to oxide / nitride

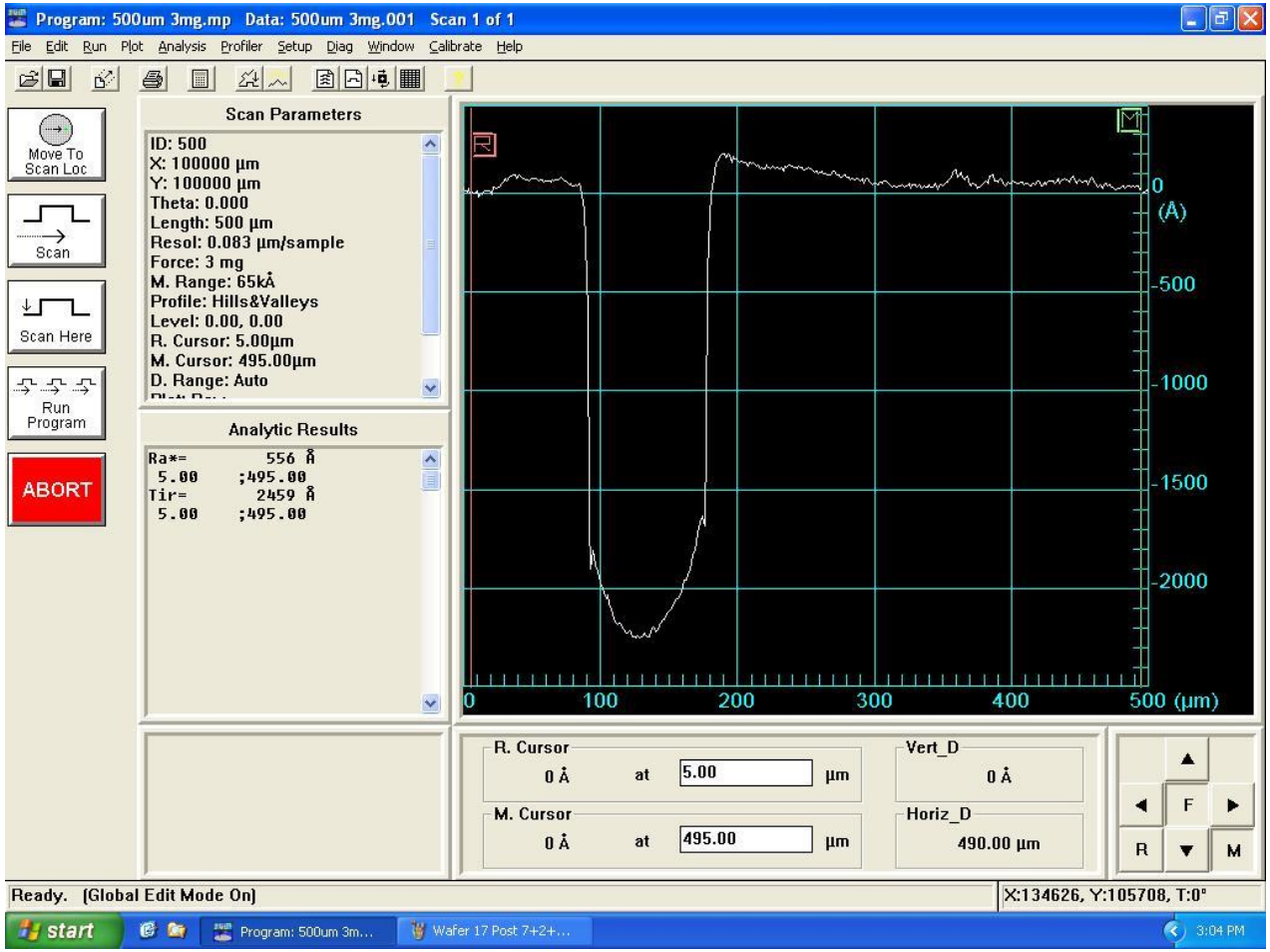


Top down SEM post CMP

Some wafers were plated with as much as 43 um of Cu overburden

Images courtesy of RTI International

Dishing on large TSV



Dektak Image of polished Cu TSV- dishing

Typical dishing across 80um TSV diameter was <250 nm

After completion of device layers on front side of wafer …

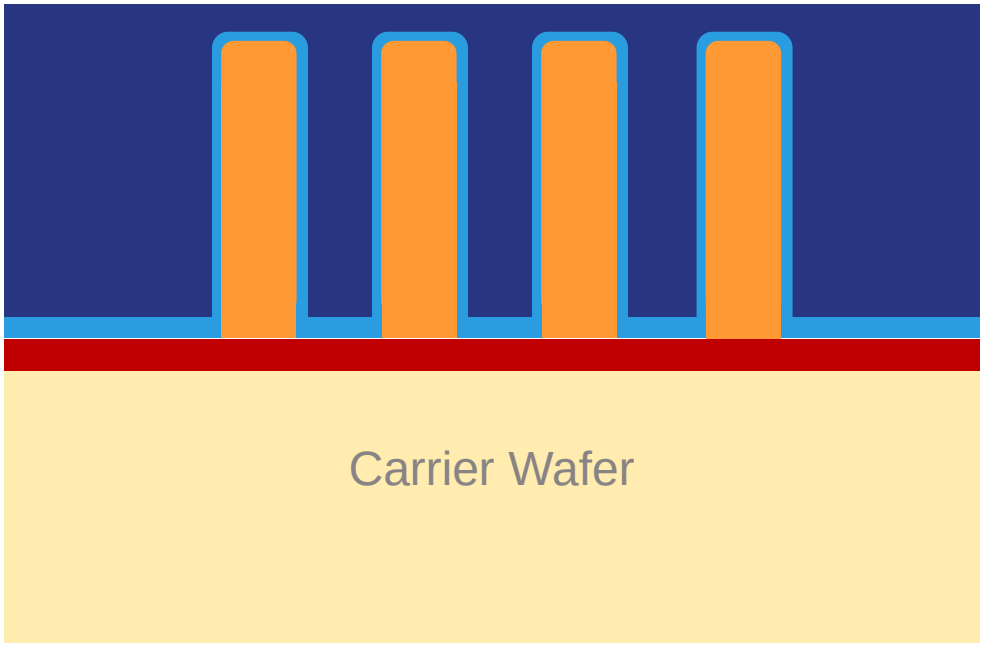
- TSV must be exposed to make contact and/or continue patterning next layers (RDL) from wafer backside.

- Various integrations are being pursued with combinations of backgrind, etch, selective CMP, or non-selective CMP.
  - Some approaches require 2 or 3 steps of CMP to achieve desired result

- CMP requirements are strongly dependent on the integration path and the final tolerance of the exposed vias for dishing, roughness, etc..

Example 2: Reveal High rate Si and Cu

Backgrind stops before reveal



Carrier Mount

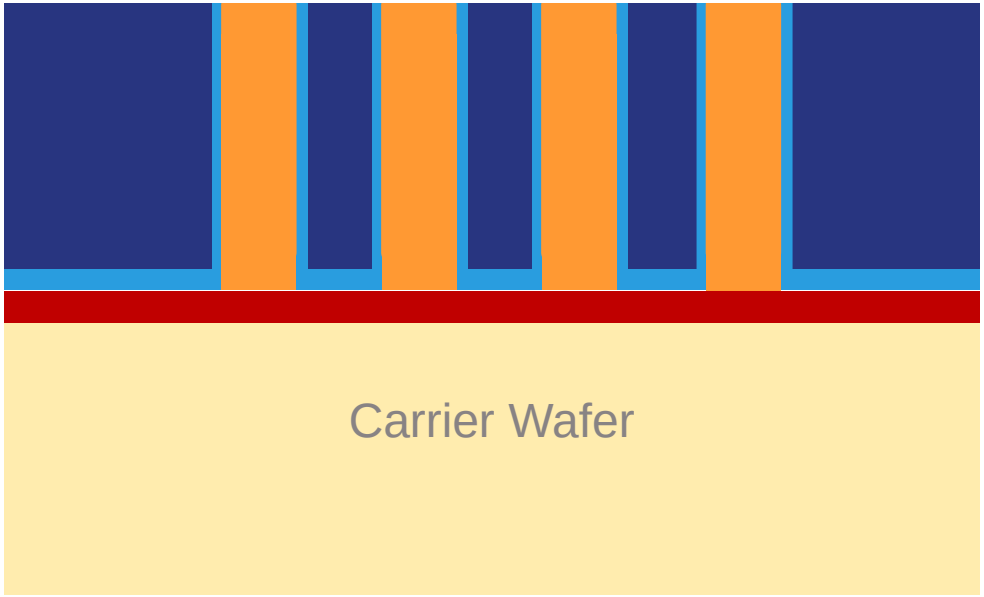
- TSV wafers mounted face down on carrier wafers

Backgrind

- TSV wafers thinned using backgrind to approx 5-15um “below” TSVs
- Reveal CMP performs dual function of removing grind damage layer and exposing center conductor of TSV’s

After CMP

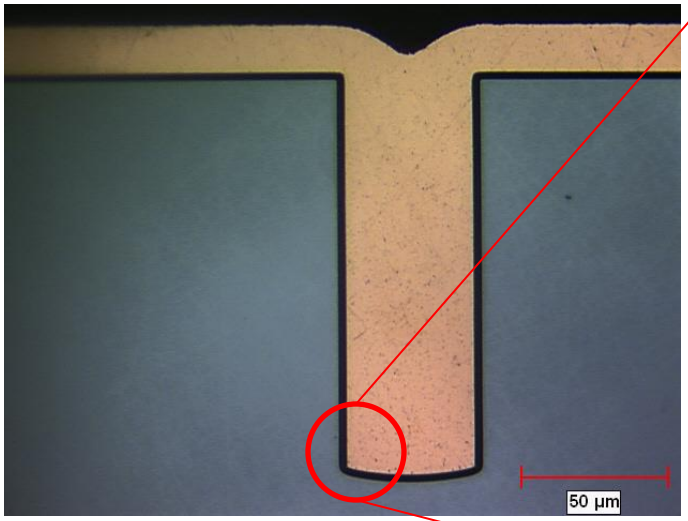
CMP to Expose & Planarize TSVs

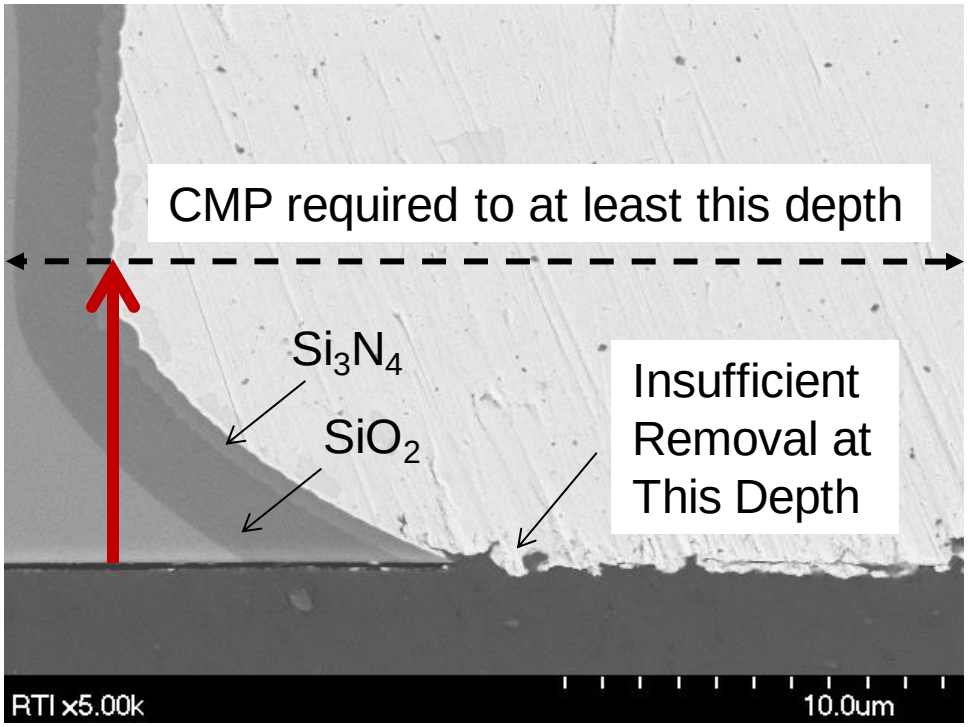


Three primary materials

- Single crystal silicon
- Oxide (optional thin nitride)
- Copper

Need to polish far enough into TSVs to remove rounded profile at base of vias





Images courtesy of RTI International

TSV Reveal Process Goals

High Si rate

Low selectivity

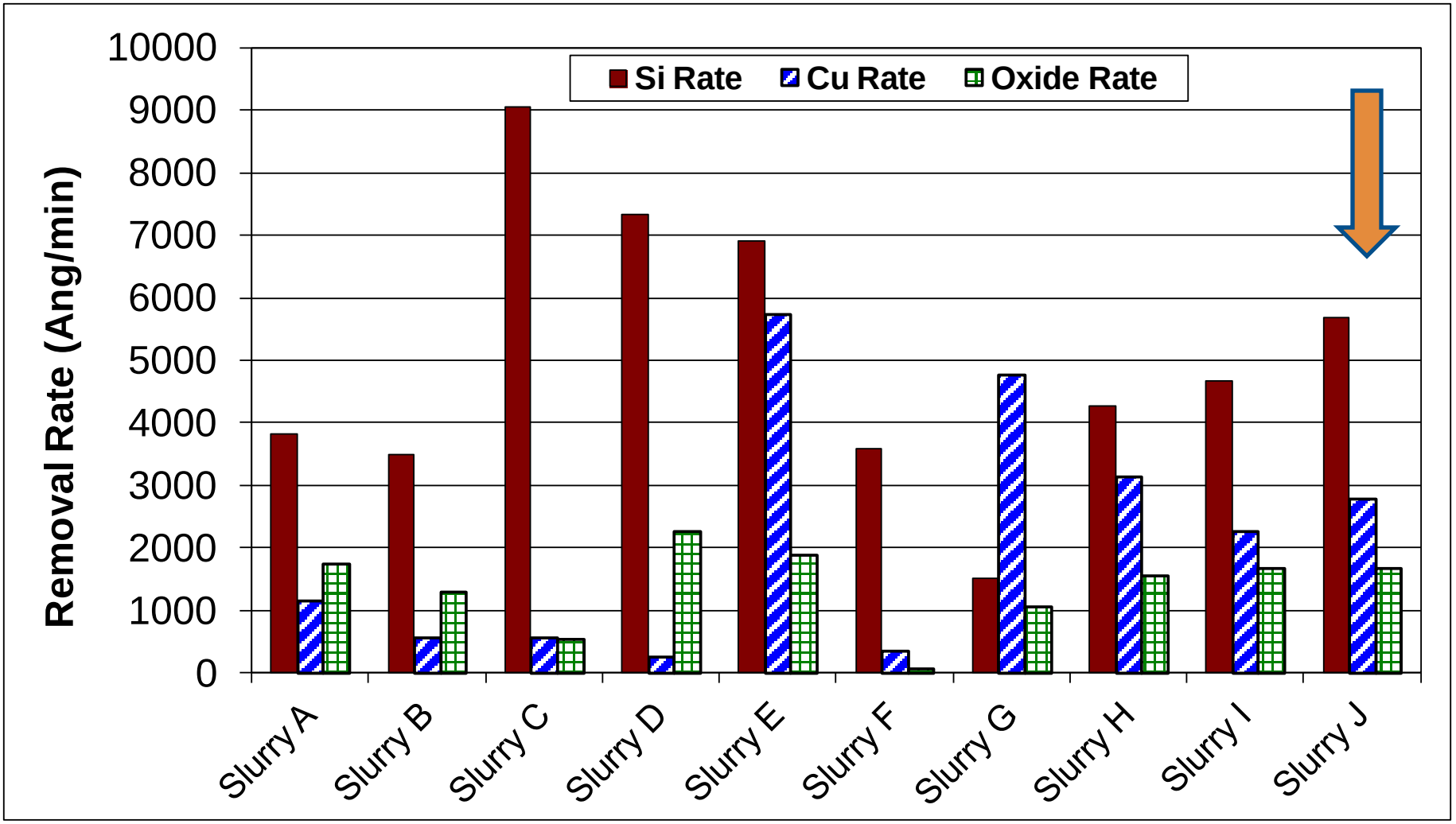
- **Reasonably matched Cu and Tox rates**
- **Minimize dishing on wide structures after reveal**

Good surface quality

- **Low roughness on both Si and Cu**
- **No scratching**
- **No as stringent as CMOS metallization**

Screening tests used same process settings used for all slurries

CMP Slurry Screening



CMP Process

Slurry J was chosen for patterned wafers

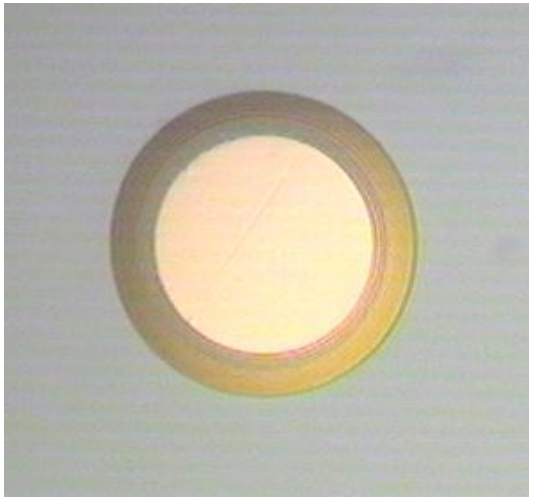
Re-optimized process for higher Si rate

- Target 1 um/min → Achieved 1.05 um/min

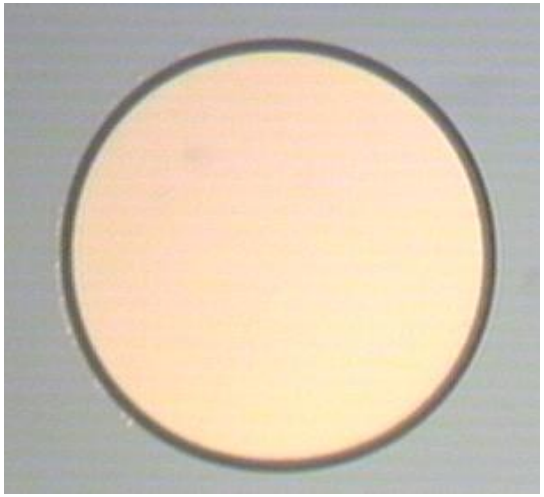
Iterative polish on first wafer

- Total amount to be removed estimated at 30 um
- Polished in 5 minute increments
- Inspection clearly showed breakthrough
- Final surface topography <250 nm achieved

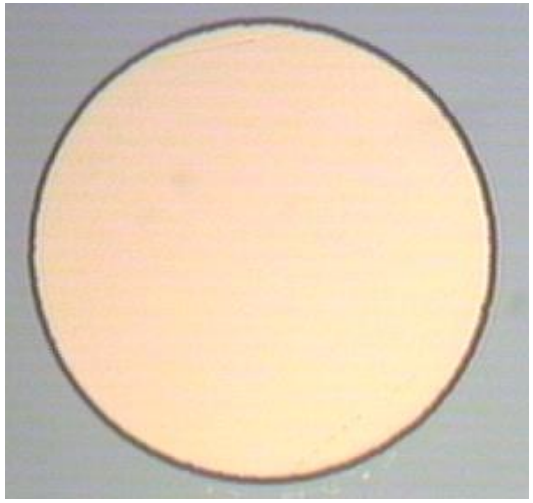
Visual endpoint



20 min



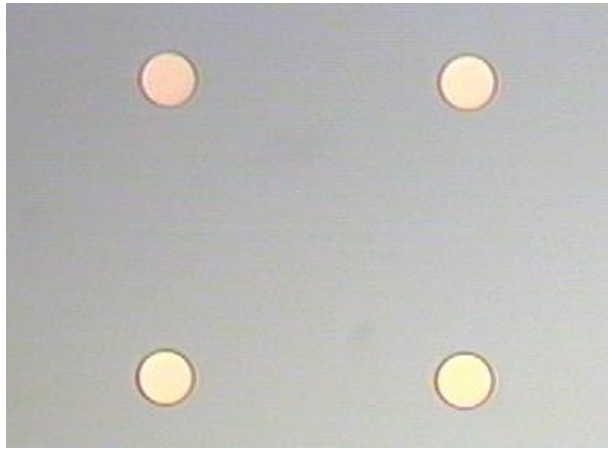
25 min



30 min

Custom Entrepix process was used to planarize Si-Ox-Cu

Polishing endpoint was determined by monitoring the exposed TSV diameter and the width of via dielectric band by microscope



Result

Completed interposer test structure: 25um via diameter, 100um thickness.
Structure has 2 frontside metal layers (4um Cu) and 1 backside metal in TSV chains.
Oxide / nitride TSV dielectric, polyimide dielectric on front / back wafer surfaces.

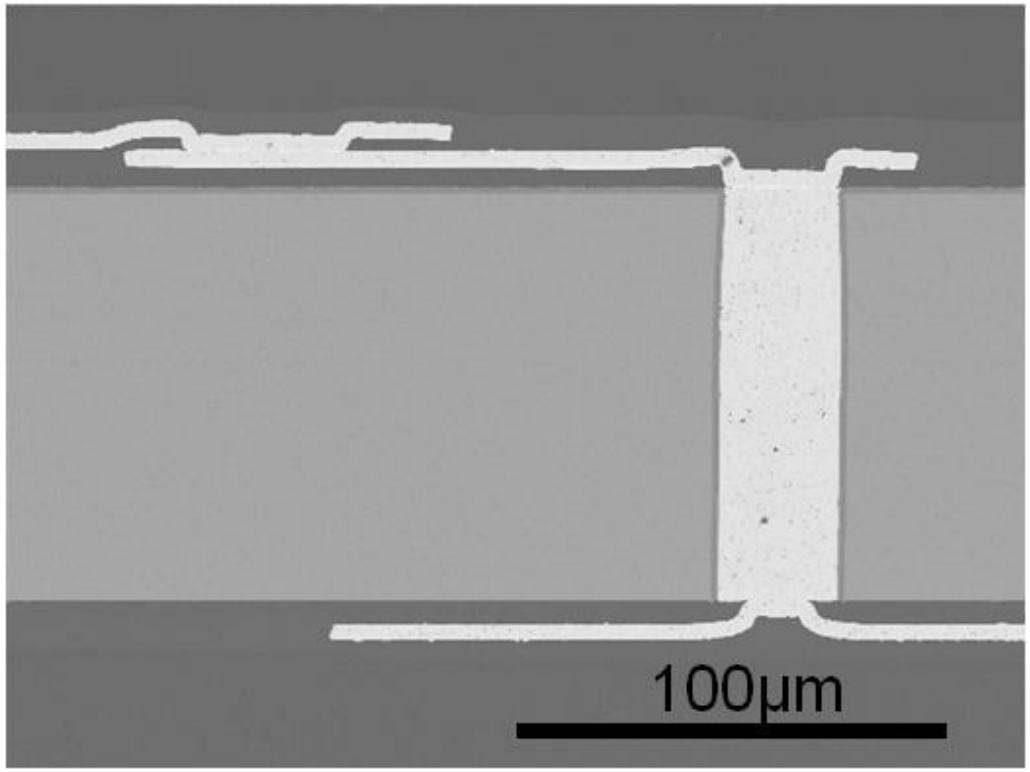


Image courtesy of RTI International

Bottom surface received TSV reveal polish

Integration Options

Interposers

- Viewed as more cost-effective than full 3D integration
- Allow more flexibility in device architecture and PCB layout

Other options or improvements for TSV reveal

- Etch (wet or plasma) to expose TSV's then planarize with CMP
- Reduce Si overburden with lower backgrind target
- Faster Si polish rate
- Develop endpoint algorithm (if possible)

Example 3: Reveal CMP after Si etch

After backgrind, bulk Si removed by an etch process

- Installed equipment already available
- Lower cost per wafer
- Can be either dry etch or wet etch, but must be highly selective to oxide

Si etch proceeds until 3-5um of encased via “bumps” are exposed

Primary goal of CMP is to planarize bumps and expose the Cu cores

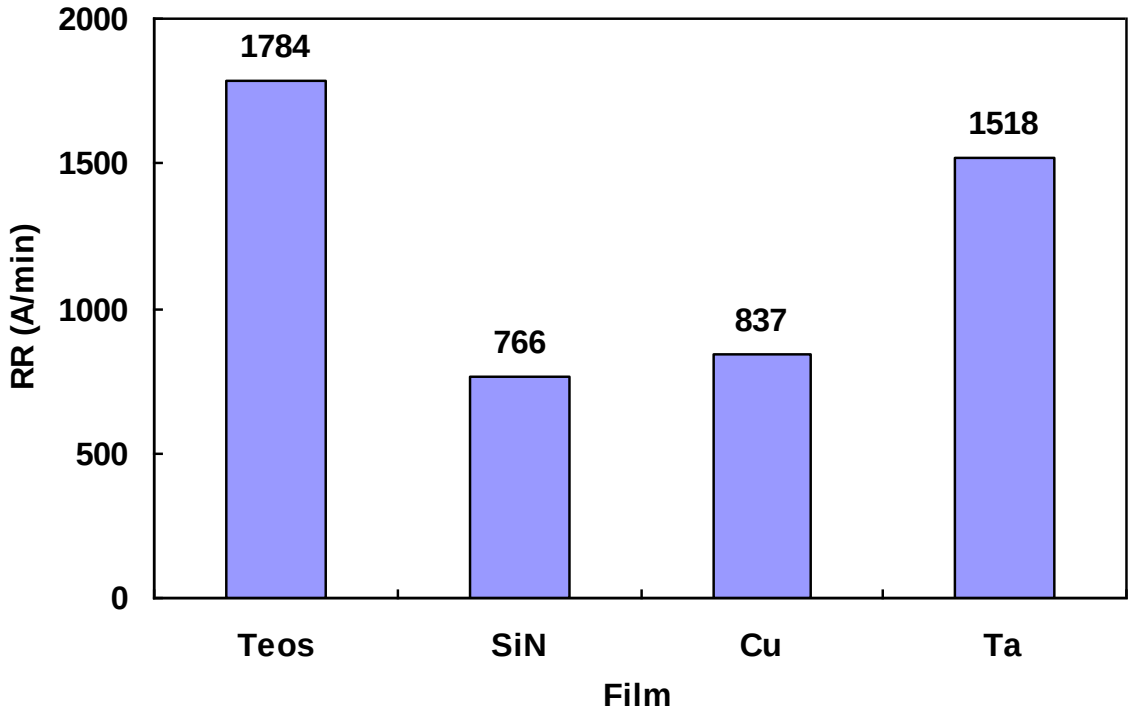
One benefit of this approach is to reduce total CMP polish time
(drops to roughly 1-1.5 min per platen on P1/P2 of a Mirra)

- Less sensitive to uniformity issues
- Faster throughput and lower cost
- Only first pass optimization so far … may drop even further as work proceeds

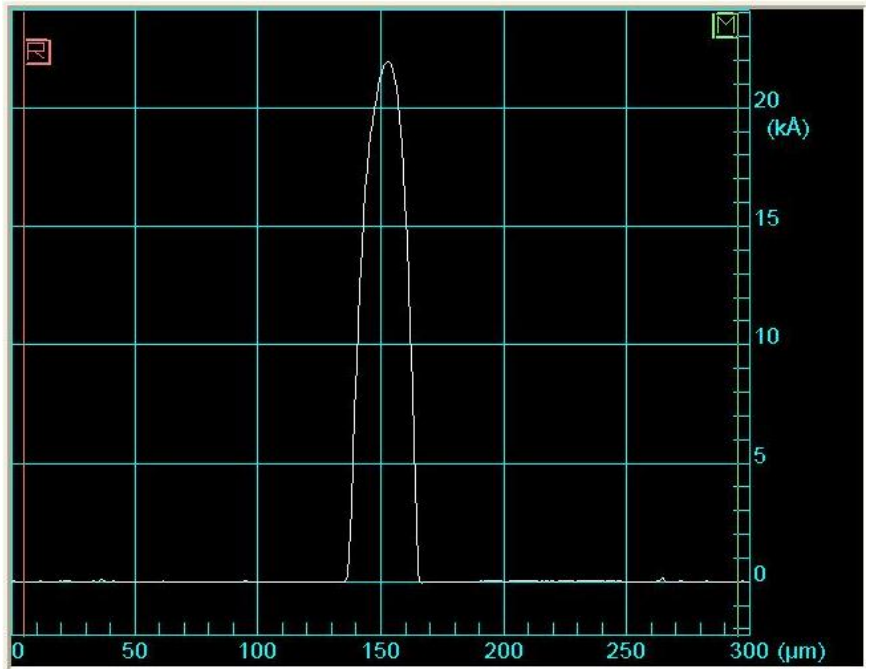
Slurry Removal Rates

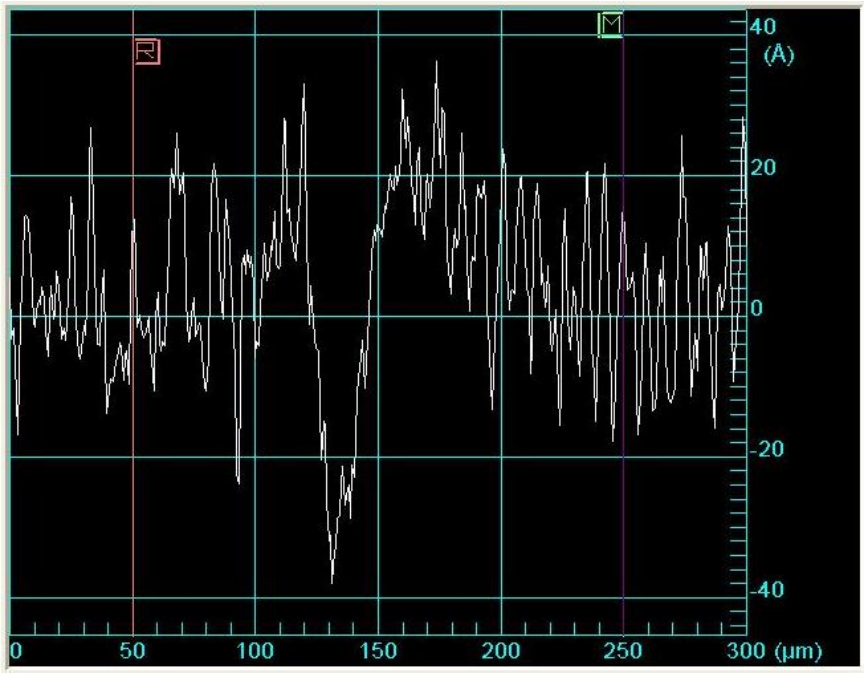
Slurry developed specifically for this type of application

Blanket film removal rates at 3psi membrane pressure



Topography – Wfr 1

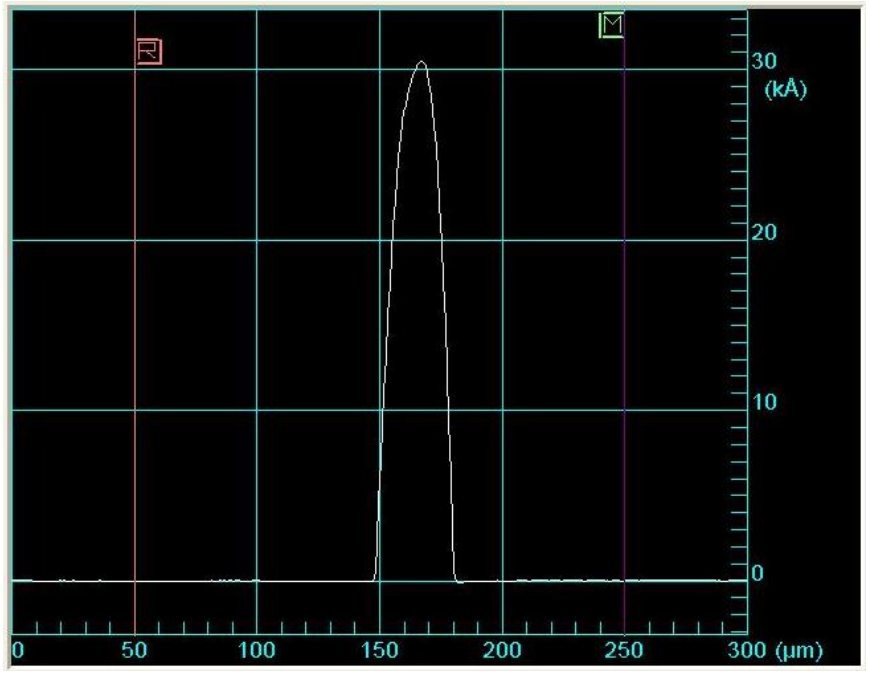


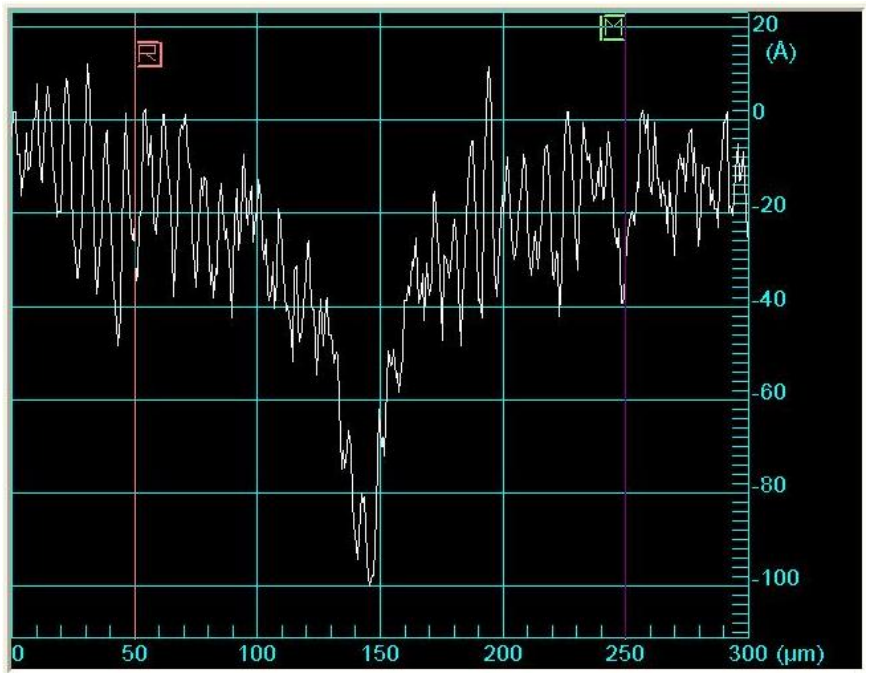


Pre-CMP Step Height
22,000 Ang

Post-CMP Step Height
60 Ang

Topography – Wfr 2





Pre-CMP Step Height
31,000 Ang

Post-CMP Step Height
100 Ang

New Applications Summary

CMP development is more efficient when approached systematically.

Polymer CMP

→ Targeted at a novel integration for multi-layer interposer
→ Required initial screening of slurries … colloidal alumina chosen
→ Achieved good surface finish and reasonable RR >0.5um/min

SiGe Transfer Layer CMP

→ Similar to Smart-Cut SOI fabrication sequence
→ Achieved RMS roughness <2 Ang with 500-700 Ang CMP removal

Oxide Nanostructure CMP

→ Planarization of very small oxide-filled trenches (50-100nm deep)
→ Minimal Si loss after clearing in field regions required using ceria slurry with high selectivity to Si
→ Final topography of <1nm achieved across 300mm wafers

TSV Summary-1

Through Silicon Via Technology (TSV)

- Enabling many 3D integrations and growing rapidly
- Most TSV flows rely on CMP twice, but very different processes
  - High rate Cu for front-side via definition (damascene)
  - TSV reveal CMP from original back-side after grind

High rate Cu slurry for via formation

- Slurry from AGC (CX-1000 series)
- Cu removal rate > 4 um/min at 4psi membrane pressure
- High selectivity to oxide, Ta, and Ti (all >100:1)
- Excellent topography control (<250 nm) even with long overpolish
- Good surface finish on all exposed materials

TSV Summary-2

TSV Reveal (High rate Si & Cu removal)

- Custom blended formulation
- Si removal rate >= 1 um/min
- Low selectivity between Si and Cu (< 2:1)
- Excellent topography control (<400 nm)
- Single step CMP … only ONE slurry required

TSV Reveal (low-selectivity for more complex integration)

- Integration demands oxide/nitride/Cu/barrier removal
- Low selectivity among all materials
- Excellent topography (<100 nm) and good surface finish
- Single step CMP … only ONE slurry required

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