TCAD Modeling for Mechanical Stress Management in 3D IC Packages

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NCCAVS Joint User Group Meeting on 3D Packaging

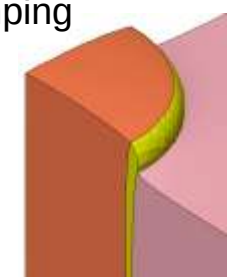
Outline

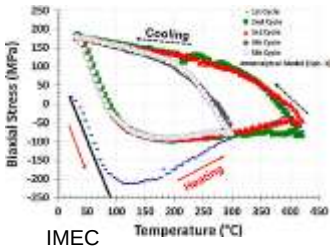
- **Thermal Mismatch Stresses in 3D IC**
- **Modeling stress evolution with TCAD**
- **Analyzing stress effects on performance and reliability**
- **Stress management in 3D IC technology integration and design**

Through Silicon Via Stress Effects

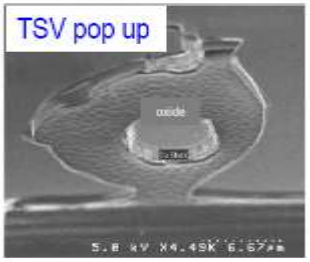
- **Reliability**

Pumping





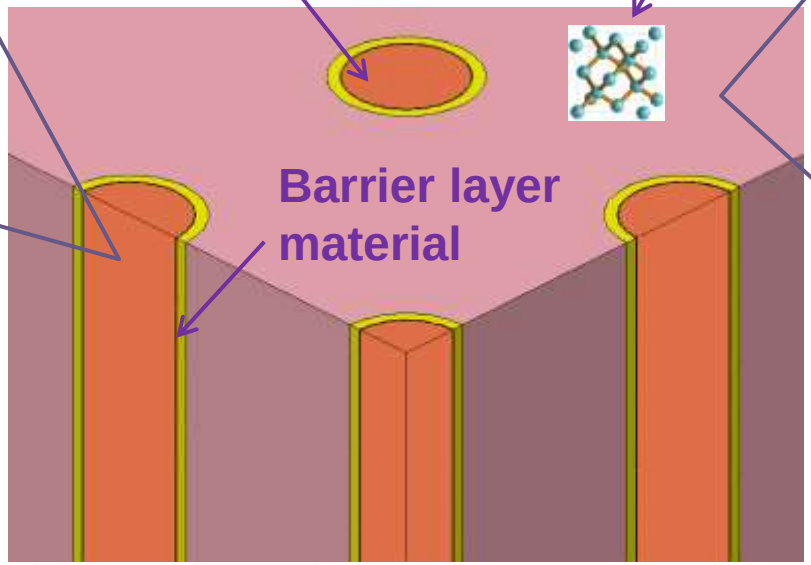
IMEC



TSV extrusion and de-lamination
- Tezzaron, RTI 2009

Via material, process

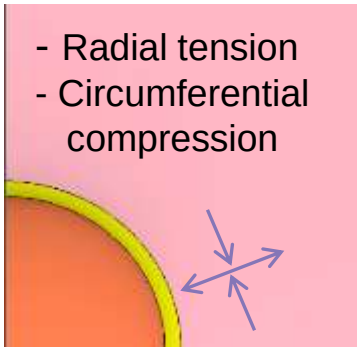
Silicon crystal orientation, P/N

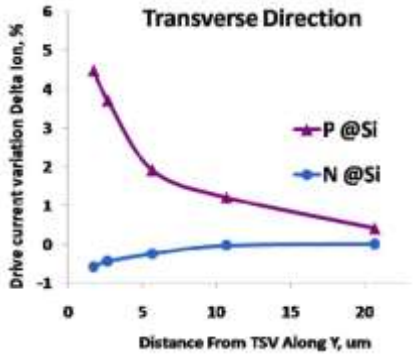


Insulation liner material and thickness

TSV pitch, diameter

- **Mobility change**

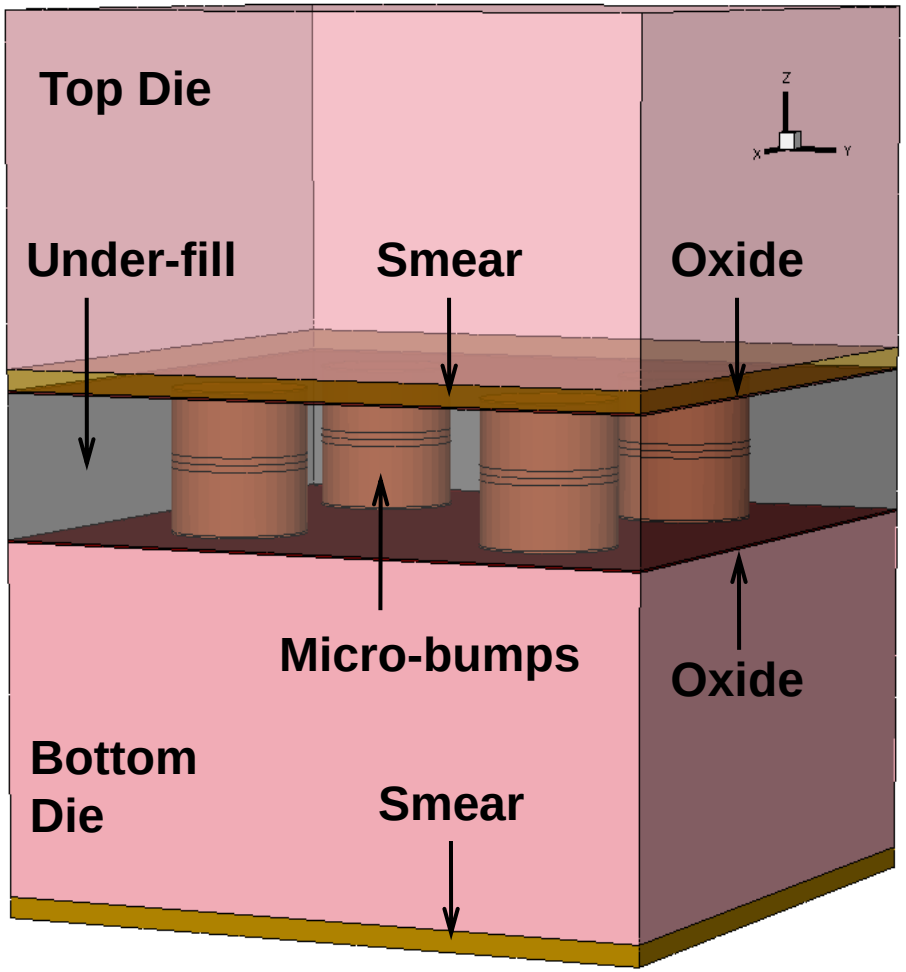




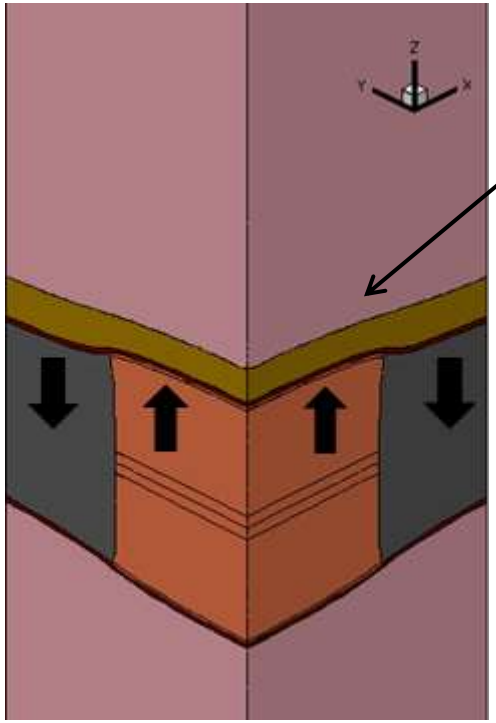
Performance shifting due to TSV stress
- IMEC, VLSI 2010

Thermal Mismatch Stress near u-bump

Micro-bump Array



Deformed Micro-bump



$$\alpha_{under-fill} > \alpha_{bump}$$

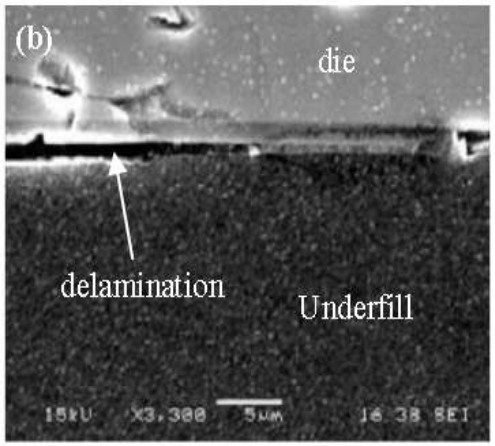
Thermal mismatch leads to die pull-down and bump push-up

Synopsys, MRS Proceedings, 2011

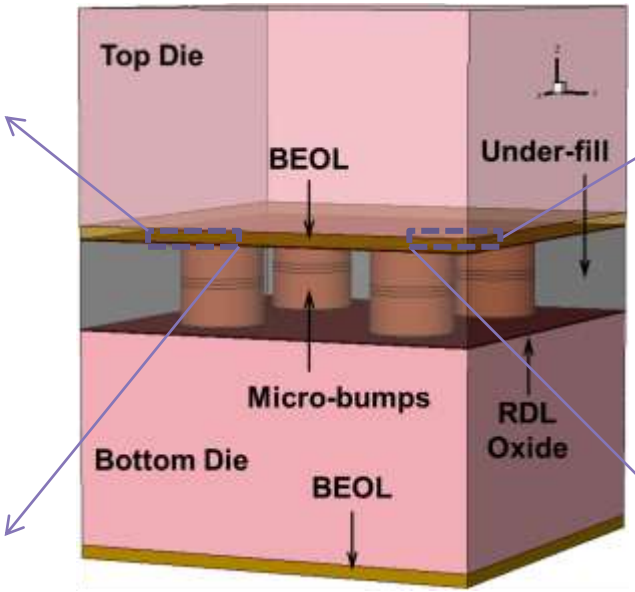
Micro-bump Stress Effects

- **Micro-bumps introduce stresses that depend on**
  - **Micro-bump and under-fill material properties**
  - **Micro-bump geometry and layout parameters**
- **Micro-bump stress effects**
  - **Current shift in devices above micro bumps**
  - **Interface delamination and cracking**

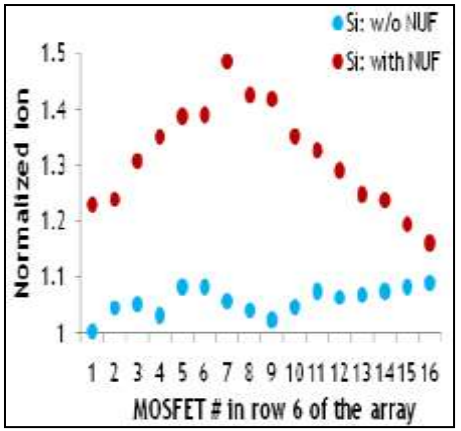
Interface cracking near micro-bump



IME, EPTC 2009



Device On current shift above micro-bump



IMEC, ECTC 2011

Synopsys, MRS Proceedings, 2011

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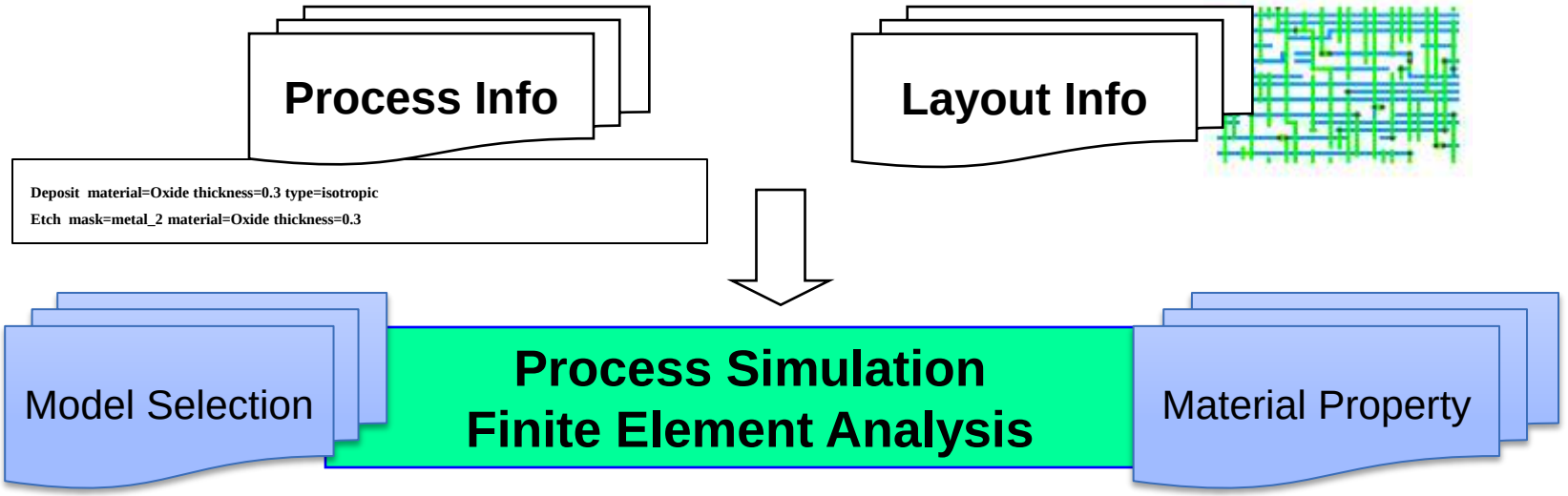
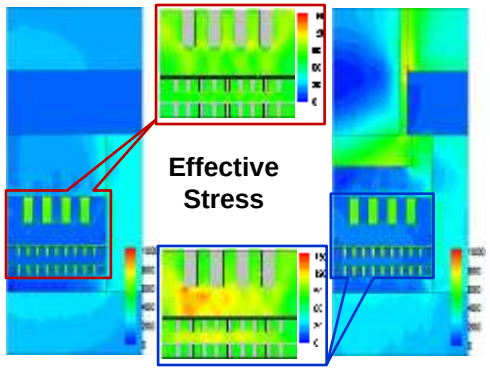
TCAD 3D IC Simulation Flow



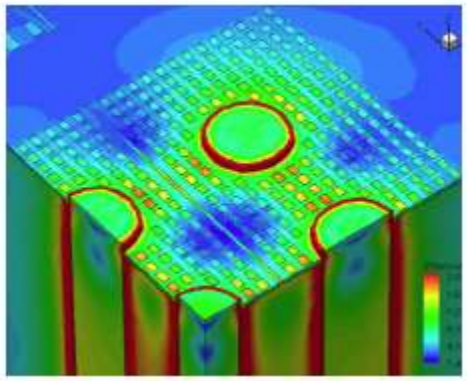
Synopsys, IRPS 2009



Reliability

3D Structures
Solution Fields
Mobility Variations
Reliability Analyses

IMEC/Synopsys et al, IEDM 2010

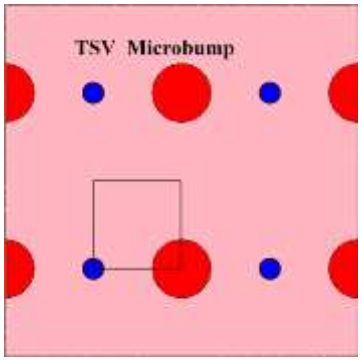


Mobility Variation

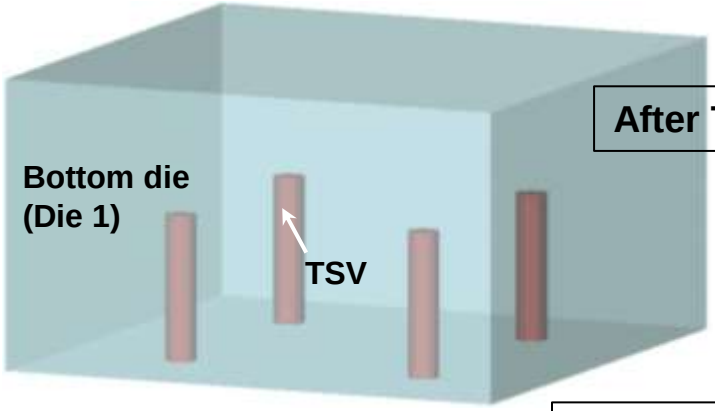
Synopsys, AIP Conference Proceedings, Vol. 1378, 2011

TSV and μ-bump Stress Simulation

Via-middle process:

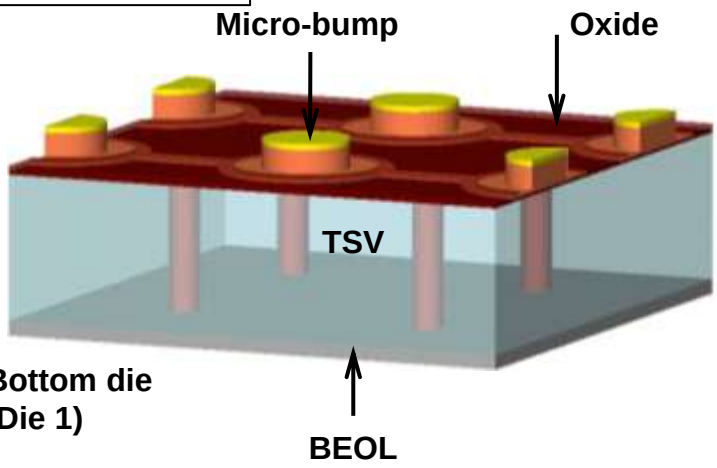


Layout

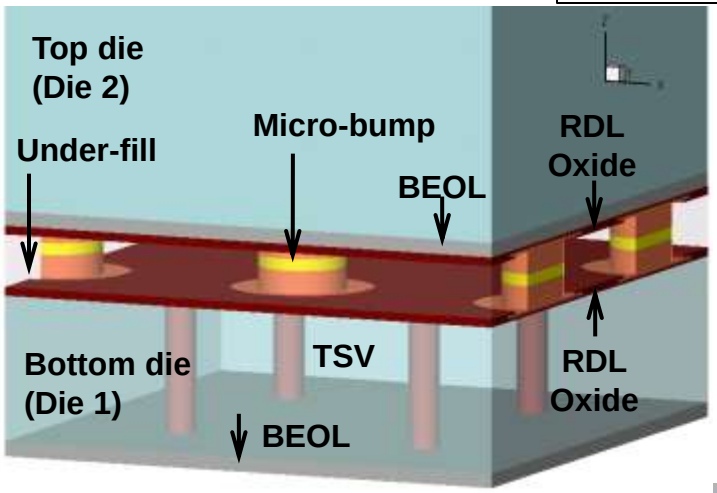


After TSV step

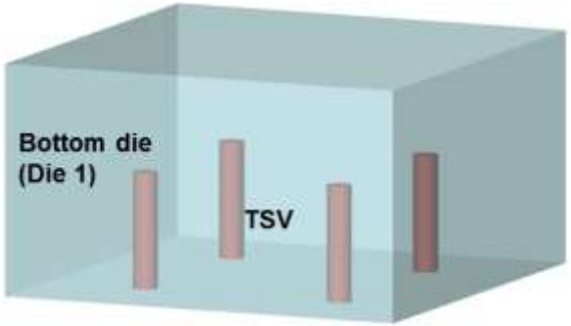
After bump step



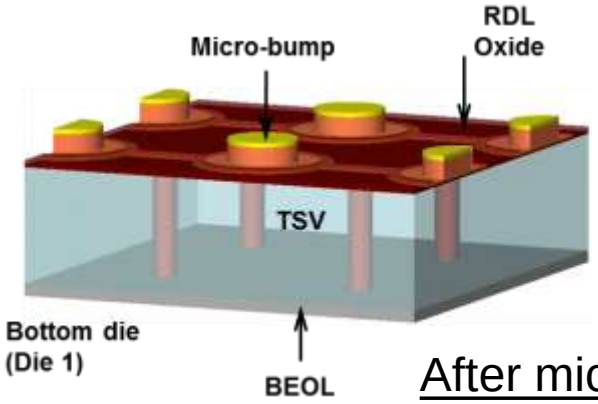
After stacking step



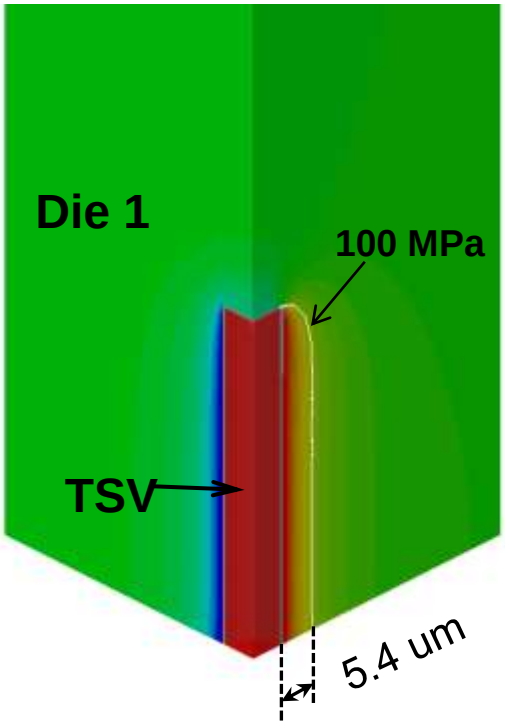
Stress Evolution with Process Steps

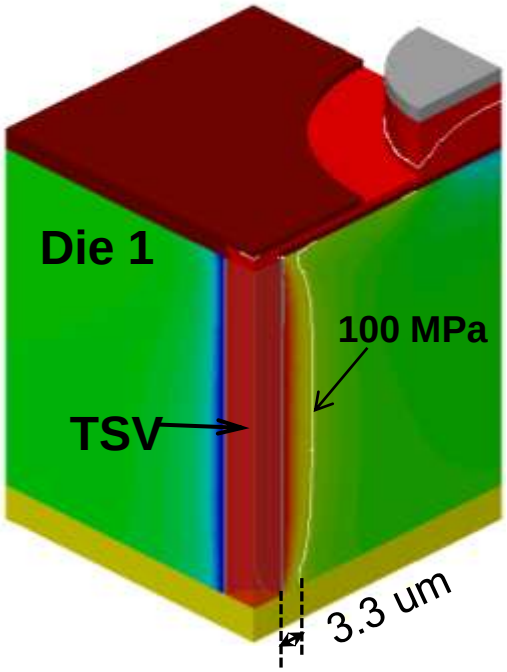


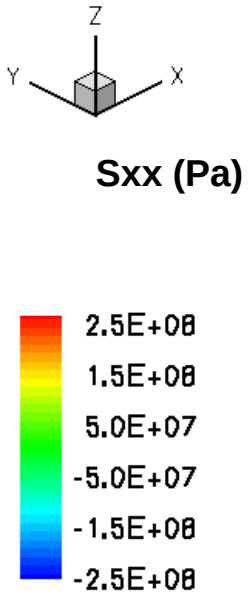
After TSV step



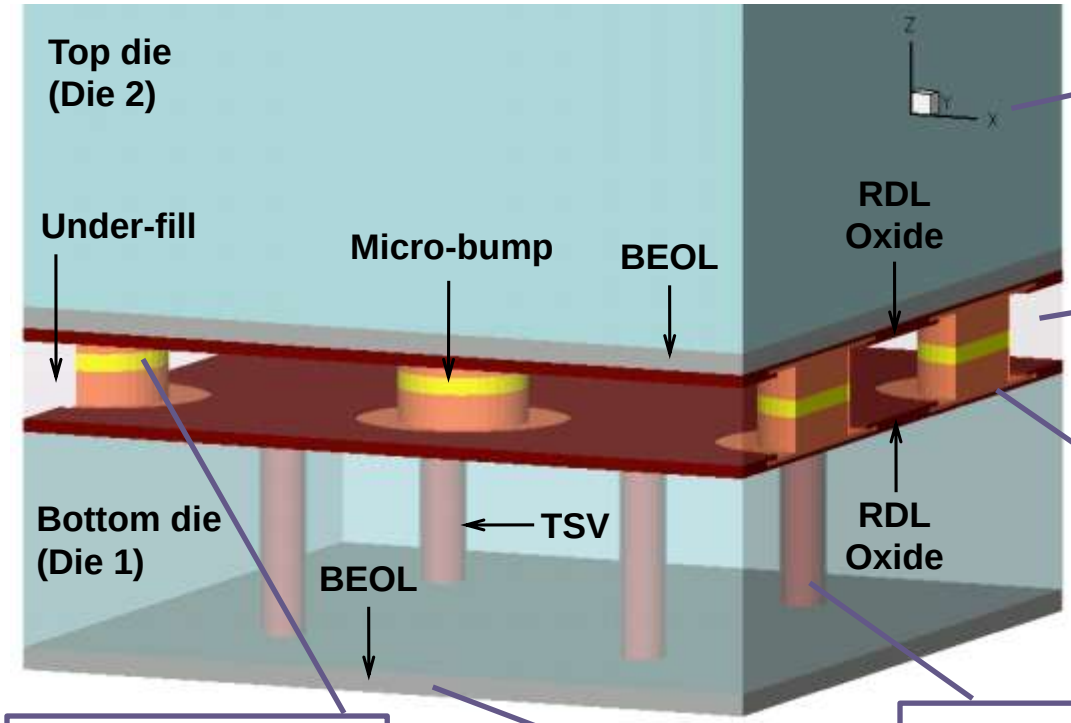
After micro-bump step







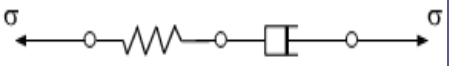
Material Behaviors in TSV Stack



Anisotropic elastic

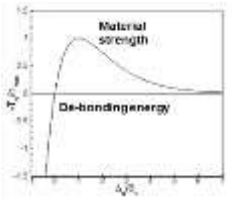
Silicon

Visco-elastic

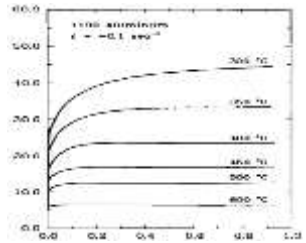


Under-fill

Cohesive Interface

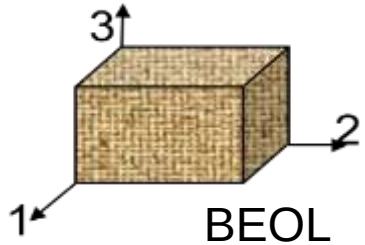


Visco-plastic



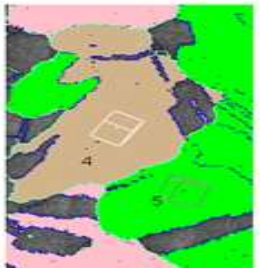
Solder

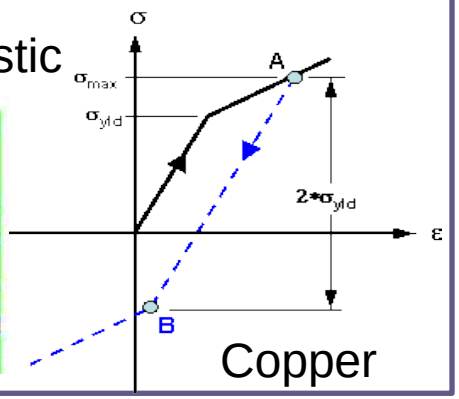
Orthotropic elastic



BEOL

Elastic-plastic





Copper

Outline

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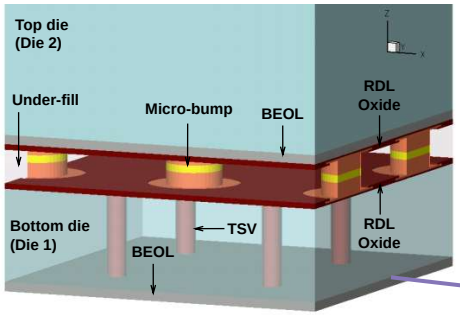
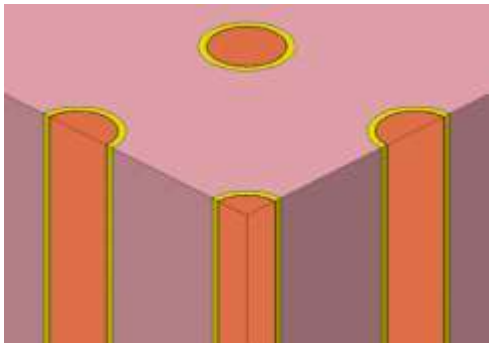
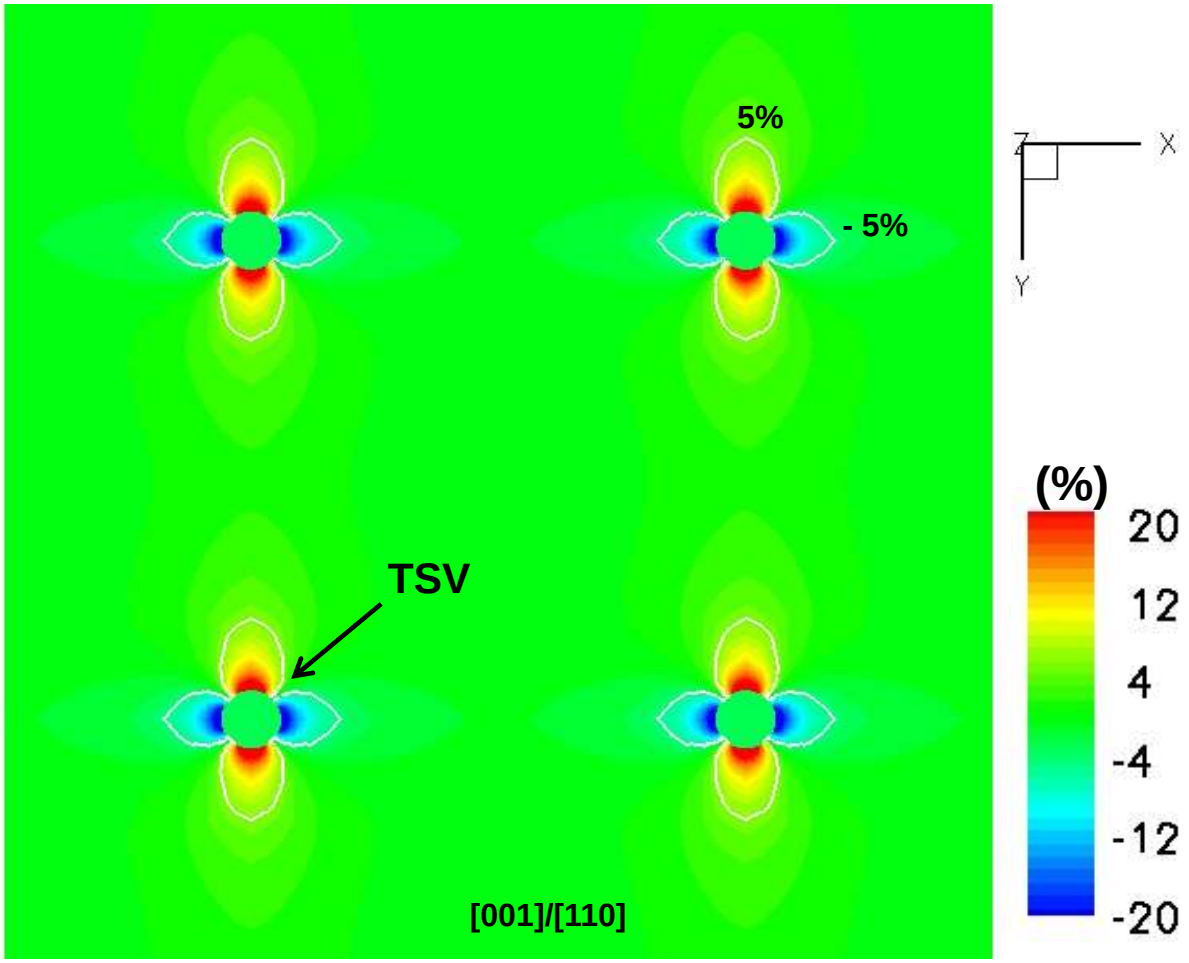
P-mobility Variation on Die-1 Surface



Stress around TSV

- Radial tension
- Circumferential compression

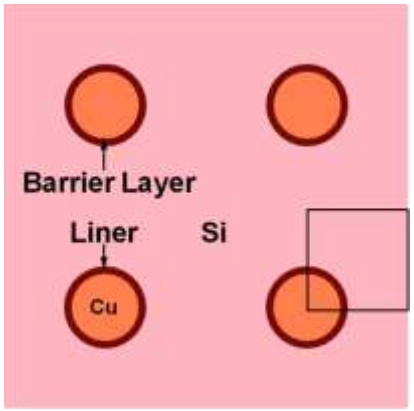


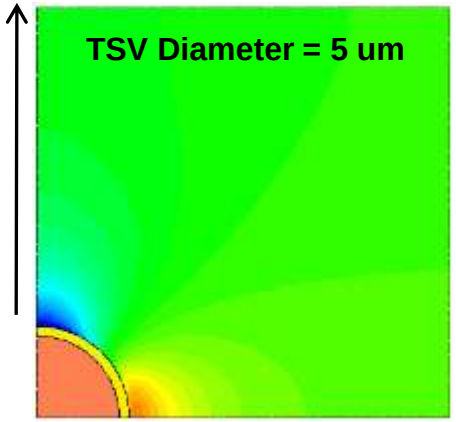


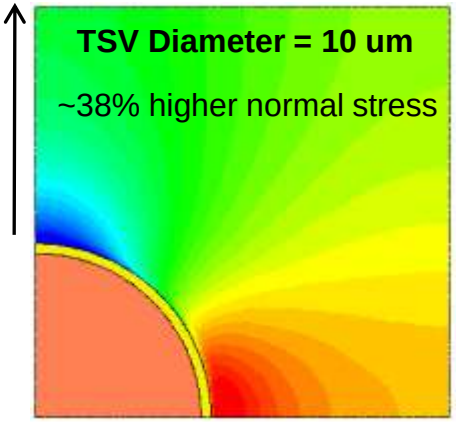
- **Mobility variation localized around TSVs**
- **Keep-Out-Zone (KOZ) design rule and place & route methodology**

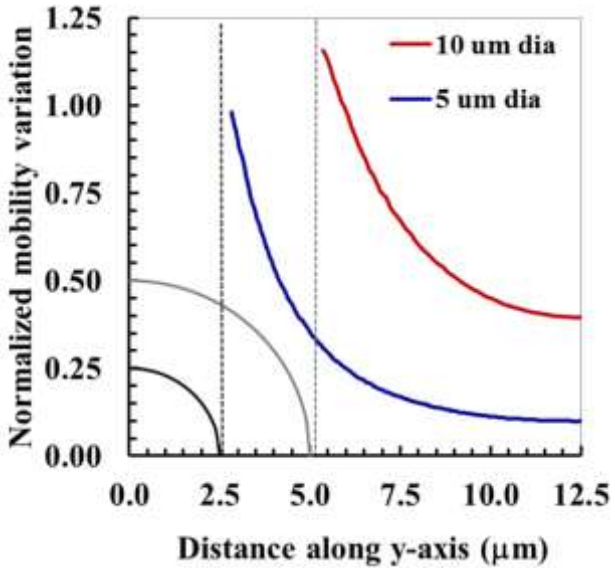
Synopsys, 12th international workshop on stress-induced phenomena in microelectronics, 2012

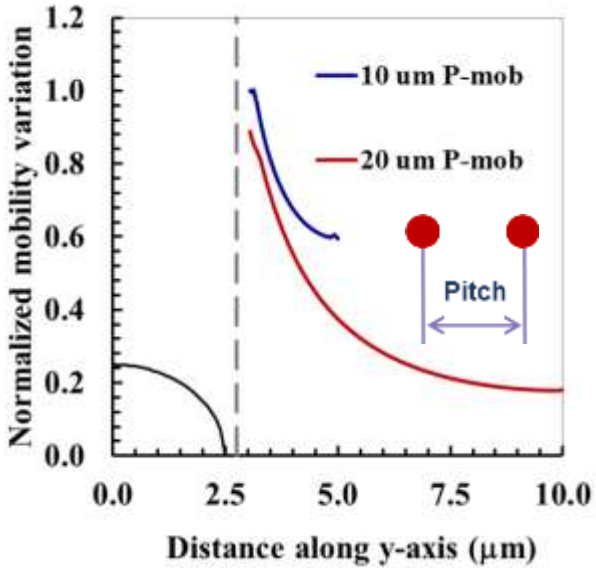
TSV Diameter and Pitch Effects





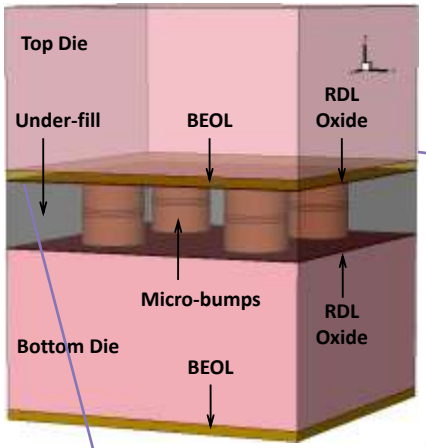




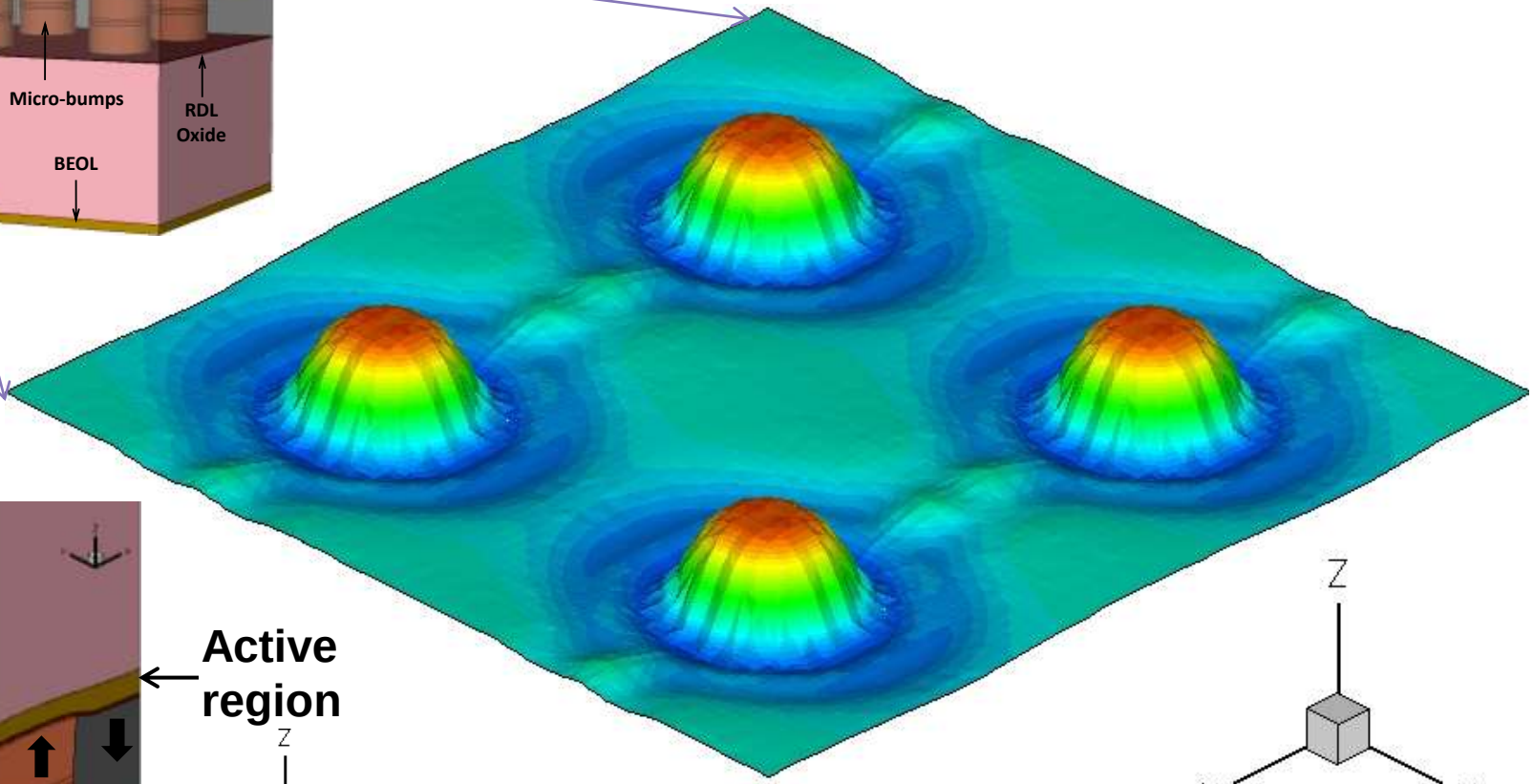


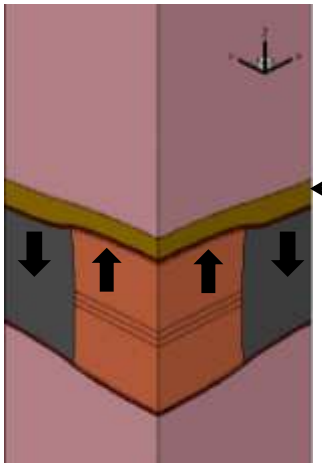
Synopsys, 12th international workshop on stress-induced phenomena in microelectronics, 2012

N-mobility Variation on Die-2 Surface

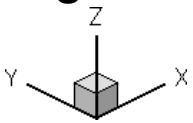


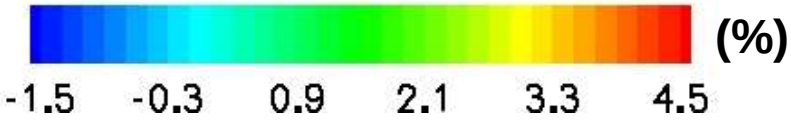
- Mobility variation localized above u-bump
- KOZ design rule and place & route methodology





Active region

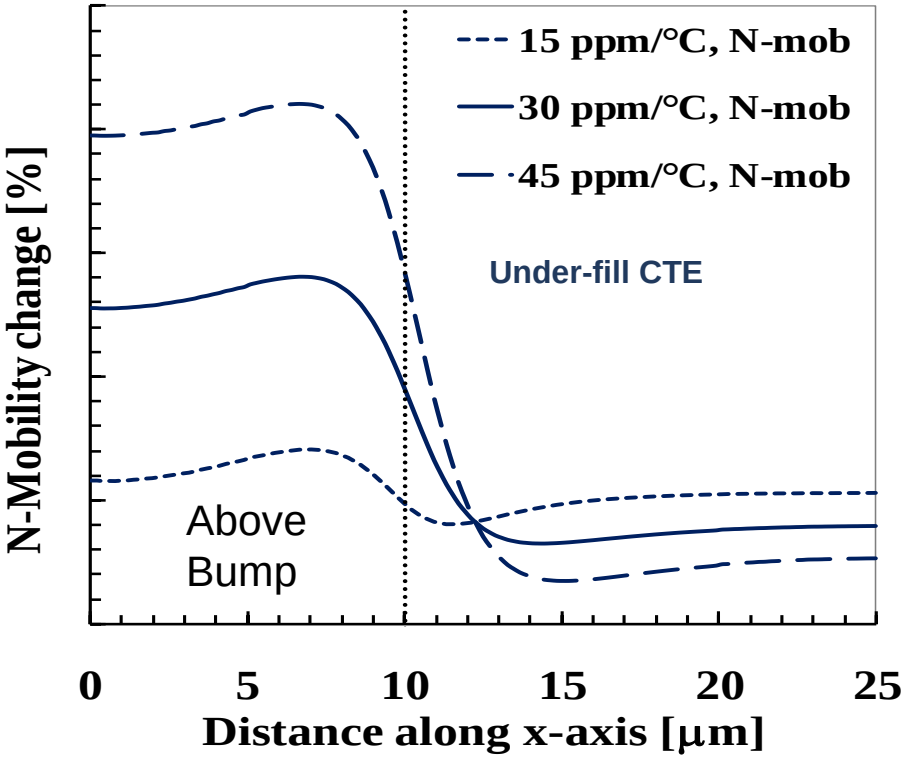


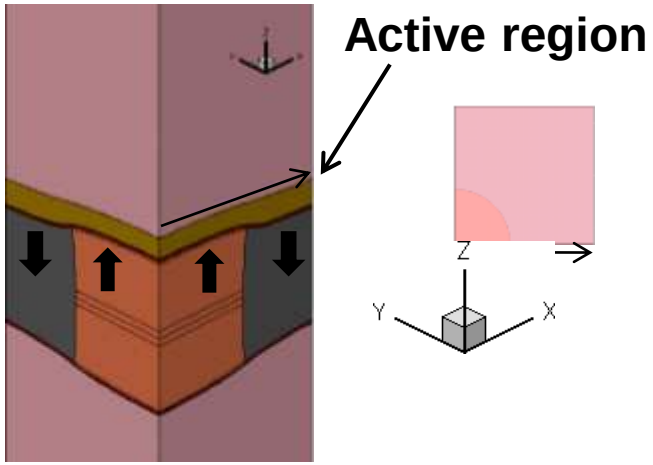


Synopsys, 12th international workshop on stress-induced phenomena in microelectronics, 2012

Under-fill CTE Impact

LCTE: 15.0, 30.0 and 45.0 ppm/°C



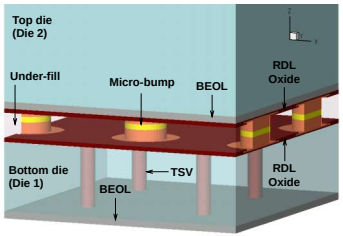


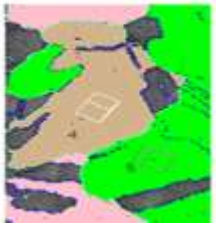
Large under-fill CTE increases contraction and pulling down

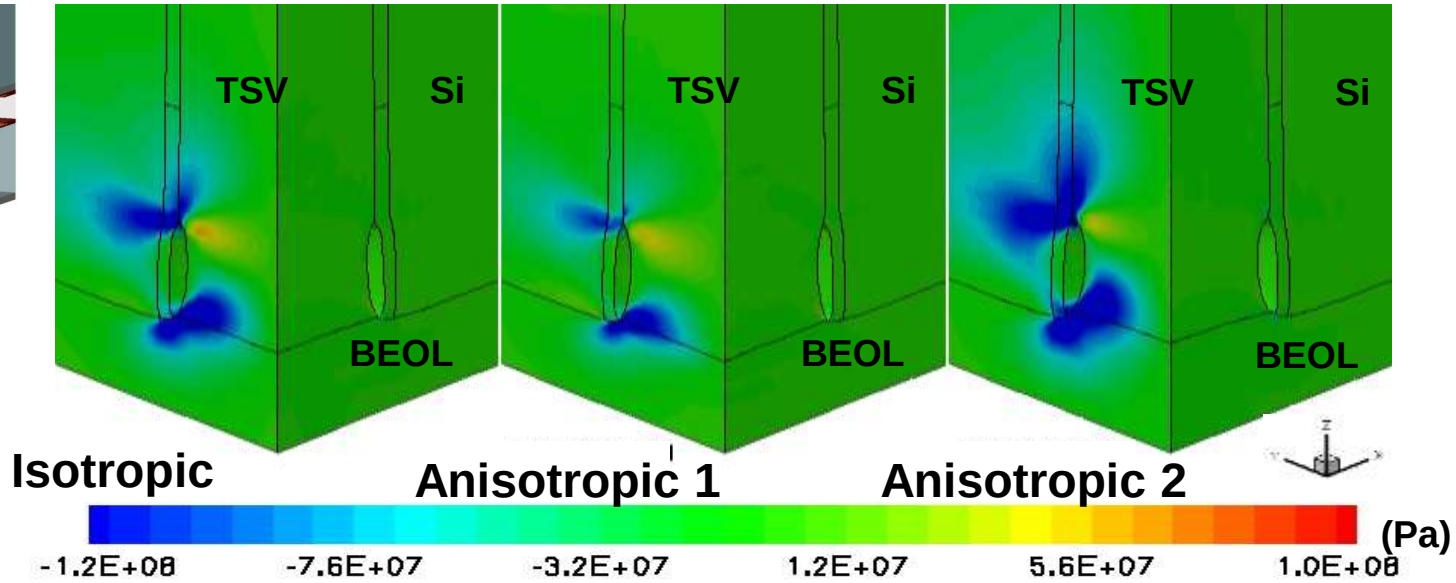
Larger under-fill CTE leads to greater mobility variation

Synopsys, MRS Proceedings, 2011

Copper Anisotropic Effect on Crack

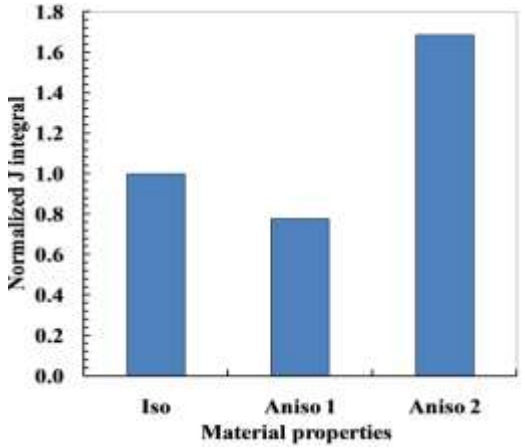






Anisotropic Copper	E1	E2	E3
Anisotropic 1	156 GPa	69 GPa	69 GPa
Anisotropic 3	69 GPa	69 GPa	156 GPa

- **Crack driving force and mode mixity depends on copper anisotropy in different crystal orientation**



Synopsys/Fraunhofer, IEEE TDMR, 2012

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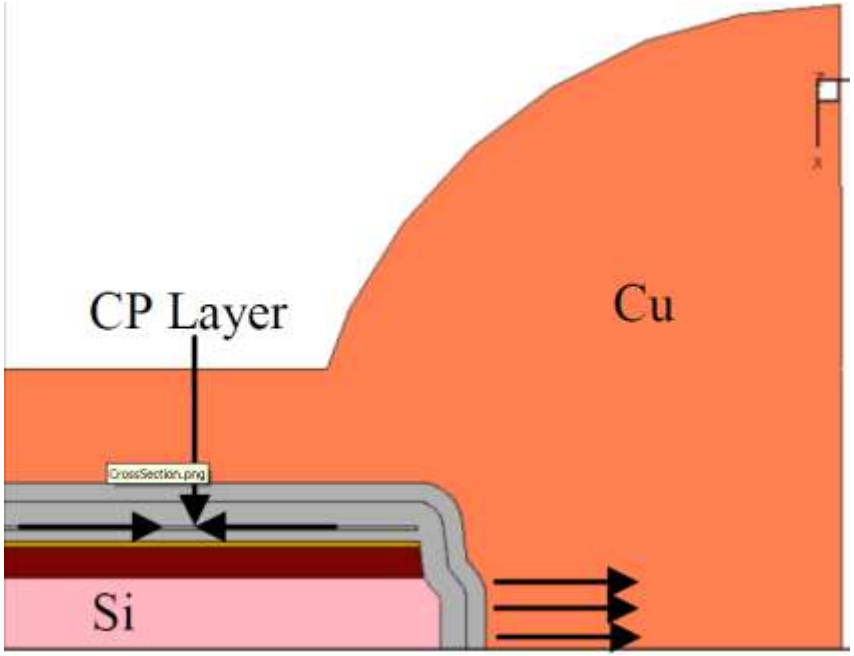
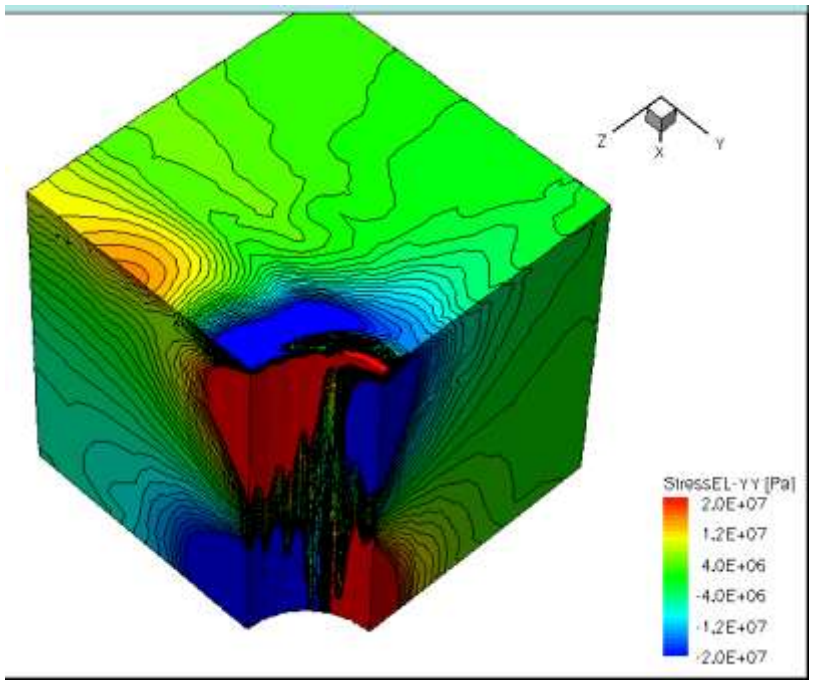
Managing KOZ with TCAD Modeling

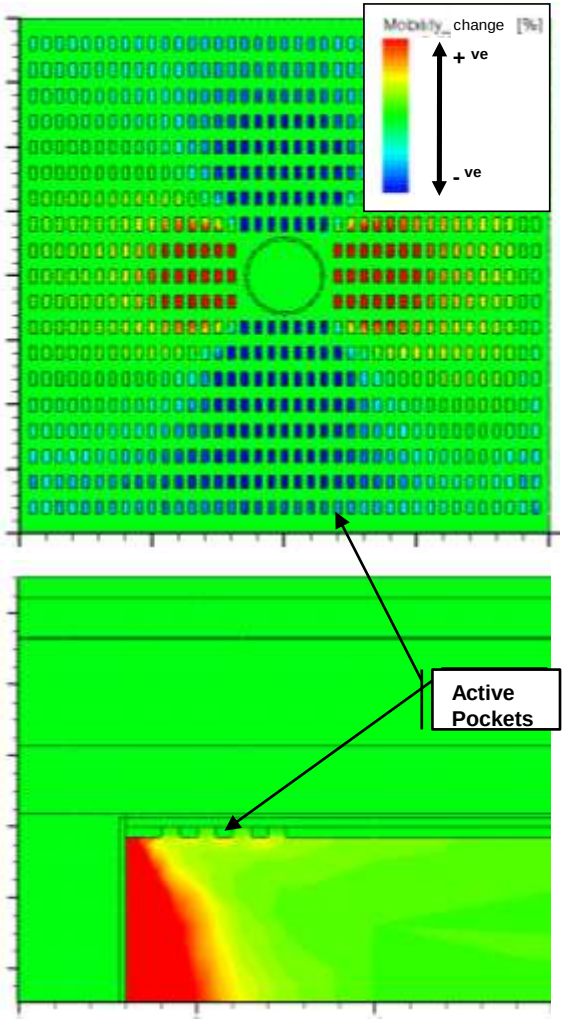
M. Rabie, et al, GLOBAL FOUNDRIES, IITC 2014



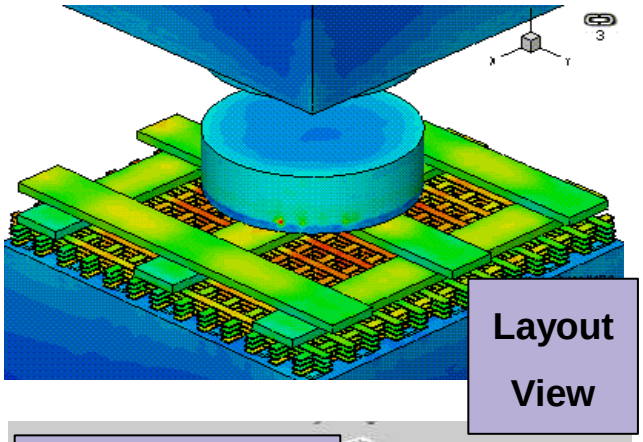


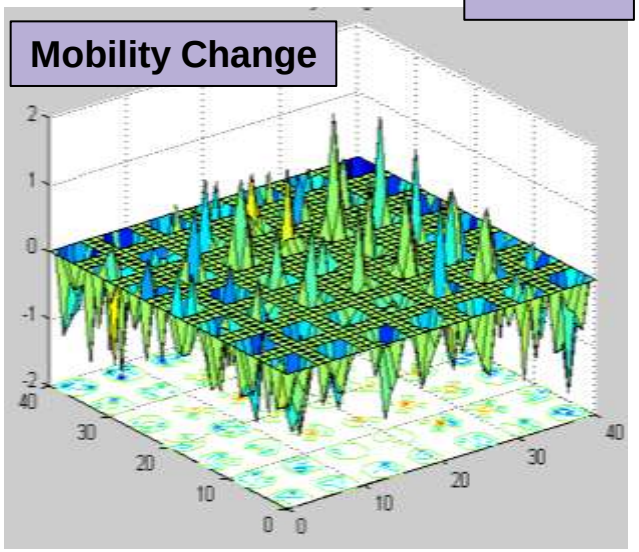
- **Tensile stress due to TSV copper shrinkage is compensated by compressive stress due to CMP stop layer**
- **Experiments and TCAD simulations**

Stress Management at Qualcomm



TSV Effect





μ-Bump Effect

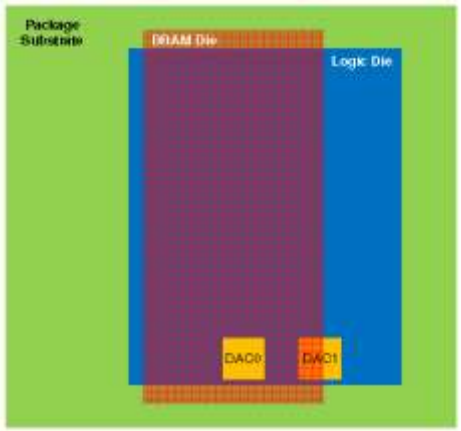


Figure 2. Top view of a DRAM die on top of a logic die

Figure 3. Side view of a DRAM die on top of a logic die

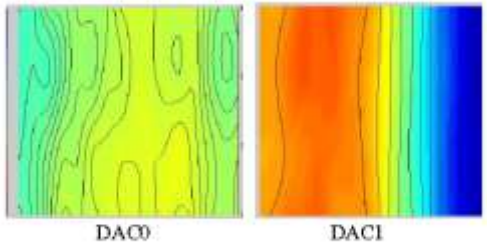


Figure 4. Color contour map of linear currents deviation in DAC transistors arrays

Stacking Effect

Qualcomm, CICC 2010, ECTC 2014

Summary

- **Mechanical stress in TSV stacks affects both performance and reliability**
- **TCAD modeling of stress evolution and stress effects provides valuable insights**
- **3D IC design and technology configurations can be optimized with stress management**

