Cooling Three-Dimensional Integrated Circuits using Power Delivery Networks (PDNs)

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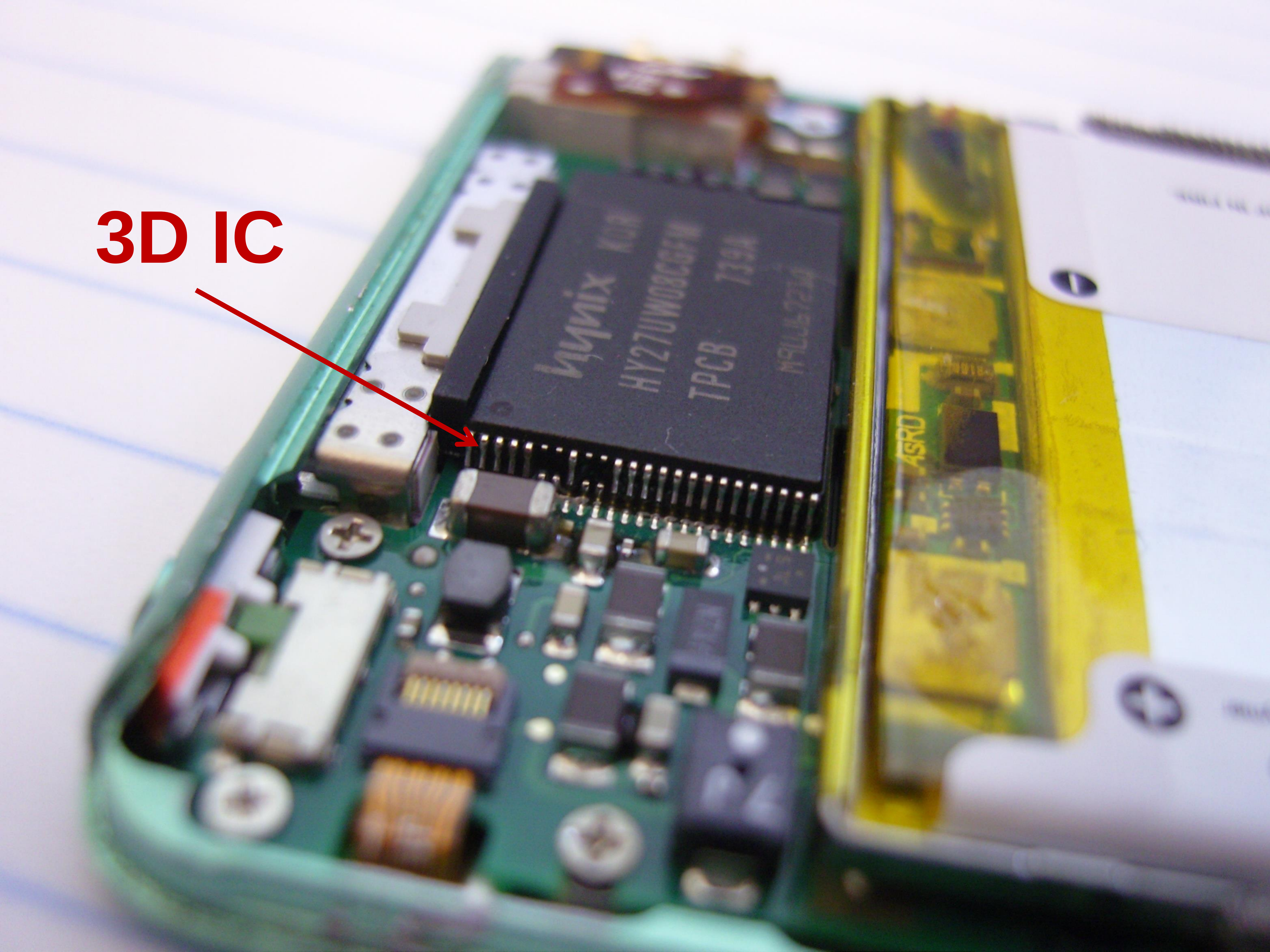
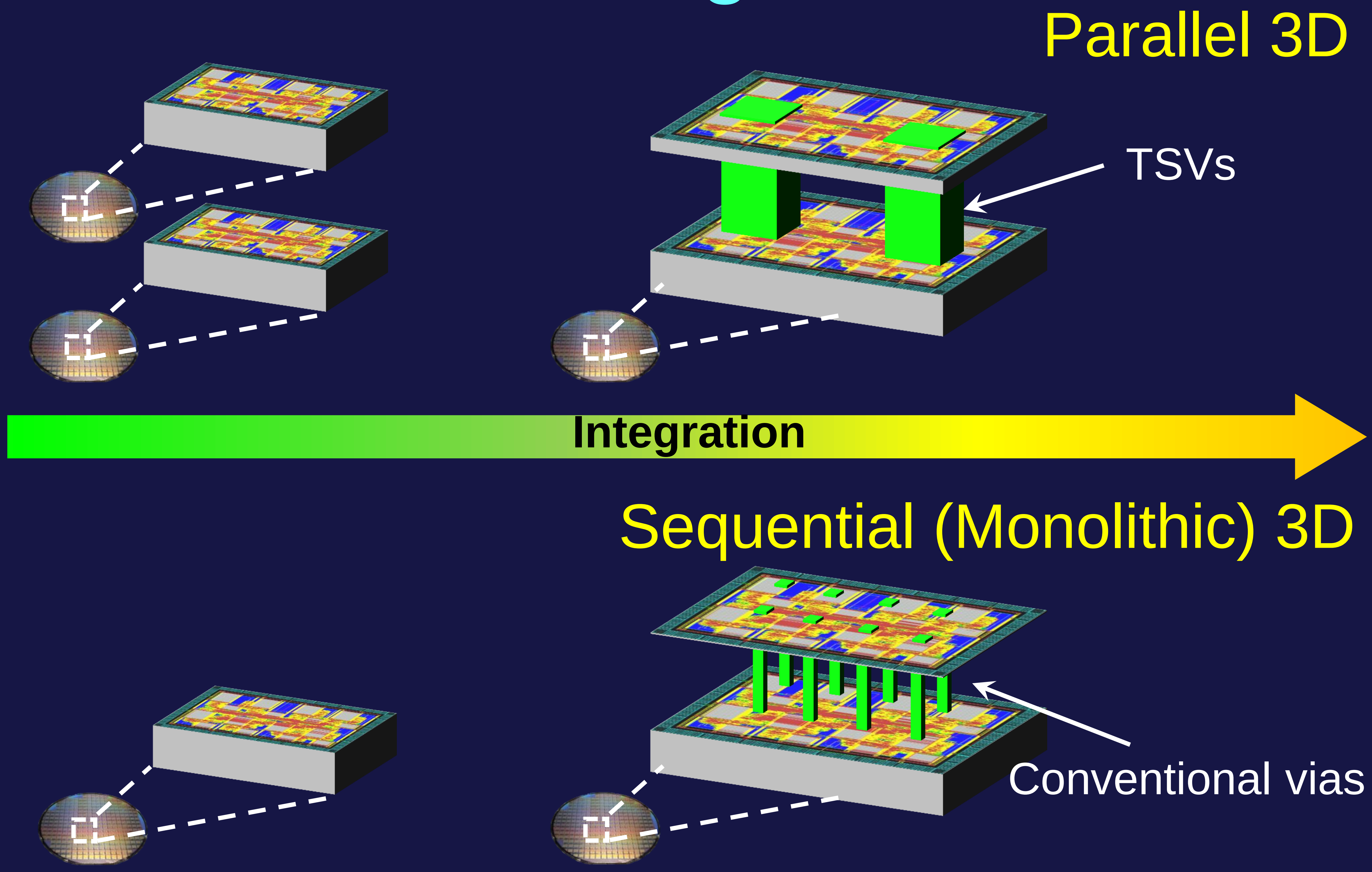
Acknowledgement: Prof. Mitra, Prof. Wong, Prof. Pease,
T. Wu, D. Sekar, B. Cronquist, N. Patil

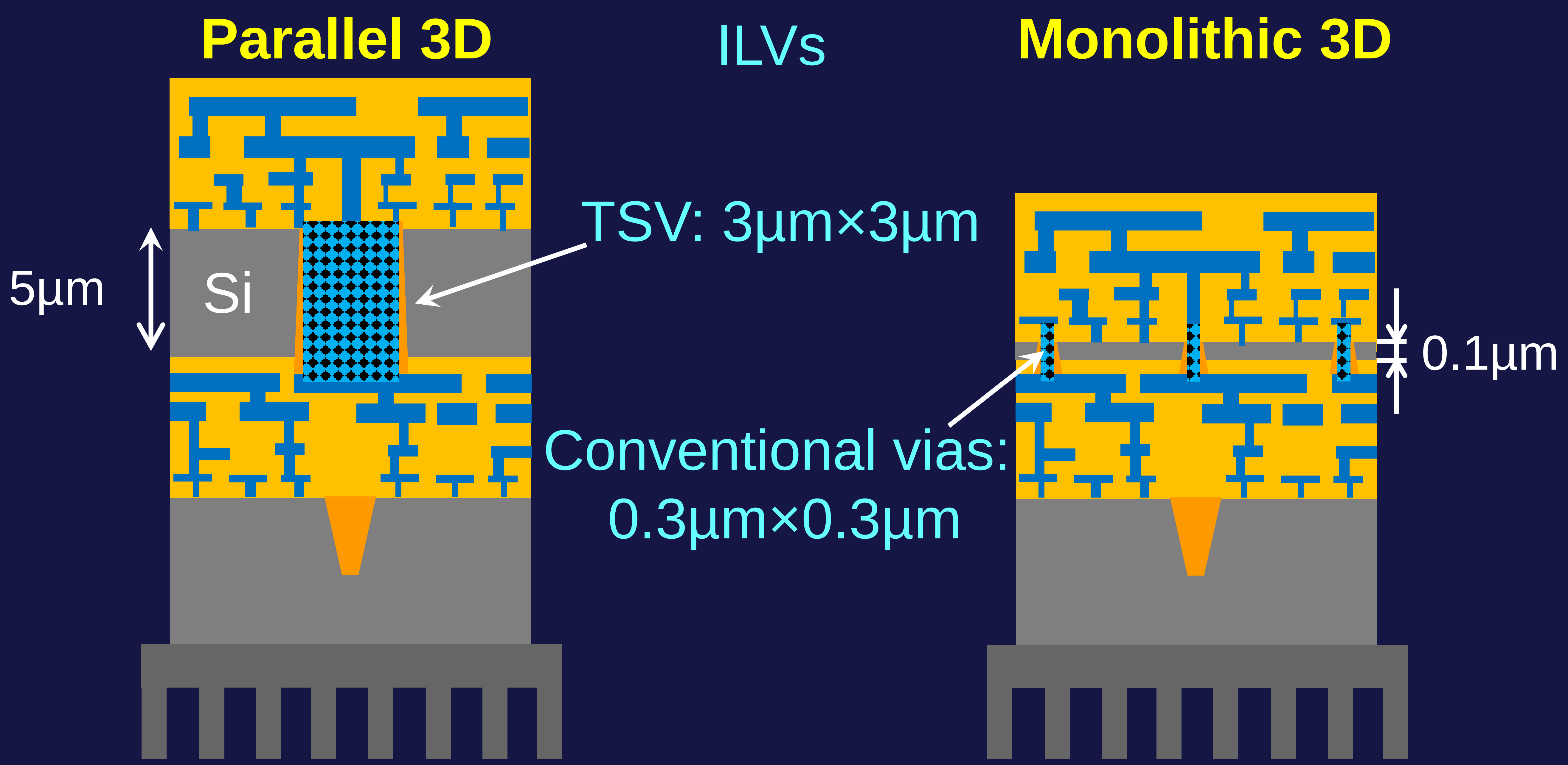

3D IC
hynix

3D Integration



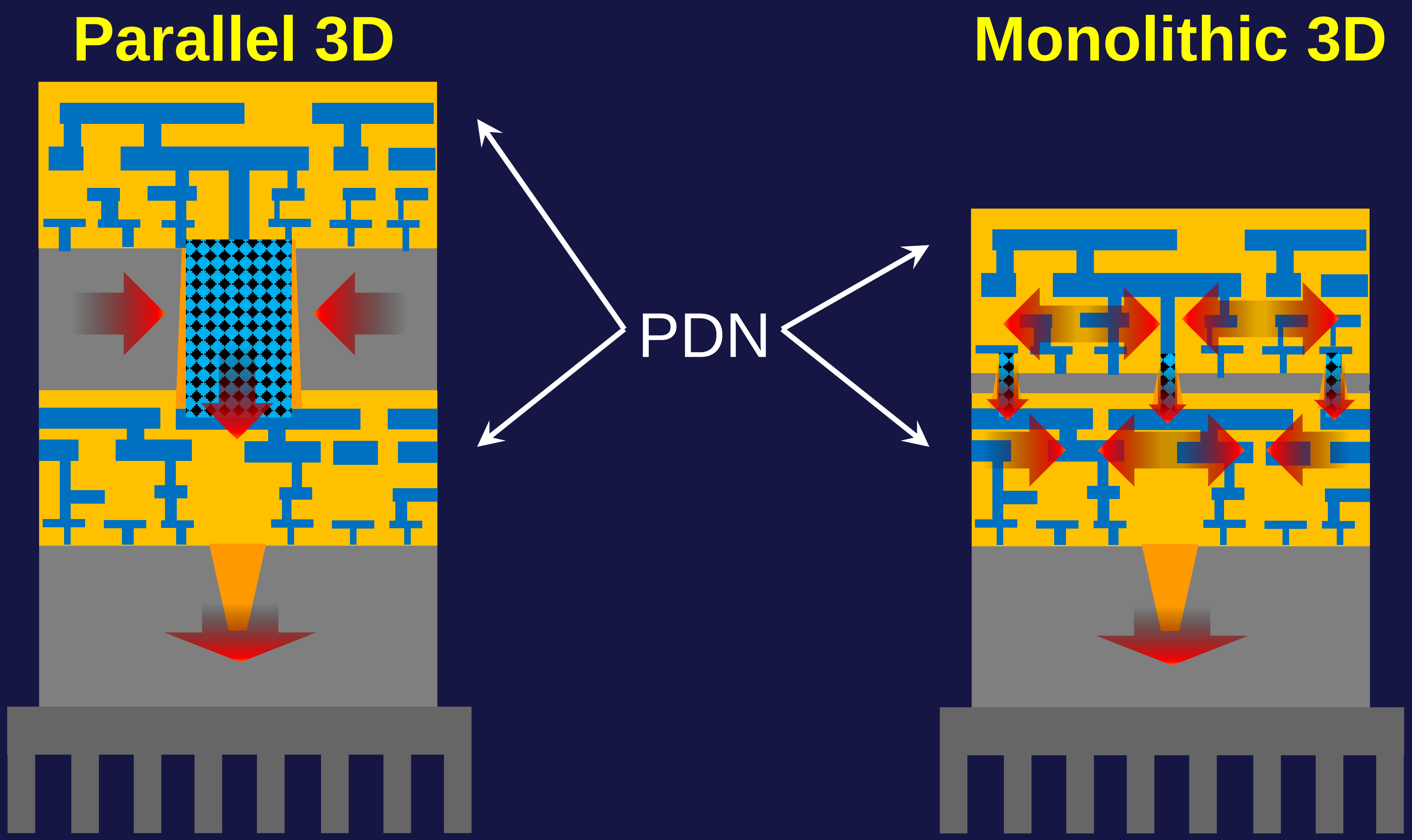
Geometries

- ILV: Inter-Layer Via

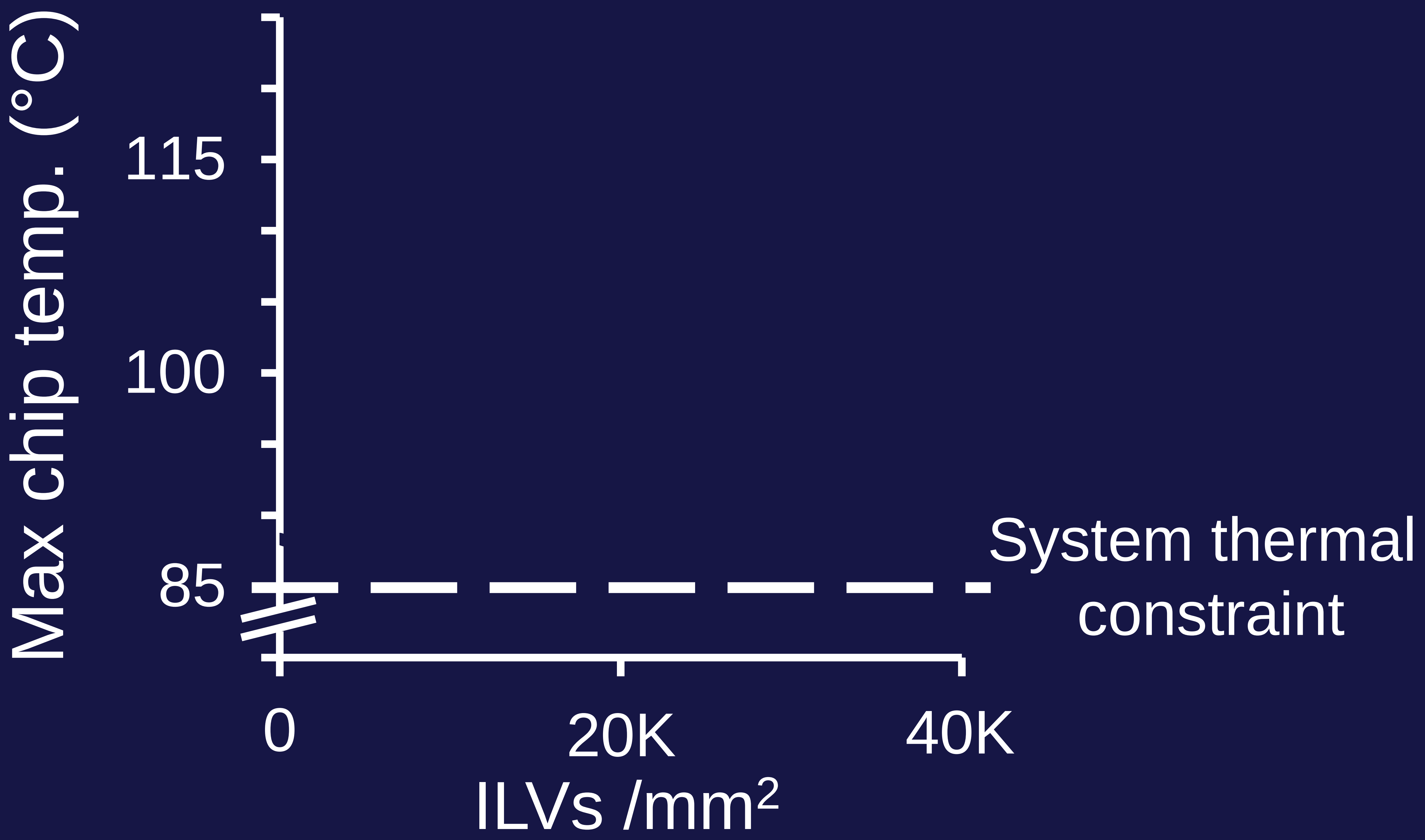


Geometries

- PDN: Power Delivery Network



Key Result for Monolithic 3D



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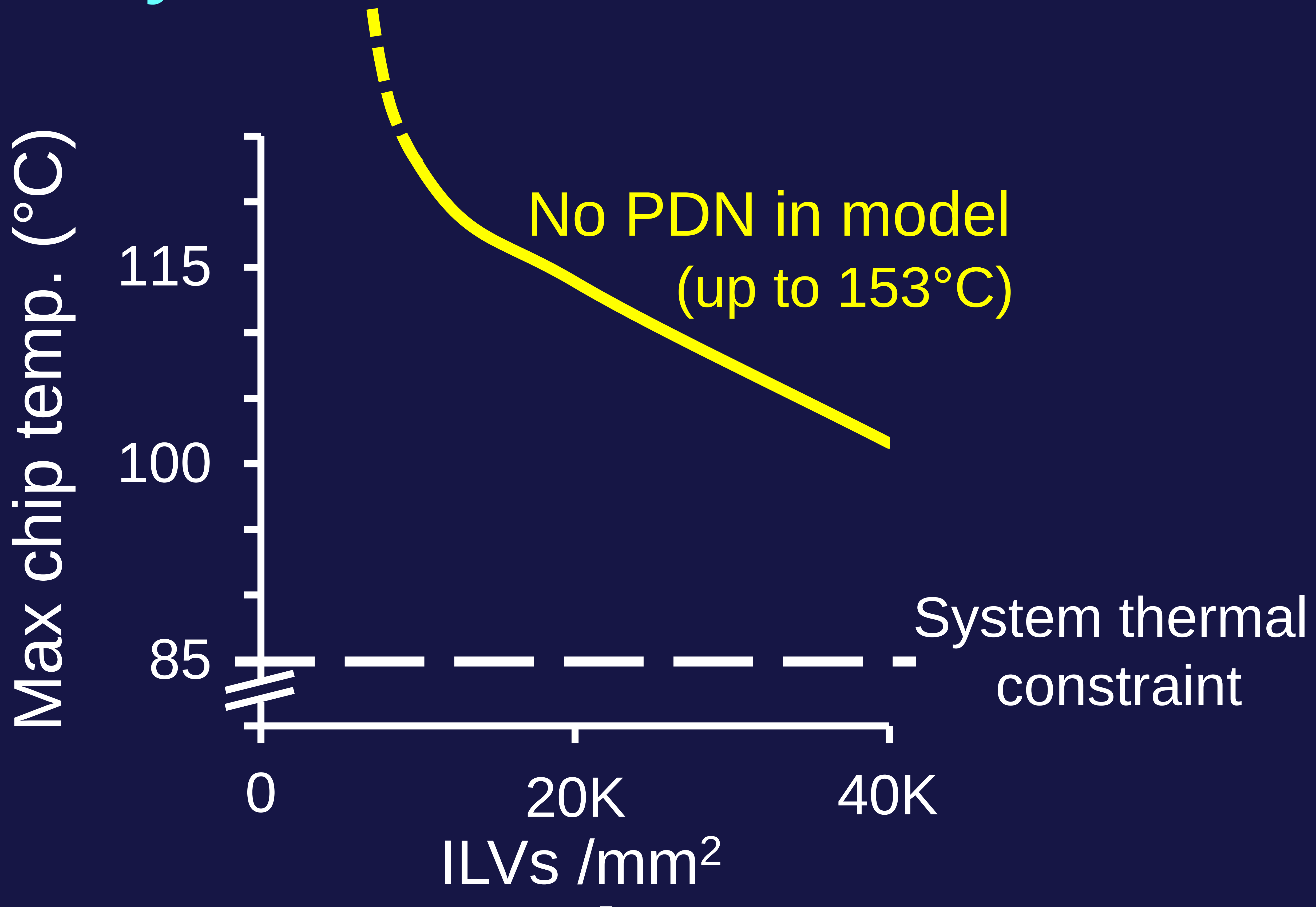

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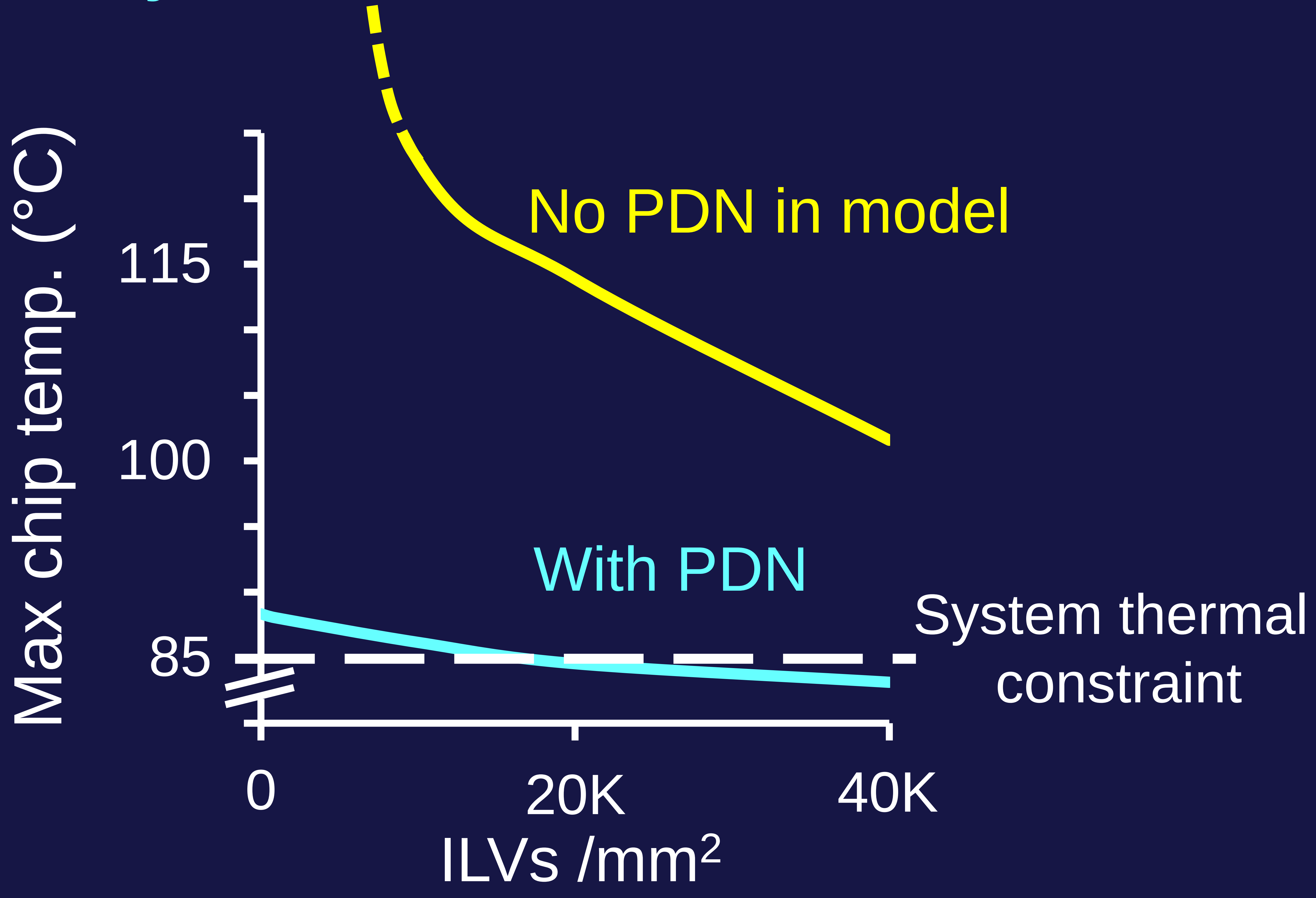

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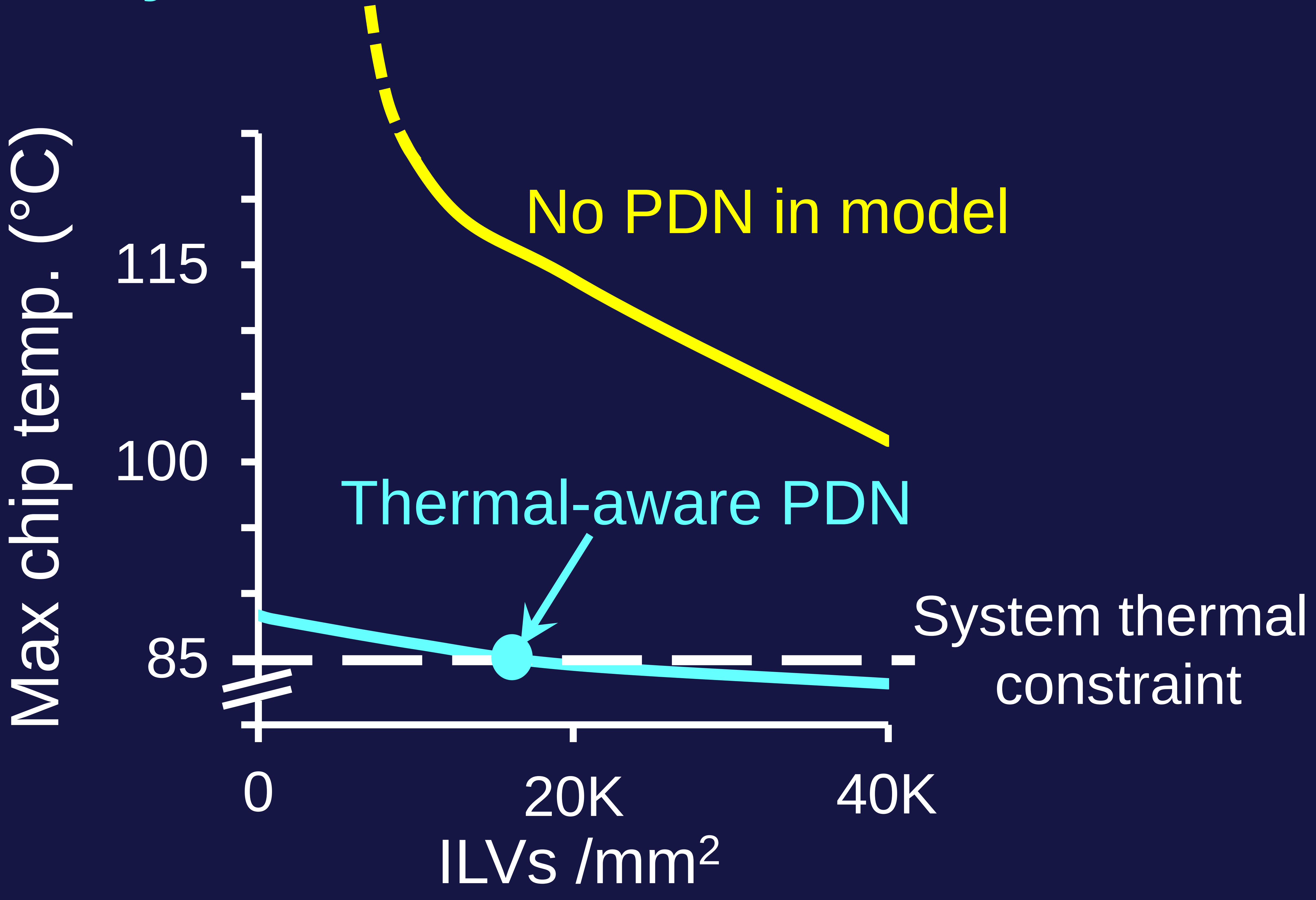
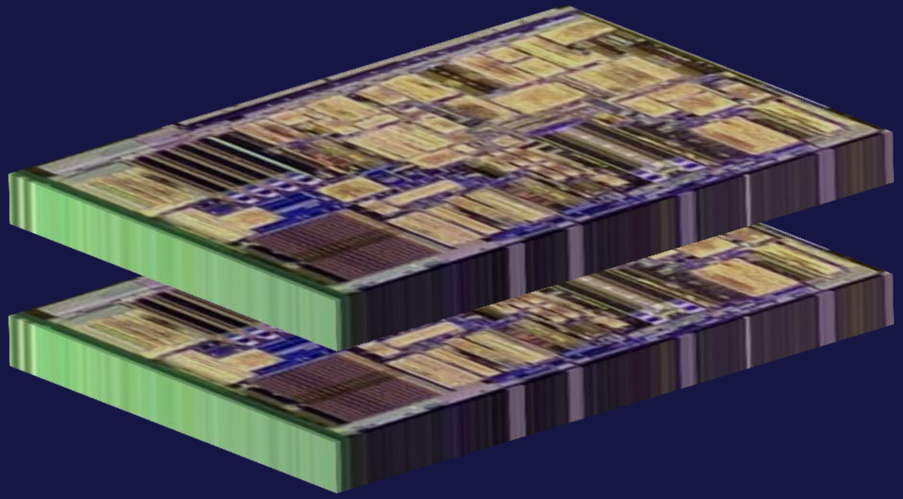


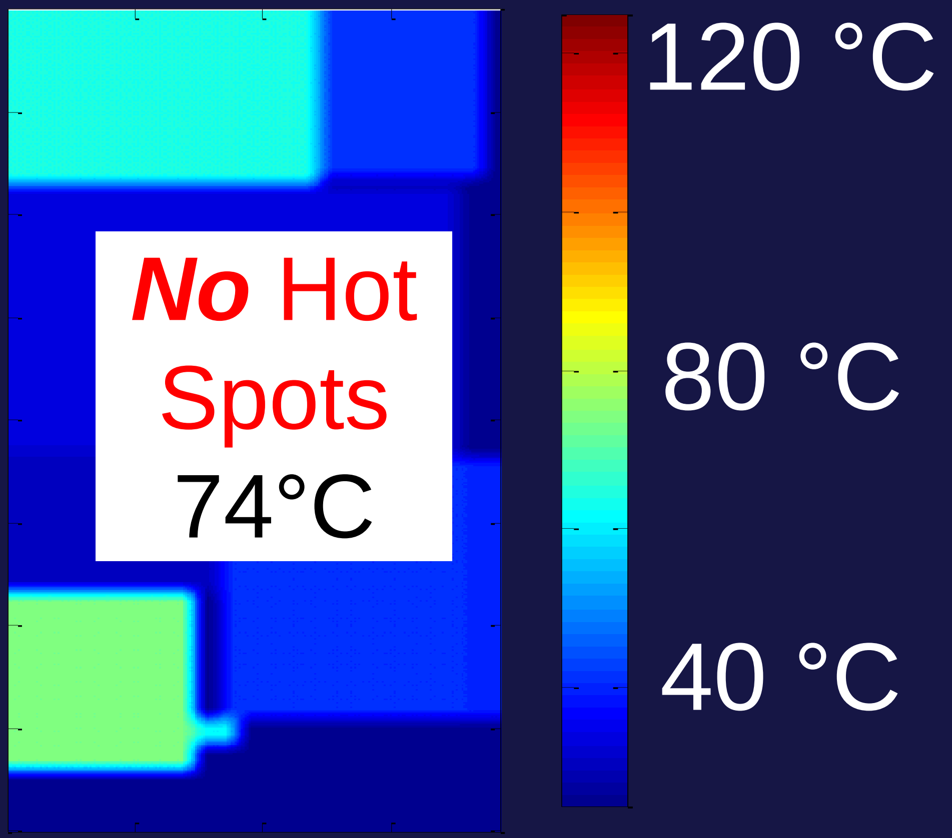
Key Result for Monolithic 3D



OpenSPARC T2 core-on-core

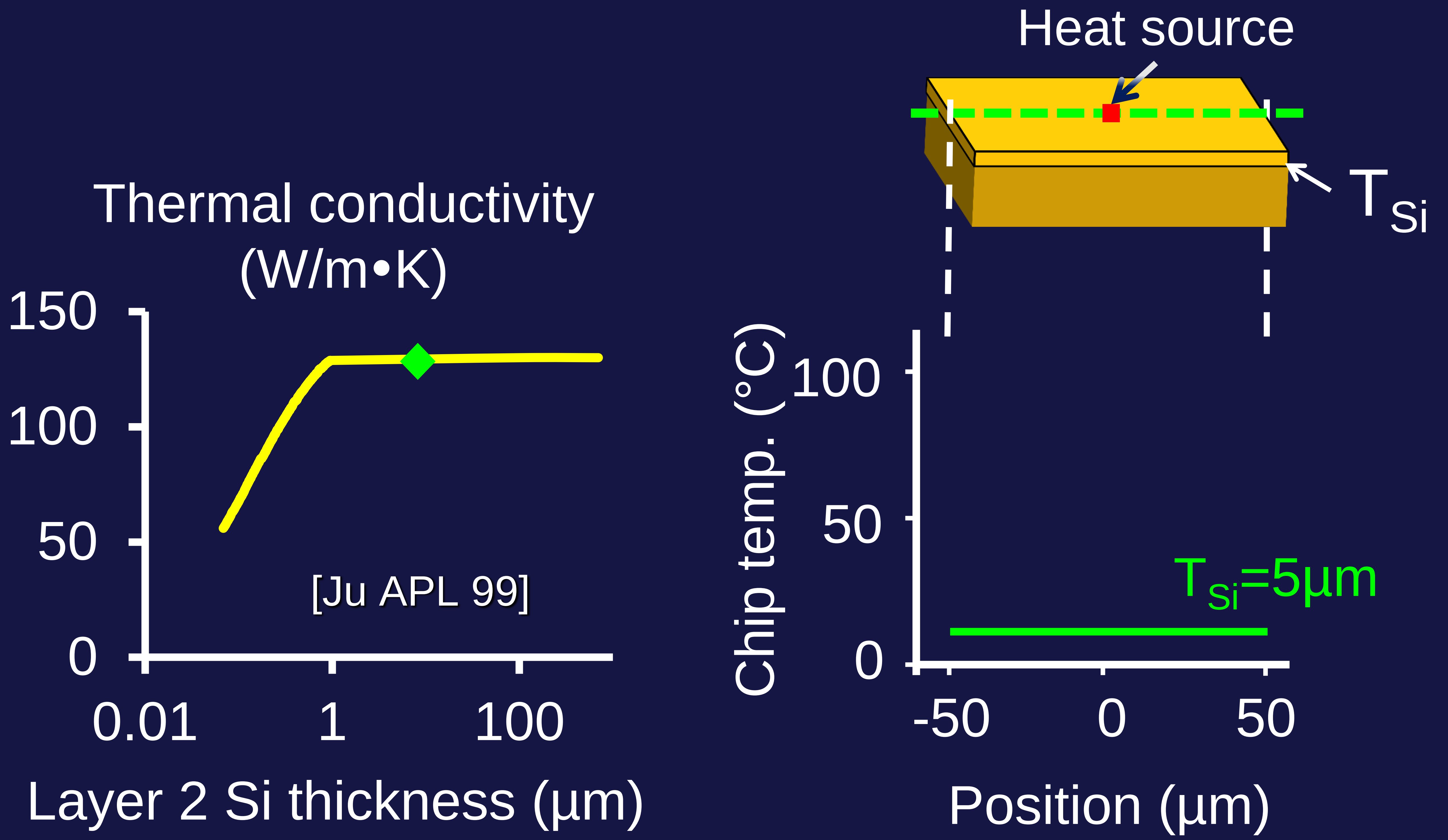
No PDN in model

Thermal-aware PDN

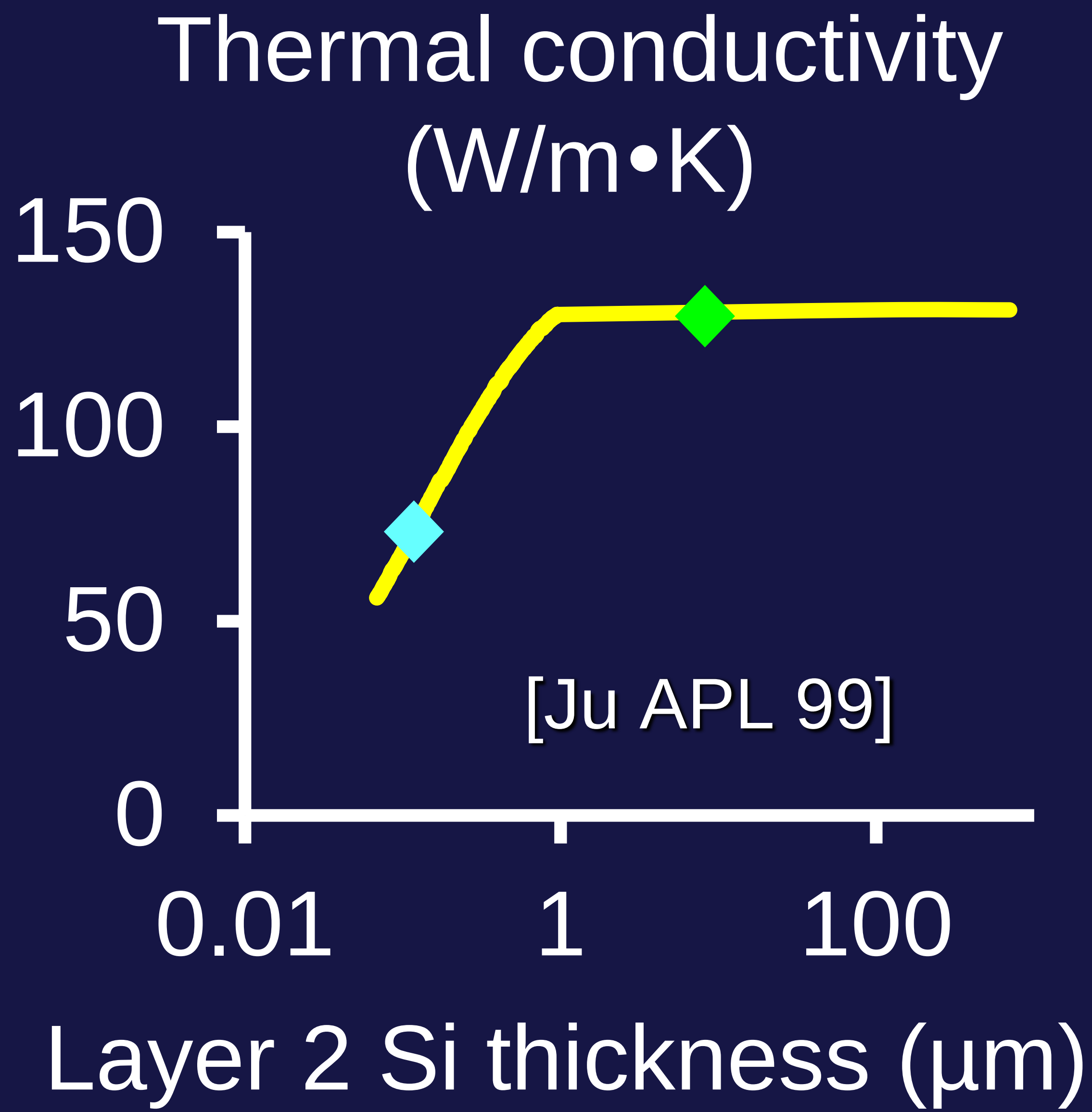


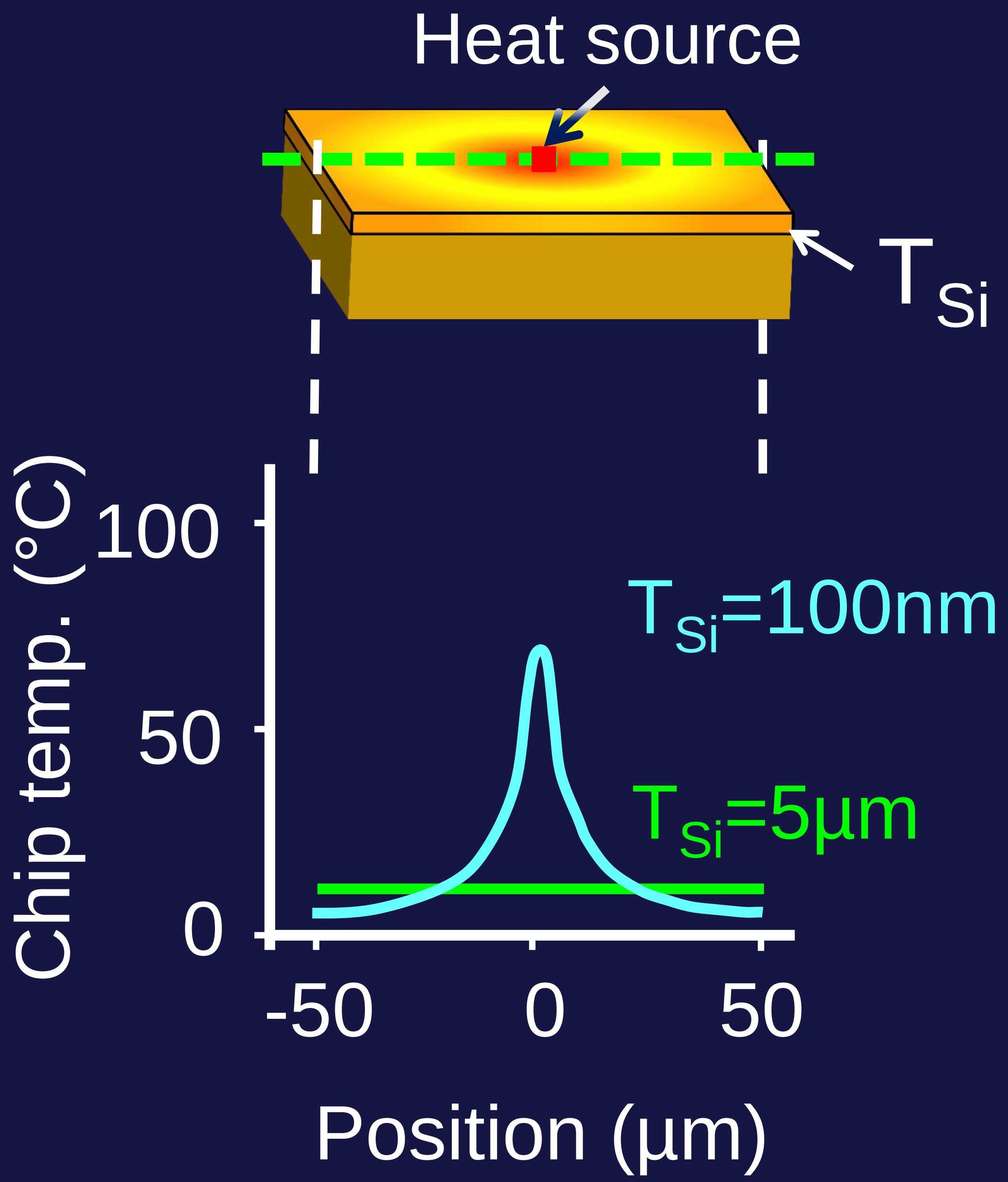
Layer 2 temp. map

Lateral Conduction Challenge



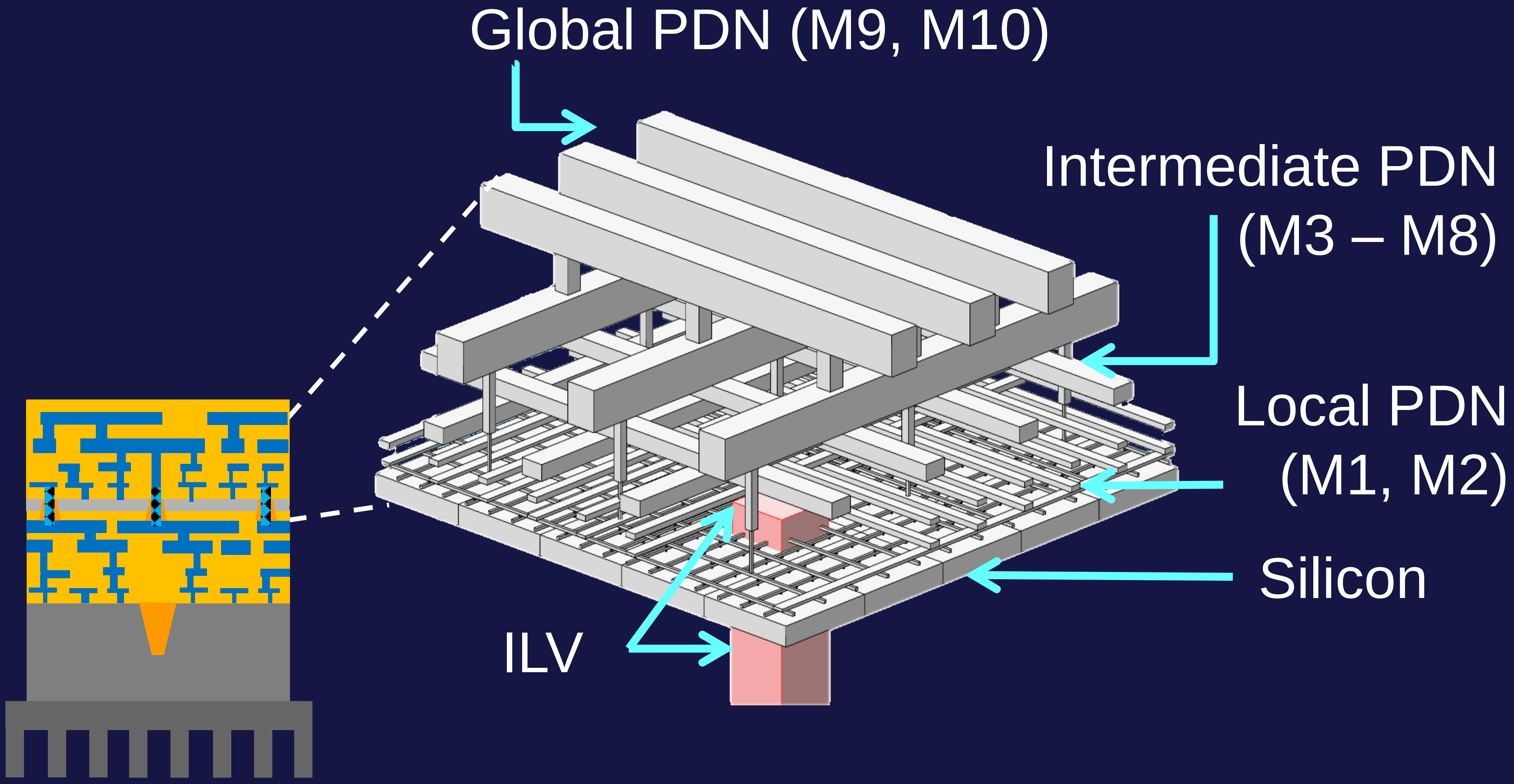
Lateral Conduction Challenge



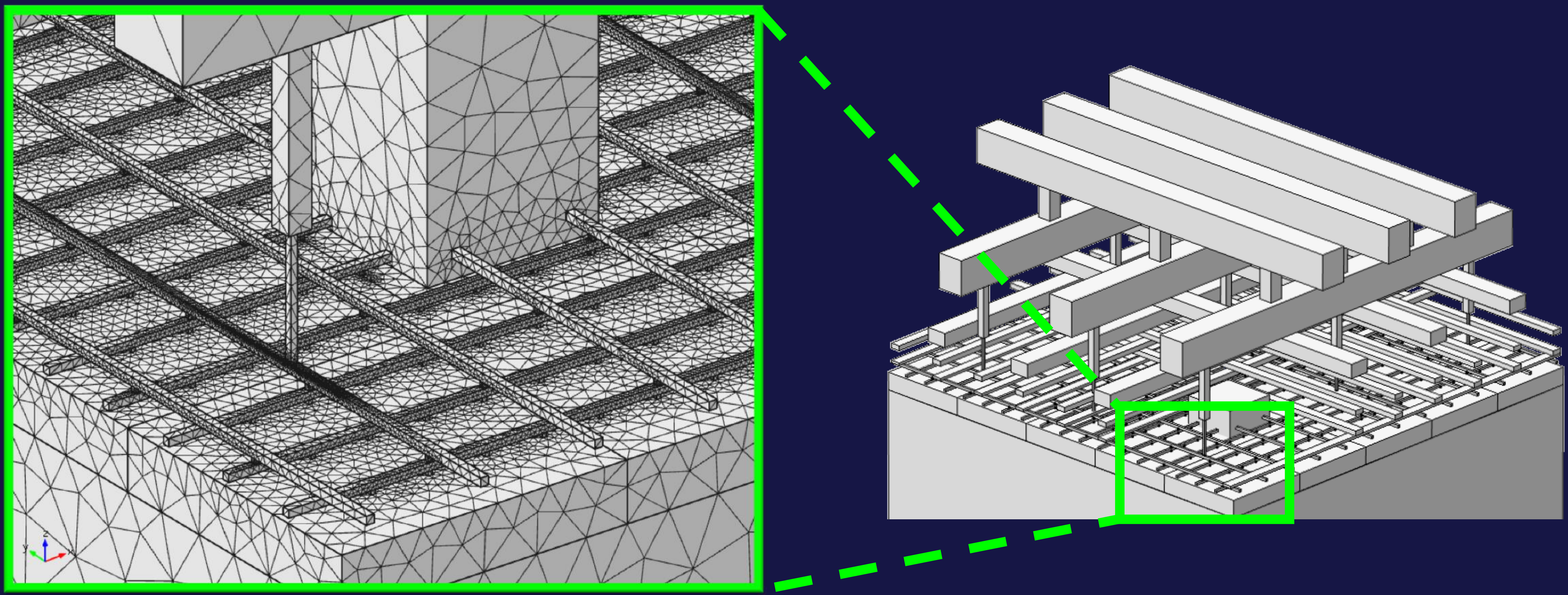


3 Grades of PDNs

- All copper



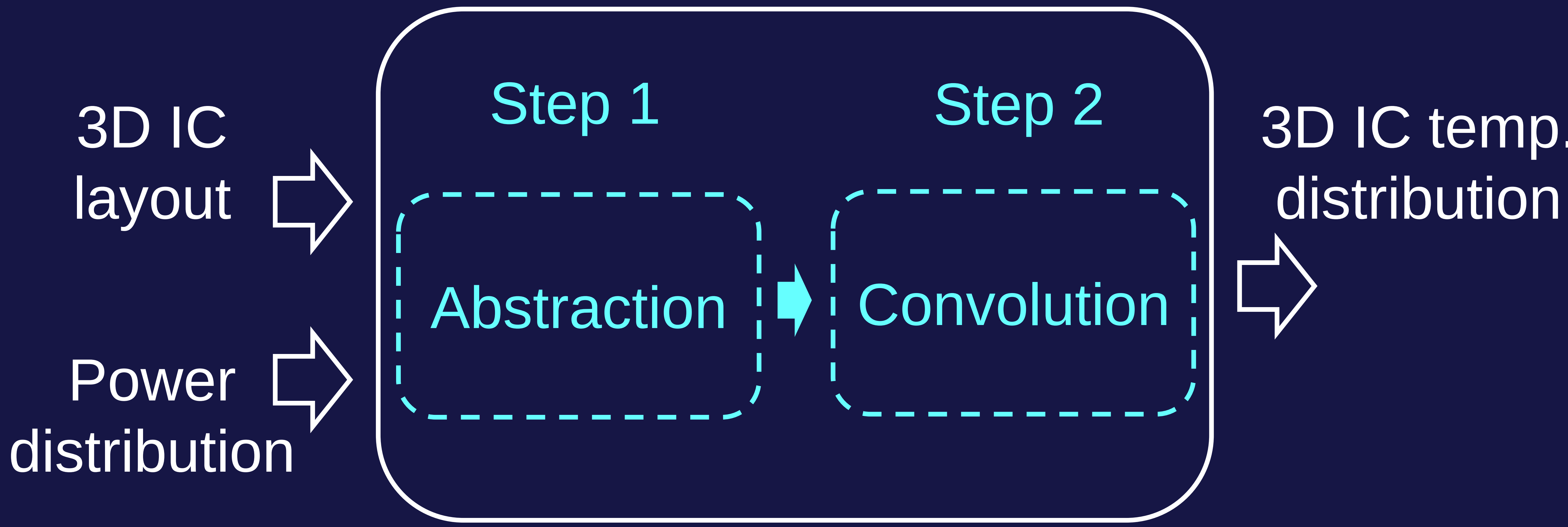
Finite Element Method



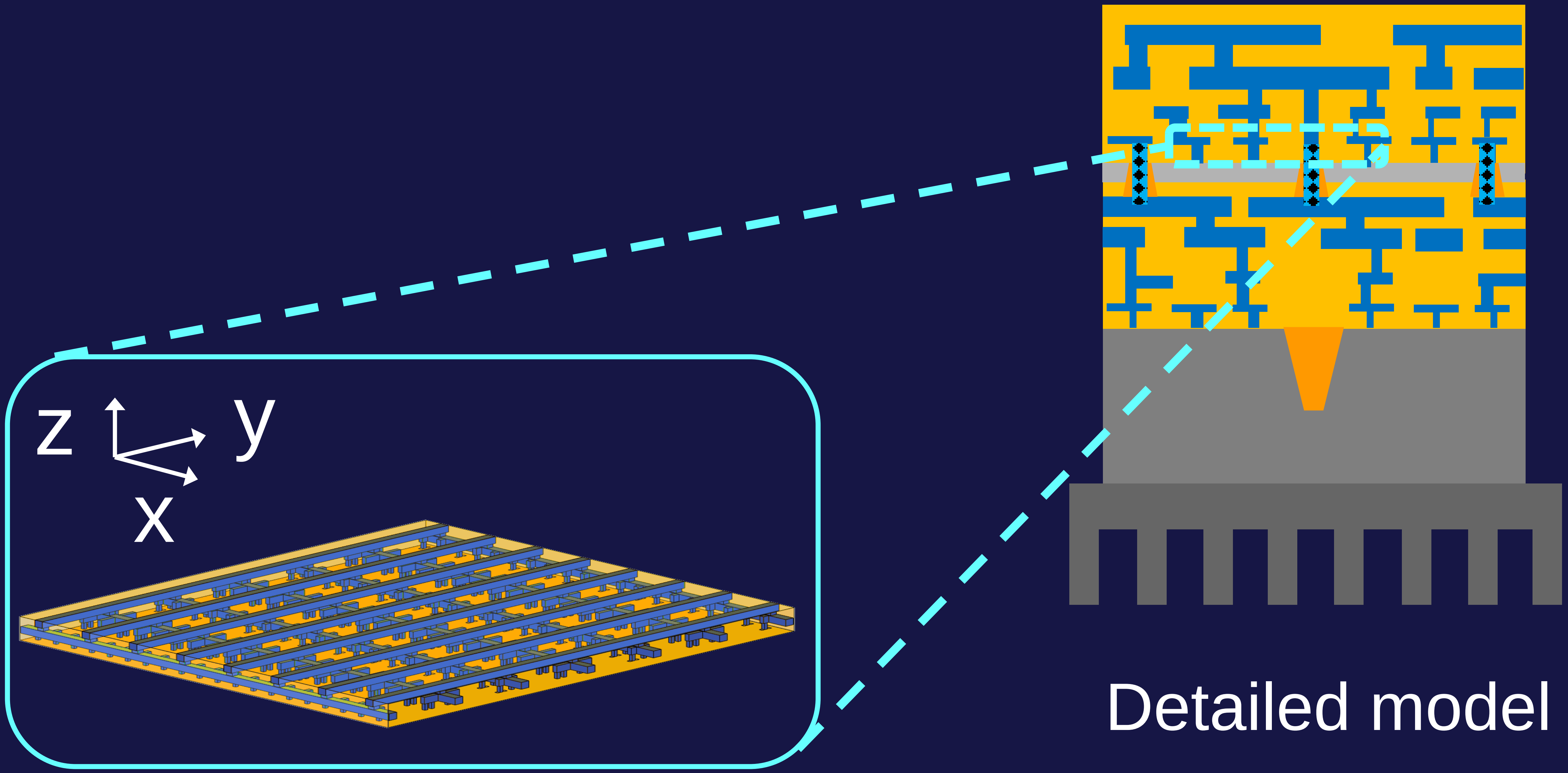
Comsol (25µm × 25µm block)
Does not complete

Our Analysis Methodology

Full chip thermal analysis



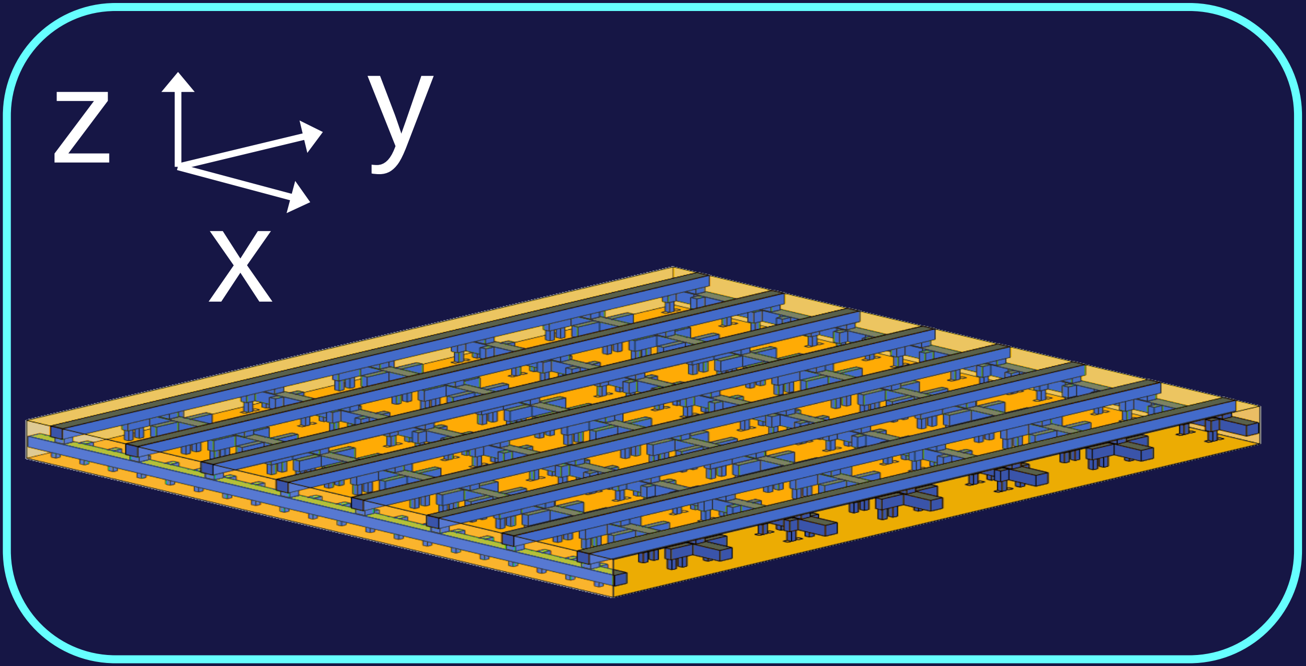
Step 1: Abstraction



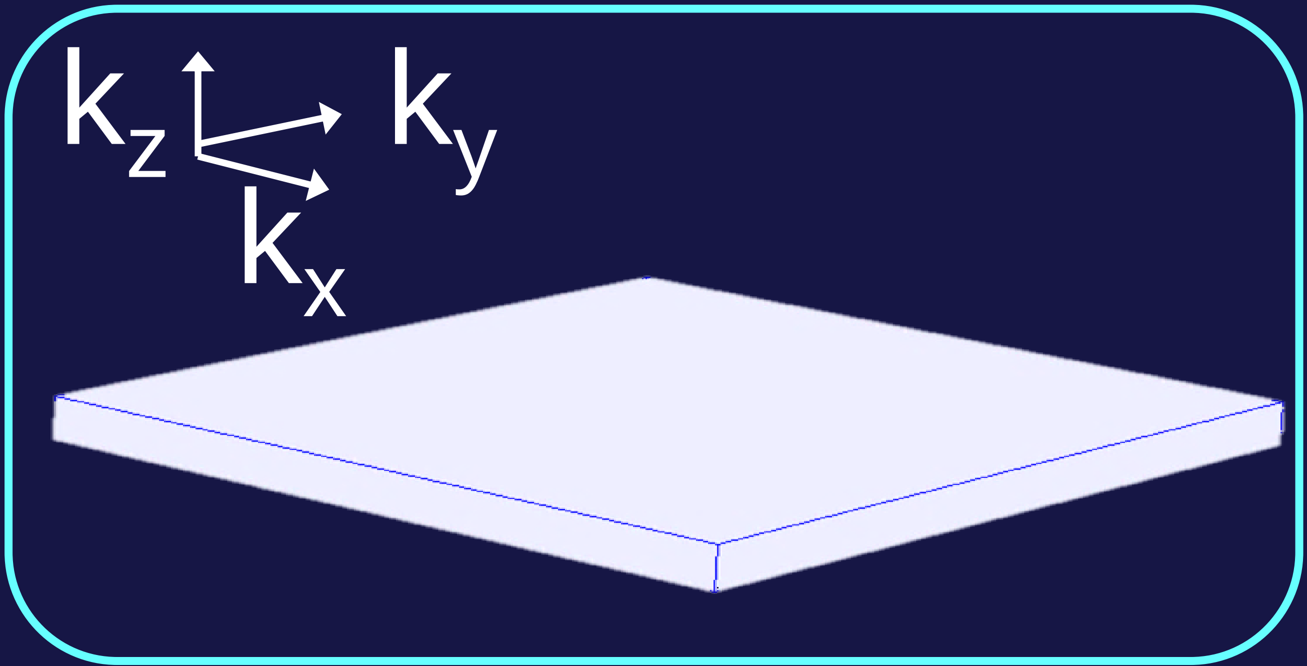
Step 1: Abstraction

- k_z = Effective thermal conductivity in z direction

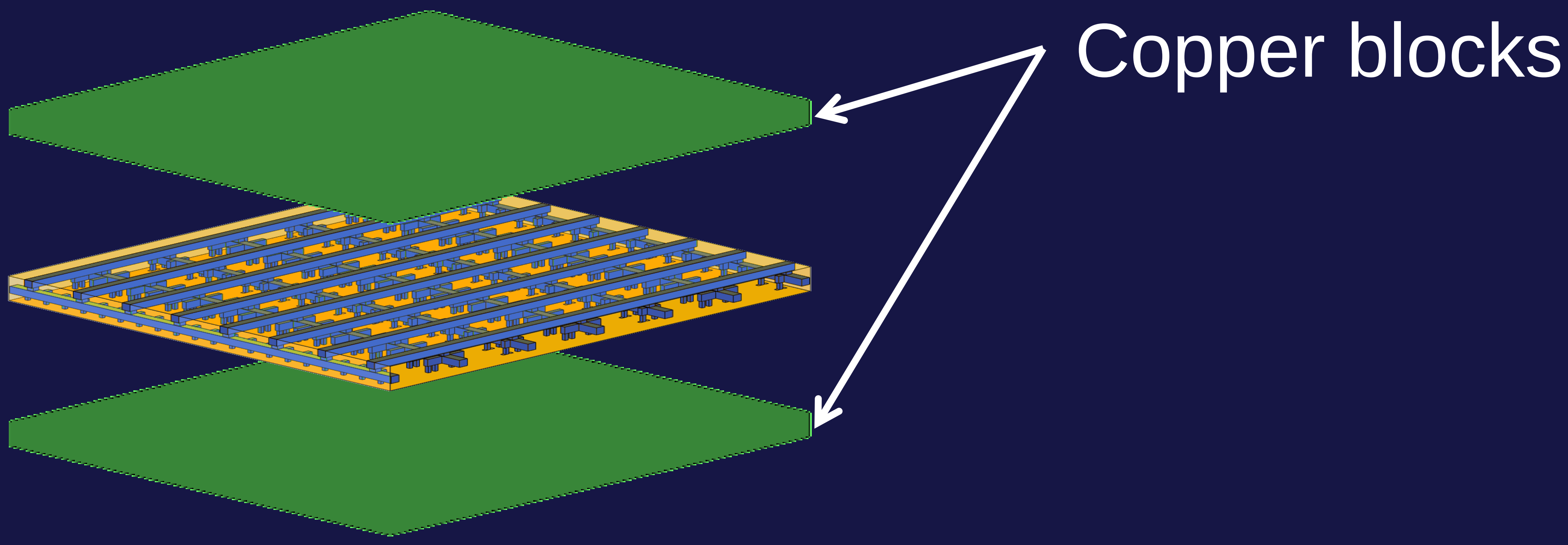
Detailed



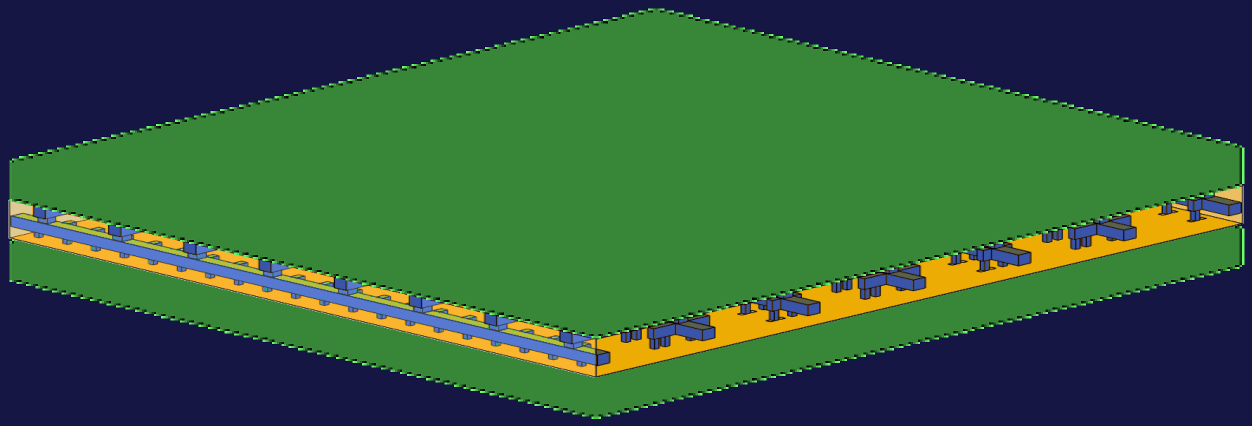
Abstract



k_z Computation



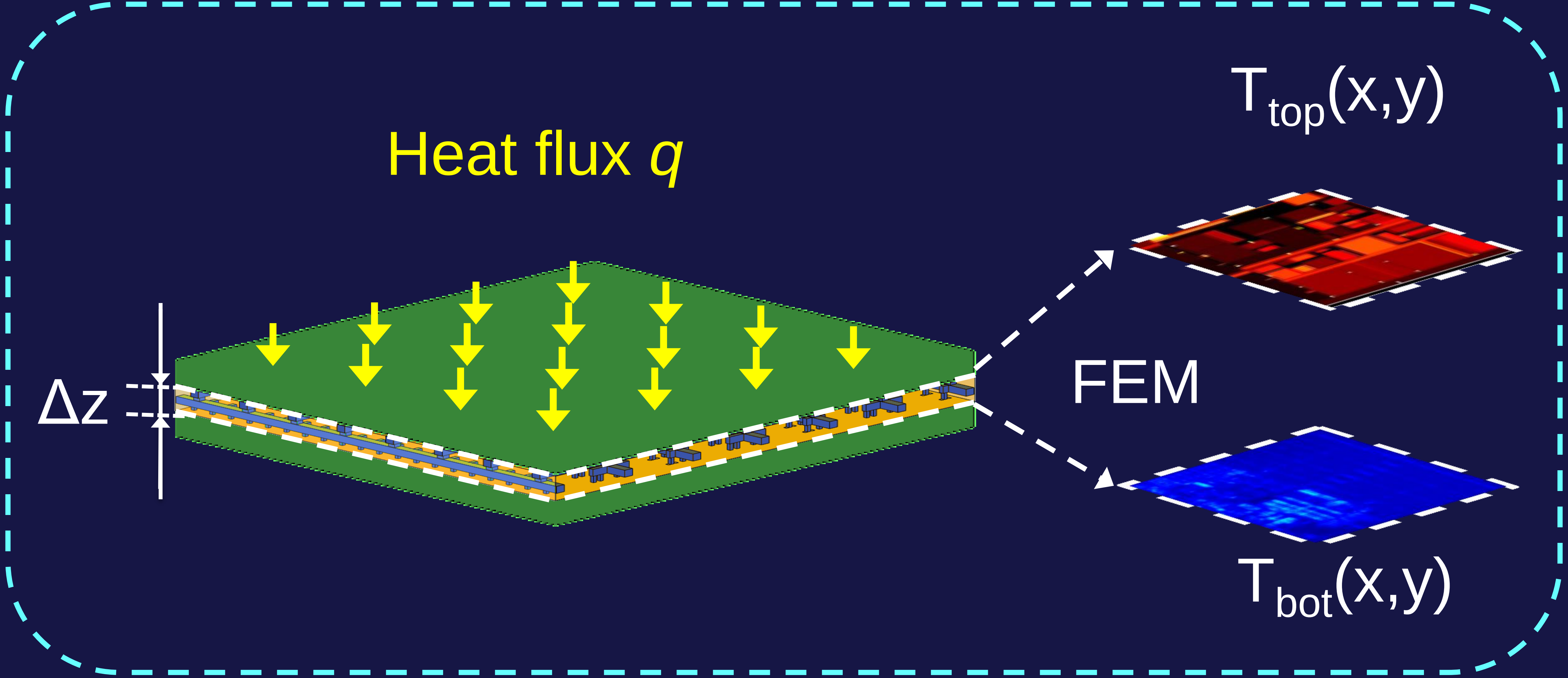
k_z Computation



k_z Computation

$$k_z = \frac{q \bullet \Delta z}{\overline{T_{top}} - \overline{T_{bot}}}$$

$\overline{X}$: mean of X



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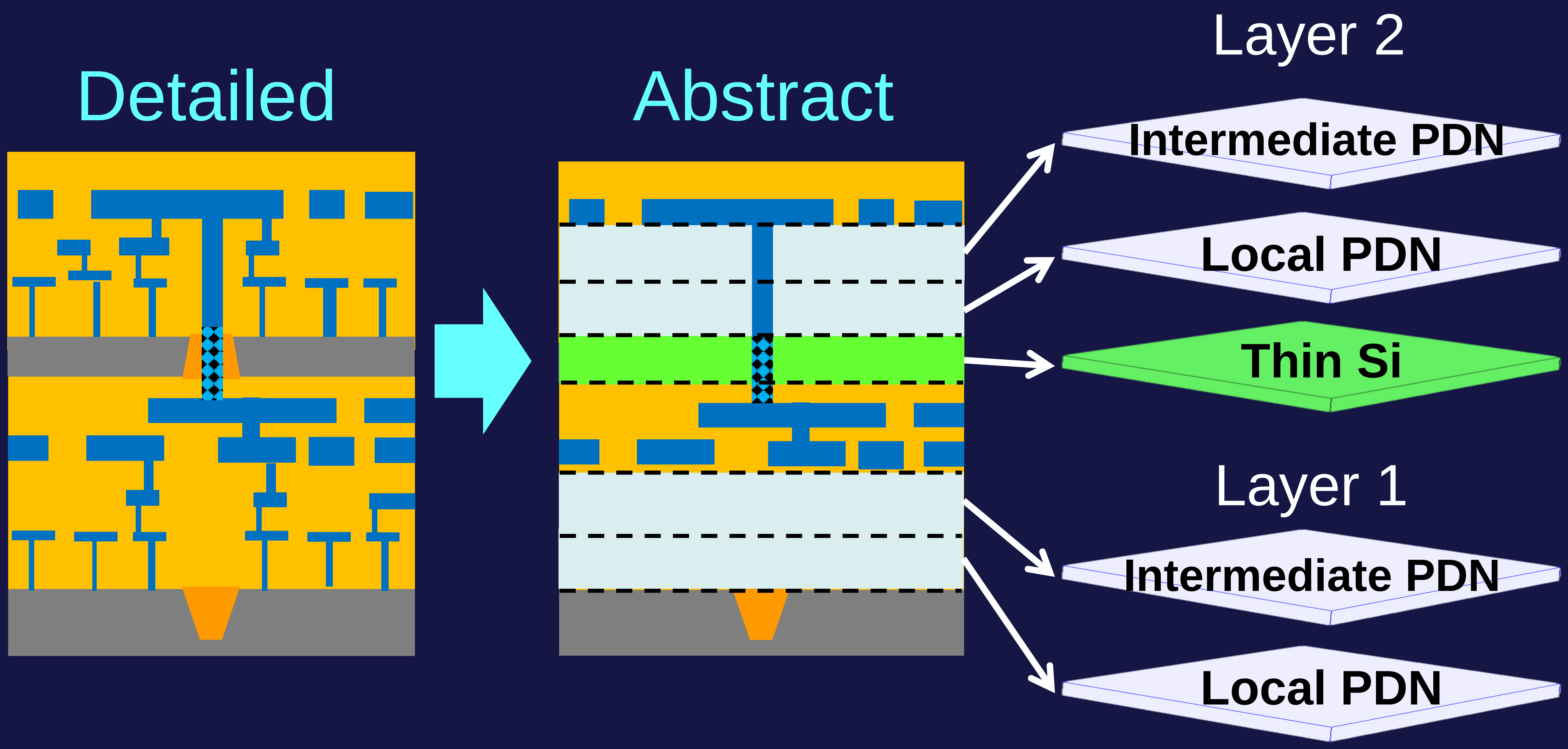


Step 2: Convolution

- 3D IC: linear system [Kemper THERMINIC 06]

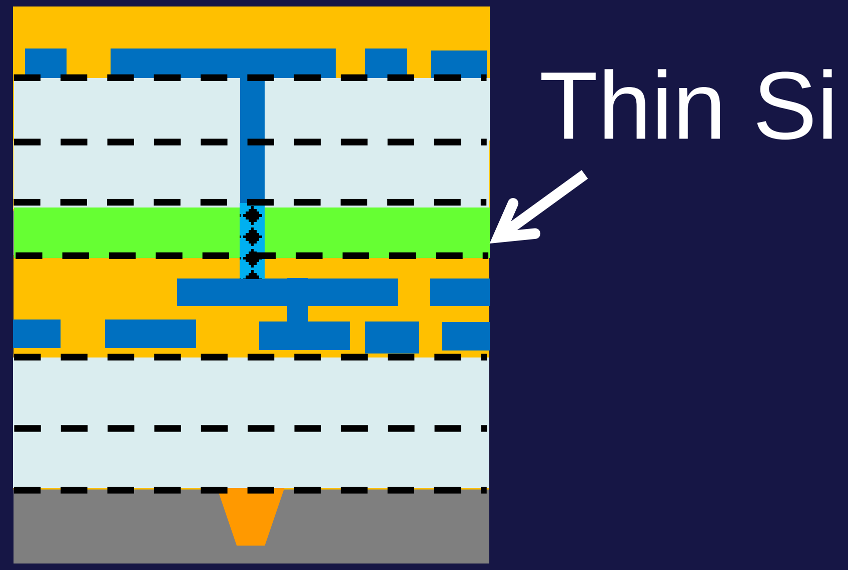
Step 2: Convolution

Power distribution

Impulse response

→ Convolution → Temp. distribution

Abstract



Step 2: Convolution

Power distribution

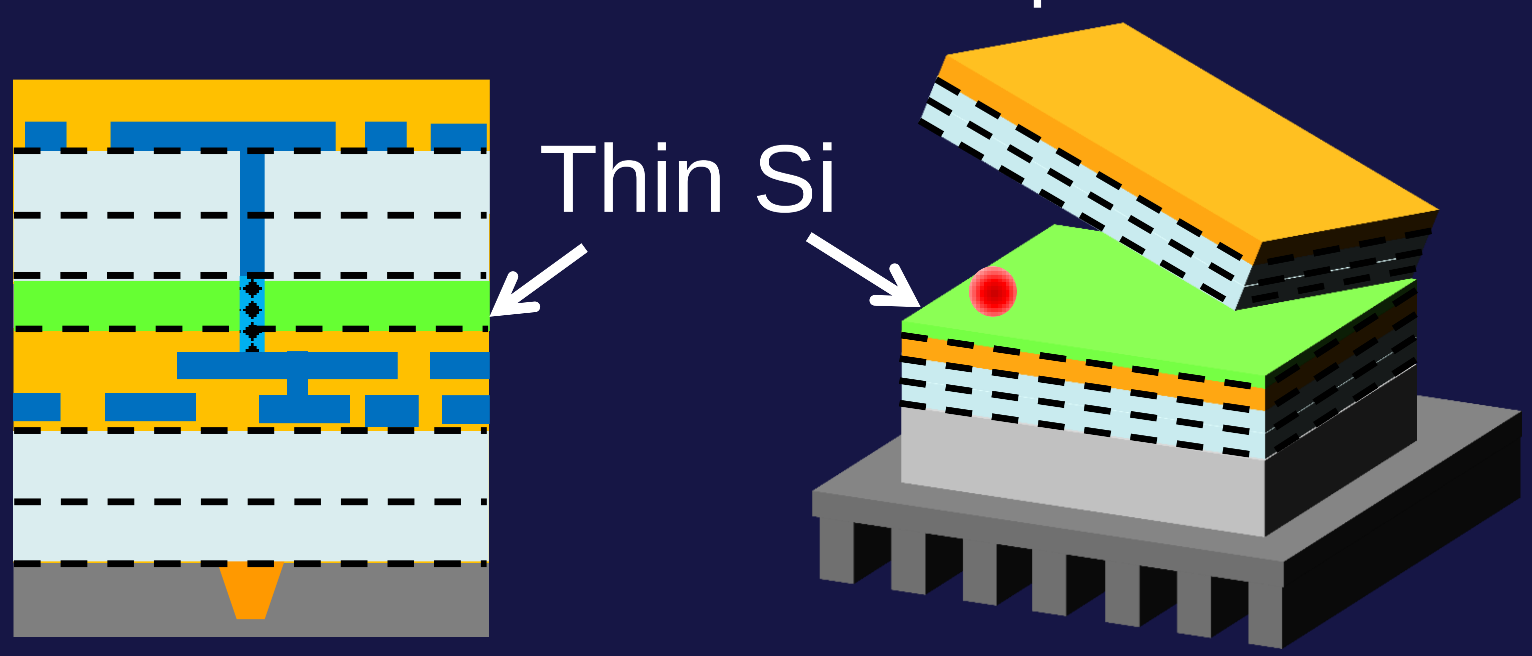
Impulse response

Convolution

Temp. distribution

Abstract

Impulse heat flux



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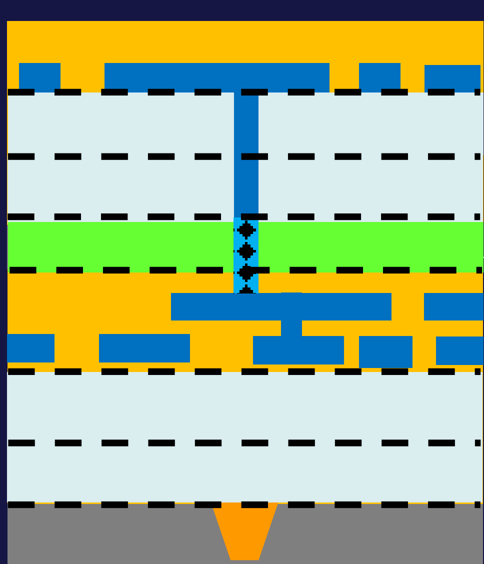
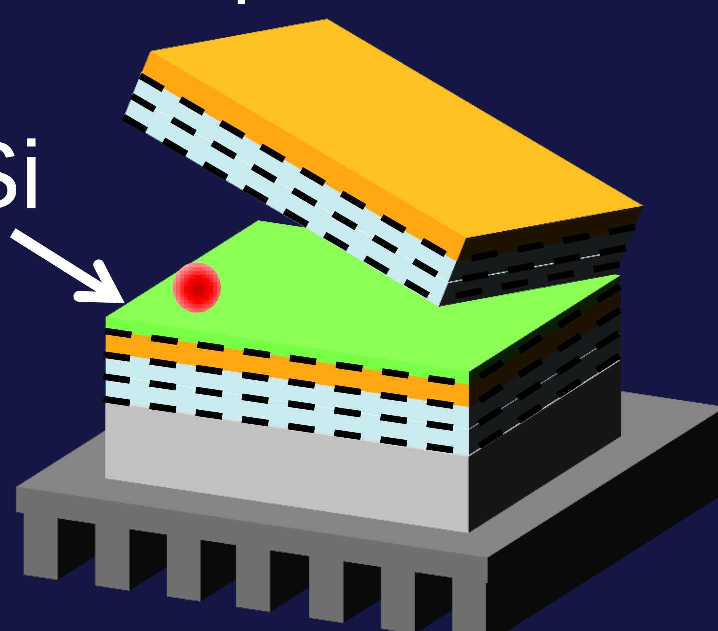


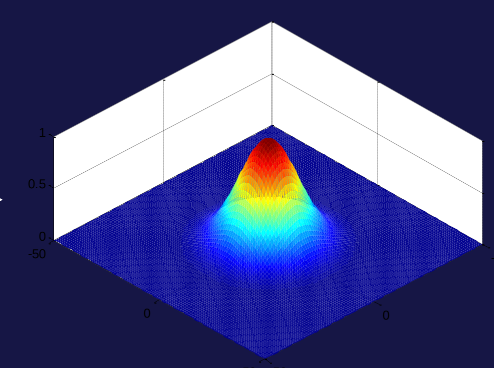
Thin Si

Impulse heat flux



FEM

Thermal response



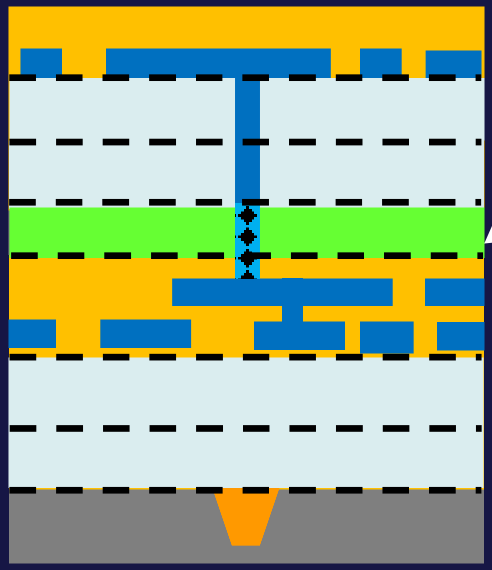
Step 2: Convolution

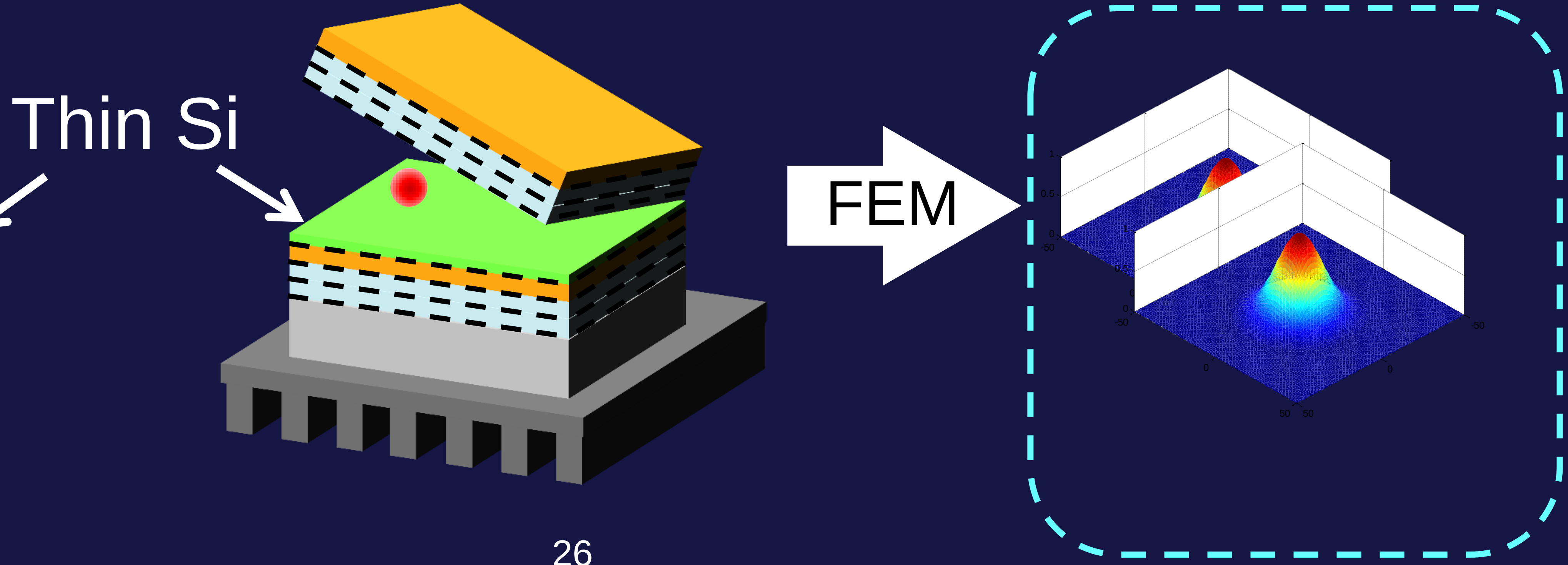
Power distribution

Impulse response

→ Convolution → Temp. distribution

Abstract



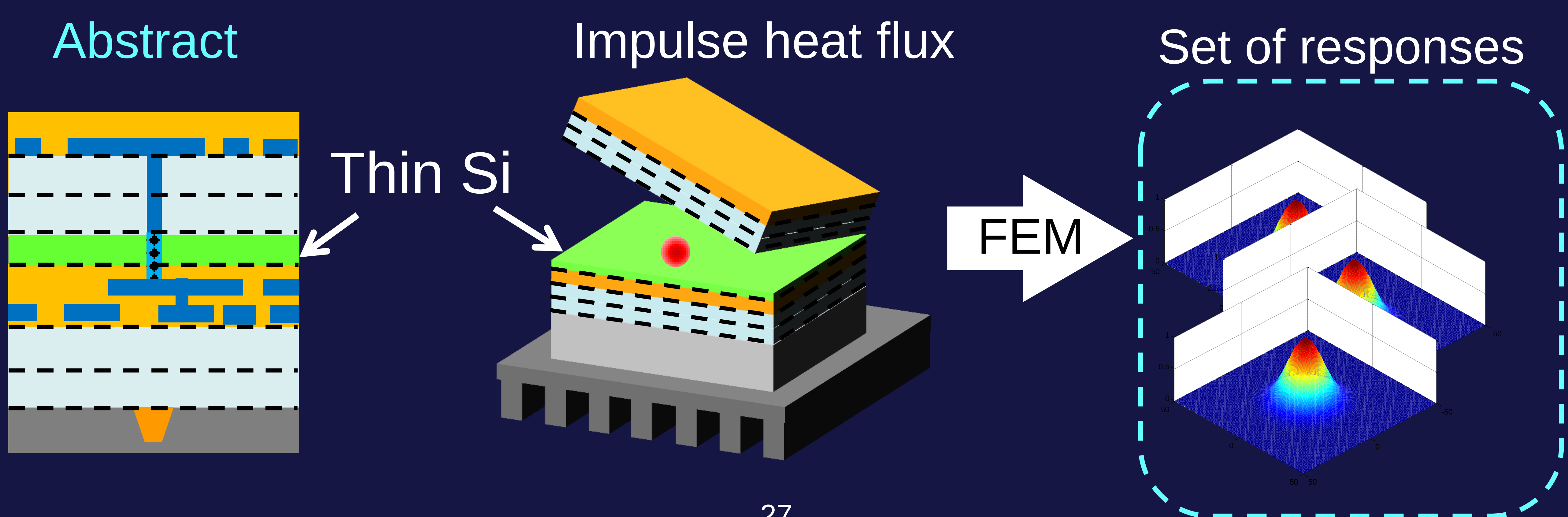


Step 2: Convolution

Power distribution

Impulse response

→ Convolution → Temp. distribution



Step 2: Convolution

Power distribution

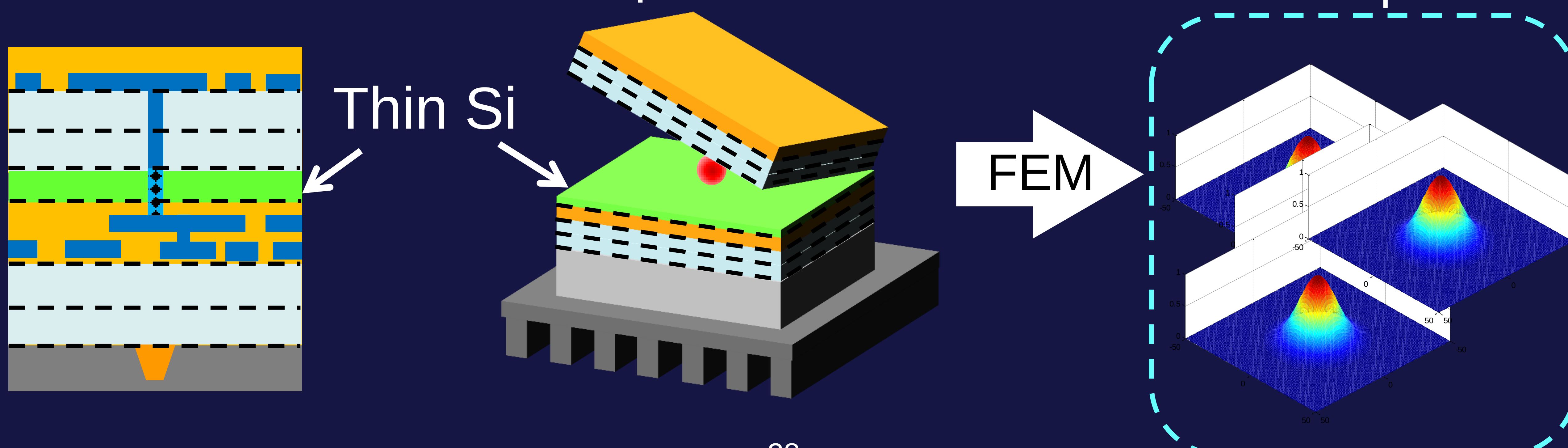
Impulse response

→ Convolution → Temp. distribution

Abstract

Impulse heat flux

Set of responses



Step 2: Convolution

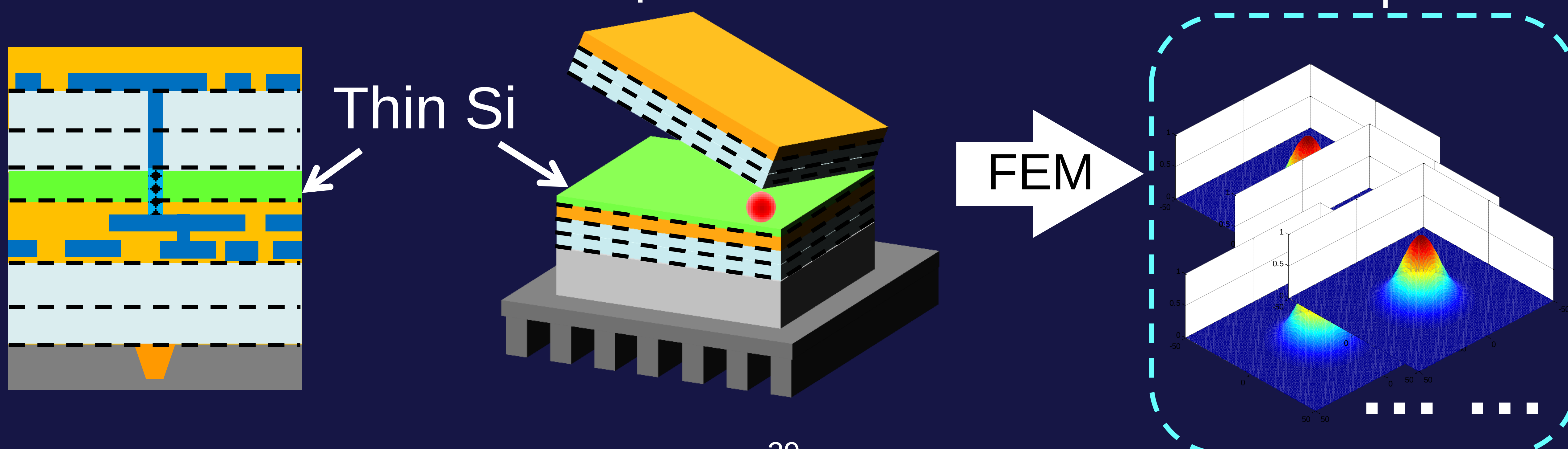
Power distribution → Convolution → Temp. distribution

Impulse response → Convolution

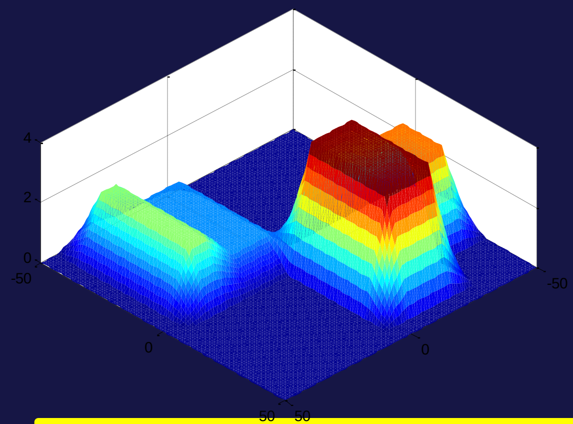
Abstract

Impulse heat flux

Set of responses



Step 2: Convolution



Power dissipation in thin Si layer
(Commercial tools)

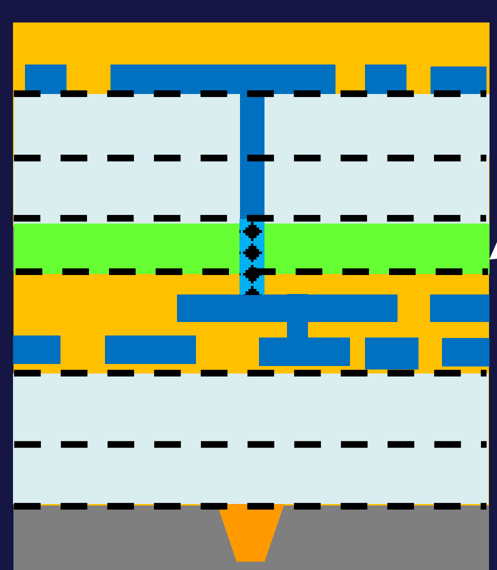
Power distribution

Impulse response

Convolution

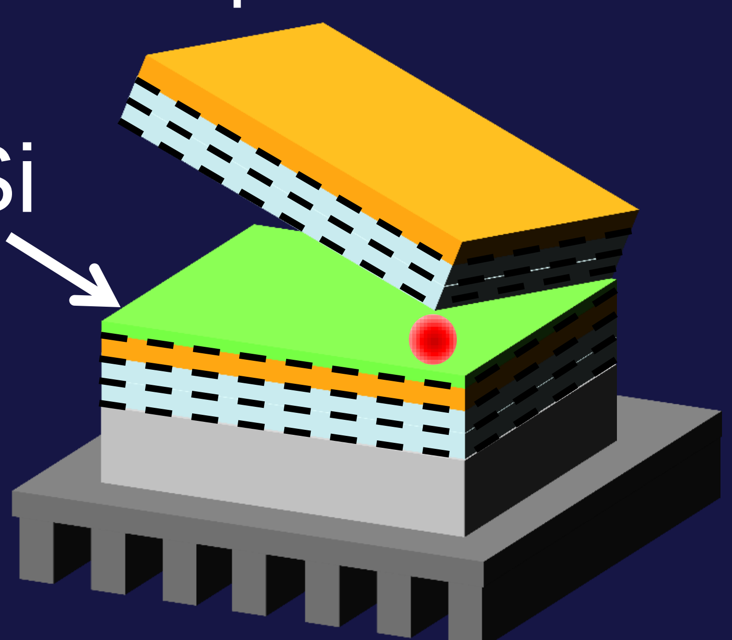
Temp. distribution

Abstract



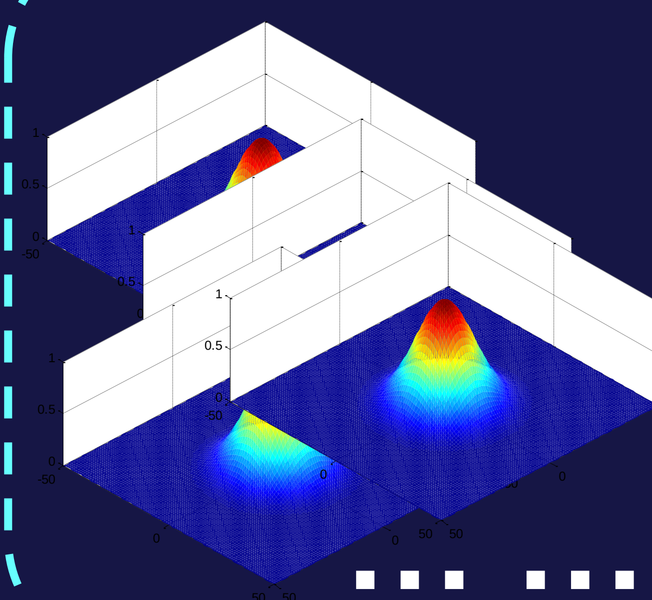
Thin Si

Impulse heat flux

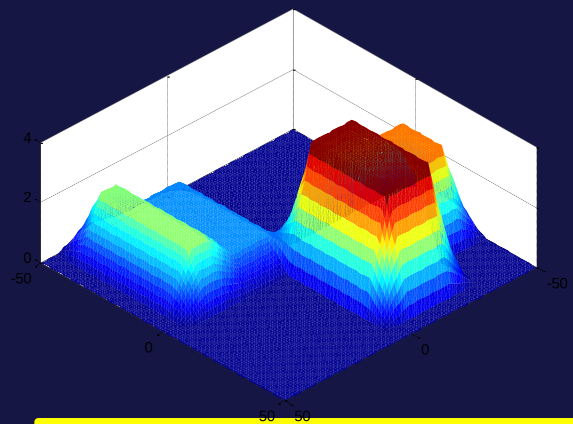


FEM

Set of responses



Step 2: Convolution



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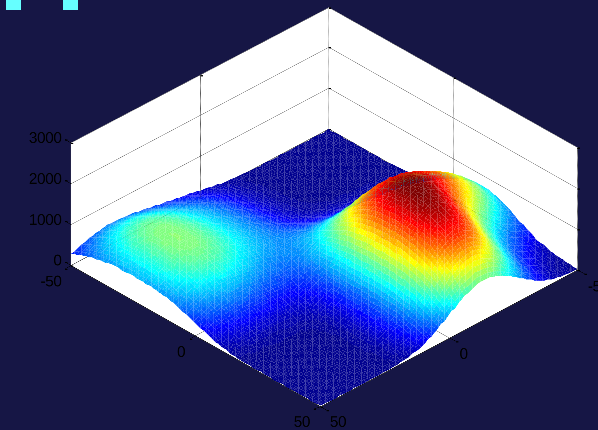


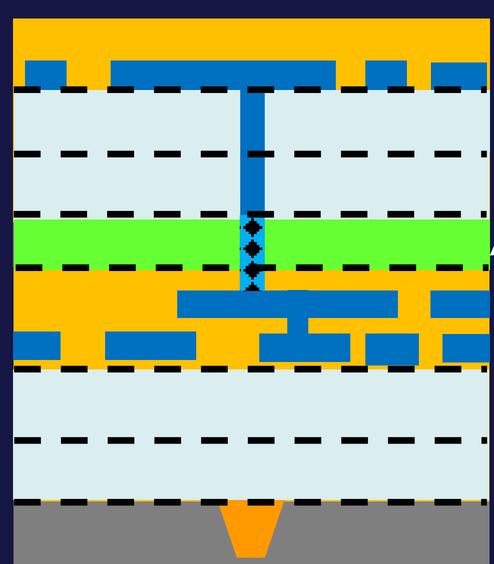
Power distribution

Impulse response

Convolution

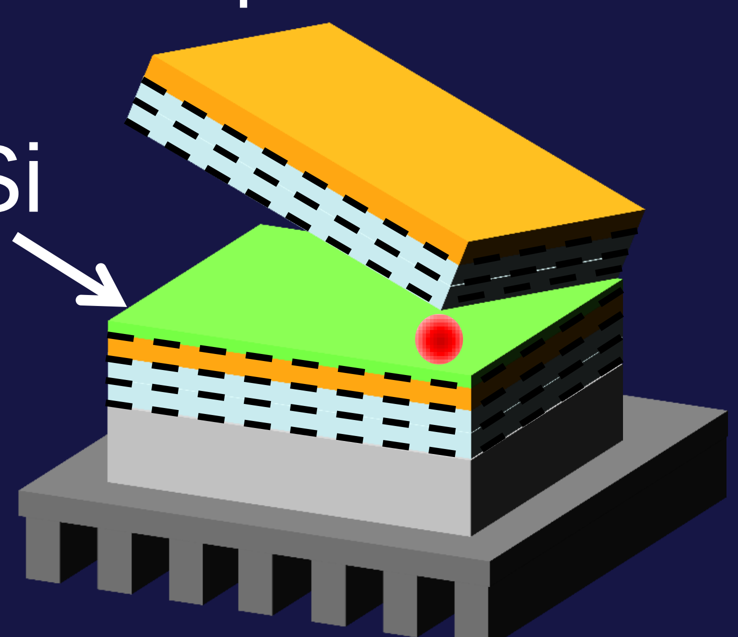
Temp. distribution

Abstract



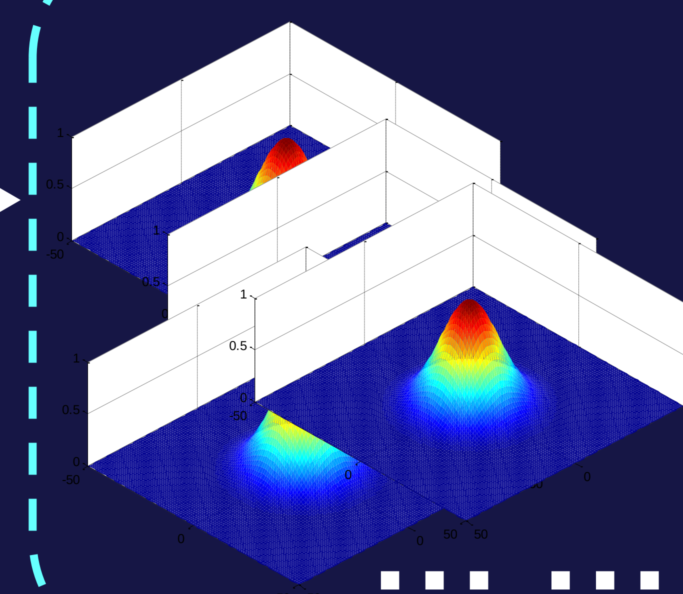
Thin Si

Impulse heat flux



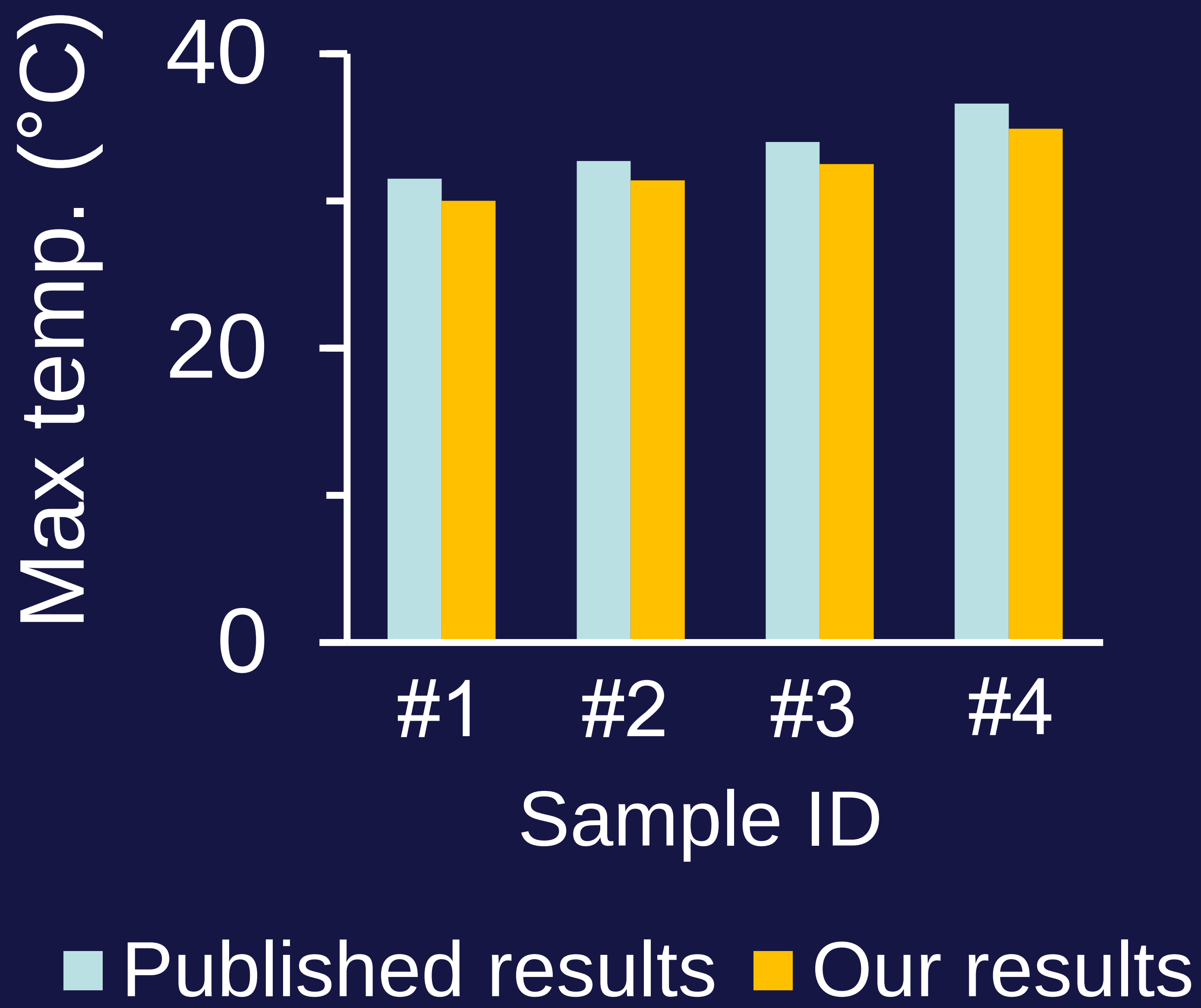
FEM

Set of responses

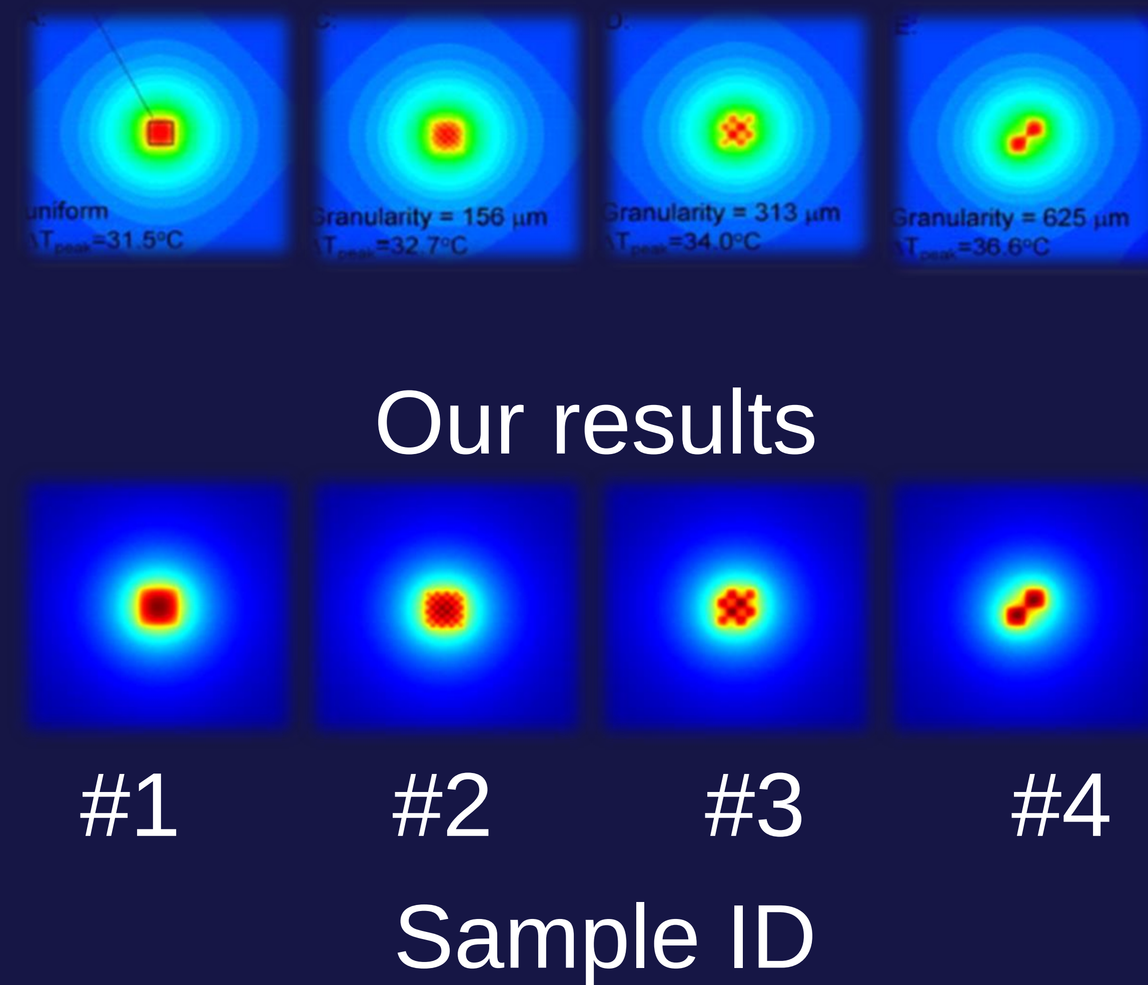


Model Verification

Relative error: 2-5%

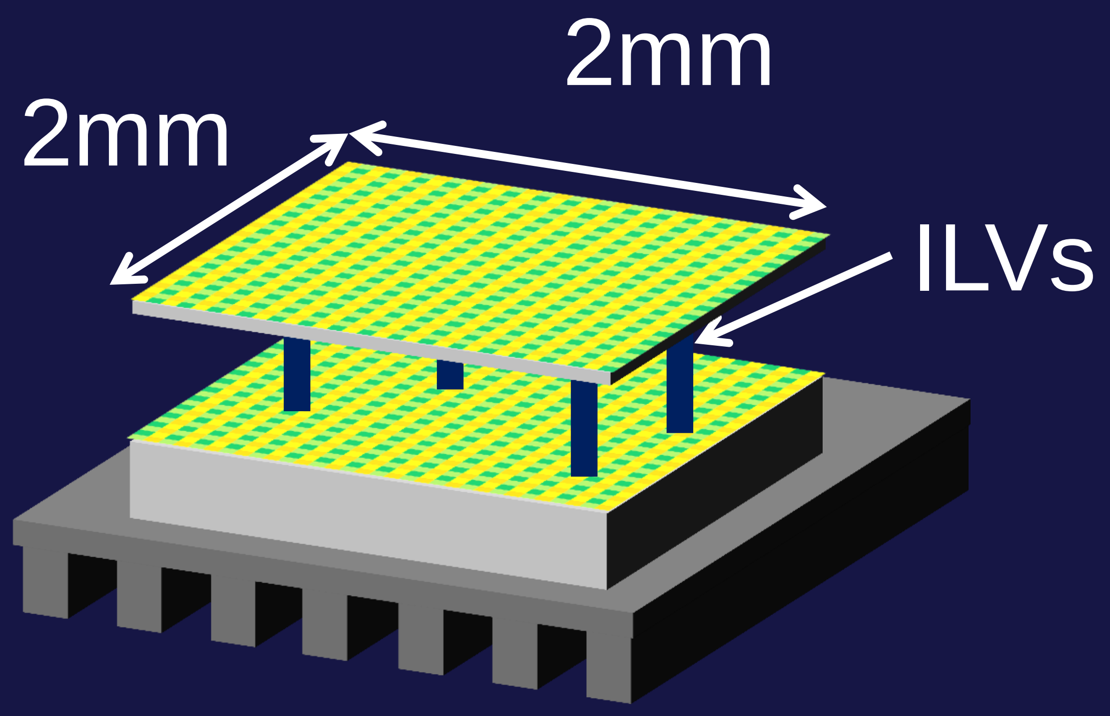


Published results
[Etessam-Yazdani ICPES 06]



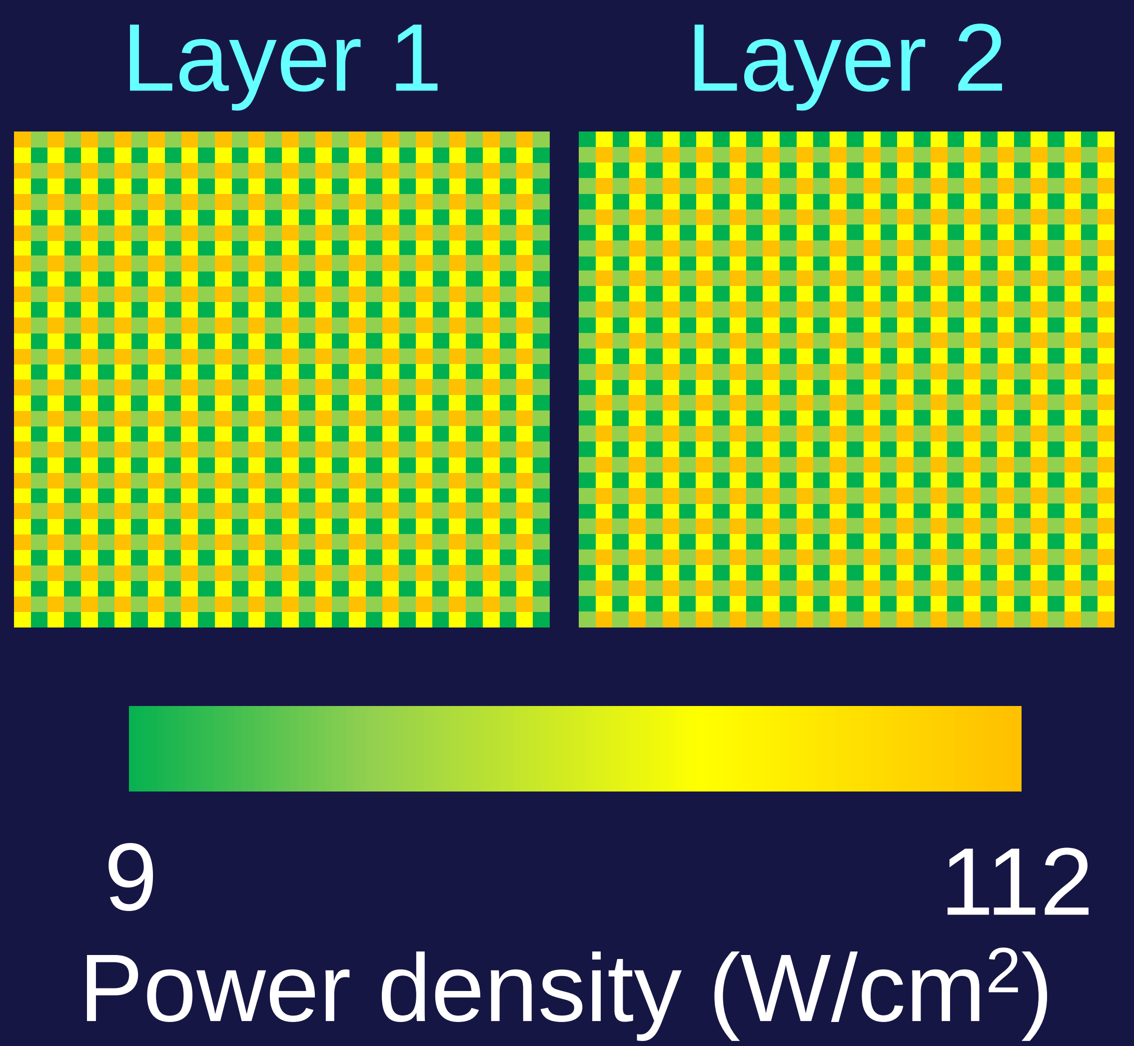
Thermal Analysis: Example 1

- Average: 50 W/cm^2 per layer



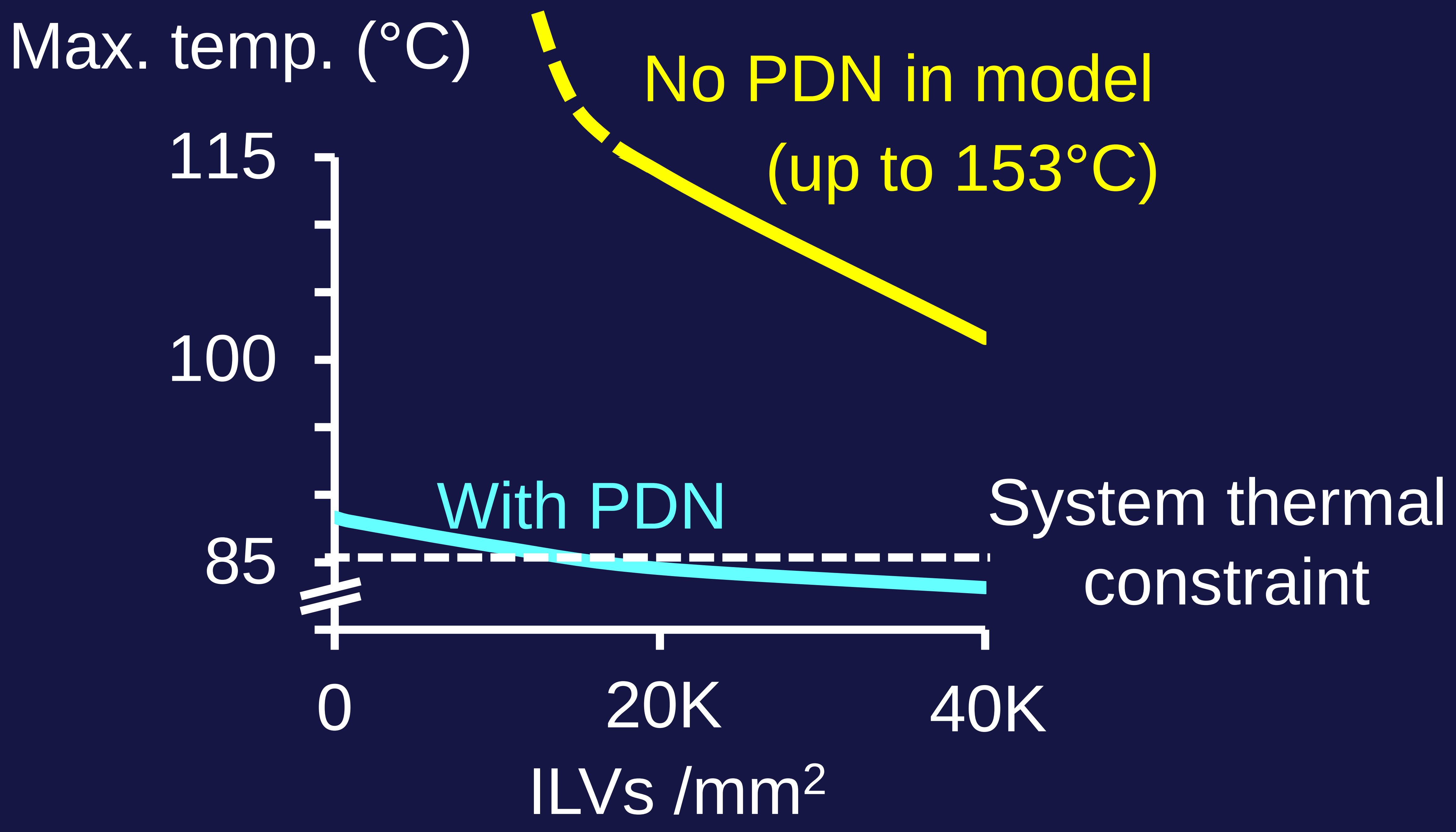
Air cooling: 2 W/K·cm^2

Power distribution map



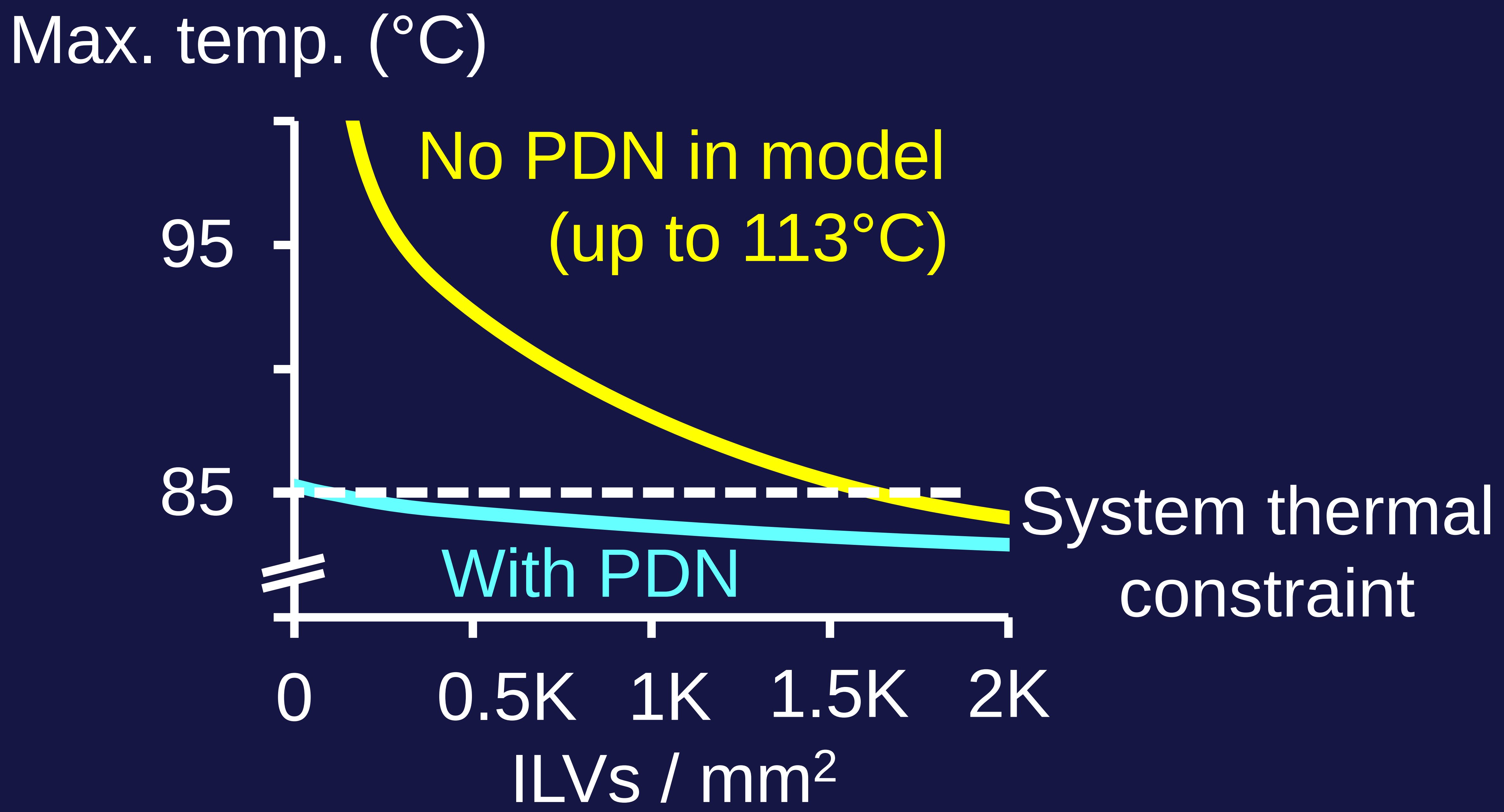
Example 1 Results

- Monolithic 3D IC: big temperature benefit



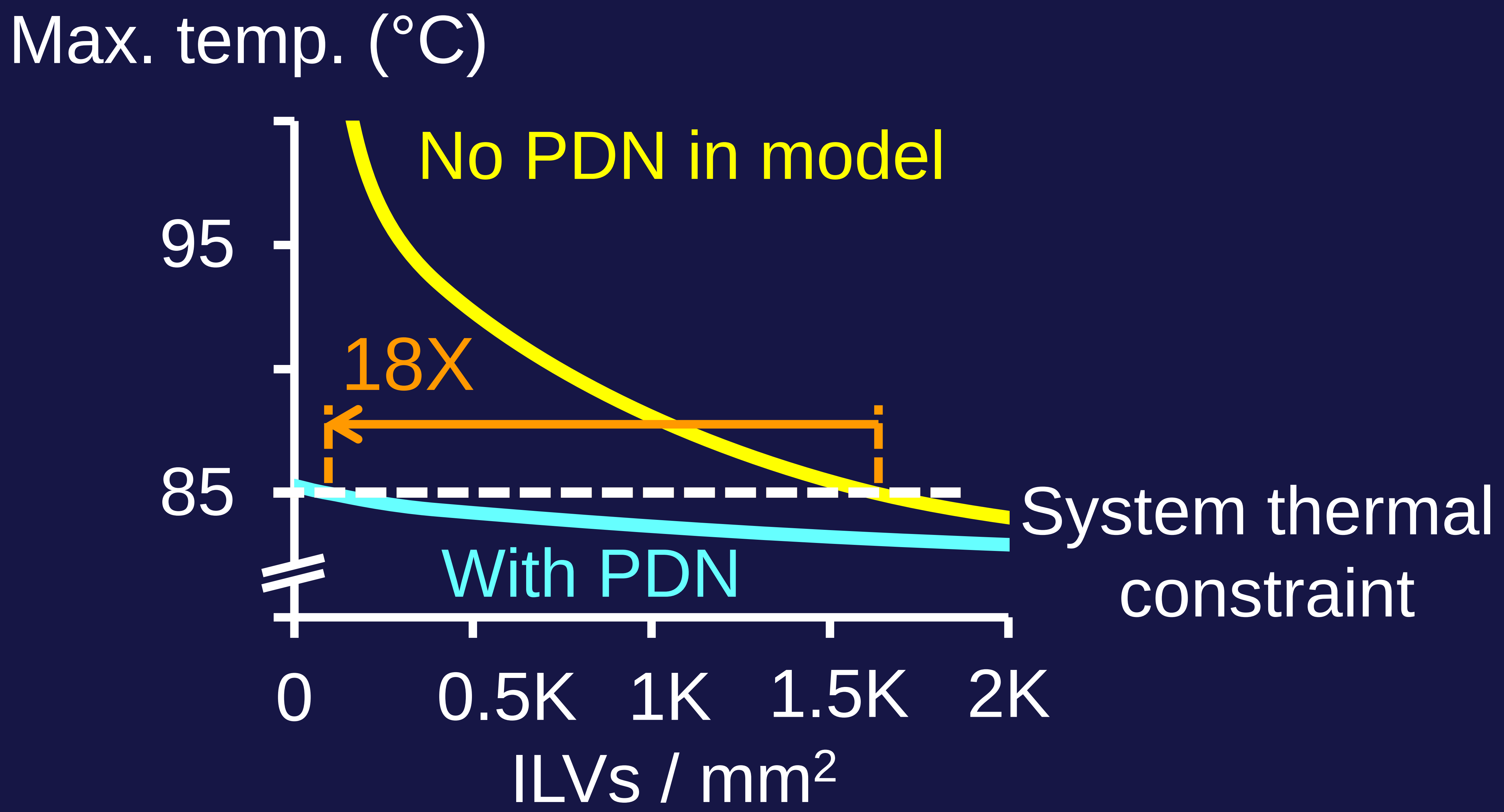
Example 1 Results

- Parallel 3D IC: area benefit



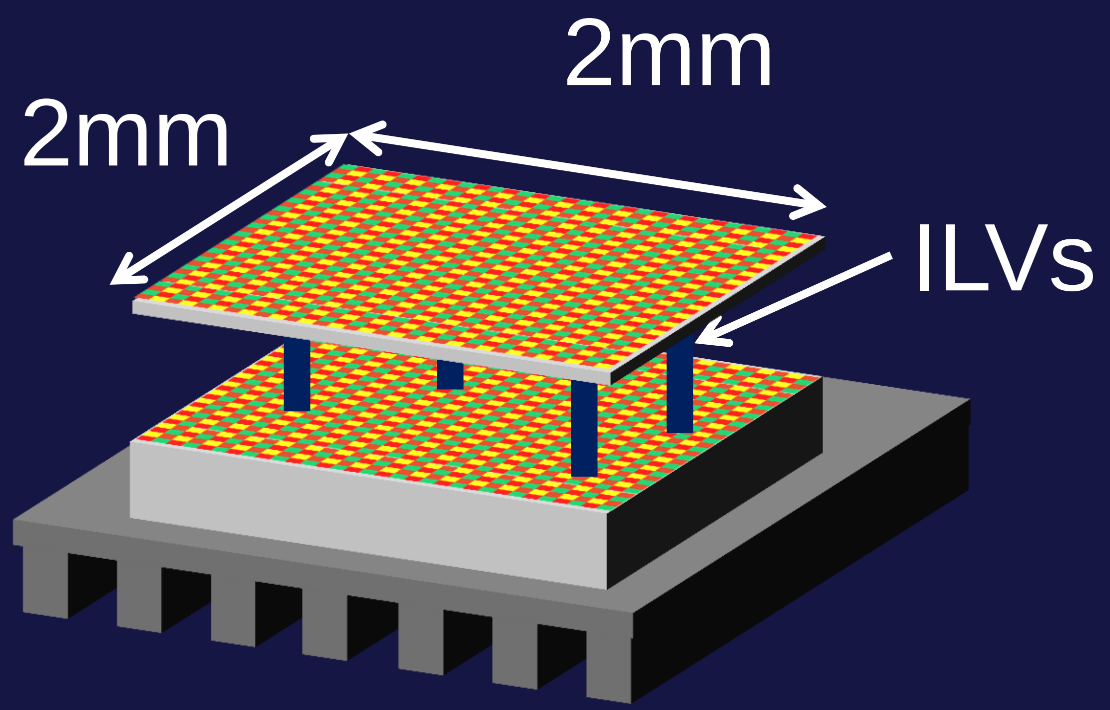
Example 1 Results

- Parallel 3D IC: area benefit



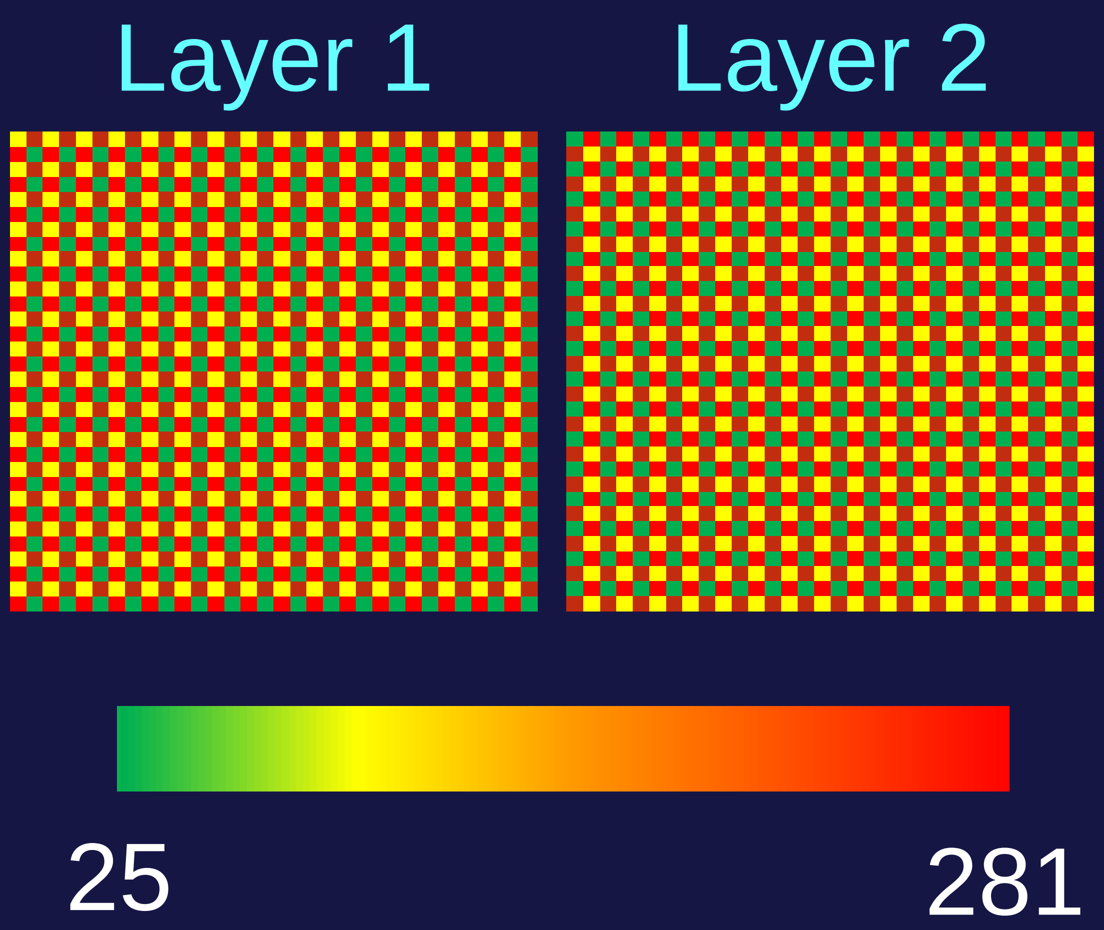
Thermal Analysis: Example 2

- Average: 125 W/cm^2 per layer



Air cooling: 2 W/K·cm^2
Temp. drop on heat sink: 125°C

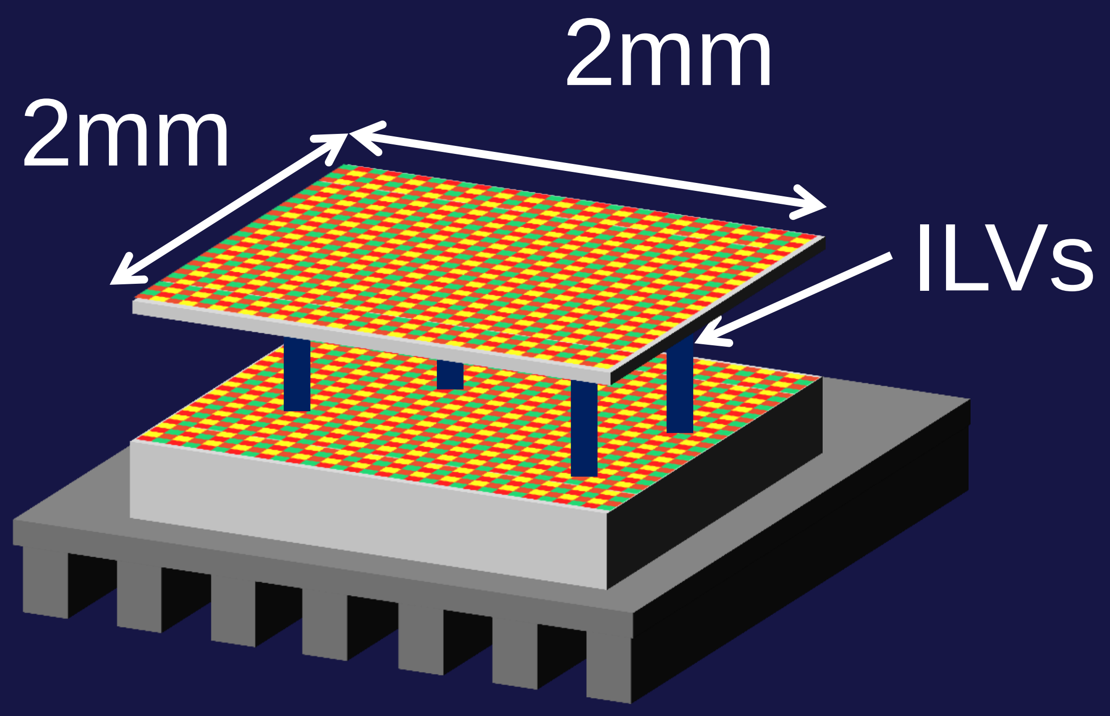
Power distribution map

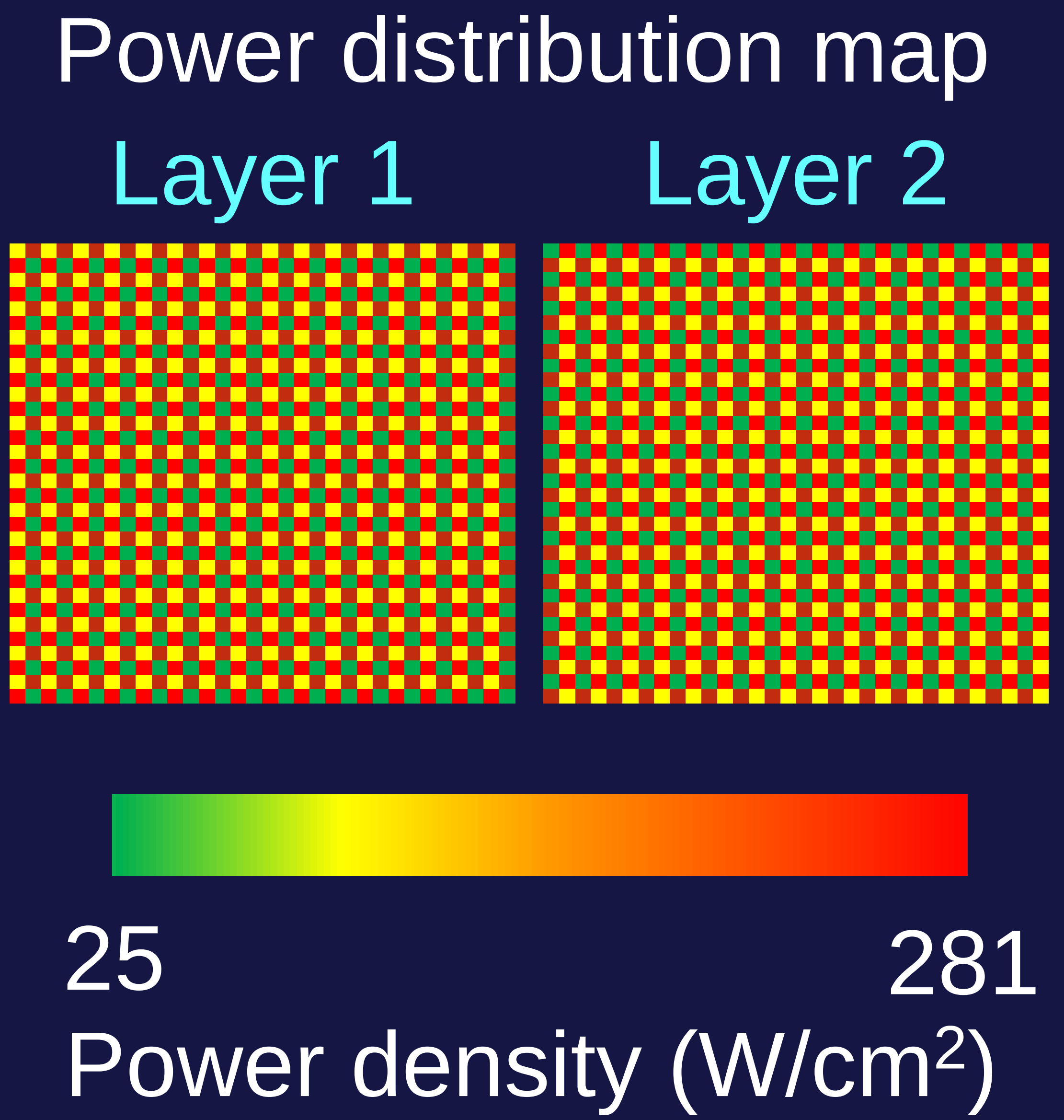


Power density (W/cm^2)

Thermal Analysis: Example 2

- Average: 125 W/cm^2 per layer



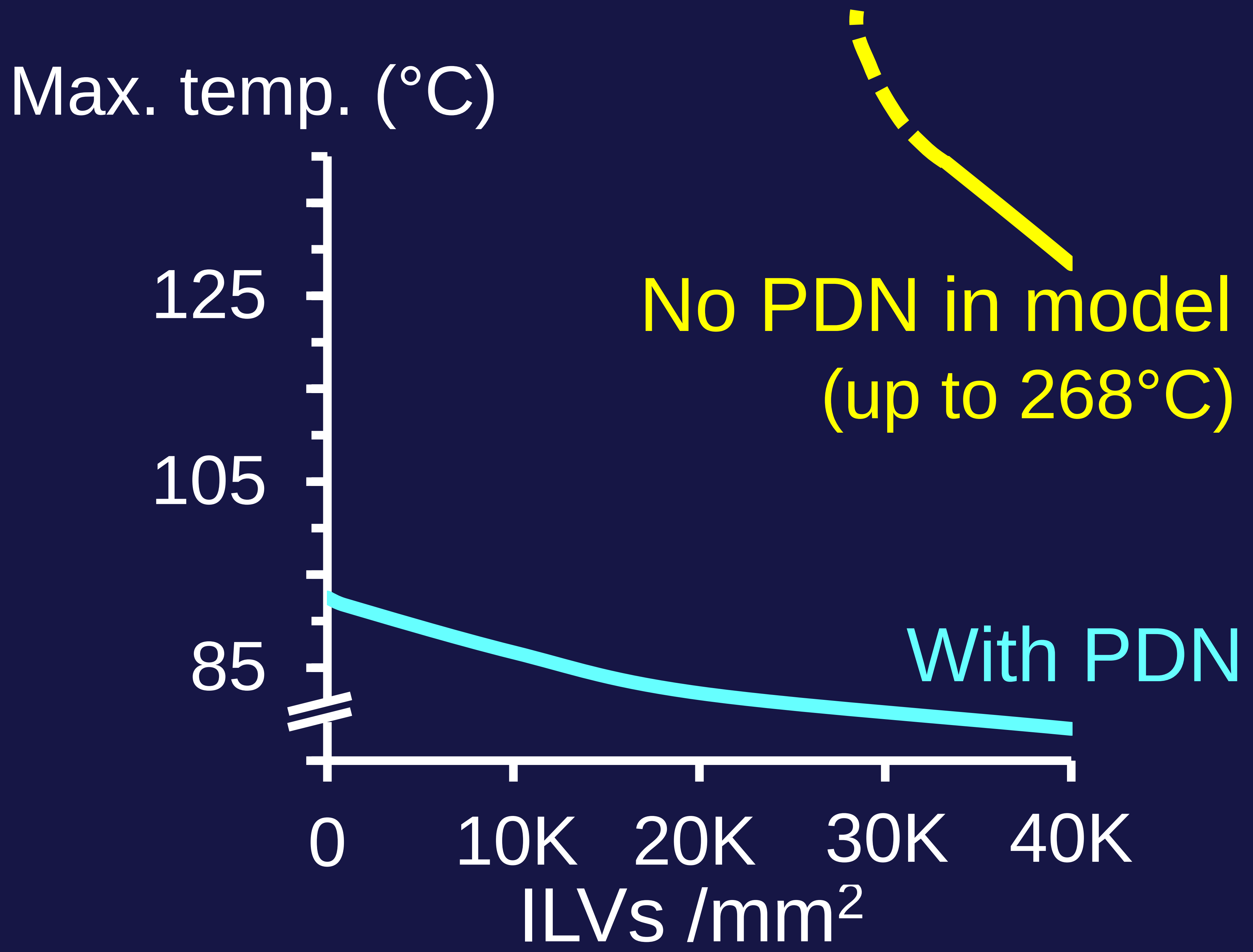


External liquid cooling: 10 W/K·cm^2

Temp. drop on heat sink: 25°C

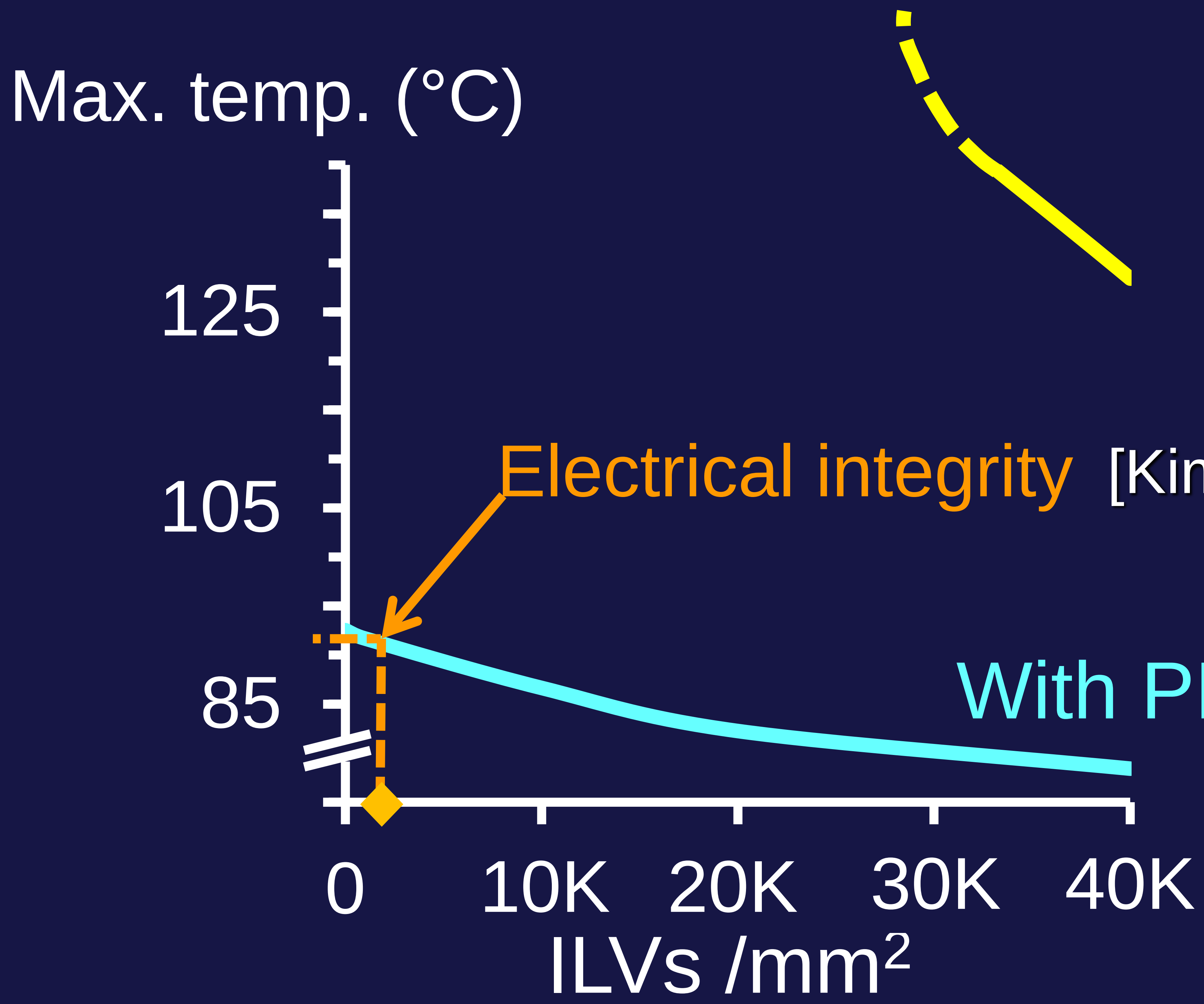
Example 2 Results

- Monolithic 3D IC: significant temperature benefit



Thermal-Aware PDN

- Thermal-aware ILV density selection



Thermal-Aware PDN

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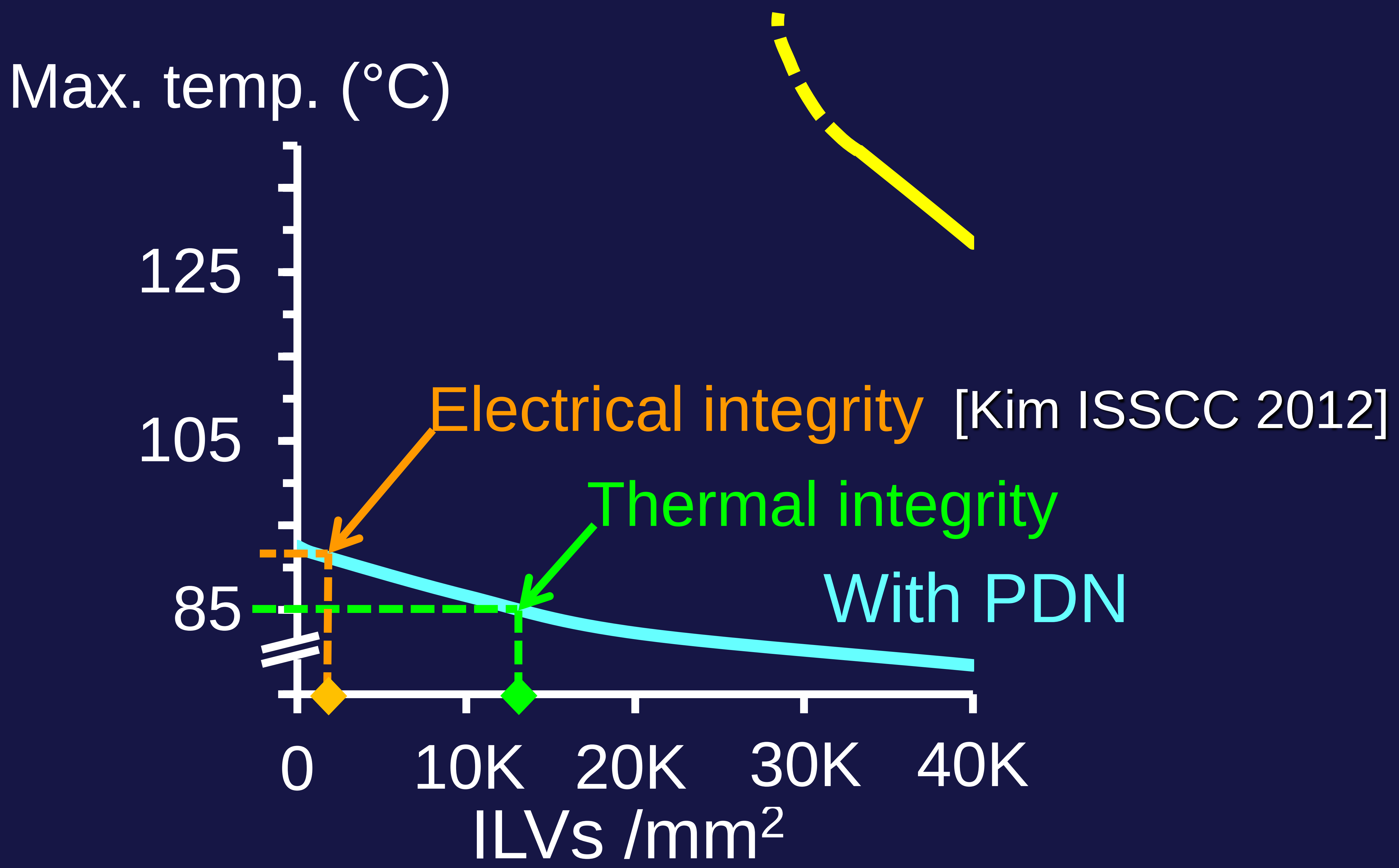
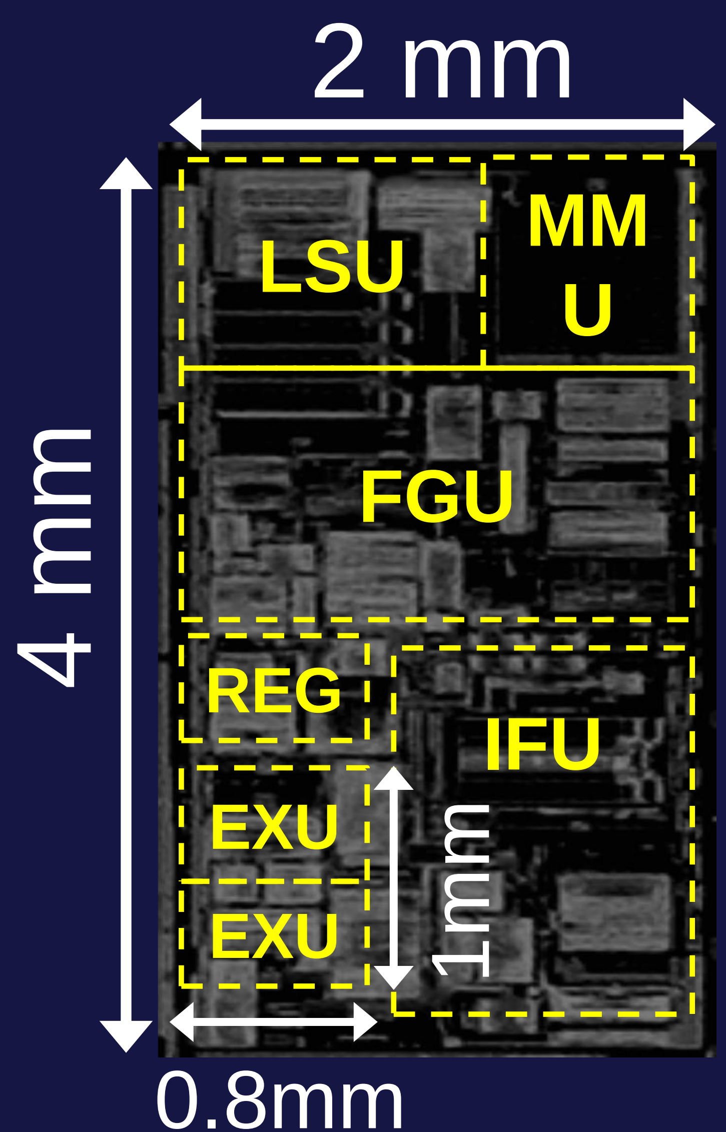
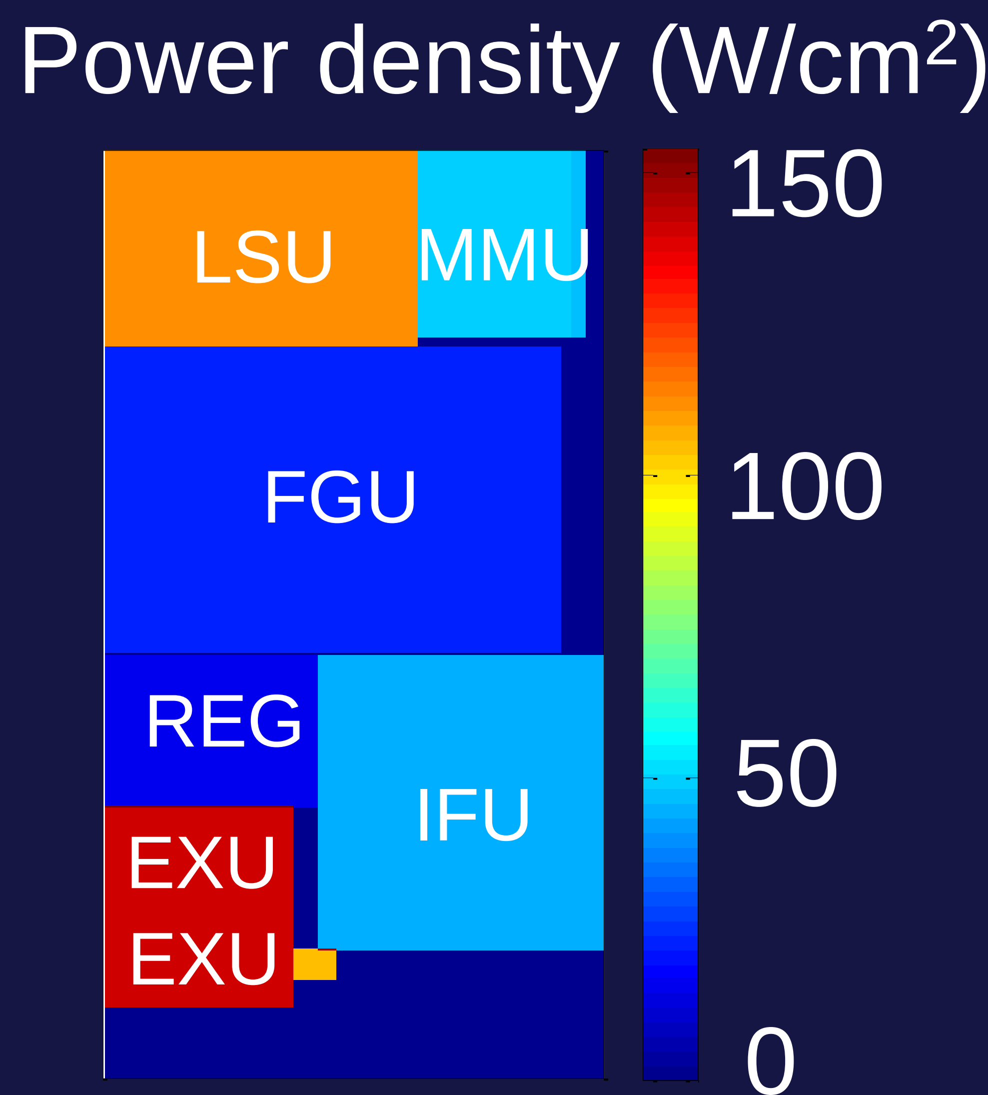
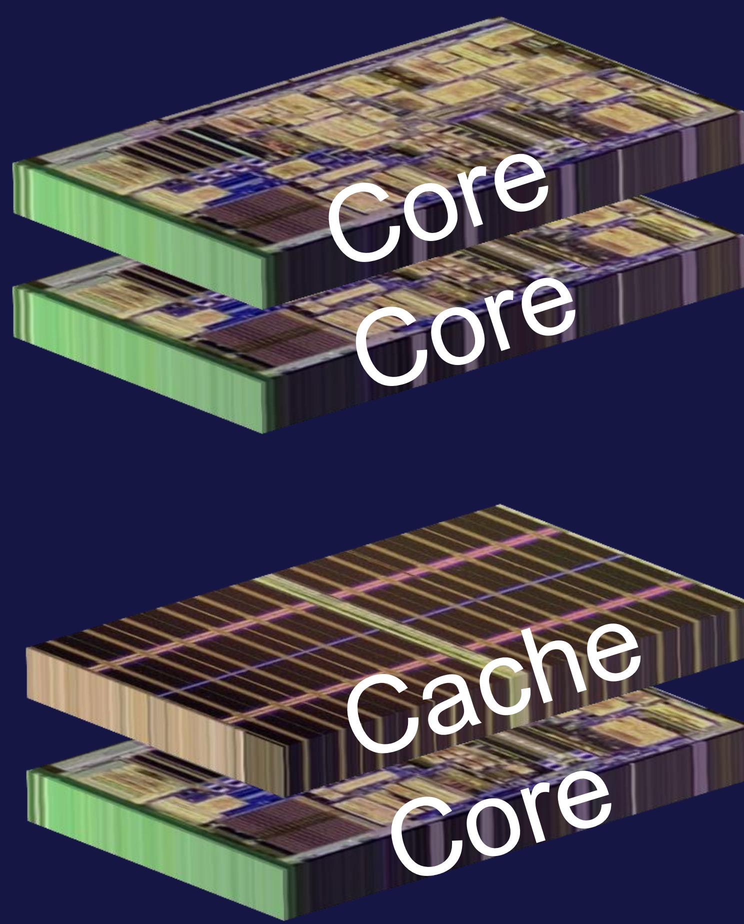


OpenSPARC T2 Core

- Industrial design: 45nm
- Power distribution for Black-Scholes application



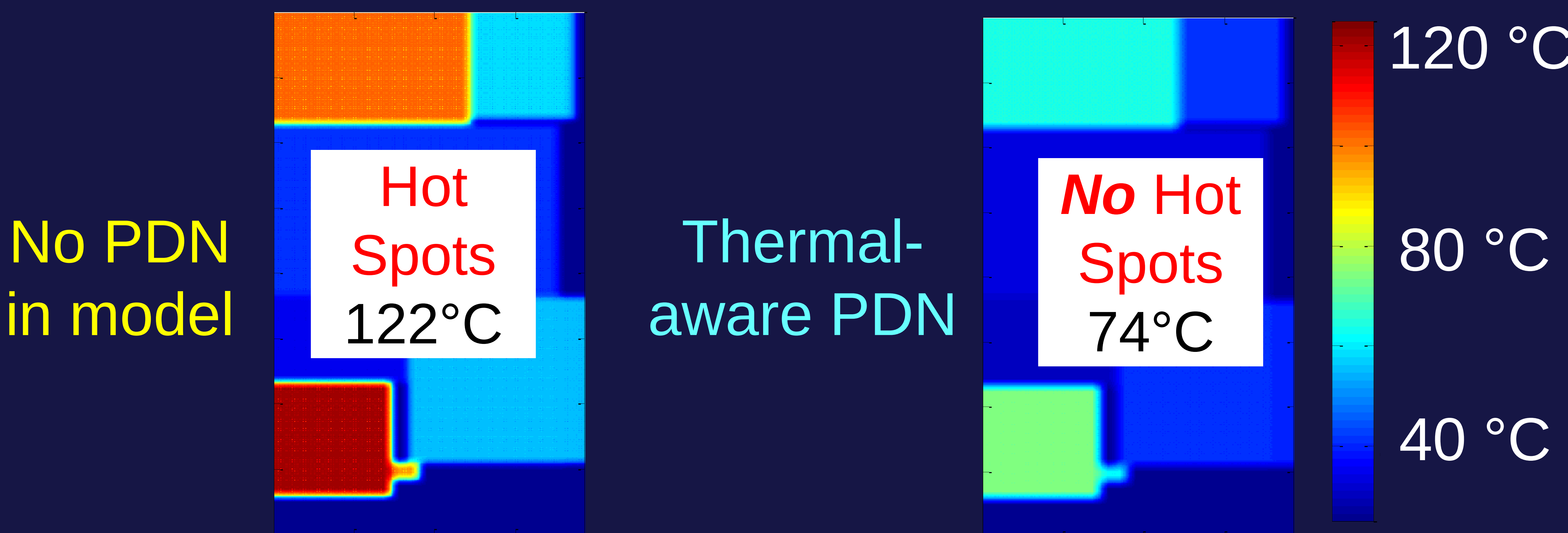




Core-on-Core Stacking

- Significant temperature benefit

Layer 2 temperature distribution

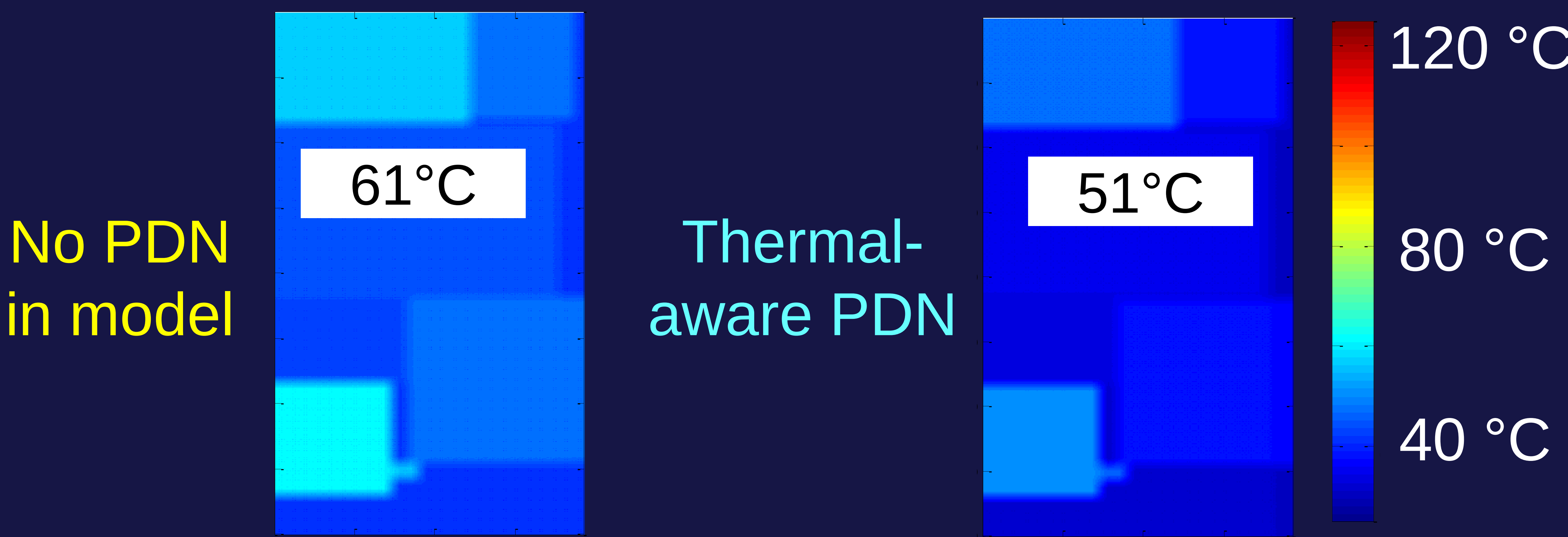


ILV density 10K ILVs/mm^2

Cache-on-Core Stacking

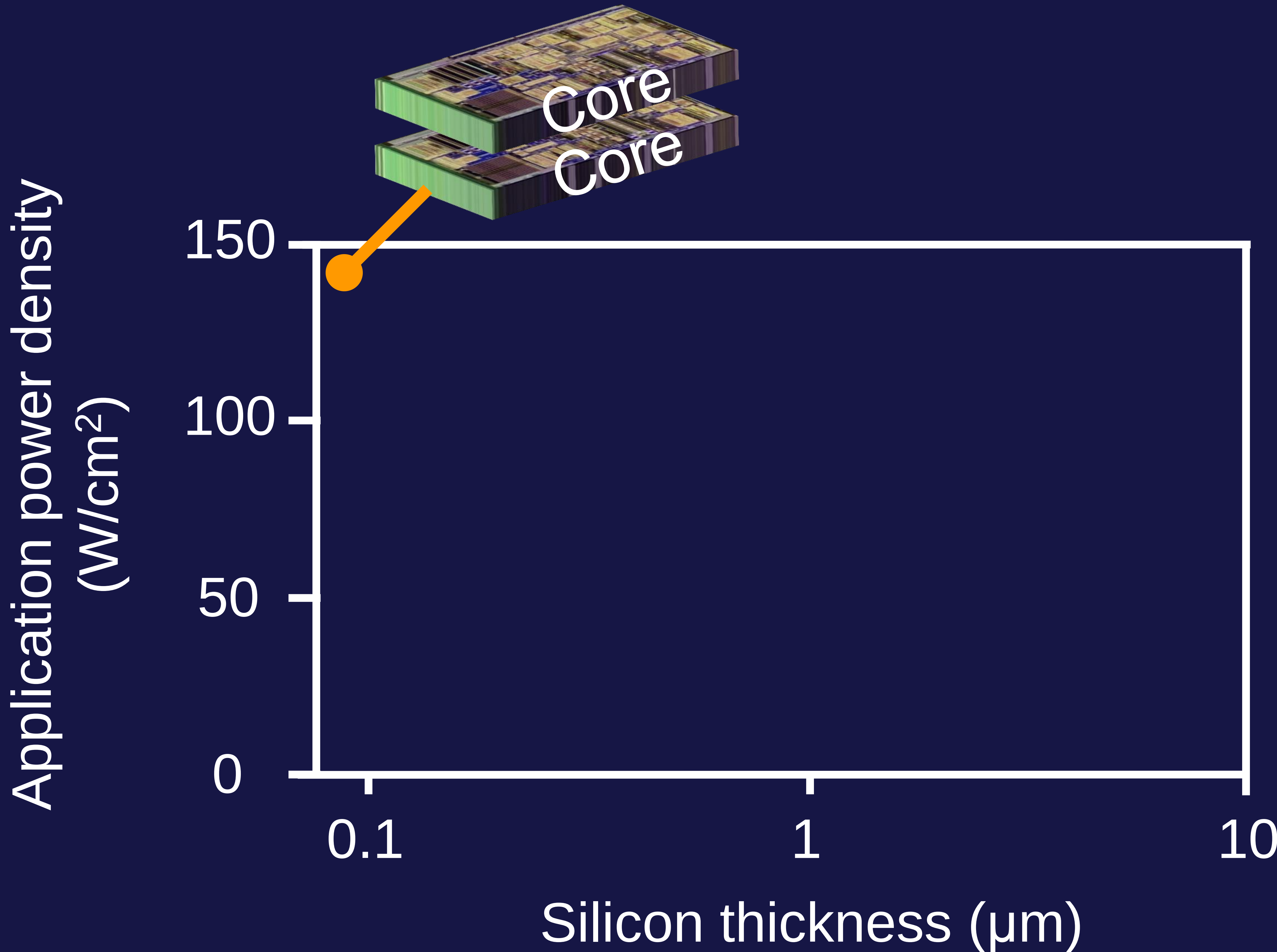
- Further temperature reduction

Layer 2 temperature distribution



ILV density 10K ILVs/mm^2

Technology vs. Application



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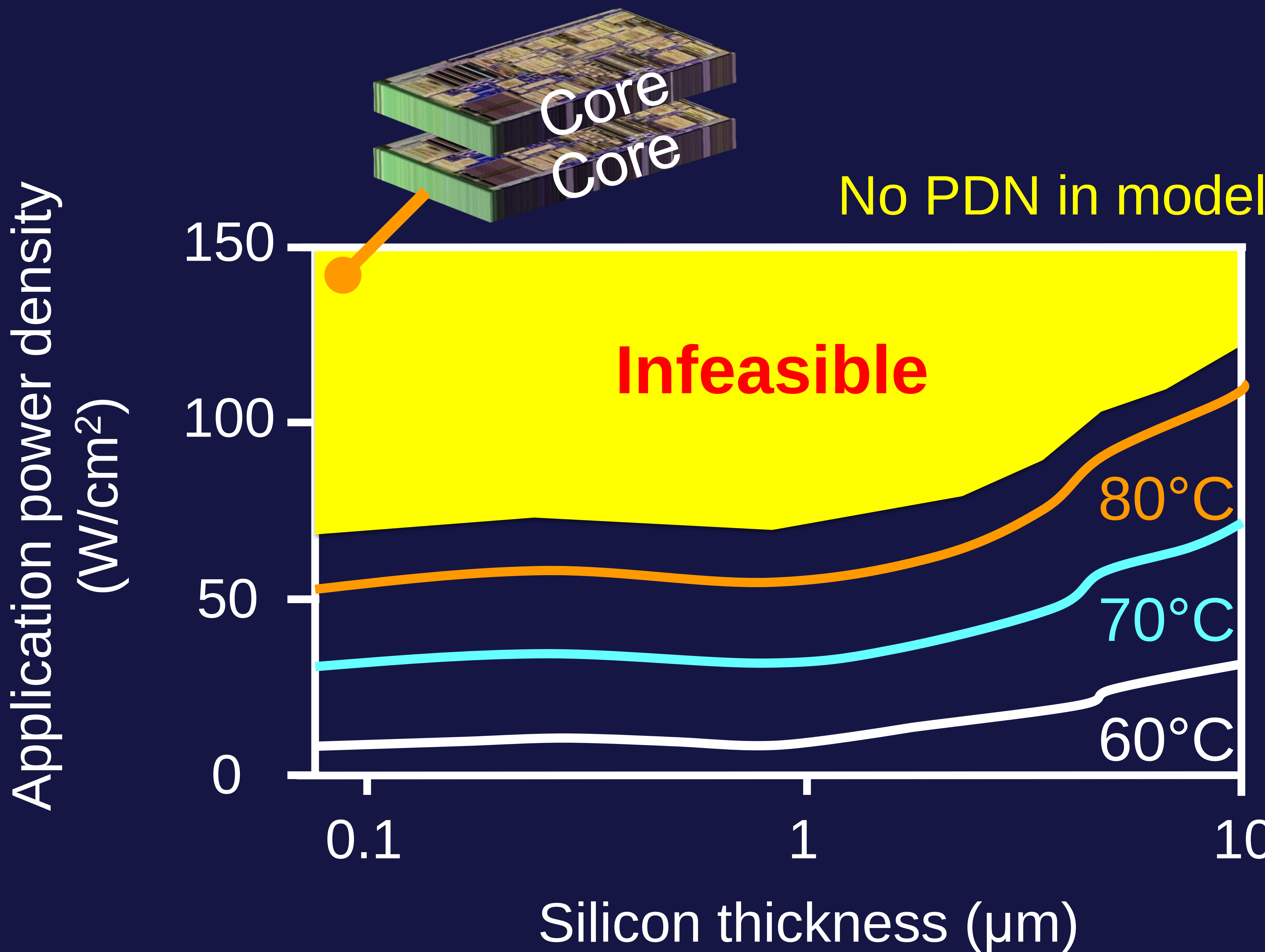

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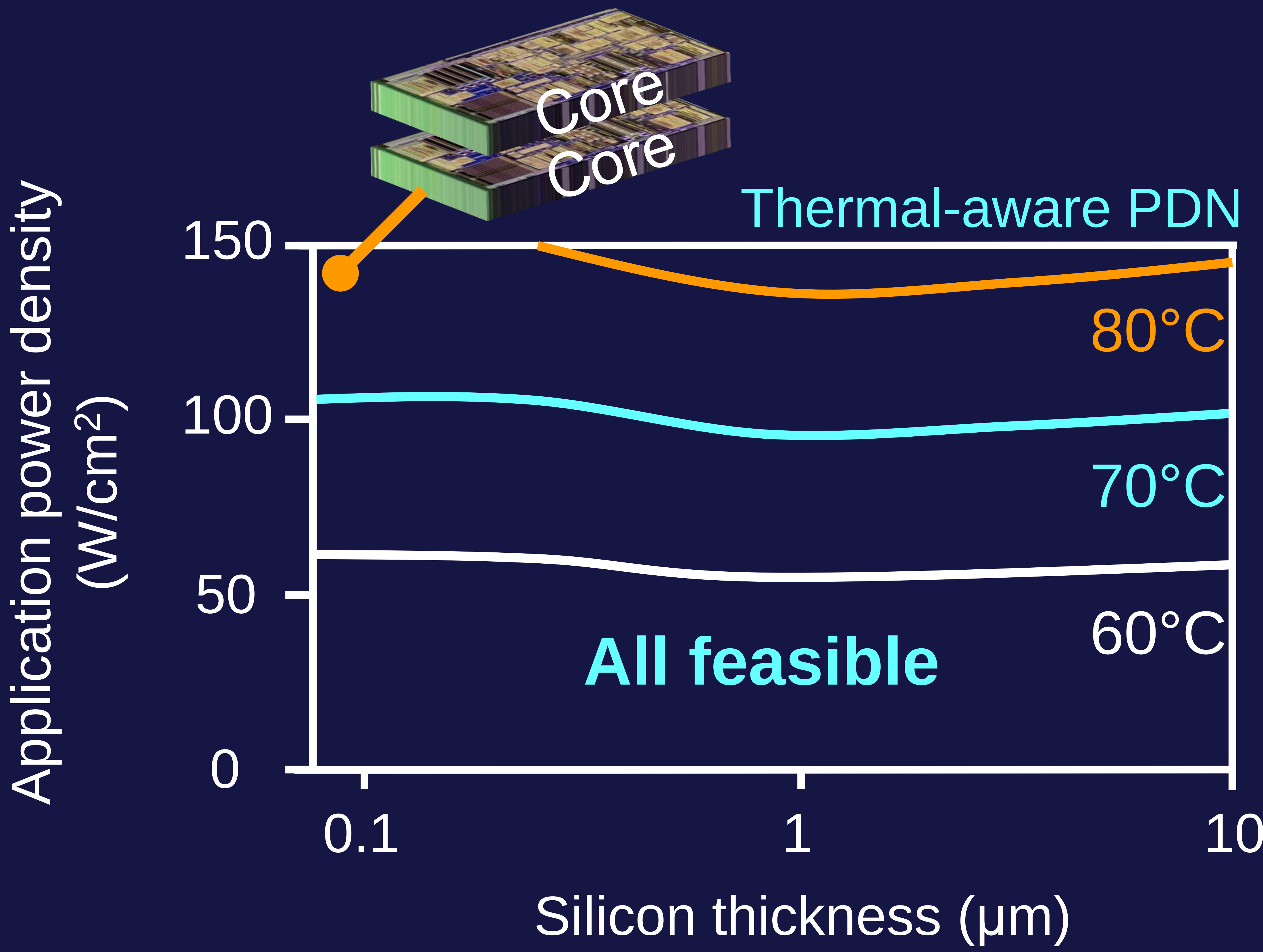

Key Result for Monolithic 3D