

Overview of CMP for TSV Applications



Robert L. Rhoades, Ph.D.

Presentation for AVS Joint Meeting – June 2013

San Jose, CA





TSV's and the Role of CMP

TSV Pattern and Fill

TSV Reveal (non-selective)

TSV Reveal After Si Etch

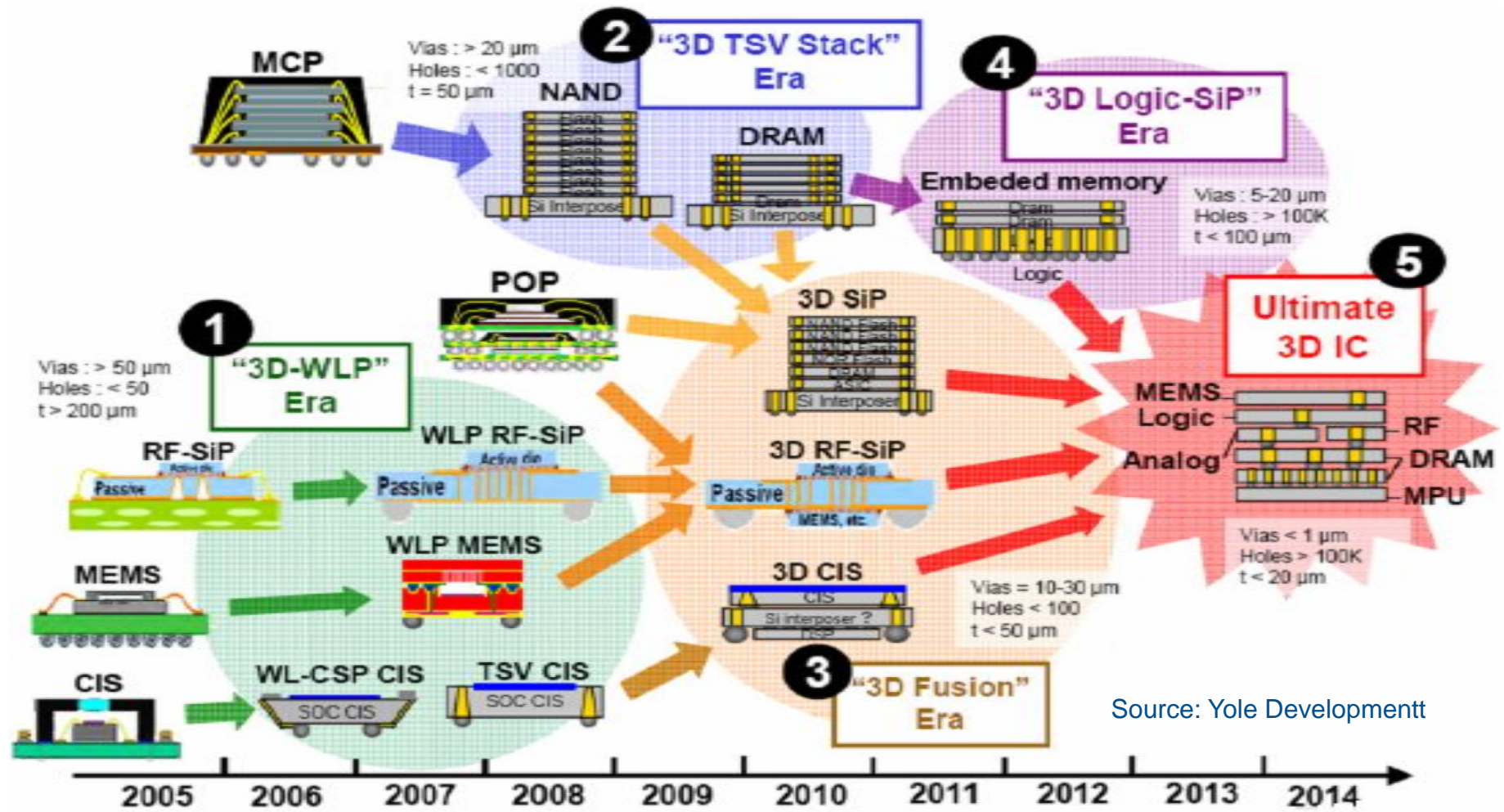
Summary

Background



- Two-dimensional device scaling is increasingly difficult and fast approaching fundamental limits of physics (or balance sheets).
- 3D integration also faces substantial process and design issues, but various approaches are now gaining traction.
- Timing for mainstream adoption of 3D is now. Several products are already in the market and more are being launched.
- One of the key technologies to enable 3D structures is TSV's.

3D Packaging Apps



Source: Yole Developmentt

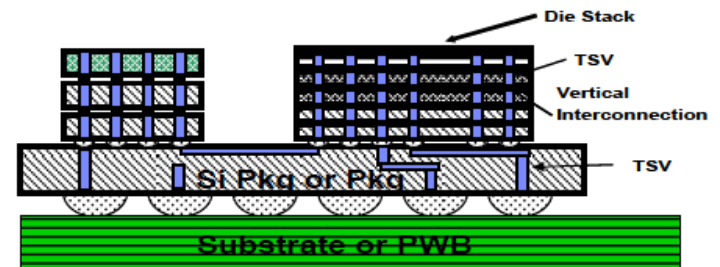
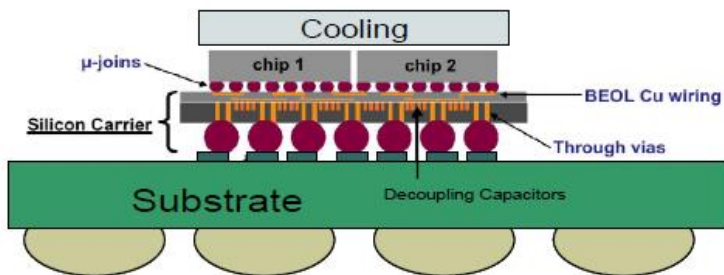
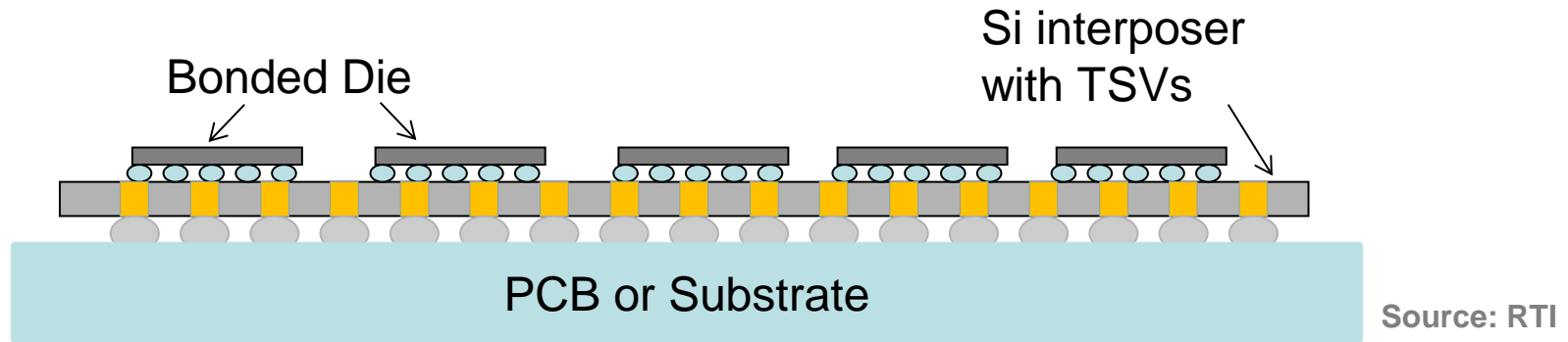
Drivers for 3D



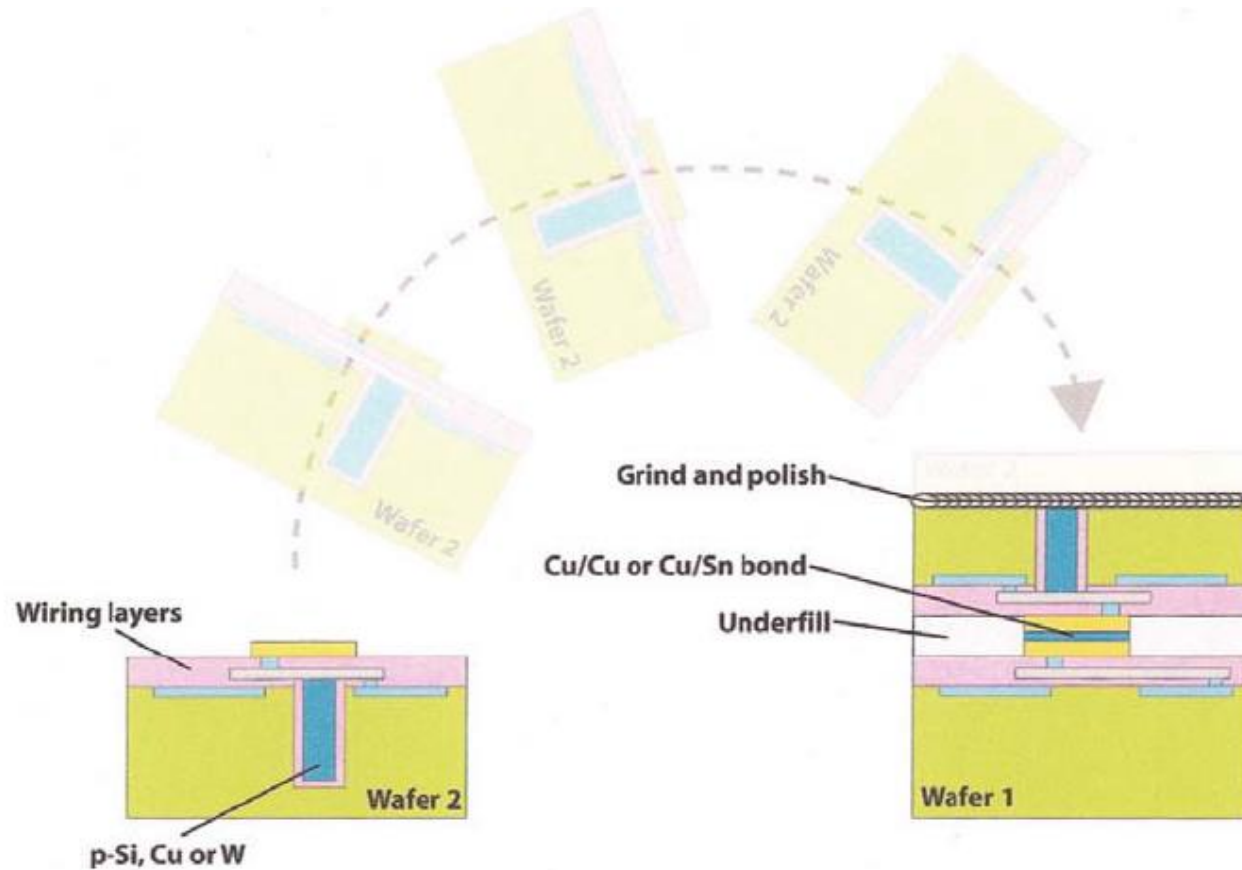
Driving Issue	Case for TSV	Caveats
Miniaturization	Stacked memories. Sensors, e.g., CMOS cameras, “smart dust”	For many cases, stacking and wire bonding is sufficient
Interconnect Delay	When delay in critical paths can be substantially reduced	Not all applications will have a substantial advantage
Memory Bandwidth	Logic-on-memory can dramatically improve memory bandwidth	While memory bandwidth can be improved dramatically, memory size can only be improved linearly
Power Consumption	In certain cases, a 3D architecture might have substantially lower power over a 2D	Limited domain. In many cases, it does not
Mixed Technology (Heterogeneous) Integration	Tightly integrated mixed technology (e.g., GaAs on silicon, or analog on digital) can bring many system advantages	Will be adopted on a case-by-case basis

Source: Published NASA/JPL report

2.5D & 3D Integration



Face to face 3D



Source: Published NASA/JPL report

Role of CMP



- CMP is used in a damascene manner to form the via after conductor deposition from one side.
- TSV's can be filled with any of several conductive materials.
 - Most common options are copper and polysilicon.
 - Final choice depends on dimensions, operating voltage and current, frequency, temperature requirements, plus other integration factors.
- CMP is used again (sometimes multiple steps) after backgrind to help expose and planarize the “bottom” of the TSV's – called TSV Reveal.

Cu TSV Formation



- Background
 - Large via needed for design (75-100um diameter)
 - Via last with extremely thick Cu plating (about 45 um)
 - Some issues with plating bumps, poor uniformity, etc.
 - Previous CMP screening partly successful using standard stock removal slurries, but very long polish times (45 mins to 1 hour)
- Goals for CMP optimization phase
 - Much shorter clear times
 - Reasonable selectivity to nitride after barrier clear
 - Dishing <1 μm across 80 μm via
 - Good surface finish on both Cu and dielectric

High Rate Cu CMP

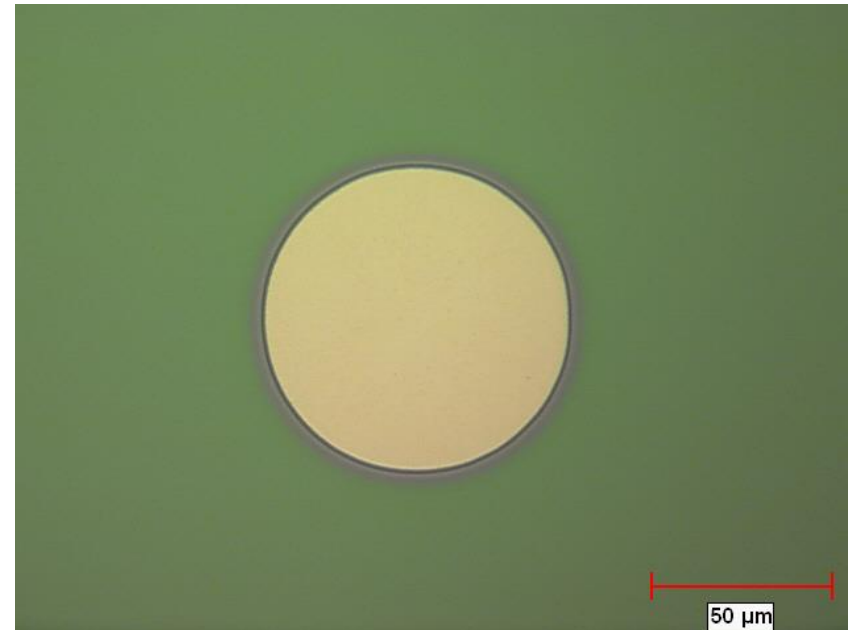
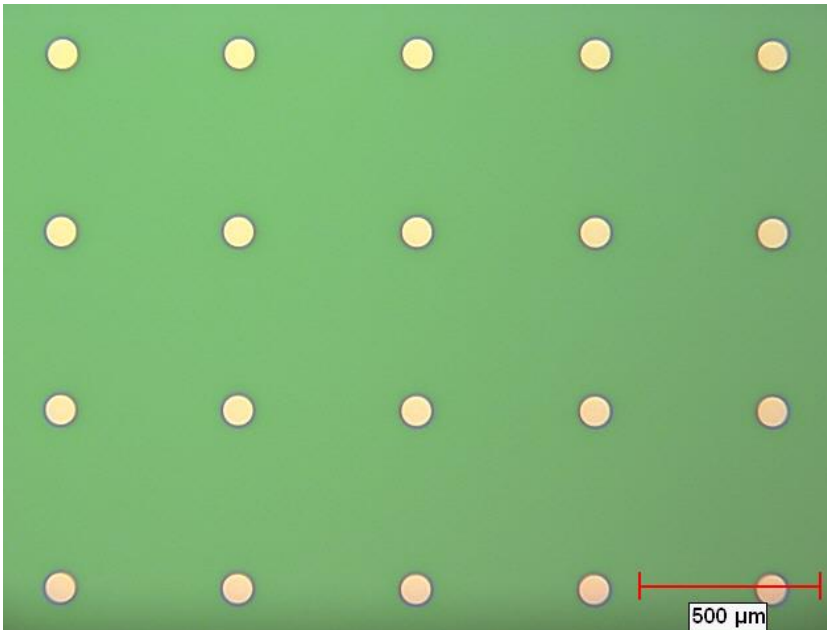


- High rate Cu CMP process (several slurry companies are developing high rate slurries)
 - Cu removal rates of $>4 \mu\text{m}/\text{min}$ achieved
 - Cu polishing times of 10-12min for most wafers with $\sim 43\mu\text{m}$ average Cu removal
 - A few wafers took longer due to Cu plating bump defects
 - Dishing $\leq 0.25\mu\text{m}$ measured on multiple wafers (80um TSV diameter) even with up to 5 min overpolish
 - Good surface finish on all exposed materials

Post-CMP Optical



- Typical surface appearance after CMP
- Field area = nitride and via liner = oxide

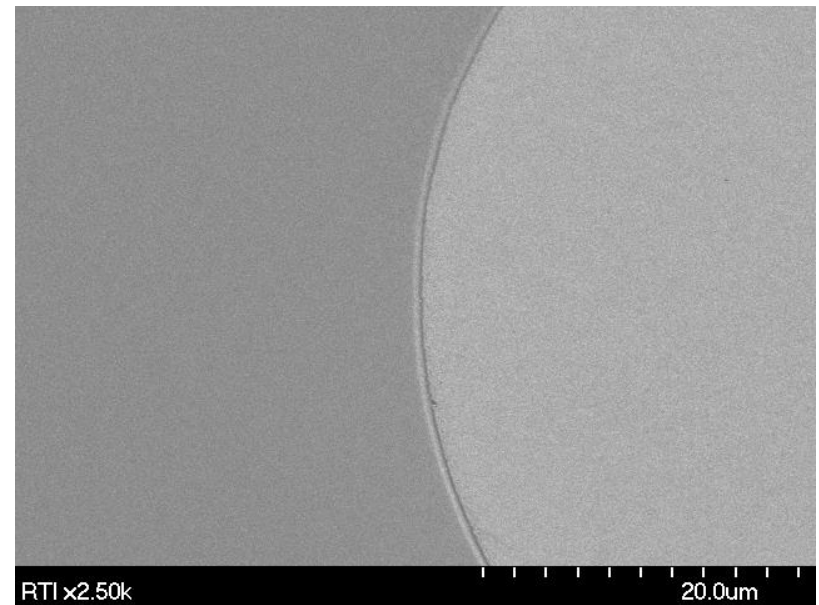
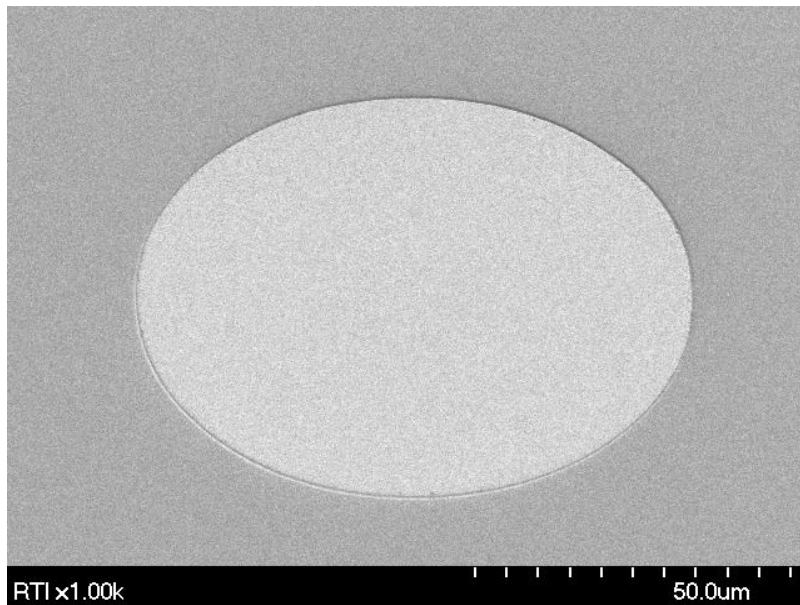


Source: RTI International, Inc.

Post-CMP SEM



- Typical TSV after high-rate Cu CMP



Source: RTI International, Inc.

High-Rate Cu CMP Summary



- Summary comments provided by end user (RTI) ...
- High rate Cu CMP process successfully developed with Entrepix, reducing polishing times from 45-60 min to 10-11 min per wafer.
 - Substantial throughput and cost improvement
- This significantly reduces the requirement for developing a low overburden Cu via fill plating process, enabling use of conformal plating and increasing plating process window.
- CMP processing of wafers completed with excellent TSV planarity ($\leq 0.25\mu\text{m}$ dishing for 80 μm TSV diameter)

TSV Summary Table



TSV Fill Material	Deposition Thickness	Demonstrated CMP Polish Rate	Dishing / Recess (Angstroms)
Copper	5 kÅ – 60 μm	1 kÅ/min – 8 $\mu\text{m}/\text{min}$	10 Å – 0.3 μm
Polysilicon	4 kÅ – 30 kÅ	2 kÅ/min – 15 kÅ/min	300 – 1200 Å
Tungsten	3 kÅ – 9 kÅ	3 kÅ;/min – 8 kÅ/min	150 – 300 Å
NiFe or NiFeCo	1.5 μm – 8 μm	3 kÅ/min – 7 kÅ/min	600 – 4000 Å
Pt	1.5 μm – 5 μm	1.5 kÅ/min – 5 kÅ/min	100 – 800 Å

TSV Reveal

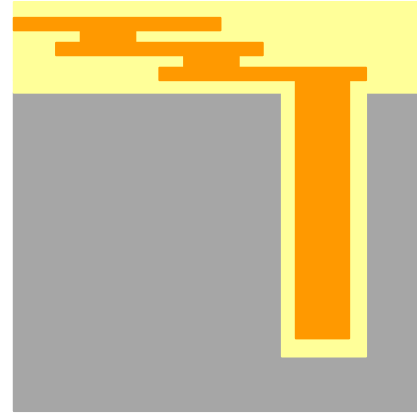


- Process module following completion processing on opposite side
- TSV must be exposed to make contact and/or continue patterning next layers (such as RDL) from wafer backside.
- Various integrations are being pursued with combinations of backgrind, etch, selective CMP, or non-selective CMP.
 - Some approaches require 2 or 3 steps of CMP to achieve desired result
- Two alternatives with very different requirements for CMP
- Example 1: Reveal Using Non-selective CMP
- Example 2: Reveal CMP Following Si Etch

Process Flow



(a)



(b)



(c)



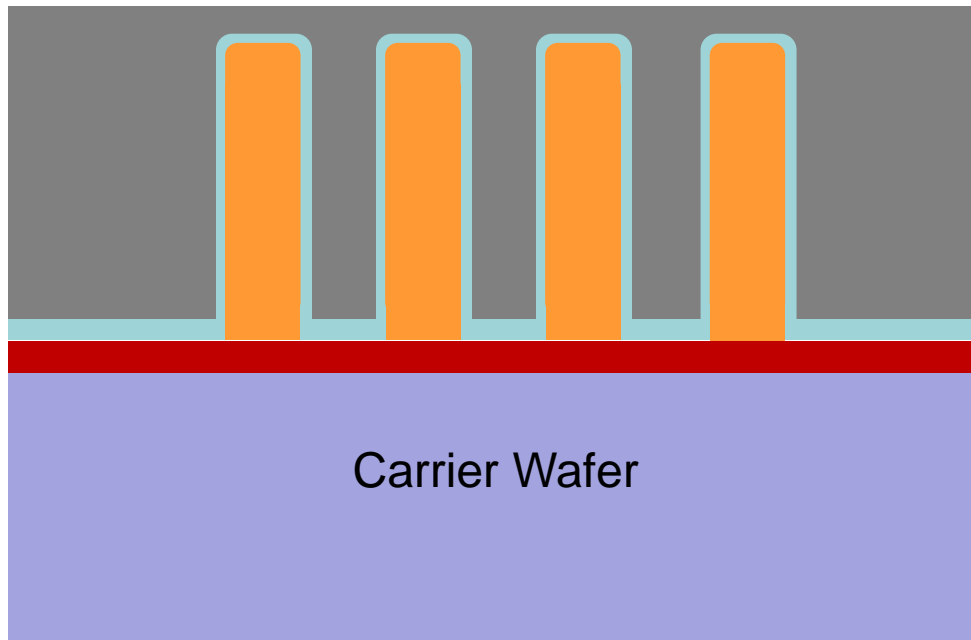
(d)

Process flow for Si interposer with TSVs: (a) TSV etch, isolation layer, plating, and via CMP, (b) Frontside multi-level metallization, (c) Wafer thinning and TSV reveal, (d) Backside metallization.

Non-Selective Reveal



Backgrind stops in Si before reaching TSV's



Carrier Mount

- TSV wafers mounted face down on carrier wafers

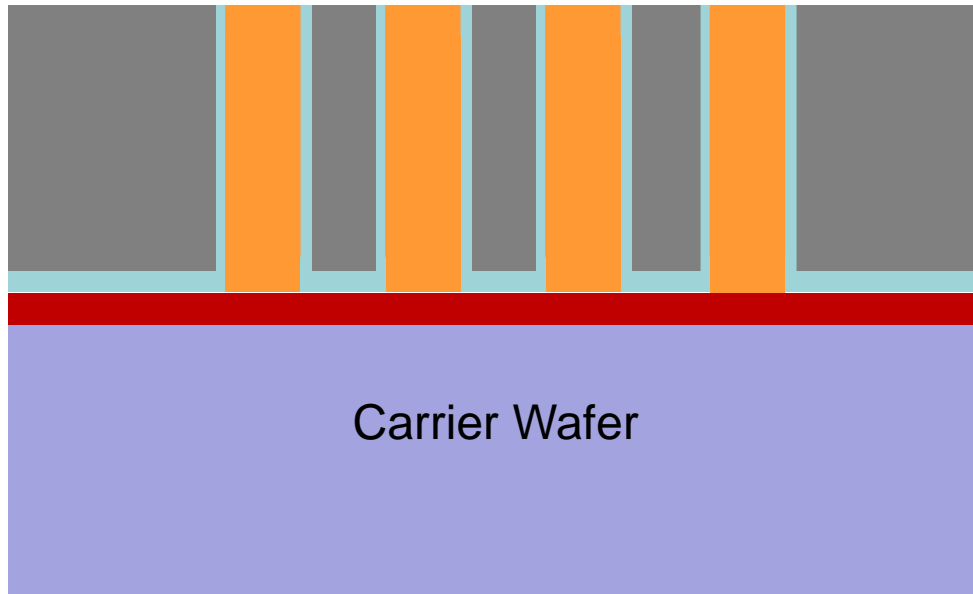
Backgrind

- TSV wafers thinned using backgrind to approx 3-15um “below” TSVs (above in dwg)
- Reveal CMP performs dual function of removing grind damage layer and remaining bulk Si then exposing center conductor of TSV's

Reveal CMP #1



Expose & Planarize TSVs



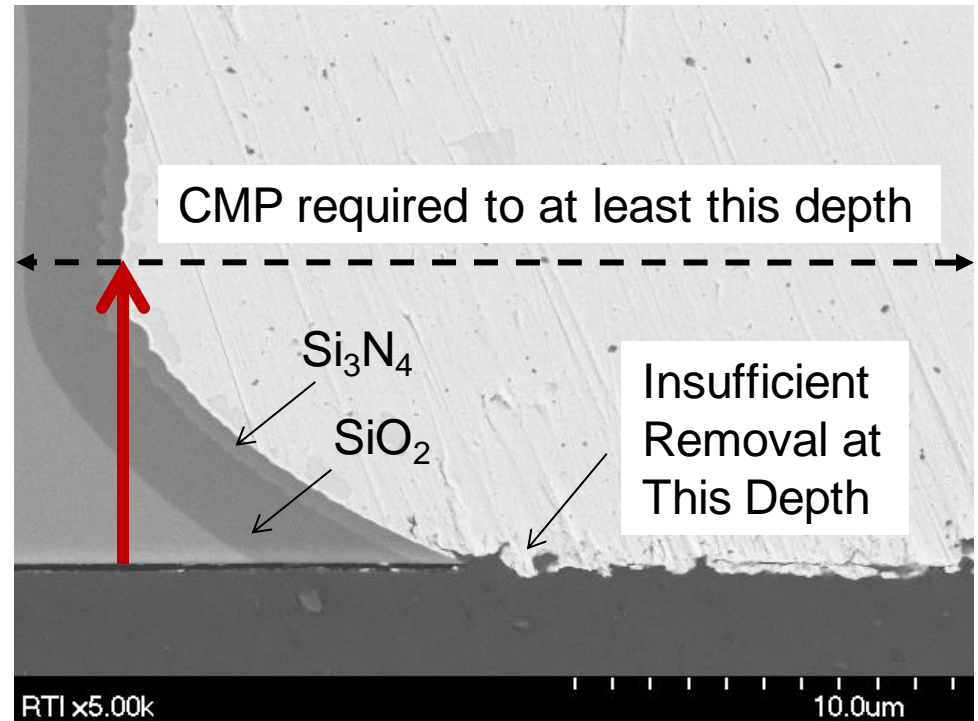
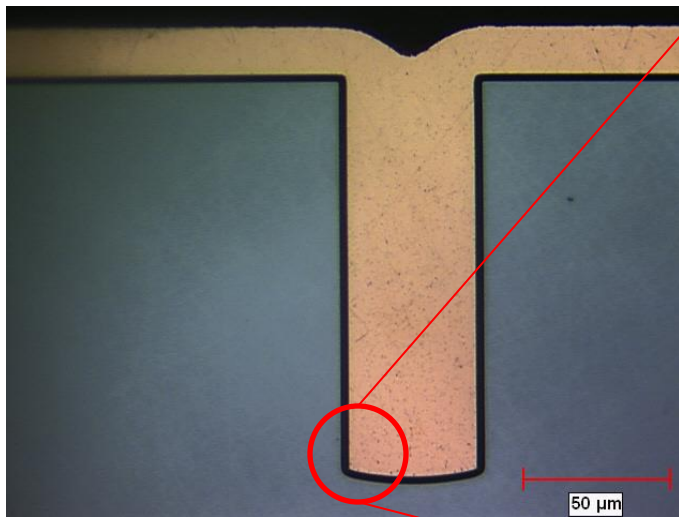
Several exposed materials

- Single crystal silicon
- Oxide (or other liner)
- Barrier metal
- Copper

Architecture



Need to polish far enough into TSVs to remove rounded profile at base of vias

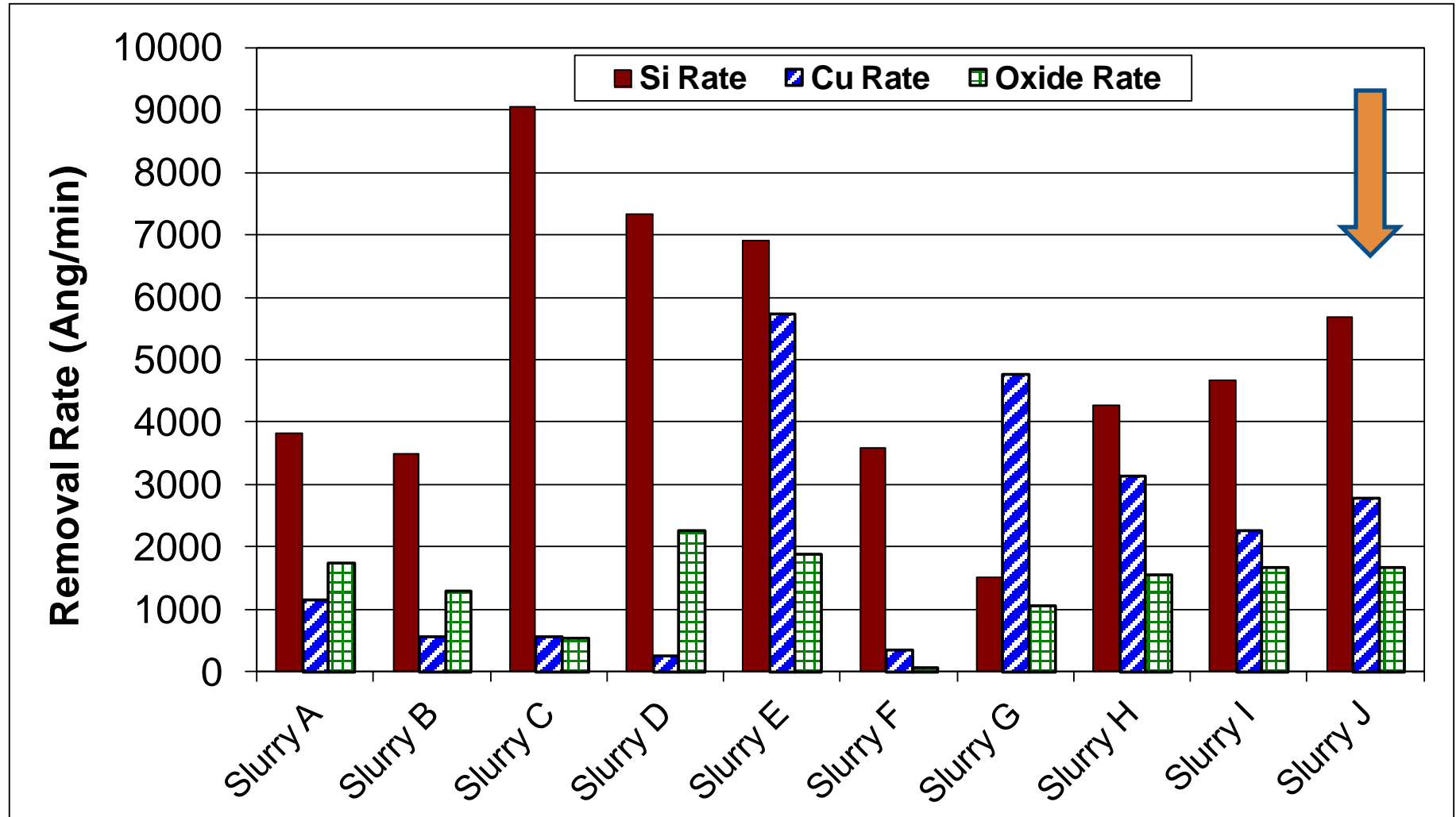


CMP Process Goals



- **High Si rate**
- **Low selectivity**
 - Reasonably matched Cu and Tox rates
 - Non-zero barrier metal rate (though usually thin layer)
- **Good planarization**
 - Low dishing of wide features
- **Good surface quality**
 - Low roughness on both Si and Cu
 - No scratching
 - Not as stringent as CMOS metallization

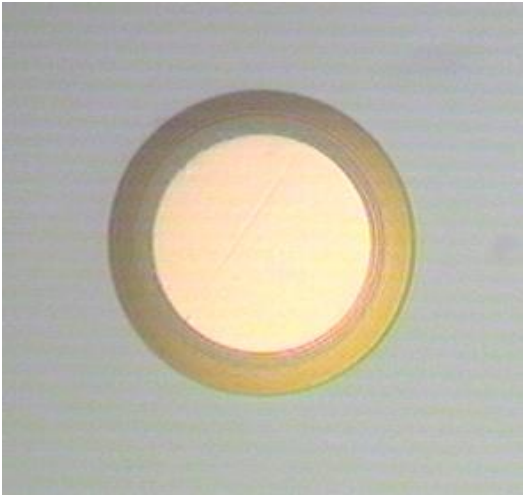
CMP Slurry Screening



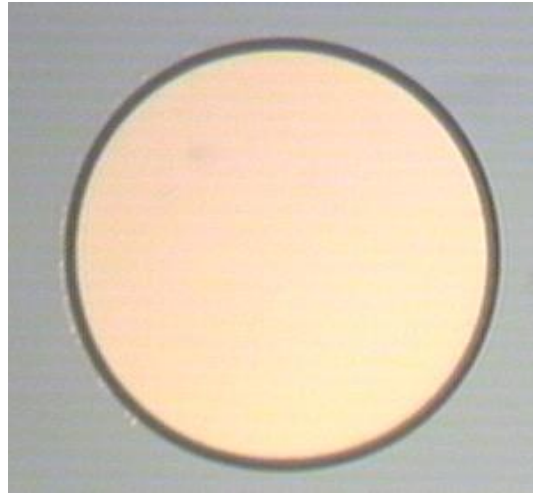


- **Slurry J was chosen for patterned wafers**
- **Re-optimized process for higher Si rate**
 - Target 1 um/min → Achieved 1.05 um/min
- **Iterative polish on first wafer**
 - Total amount to be removed estimated at 30 um
 - Polished in 5 minute increments
 - Inspection clearly showed breakthrough
 - Final surface topography <250 nm achieved

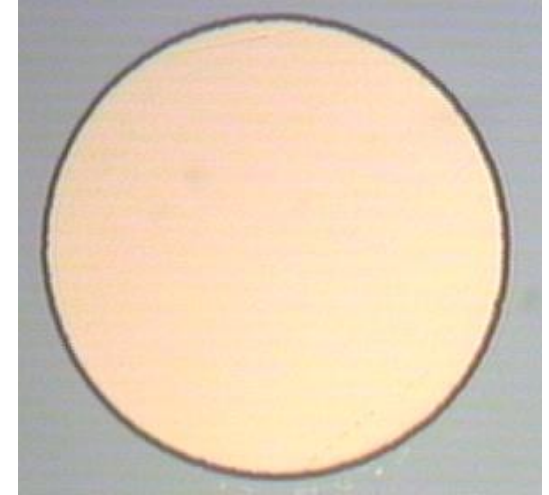
Visual endpoint



20 min



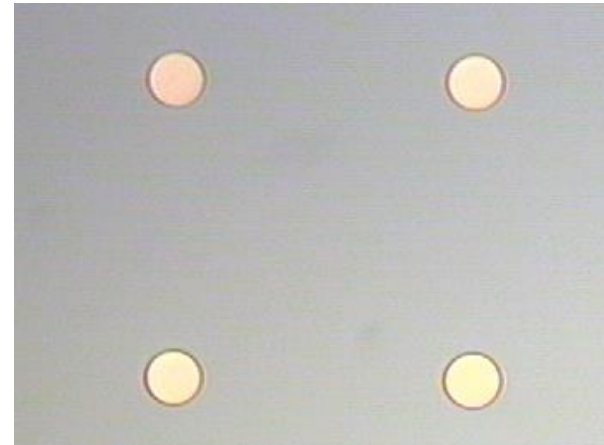
25 min



30 min

Custom Entrepix process was used to planarize Si-Ox-Cu

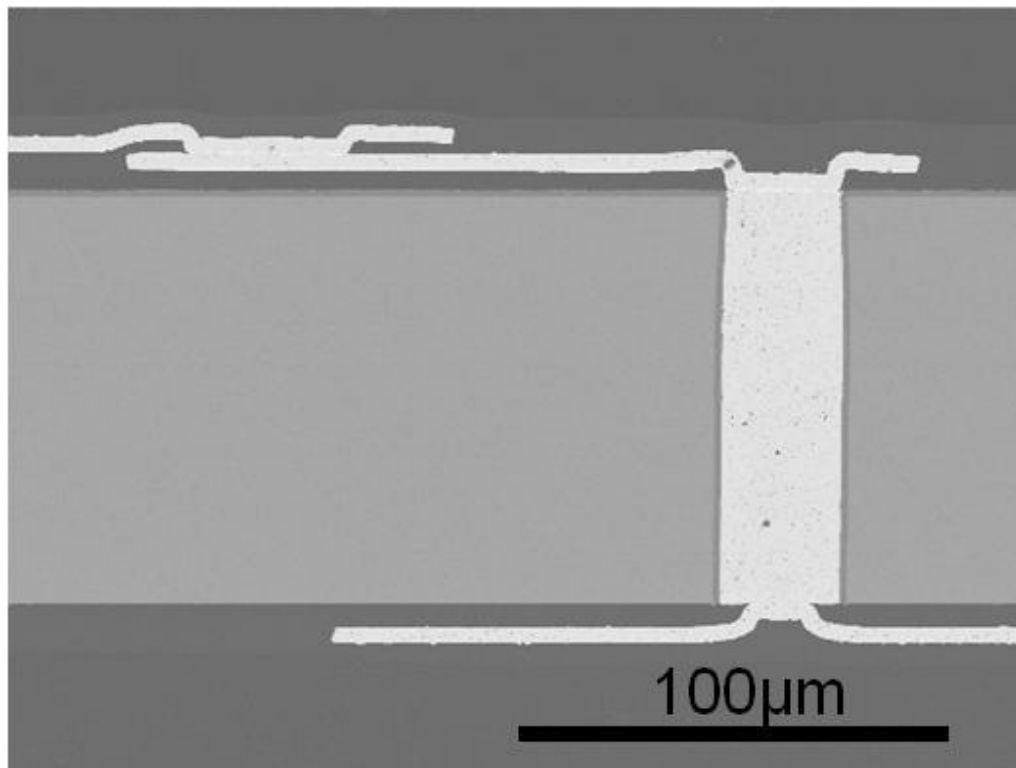
Polishing endpoint was determined by monitoring the exposed TSV diameter and the width of via dielectric band by microscope



Result #1



Completed interposer test structure: 25 μ m via diameter, 100 μ m thickness.
Structure has 2 frontside metal layers (4 μ m Cu) and 1 backside metal, forming TSV chains.
Oxide / nitride TSV dielectric, polyimide dielectric on front / back wafer surfaces.



Bottom surface received
TSV reveal polish

Reveal CMP #2

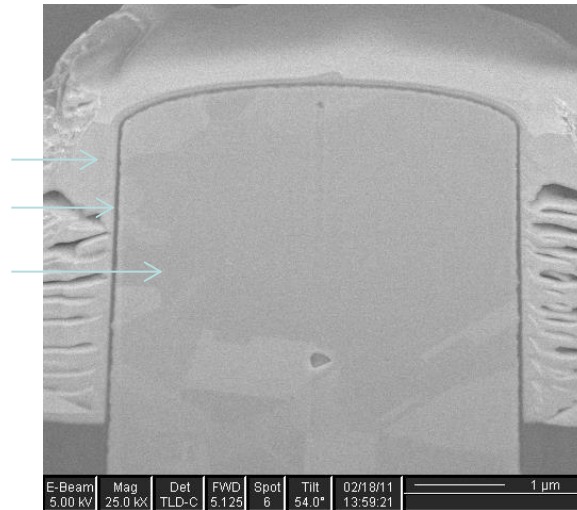


- After backgrind, bulk Si removed by an etch process
 - Favored if installed etch equipment is already available
 - Lower cost per wafer
 - Can be either dry etch or wet etch, but must be highly selective to oxide
- Si etch proceeds until 3-5um of encased via “bumps” are exposed
- Primary goal of CMP is to planarize bumps and expose the Cu cores
- One benefit of this approach is to reduce total CMP polish time (drops to roughly 1-1.5 min per platen on P1/P2 of a Mirra)
 - Less sensitive to uniformity issues
 - Faster throughput and lower cost
 - Only first pass optimization thus far ... may drop even further as work proceeds

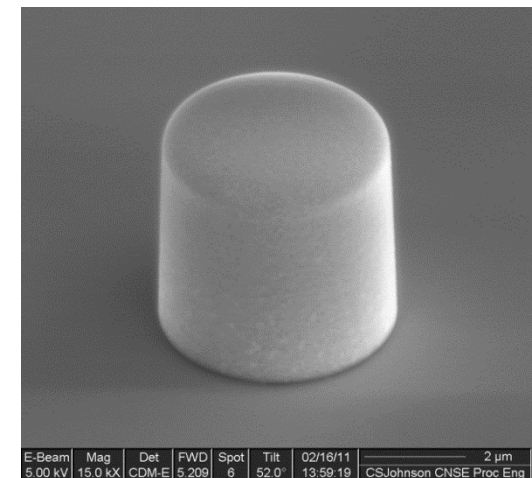
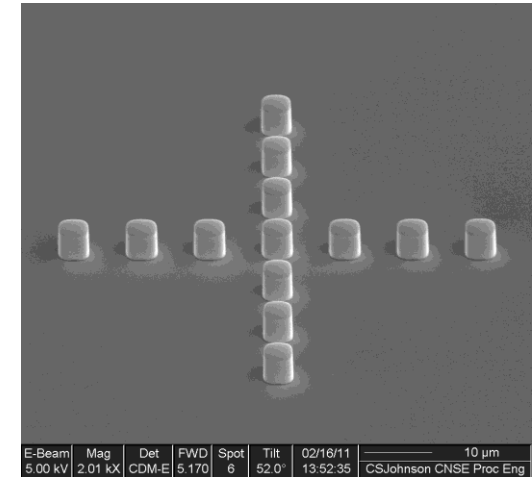
Typical After Si Etch



FIB Pt
Dielectric liner
Cu



FIB/SEM image of revealed via

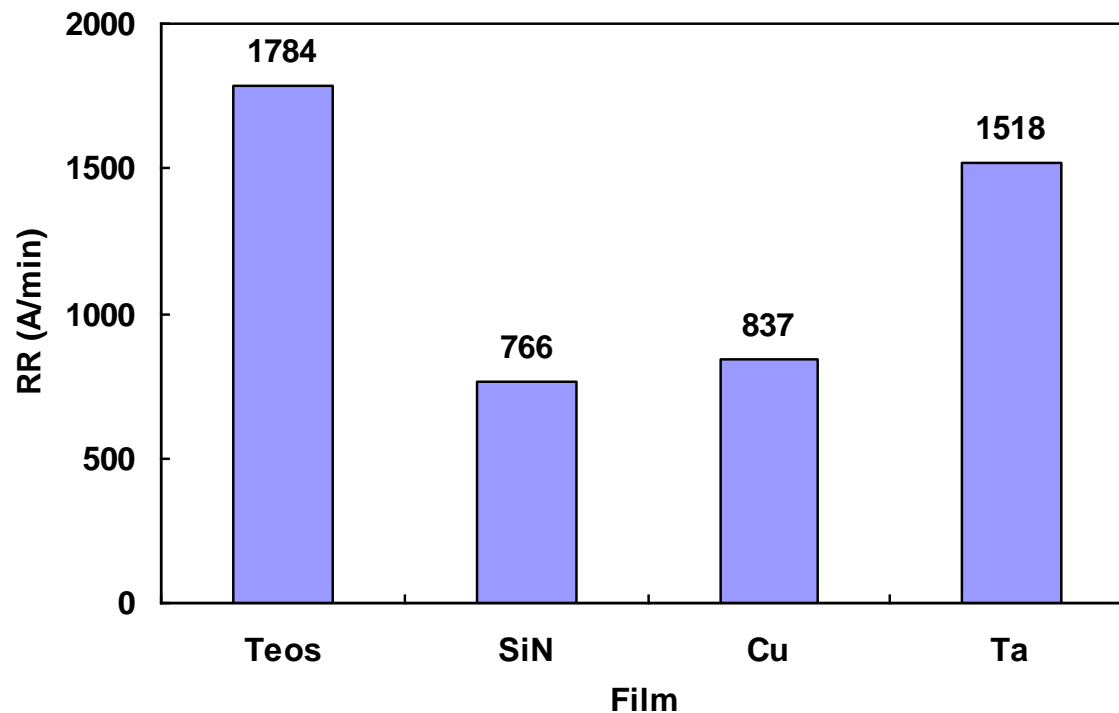


- FIB images show the dielectric liner remains intact
- No footing is observed at the base of the via
- Revealed TSVs and the Si surface are clean
- Si surface does not show pyramids or other etching defects

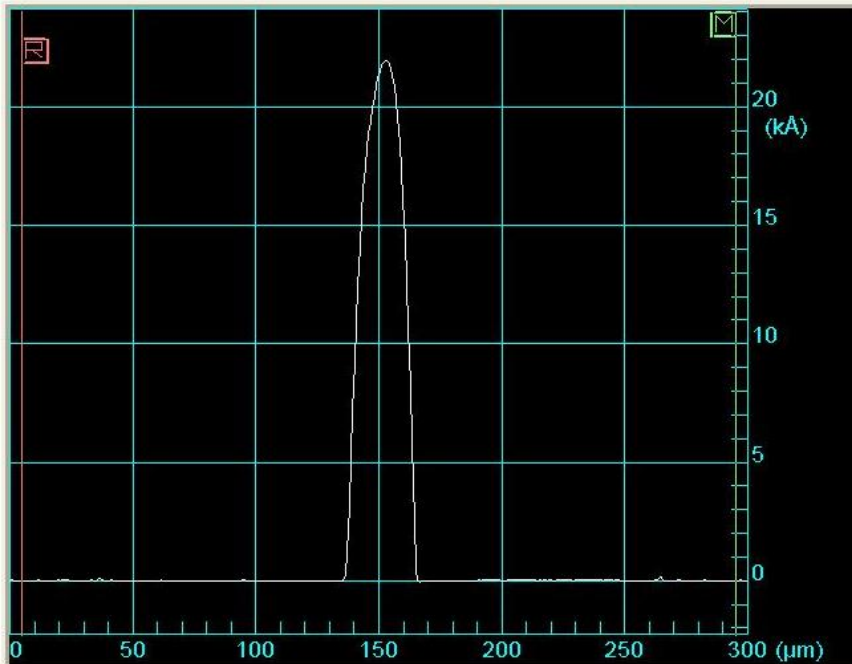
Slurry Properties



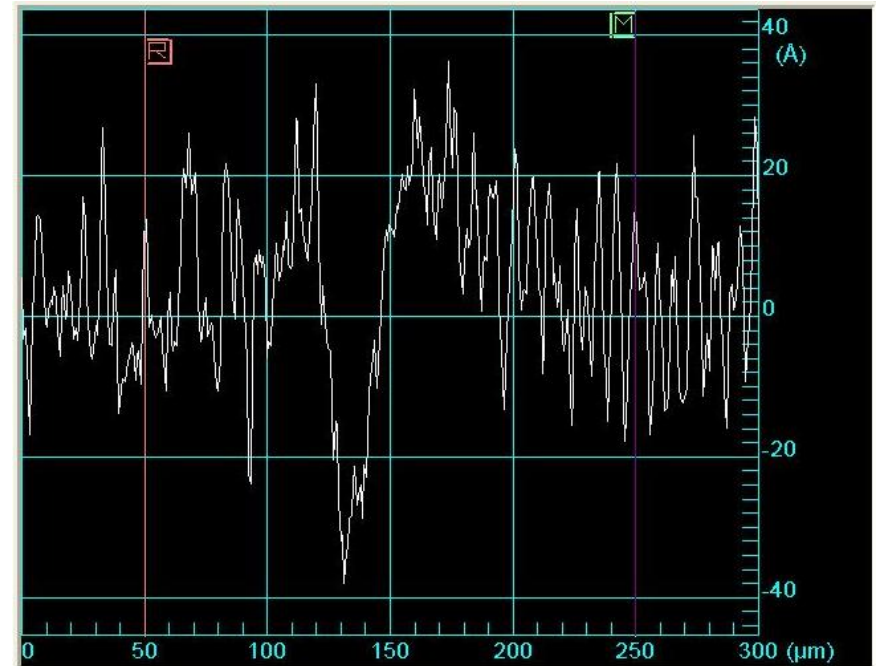
- Slurry developed specifically for this type of application
- Blanket film removal rates at 3psi membrane pressure
 - Effective bump removal rate is much higher due to force concentration on small, low density features



Topography – Wfr 1

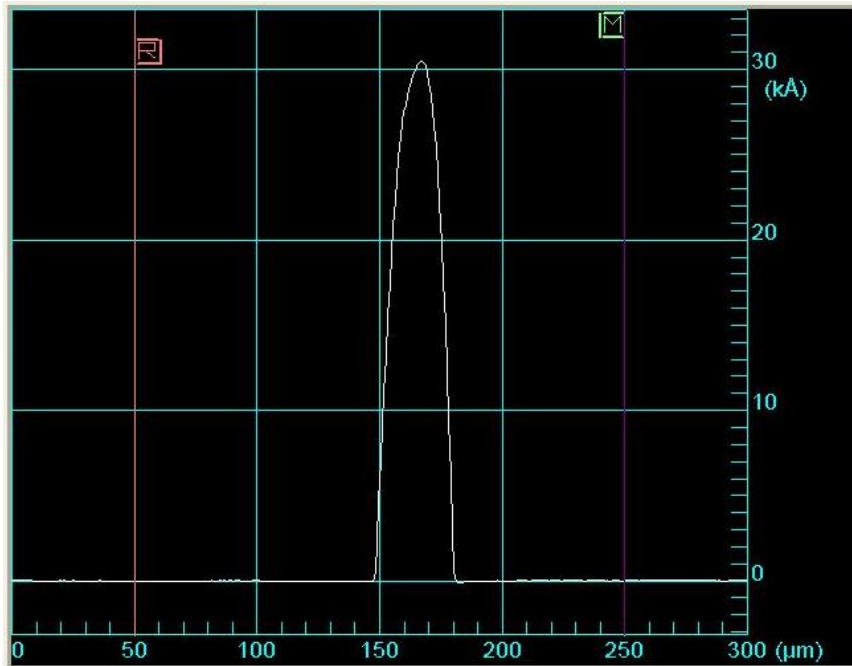


**Pre-CMP Step Height
22,000 Ang**

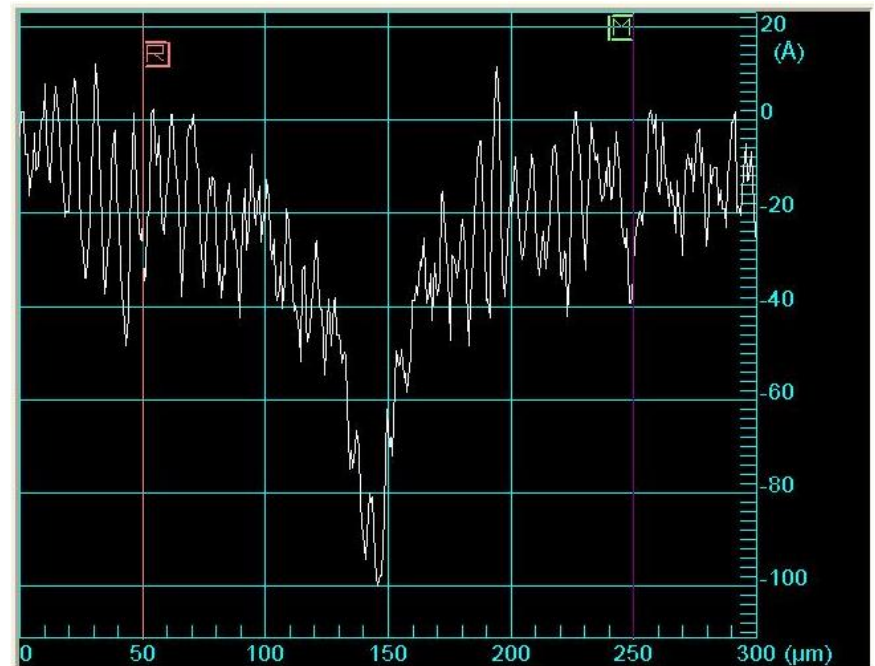


**Post-CMP Step Height
60 Ang**

Topography – Wfr 2



Pre-CMP Step Height
31,000 Ang



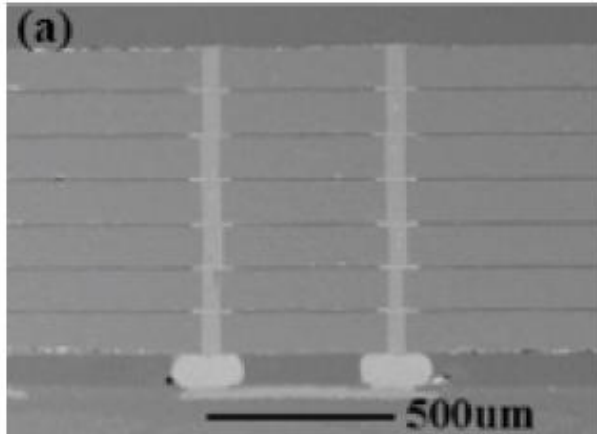
Post-CMP Step Height
100 Ang

Reveal Summary



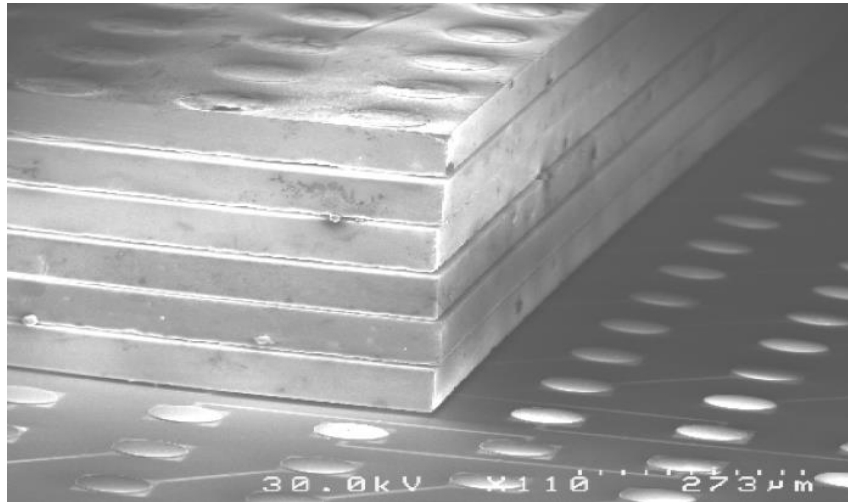
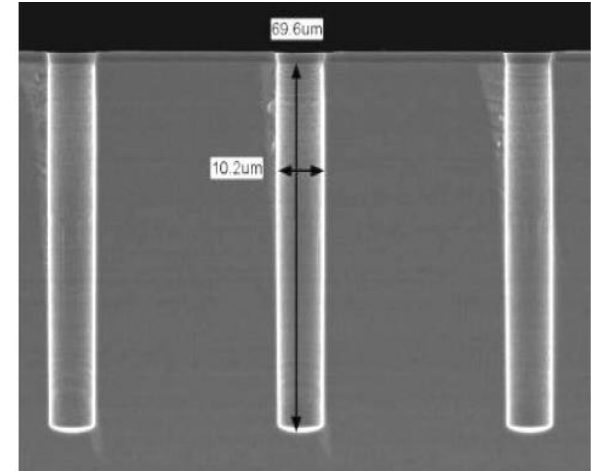
- Single Step Non-Selective TSV Reveal
 - Custom blended formulation for high Si rate and Cu removal
 - Si removal rate ≥ 1 $\mu\text{m}/\text{min}$
 - Low selectivity between Si and Cu ($< 2:1$)
 - Excellent topography control (< 400 nm)
 - Single step CMP ... only ONE slurry required
- TSV Reveal CMP After Highly Selective Si Etch
 - Integration demands oxide/nitride/Cu/barrier metal removal
 - Low selectivity among all materials
 - Excellent topography (< 100 nm) and good surface finish
 - Single step CMP ... only ONE slurry required

Examples



Stacked die (7 on 1)
Published by NASA/JPL

10um TSV (AR=7)
Published by UMC



Stacked die (6 high)
Published by IBM

Summary



- Through Silicon Via Technology (TSV)
 - Enabling many 3D integrations and growing rapidly
 - Most TSV flows rely on CMP twice – formation and reveal
- Areas for Further Optimization
 - Design rule consistency / standardization
 - Incoming variation at CMP (esp for thick Cu plating)
 - Selectivity control
 - TSV recess/protrusion
 - Automation and repeatability
 - Throughput
 - Cost per unit operation (slurry, pad life, etc.)

THANK YOU !



- Thank you to the following companies and individuals:
 - RTI International
 - Anji Microelectronics
 - Engineering Staff of Entrepix (Terry Pfau, Paul Lenkersdorfer, Donna Grannis)
- For more information, please contact:

Robert L. Rhoades, Ph.D.
Entrepix, Inc.
Chief Technology Officer
+1.602.426.8668
rrhoades@entrepix.com