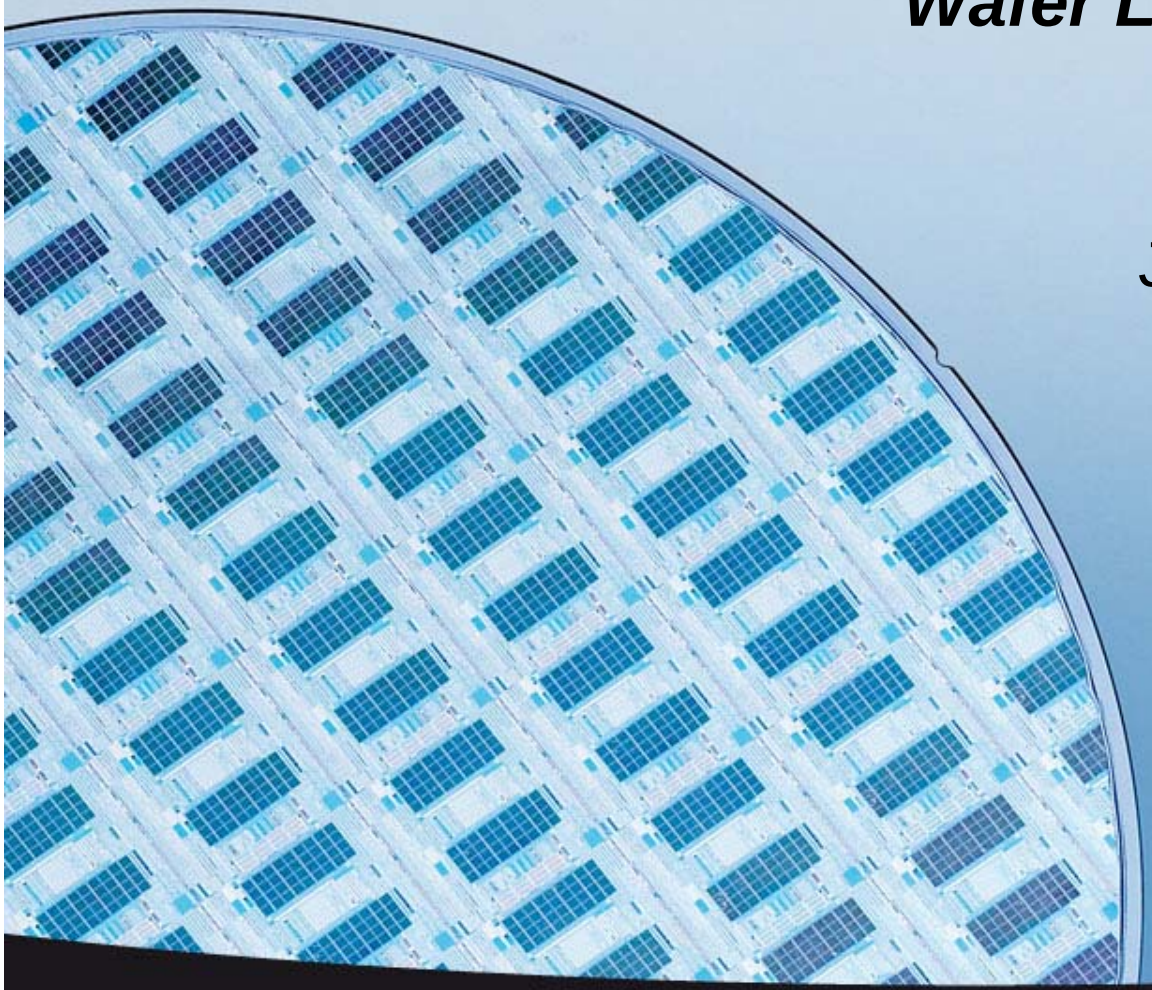
EV Group

Considerations When Selecting A Wafer Level Bonding Process



NCCAVS
Joint User Group Meeting
June 11, 2013

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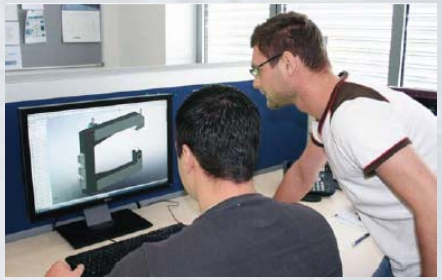
Best Known Practice for Selecting a Wafer Bonding Process

Outline

- EVG in a glance
- Overview of Bonding Processes
- Bonding Process Selection Flow
- Overview of Inputs
- Process Performance, Requirements & Conditions
- Cost Considerations
- Types of Alignment
- Bonding Process Variables
- Some Classic Problems

EVG – At a glance

- Founded in 1980 by Erich and Aya Maria Thallner as an engineering partner for the semiconductor industry
- Headquartered in Austria, with fully owned subsidiaries in the United States, Japan, South Korea and Taiwan; worldwide network of representatives
- More than 650 employees globally
- Recognized technology and market leader in wafer processing solutions for semiconductor, MEMS and nanotechnology applications
- Install base in excess of 1,700 tools in high volume production, university and industrial R&D institutions
- EVG continues to invest a significant percentage of our revenue in application-oriented research and development



Global Presence

EVG North America | EVG Japan | EVG Taiwan | EVG Korea

Fully owned subsidiaries
Representatives

invent
innovate
implement

Product Categories

EVG is a global supplier of:

- Wafer Bonders
- Aligners
- Coaters / Developers
- Temporary Bonders / Debonders
- Cleaners
- Inspection / Metrology Systems

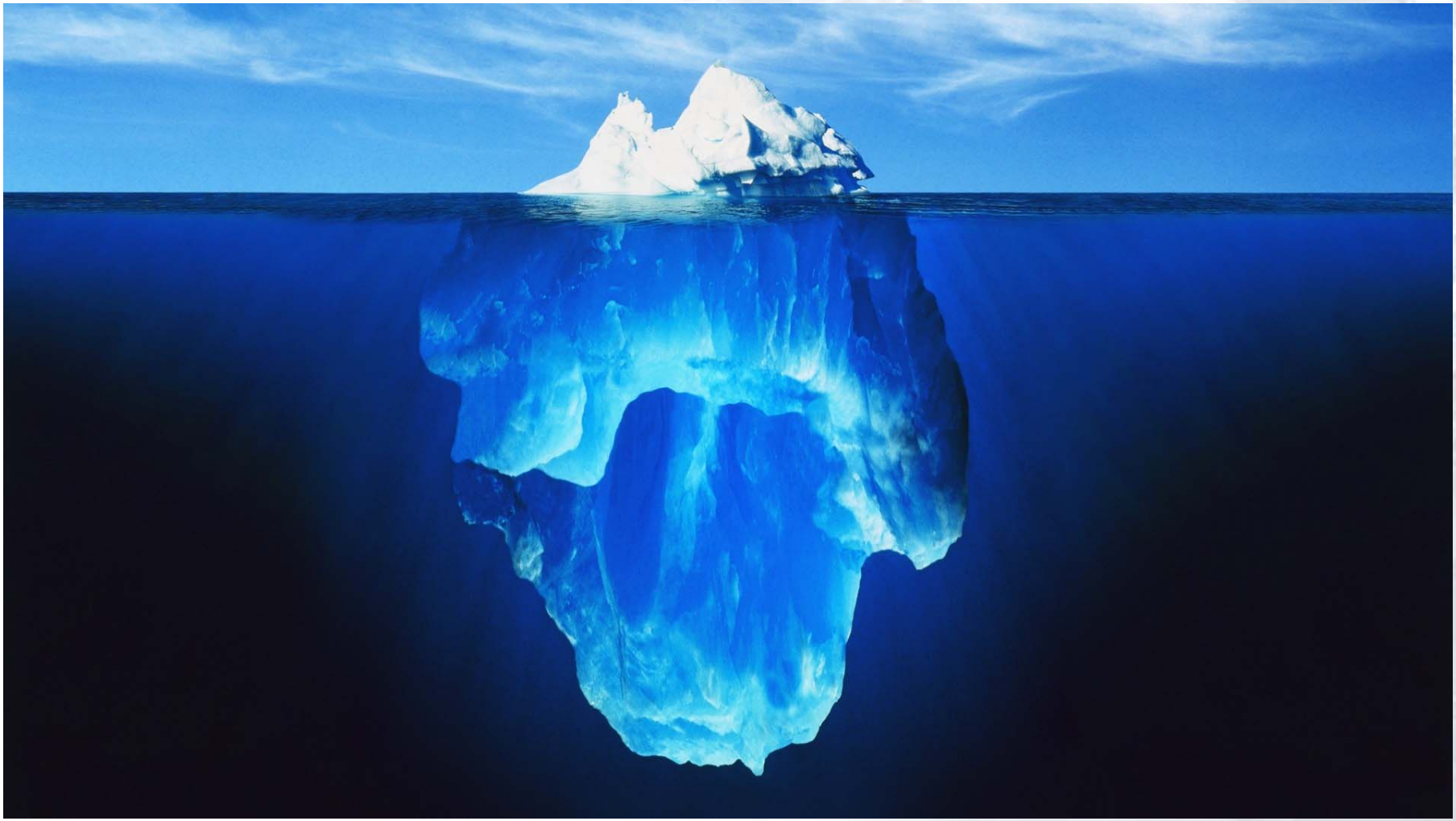
EV Group holds the dominant share of the market for wafer bonding equipment and is a technology leader in lithography for advanced packaging and nanotechnology.


Lithography

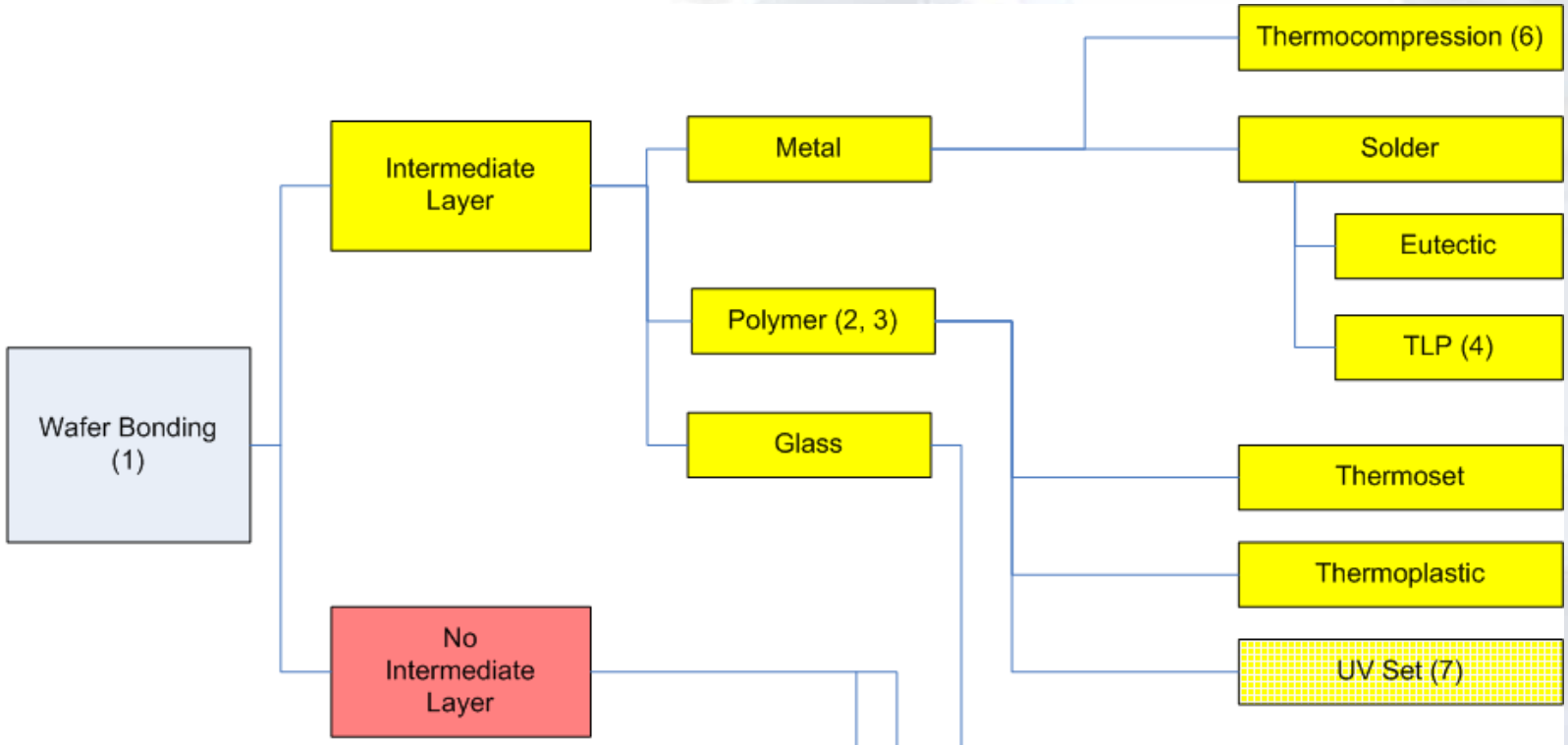

Bonding


Process Technology

That was the easy part

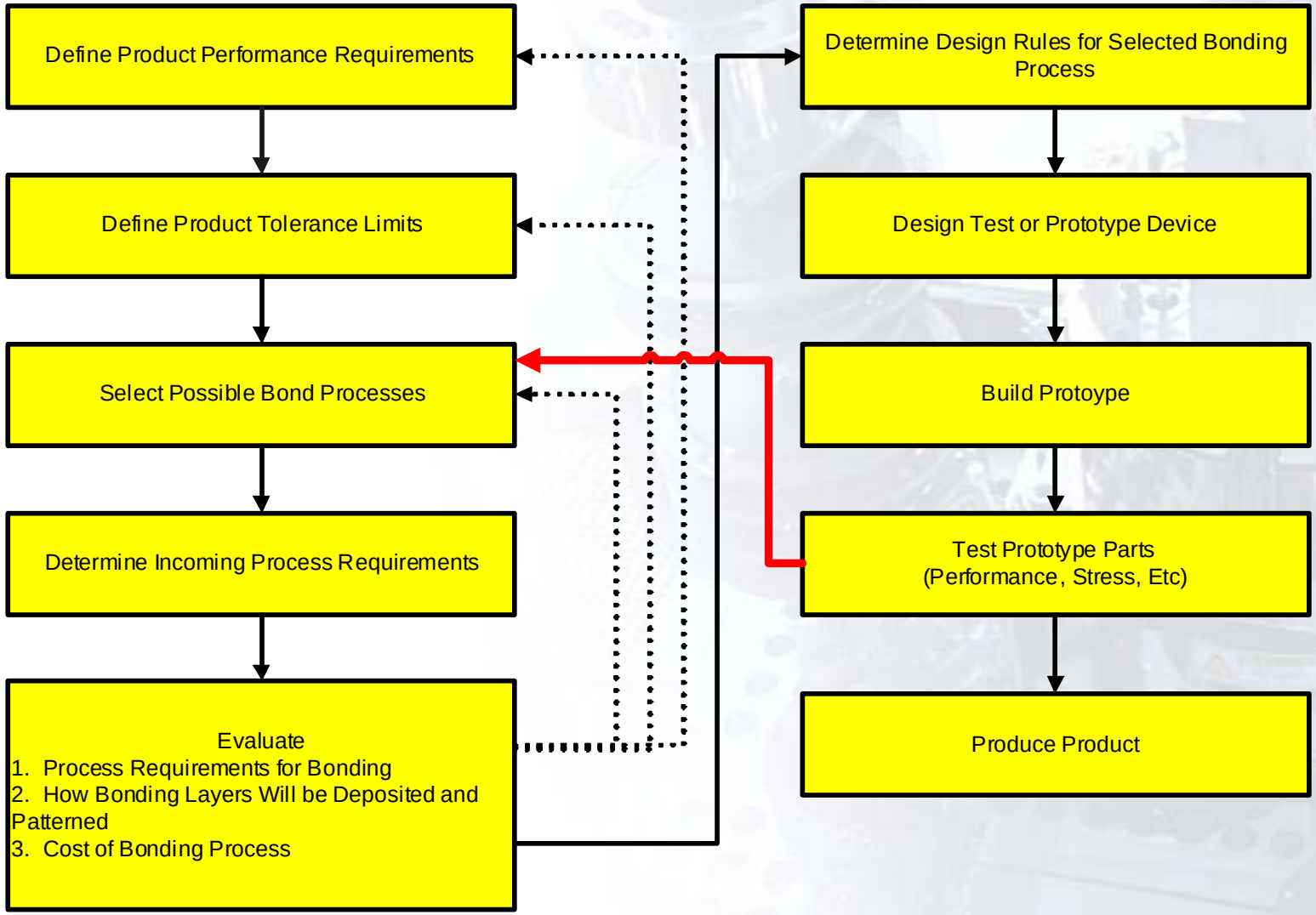


Best Known Practice for Selecting a Wafer Bonding Process



NOTES
1. May be mechanically or optically aligned. Bonding process will effect final alignment results
2. May be used for permanent or temporary bonding.
3. Inludes adhesive bonding
4. TLP – Transient Liquid Phase
5. Also called direct bonding or molecular bonding. Has strict requirements for flatness, surface finish, and contamination.
6. Also called metal diffusion
7. Requires special bond chamber.

Best Known Practice for Selecting a Wafer Bonding Process



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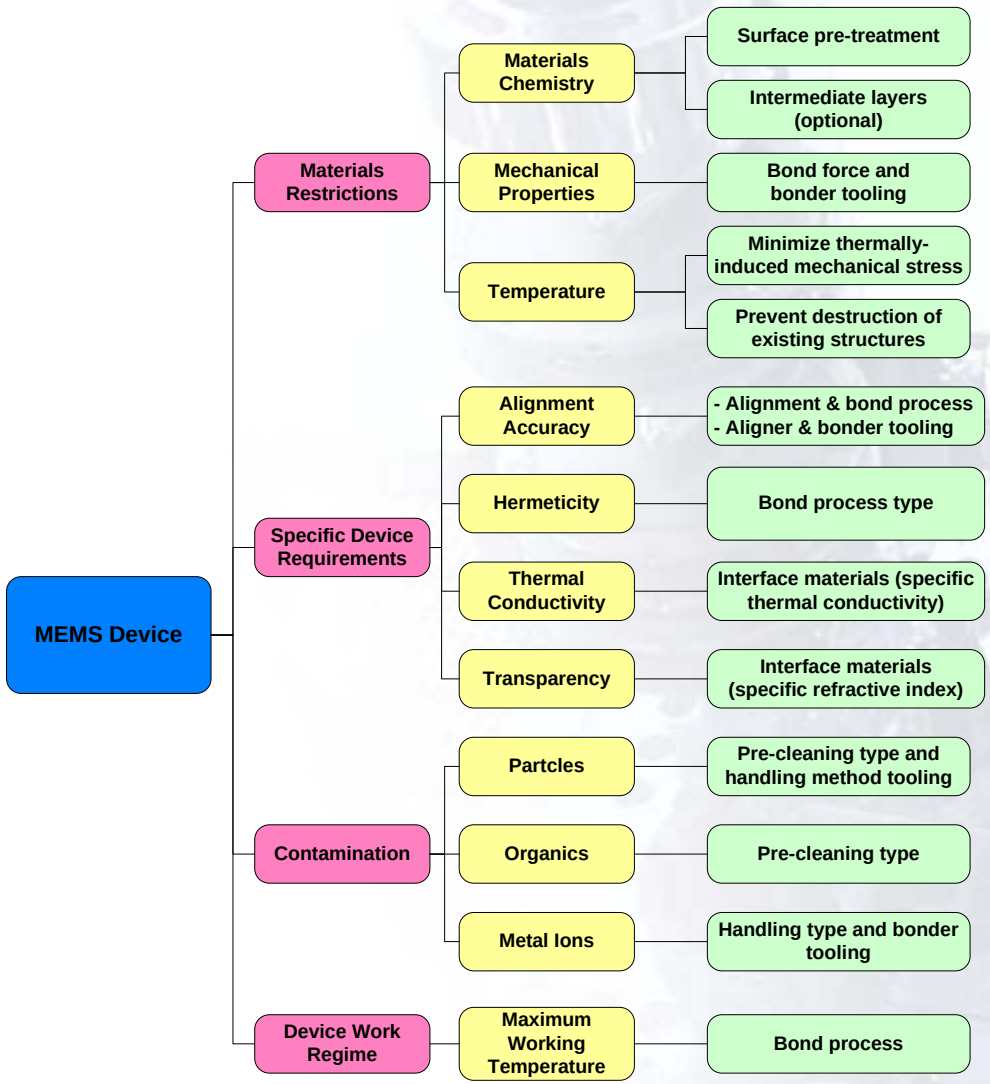


Best Known Practice for Selecting a Wafer Bonding Process
Process Performance

	No Intermediate Layer					Intermediate Layer					
Bonding Type	Anodic Bonding (Electric Filed)	Direct Bonding		Plasma Activated Direct Bonding		Glass Frit	Thermo Compression	Solder / Eutectic / TLP	Adhesive	Epoxy (Thermally Cured)	Epoxy (UV Cured)
Bonding Sub-Type		Hydrophilic	Hydrophobic	Hydrophilic	Hydrophobic						
CMOS Compatible	No	No	No	Yes	Yes	No	Yes	Some	Some	Yes	Yes
Electrically Conductive	No	No	No	No	No	No	Yes	Yes	No	No	No
Step Coverage	No	No	No	No	No	?	No	Yes	Yes	Yes	Yes
Hermeticity	Medium to High	Medium to High	Medium to High	Medium to High	?	Medium	High	High	Low	Low	Low
Current Manufacturing Volume	High Mature	High Mature	Very Low	High Mature	?	High Mature	Medium to High Mature	High Mature	High Mature	High Mature	High Mature
Mechanical Strength Sufficient for Backgrinding	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Maximum Post Bond Temperature	> 1000 °C	> 1000 °C	> 1000 °C	> 1000 °C	> 1000 °C	350 °C to 450 °C depending on material	Limited by selected metallurgy	Limited by selected metallurgy (TLP can be higher)	Low, limited by adhesive		

Best Known Practice for Selecting a Wafer Bonding Process
Incoming Requirements for Process

	No Intermediate Layer					Intermediate Layer					
Bonding Type	Anodic Bonding (Electric Filed)	Direct Bonding		Plasma Activated Direct Bonding		Glass Frit	Thermo Compression	Solder / Eutectic / TLP	Adhesive	Epoxy (Thermally Cured)	Epoxy (UV Cured)
Bonding Sub-Type		Hydrophilic	Hydrophobic	Hydrophilic	Hydrophobic						
Requires Planarized Surface	Yes	Yes	Yes	Yes	Yes	No*	Yes	No	No	No	No
Surface Roughness	≤ 20 nm	≤ 0.5 nm		≤ 2.0 nm		≤ 1000 nm	≤ 2.0 nm	≤ 1000 nm	≤ 1000 nm	≤ 1000 nm	≤ 1000 nm
Layer Thickness	NA	Oxide ≥ 500 Å	Challenge is removing oxide	Oxide ≥ 500 Å	Challenge is removing oxide	Determined by process	≥ 1000 nm per side	≥ 1000 nm per side	Highly Variable	Highly Variable	Highly Variable
Sensitivity to Particles	Medium	High	High	High	High	Low	Medium	Medium	Low	Low	Low
… to Bulk Contamination	Low	?	?	?	?	Low	High	Medium	Low	Low	Low
… to Oxide Growth	N/A	Low	High	Low	Very High	No	Layer dependent	Layer dependent	N/A	N/A	N/A
… to Surface Contamination	Medium	Very High	Very High	Very High	Very High	Medium	High	High	Low	Low	Low

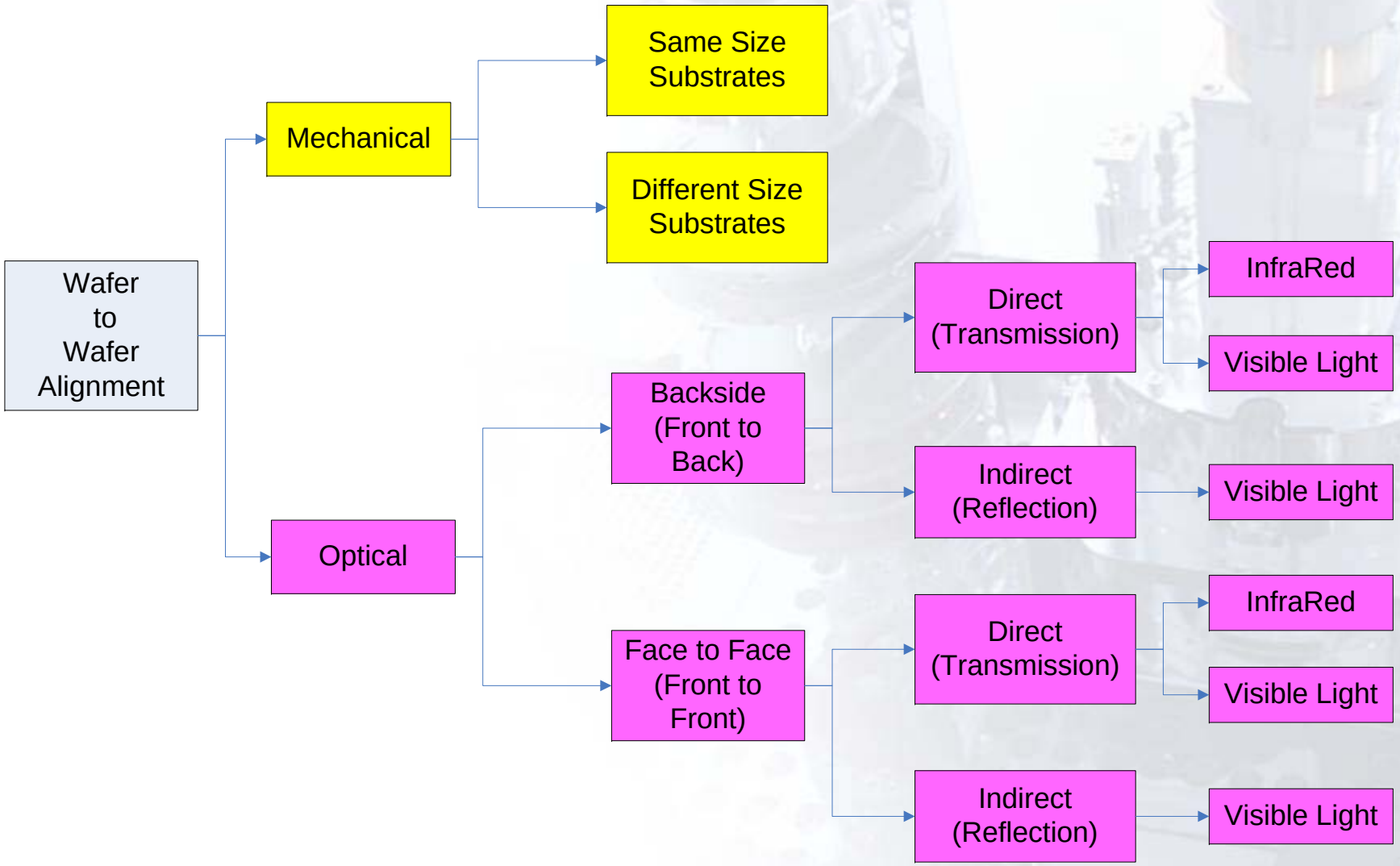
Best Known Practice for Selecting a Wafer Bonding Process Process Conditions

	No Intermediate Layer					Intermediate Layer					
Bonding Type	Anodic Bonding (Electric Filed)	Direct Bonding		Plasma Activated Direct Bonding		Glass Frit	Thermo Compression	Solder / Eutectic / TLP	Adhesive	Epoxy (Thermally Cured)	Epoxy (UV Cured)
Bonding Sub-Type		Hydrophilic	Hydrophobic	Hydrophilic	Hydrophobic						
Plasma Exposure	No	No	No	Yes	Yes	No	No	No	No	No	No
Cycle Time Activation	N/A	N/A	N/A	300 s	300 s	N/A	N/A	N/A	N/A	N/A	N/A
… Align	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes	≤ 10 minutes
… Bond	≤ 90 minutes	≤ 60 seconds	≤ 60 seconds	≤ 60 seconds	≤ 60 seconds	≤ 45 minutes	≤ 90 minutes	≤ 60 minutes	≤ 45 minutes	≤ 30 minutes	≤ 15 minutes
… Anneal		60 - 300 minutes	60 - 300 minutes	60 - 300 minutes	60 - 300 minutes						
Process Temperature	400 °C - 500 °C	1000 °C	1000 °C	R.T. and 200 °C - 400 °C		400 °C - 500 °C	300 °C - 500 °C	200 °C - 500 °C	≤ 200 °C	≤ 200 °C	R. T.
Force	Low	Low	Low	Low	Low	Medium	High	Low	Low	Low	Low
Vacuum During Bonding	Ambient to Hight	Ambient to Hight	Ambient to Hight	Ambient to Hight	Ambient to Hight	Ambient to Hight	Ambient to Hight	Ambient to Hight	Ambient to Low	Ambient to Low	Ambient to Low
Vacuum Level Possible	Low to Medium	Low	Low	Low	Low	Medium	High	Low	Low	Low	Low
Electric Field	Yes	No	No	No	No	No	No	No	No	No	No
Na^+ Present	Yes	No	No	No	No	No	No	No	No	No	No
Cleanroom Class	≤ 100	≤ 10	≤ 10	≤ 10	≤ 10	≤ 1000	≤ 10	≤ 100	≤ 100	≤ 1000	≤ 1000

Best Known Practice for Selecting a Wafer Bonding Process
Bonding Cost Considerations

- Upstream Processes
  - Cost
    - Materials
    - Throughput
    - Yield
  - Availability
    - Does process exist?
    - Does equipment exist?
  - Control Plan
- Bonding Process
  - Cost
    - Throughput
    - Yield
  - Availability
  - Control Plan
    - Metrology
      - Equipment
      - Test Structures

Best Known Practice for Selecting a Wafer Bonding Process
Types of Alignment for Bonding



Best Known Practice for Selecting a Wafer Bonding Process
How EVG Can Help

- Bond Process Selection
  - Access to our expertise
- Alignment Process Selection
  - Access to our expertise
- Applications Labs in
  - Tempe, AZ
  - Schärding Austria
  - Yokohama, Japan
- Demonstration Runs
- Process Development

Bonding Process Variables

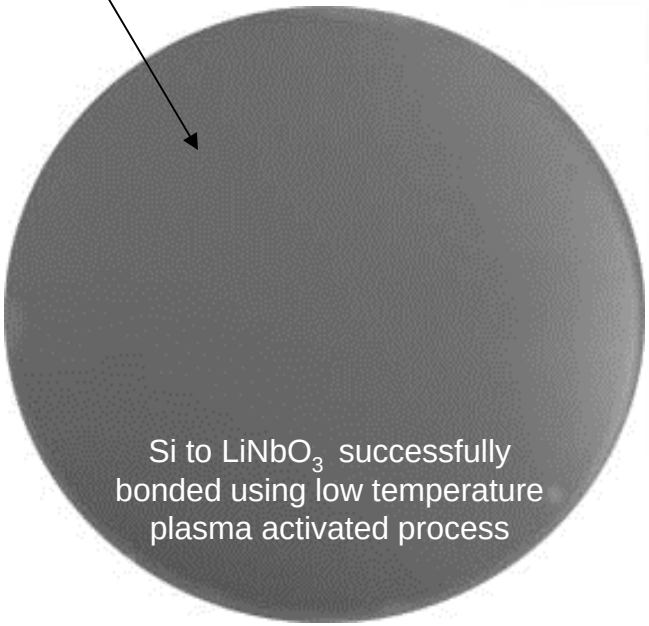
Incoming	In Chamber	Outgoing
1.Wafer a.Size i.Diameter ii.Thickness b.Material i.CTE c.Bow & Warp d.TTV e.Vacuum integrity[1]	1.Wafer	1.Wafer a.Bow & warp b.TTV c.Breakage
1.Contact Layers a.Thickness b.TTV c.Roughness d.Bulk Composition e.Surface Composition f.Surface Particles g.Surface Contamination h.Pattern	1.Standard Bond Chamber a.Time b.Temperature c.Force[2] d.Atmosphere[3] e.Wafer to wafer spacing (flags) f.Bow Pin g.Voltage / current 2.Special Bond Chamber a.UV energy b.Plasma 3.Materials a.T_g or Melting Point b.Outgassing c.Shrinkage d.Adhesion e.Flow	1.Bond Layers a.Percent bonded (voids) b.Thickness c.Strength d.Hermeticity e.Conductivity f.Pattern 2.Atmosphere in cavities if present a.Gas b.Pressure
1.Alignment 2.Spacing (gap between wafers)		1.Alignment 2.Wafer to wafer spacing

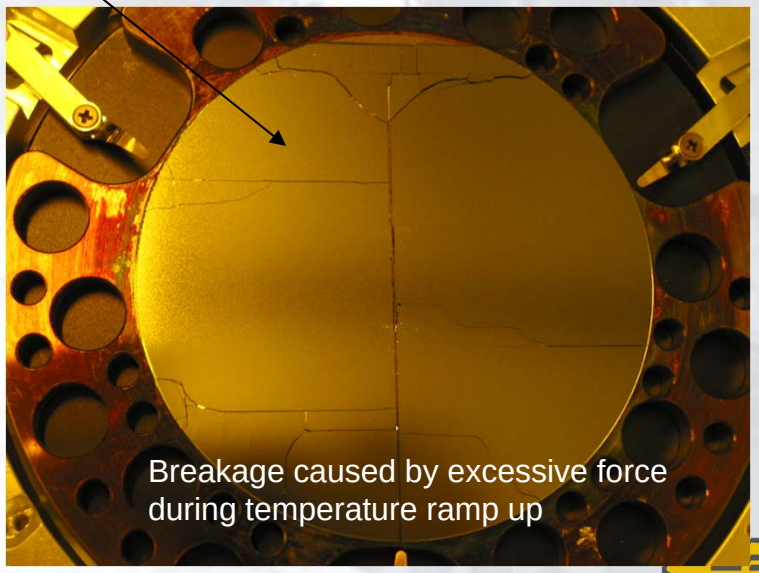
[1] Can the wafer be handled by backside vacuum or will edge handling or other special handling be required?
[2] Translates to pressure based on bond contact area
[3] Vacuum, forming gas, inert gas; no toxics or corrosive gasses.

Color Code
Items in RED are controlled by upstream process
Items in Green are controlled by alignment system
Items in BLACK are controlled by bond chamber
Items in BLUE are output variables

Best Known Practice for Selecting a Wafer Bonding Process
Classic Problems

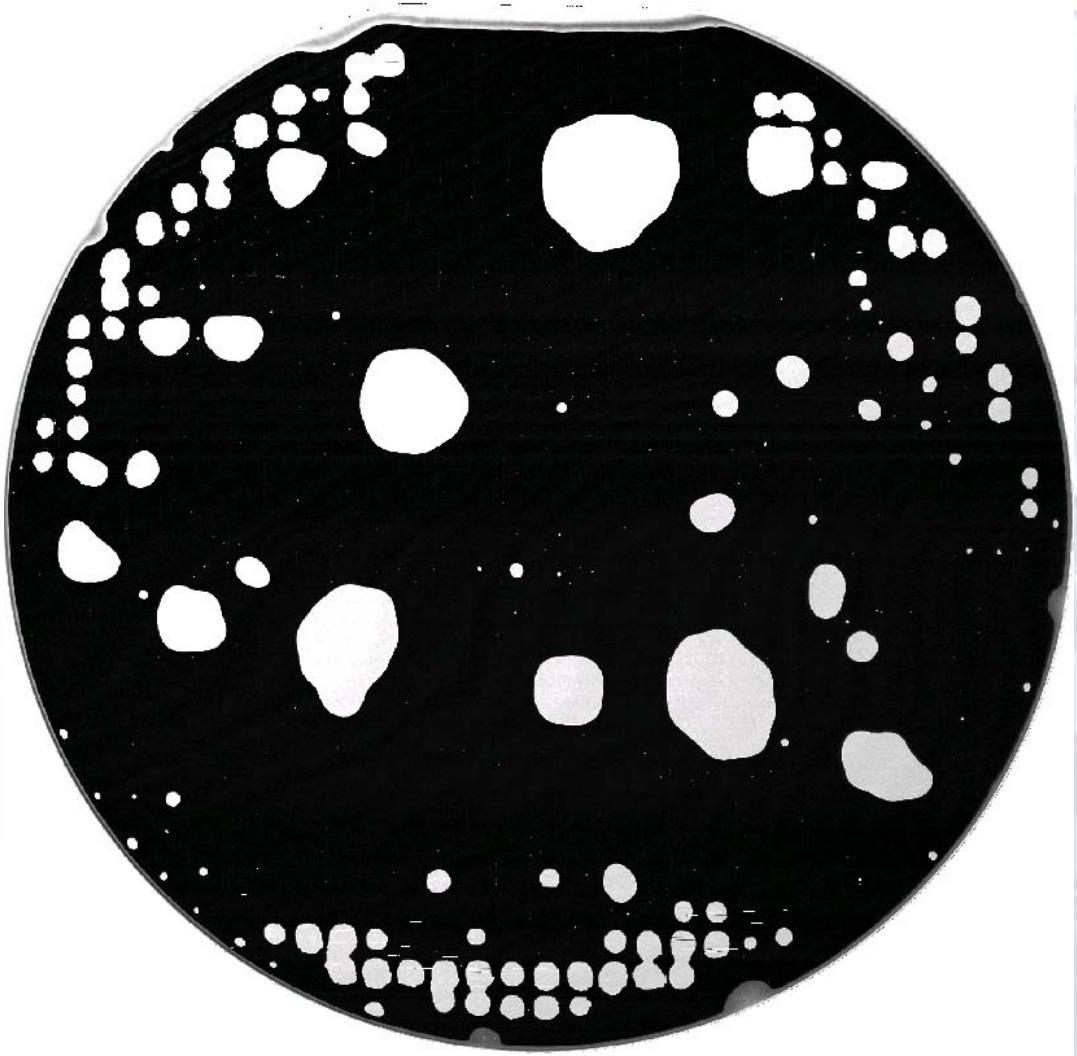
- Failure to consider TCE mismatch and bonding temperature
- Improper bonding recipe
- Success!





Best Known Practice for Selecting a Wafer Bonding Process
Classic Problems

- Poor planarization of CMOS wafer by CVD (Chemical Vapor Deposition) oxide deposition and CMP (Chemical Mechanical Polishing) resulting in voids. The regular die pattern is a classic signature of this problem
- SAM (Scanning Acoustic Microscopy) Image



Poor planarization of CMOS wafer (CVD oxide and CMP).

Acknowledgements

- Thank you to Tian Tang and Eric Pabo
- Special thank you to Lucia Feng

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Thank You for Your Attention

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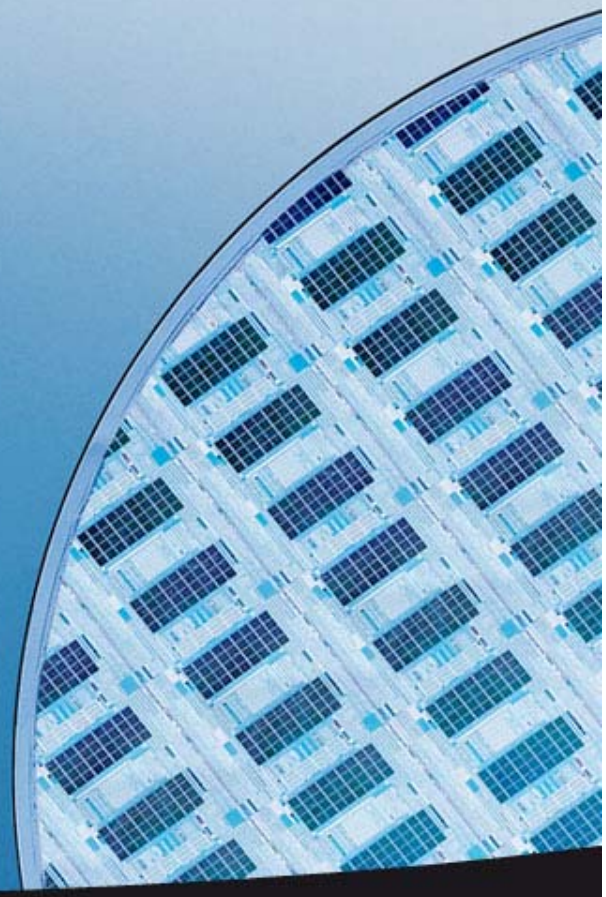
Triple i - The key to your success



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