3D Packaging for Memory Application
(NCCAVS Joint User Group Meeting)

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Outline

• Motivations for 3D Packaging Technology Adoption in Memory Space
  ◦ Memory Cost Scaling Challenge
  ◦ Power Efficiency Requirement
  ◦ Memory Sub-system Performance Demand

• Traditional 3D Packaging Technologies for Memory Application
  ◦ System-in-Package (SiP)
  ◦ Package-on-Package (PoP)

• Emerging TSV Based 3D Packaging Technologies for Memory Application
  ◦ Mobile Wide IO DRAM
  ◦ Hybrid Memory Cube (HMC)
  ◦ High Bandwidth Memory (HBM)

• Rambus 3D Package for Logic/Memory Application

• Summary
Memory Cost Scaling Challenge

Memory Cost Scaling Over Time

- ~30% YoY Reductions
- ~40% YoY Reductions
- 25-30% YoY Reductions

- NAND Cost/GB
- DRAM Cost/GB

Physical and Electrical Materials Limitations
Equipment Capability
Cost and Complexity

(Source: Mike Black, Micron, EDPS 2013)
Power Efficiency Requirement

- Scaling of I/O data rate with constant I/O power dissipation
- Even more challenging for computing memory subsystem memory bandwidth (BW) scaling

(Source: ITRS 2011 Roadmap & Dr. Bill Bottoms)
Memory BW Demand

- Packaging and interconnect technology vital in defining memory sub-system performance
- Traditional off-package interconnection between CPU and memory chip not going to scale, trends: on-package interconnection and 2.5D/3D interconnection

(Source: Intel Tech Journal August 2007)
Traditional 3D Packaging for Memory Application - SiP

- System-in-Package (SiP)
  - Die stacking using wire bond (WB) interconnects
  - Same memory die stacking for memory capacity (NAND or DRAM)
  - Logic/memory die stacking for memory bandwidth (BW)
  - Low cost solution
  - Limited BW scalability due to limited WB interconnect density
  - Know-Good-Die (KGD) concern

(Source: Internet)
Traditional 3D Packaging for Memory Application - PoP

- Package-on-Package (PoP)
  - Top memory package
  - Bottom logic package
  - Logic and memory packages separated for logistic control and KGD
  - Standard memory interface between top and bottom
  - Limited BW scalability due to limited interface memory bus width
  - Mainly for mobile application

(Source: Internet)
TSV Based 3D Packaging Technology for Memory Application – Wide IO DRAM

- Low power for mobile application
- Small formfactor
  - Thin profile
- High cost
- Complicate business model
  - Yield loss
  - Scrap management

<table>
<thead>
<tr>
<th></th>
<th>WideIO</th>
<th>LPDDR3</th>
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<tbody>
<tr>
<td>Power</td>
<td>1.2 volts</td>
<td>1.2 volts</td>
</tr>
<tr>
<td>Speed</td>
<td>200 Mbps</td>
<td>1600 Mbps</td>
</tr>
<tr>
<td>Data width</td>
<td>512 bits</td>
<td>32 or 64 bits</td>
</tr>
<tr>
<td>Data rate</td>
<td>single</td>
<td>double</td>
</tr>
<tr>
<td>Maximum channel bandwidth</td>
<td>12.8 Gbps</td>
<td>@32 bits -- 6.4 Gbps</td>
</tr>
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</table>
Wide IO DRAM Stacking vs. PoP

- Conventional PoP Solution (package-on-package)
- Direct Chip Connection using TSV (TSV-micro bump joint)

Package Size: 35%
Power Consumption: 50%
Bandwidth: 8x

Note: Wide IO DRAM (512bits @ 200MHz SDR)
TSV Based 3D Packaging Technology for Memory Application – Hybrid Memory Cube (HMC)

(Source: HMCC, Micron)
Hybrid Memory Cube (HMC)

Fast process logic and advanced DRAM design in one optimized package

- Power Efficient
- Smaller Footprint
- Increased Bandwidth
- Reduced Latency

(Source: MemCon Memory Conference 2012)
HMC Link Controller Interface

HMC (Gen2) has Four Links

Each Link has 32 differential Lanes

(*) HMC-SR supports up to 15Gbps SERDES options

Designed with Off-the-Shelf, High Speed SerDes Interface

### Link Interface Examples

4 Link Example (160GB/s)
- 10Gb/s per lane
- 32 lanes per link (320Gb/s = 40Gb/s)
  - 16 TX and 16 RX
- 4 Links (40Gb/s x 4) = 160GB/s

(*) Aggregate DRAM peak bandwidth remains 160GB/s

- Up to 15X the bandwidth of a DDR3 module
- 70% less energy usage per bit than existing technologies
- Occupying nearly 90% less space than today’s RDIMMs

(Source: Mike Black, Micron, EDPS 2013)
HMC Application

Through-Silicon Vias (TSV)

(Source: J. Thomas Pawlowski, Micron, Hot Chips 23, 2011)
TSV Based 3D Packaging Technology for Memory Application - High Bandwidth Memory (HBM)

(Source: SK/Hynix, Jan 2013)
High Bandwidth Memory (HBM)

Major Features of HBM

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wide I/O</td>
<td>Stacked DRAM</td>
</tr>
<tr>
<td></td>
<td>with TSV</td>
</tr>
<tr>
<td>GDDR5</td>
<td></td>
</tr>
<tr>
<td>x32</td>
<td>IO</td>
</tr>
<tr>
<td>7Gbps</td>
<td>Data Rate</td>
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<td>1.5V</td>
<td>Voltage</td>
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<tr>
<td>HBM</td>
<td></td>
</tr>
<tr>
<td>x 1024</td>
<td>Voltage</td>
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</tbody>
</table>

(Source: SK/Hynix, Jan 2013)
Markets for TSV Based 3D Packaging Technologies

(Source: Internet)
Rambus 3D Package for Logic/Memory

- Introduction

- CPU/GPU performance often constrained by both insufficient memory bandwidth and excessive memory power
- Stacked CPU/GPU and DRAM (using TSV) poses significant challenges to thermal management and power delivery
- One solution is double-sided flip-chip package with a processor on top and stacked DRAMs on bottom
- Middle-ground approach between traditional package-to-package, on-PCB solutions and pure-3D integration
- Processor interfaces with memory directly through package
- Very high IO density and low-loss interconnect paths
- Thermally decoupled processor and memory devices

(Package co-design & optimization: Secker D.; et al., ECTC 2012)
3D Package Physical Architecture

- Organic Substrate and Assortment of BEOL Technologies
  - Controller and DRAM stack share a 5-2-5 organic substrate
  - RDL on Controller and DRAM
  - Disaggregated DRAM with fine-pitch TSV’s
  - 256 GB/s peak DQ bandwidth across 800 diff. pairs (4 Gb/s per pair)

(Package co-design & optimization: Secker D.; et al., ECTC 2012)
Thermal Design

- High power of stacked memory with high-performance processor creates thermal management issue in 3D IC
- Thermal isolation achieved mounting components on opposite sides of package substrate
- Memory stack cooled using combination of thermal interface material, PCB thermal vias and back-side heat sink

(Package co-design & optimization: Secker D.; et al., ECTC 2012)
3D Package Implementation

Controller and DRAM Floorplans

Controller Die
- 12.3 x 21.6mm
- 200um C4 pitch

Organic Package Substrate
- 35x35mm outline
- Thin-core 5-2-5 buildup
- 718 BGA (1mm pitch)
- ~ 8800 C4 (total)

(A 256GB/s Memory Subsystem Built Using a Double-Sided IC Package with a Memory Controller and 3D-Stacked DRAM: Best S.; et al., DesignCon 2013)
Rambus 3D Package for Logic/Memory
Summary

• Cost scaling, power efficiency and bandwidth are three main factors that drive the adoption 3D packaging technology for memory application.

• Traditional 3D packaging technologies like SiP and PoP have reached the scaling limit for performance and power efficiency.

• Emerging TSV based 3D packaging technology shows great potential for scaling but many issues have to be resolved before it could be a mature technology.

• Rambus 3D packaging technology for logic/memory application bridges both mature technologies and advanced 3D IC technology and shows great potential for immediate implementation.
Thank you

rambus.com