Ultratech

# Technology and Economic Considerations for High Volume HBLED Lithography Manufacturing

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# Topics for Discussion

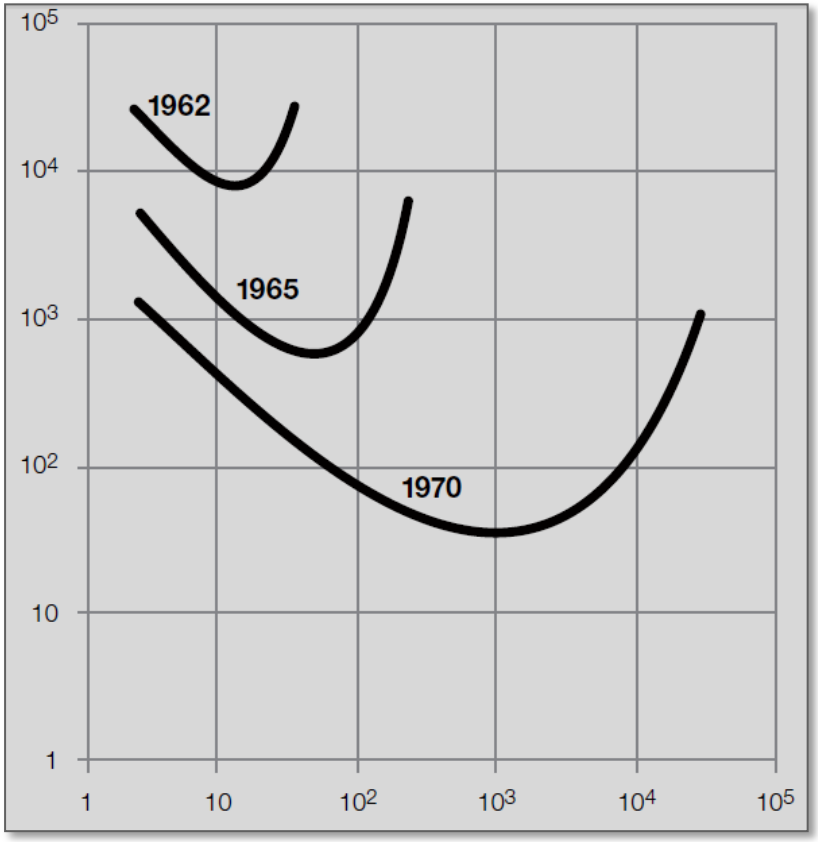
- Market Momentum
- Key Lithography Considerations
- Technology and Economic Considerations
- Summary

# HBLED Market Momentum

## (LED Lighting Only Accounts for Small Portion of Worlds Lighting)

# HBLED Market Momentum

## (Semi Market Perspective)




Moore's Law Illustration

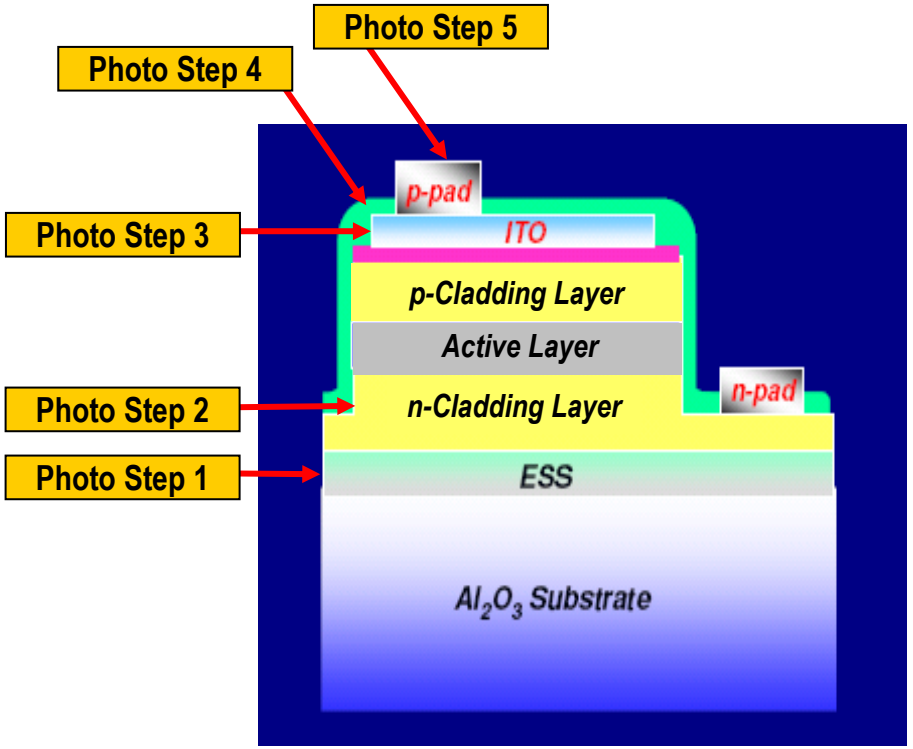
### Highlights

- HBLED industry will follow similar manufacturing path as established semiconductor market segment
- Intense focus on technology and productivity enhancement will reduce cost thereby driving demand

# Key Lithography Challenges

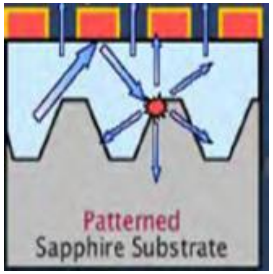
## Highlights

- Challenges during photolithography process include fine resolution exposure for PSS and metal pad layers, alignment for rough epi layers and warped wafer processing
- Use of 1X technology offers significantly superior technical and economic solutions for HBLED manufacturing



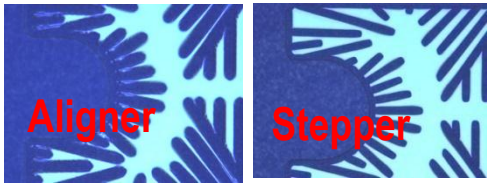

**LED Device Fabrication Requires Multiple Lithography Process Steps**

# Key Lithography Challenges



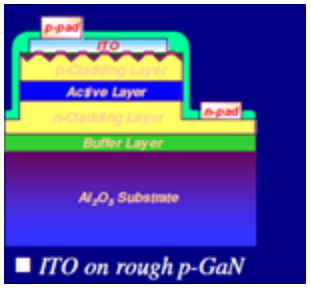

**PSS Layer Considerations**

- Use of PSS layer increases light extraction efficiency




**Pad Layer Considerations**

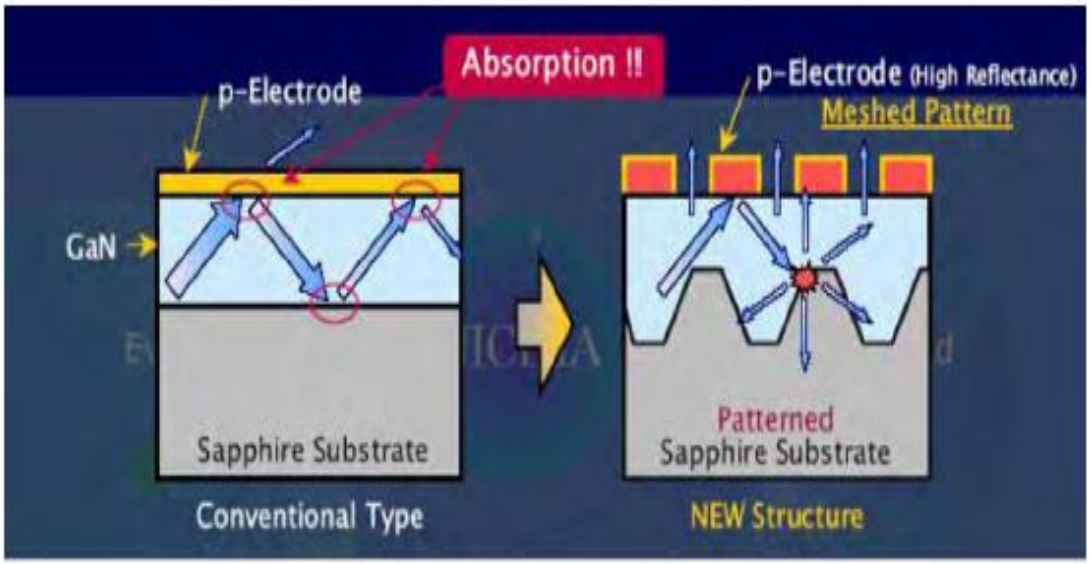
- Smaller metal pad geometries provide superior brightness




**Process Considerations**

- Use of unique process requires new feature development

# Key Lithography Challenges
## (Photolithography Process: PSS Layer)

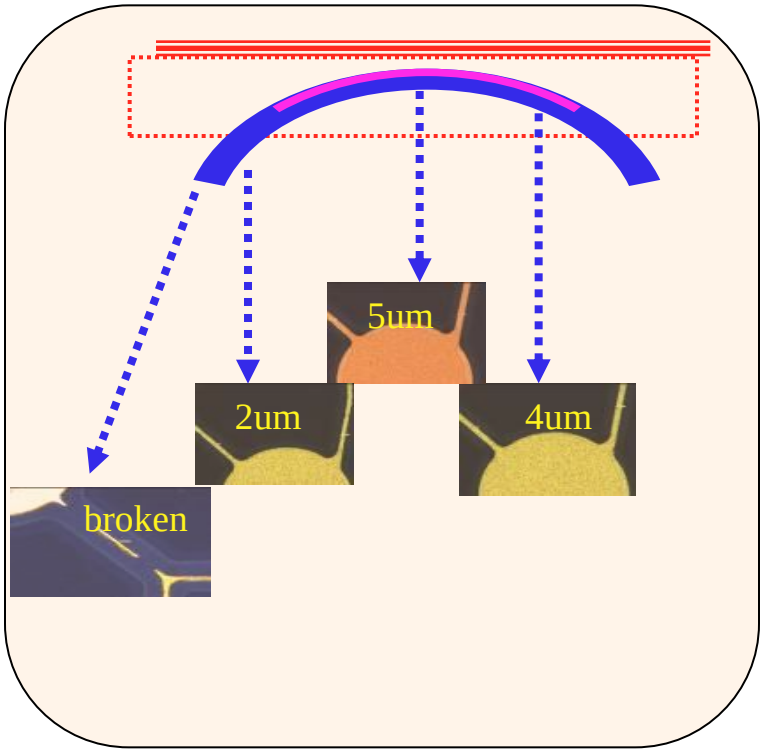



**Transition to PSS Substrates Requires Use of Projection Lithography Technology**

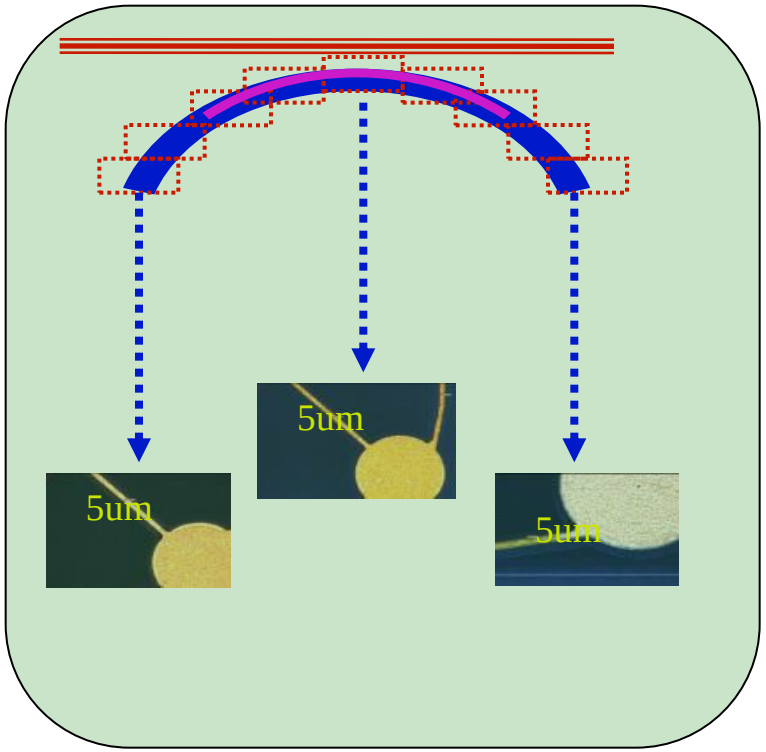
### Highlights

- Patterned Sapphire Substrate (PSS) technology is used to enhance the light extraction efficiency
- Transition to fine resolution PSS necessitates use of projection lithography technology

# Key Lithography Challenges
## (Photolithography Process: Metal Pad Layer)

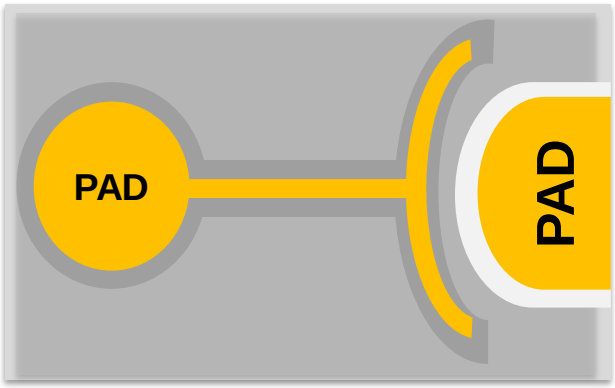



Mask Aligner Performance

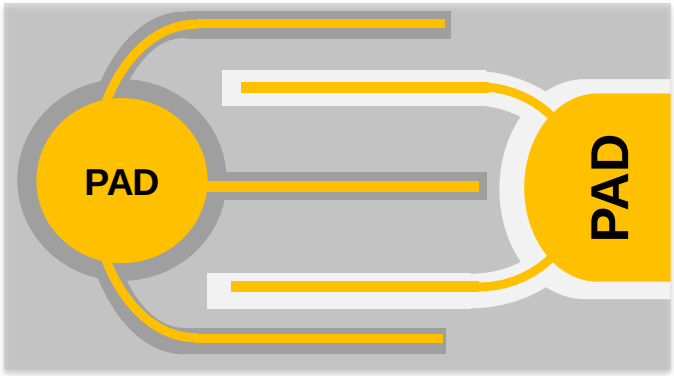



Projection Lithography Performance

# Key Lithography Challenges
## (Photolithography Process: Metal Pad Layer)




**Classic Current Finger Design**

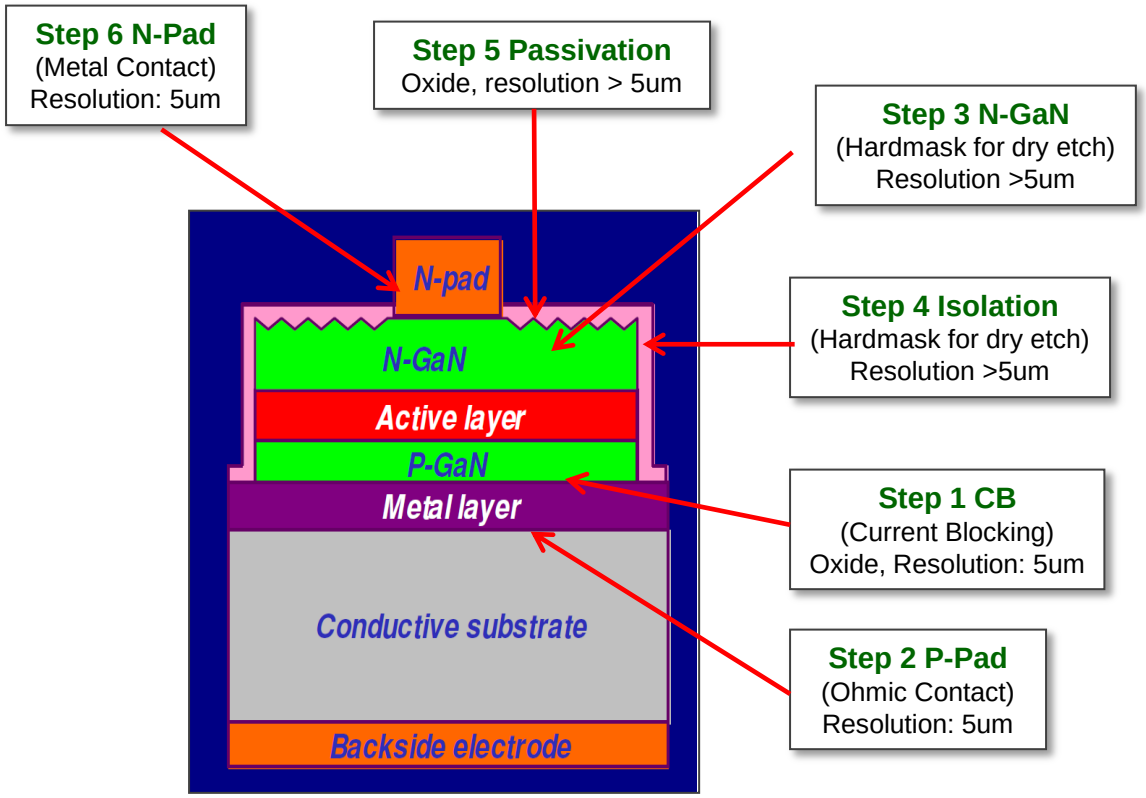



**Advanced Current Finger Design for Maximum Light Extraction**

### Highlights

- Advanced current spreading finger layout with reduced width will significantly improve the light output
- Use of projection lithography meets the imaging requirements without any impact to product yield

# Key Lithography Challenges
## (Photolithography Process: VLED)

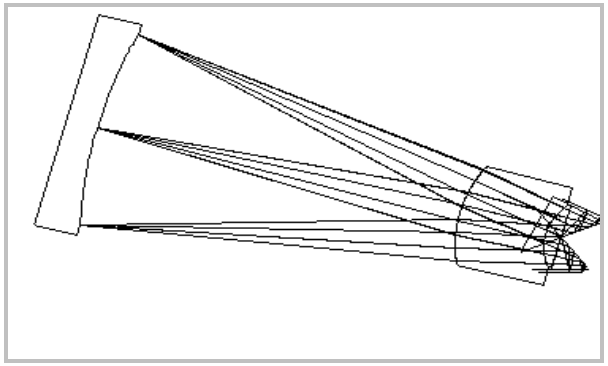



VLED Illustration

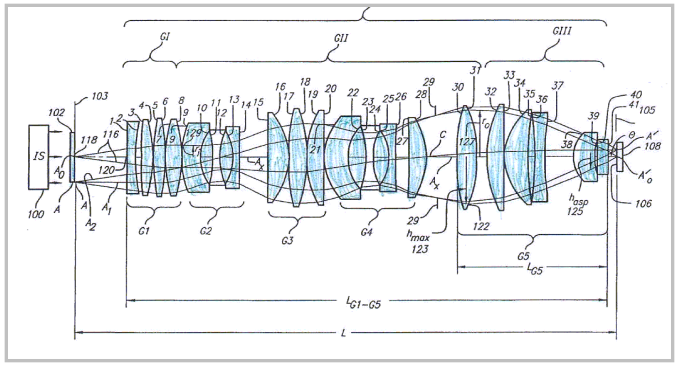
## Highlights

- Most HBLED companies are developing a vertical LED structure for solid state lighting applications
- VLED structure provides more uniform current flow, effective heat dissipation and maximum use of active sapphire substrates

# Key Lithography Challenges
## (Imaging Performance)



1X LENS ILLUSTRATION




REDUCTION STEPPER LENS

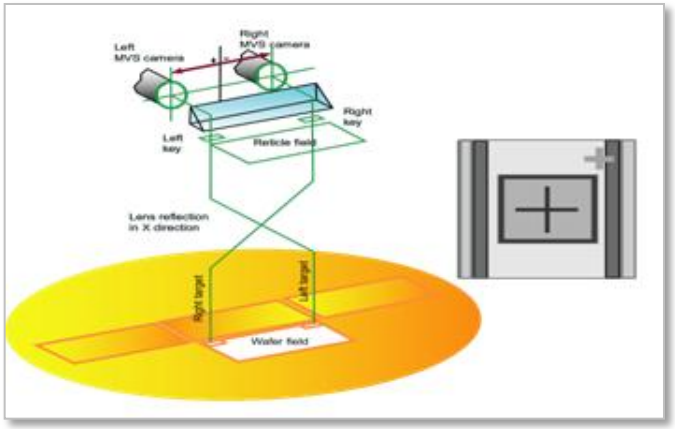
### 1x Lens Highlights

- Robust 1X lens design with low numerical aperture for large depth of focus for maximum process flexibility

### Risks with Reduction Lens

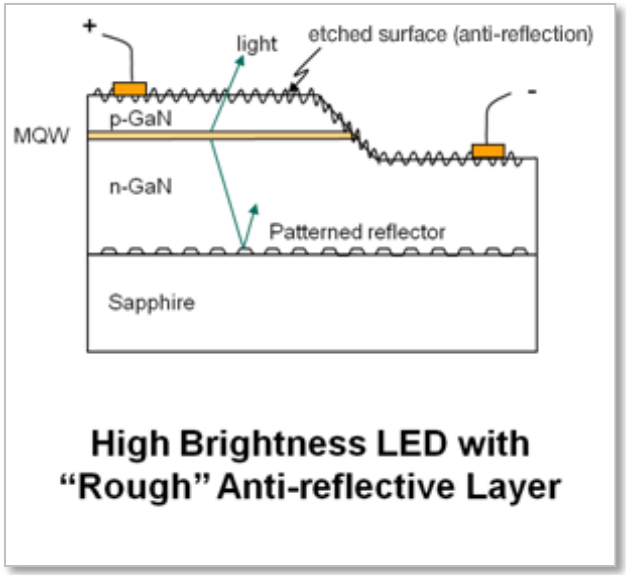
- Narrow depth of focus from a high numerical aperture system is not suited for warped LED substrate

# Key Lithography Challenges
## (Alignment Performance)




### Highlights of Off-Axis Alignment System

- Production-proven alignment for thick resist applications. Both top-side and off axis alignment systems use pattern recognition for operational flexibility

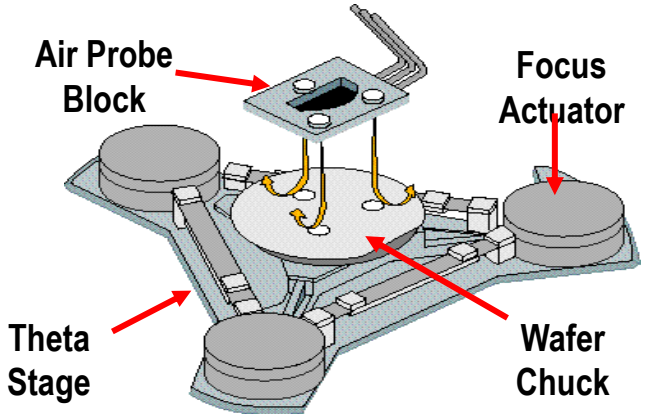



**High Brightness LED with "Rough" Anti-reflective Layer**

### Secondary Alignment Solution

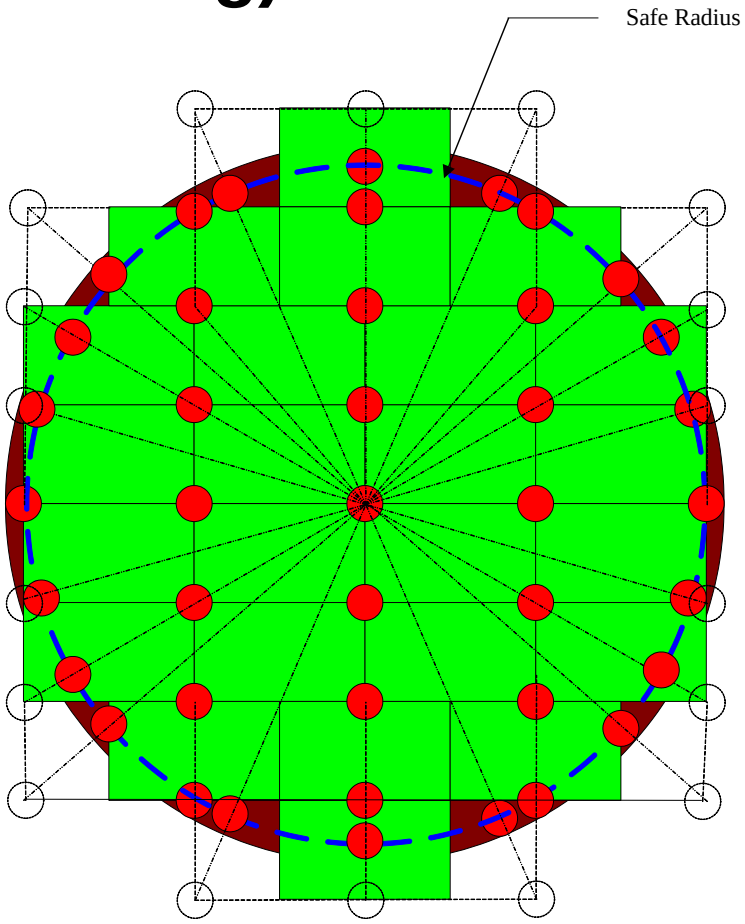
- Target recognition is a concern for certain process layers. Production proven unique off axis alignment solution for certain process levels

# Key Lithography Challenges
## (Warped Wafer Handling)



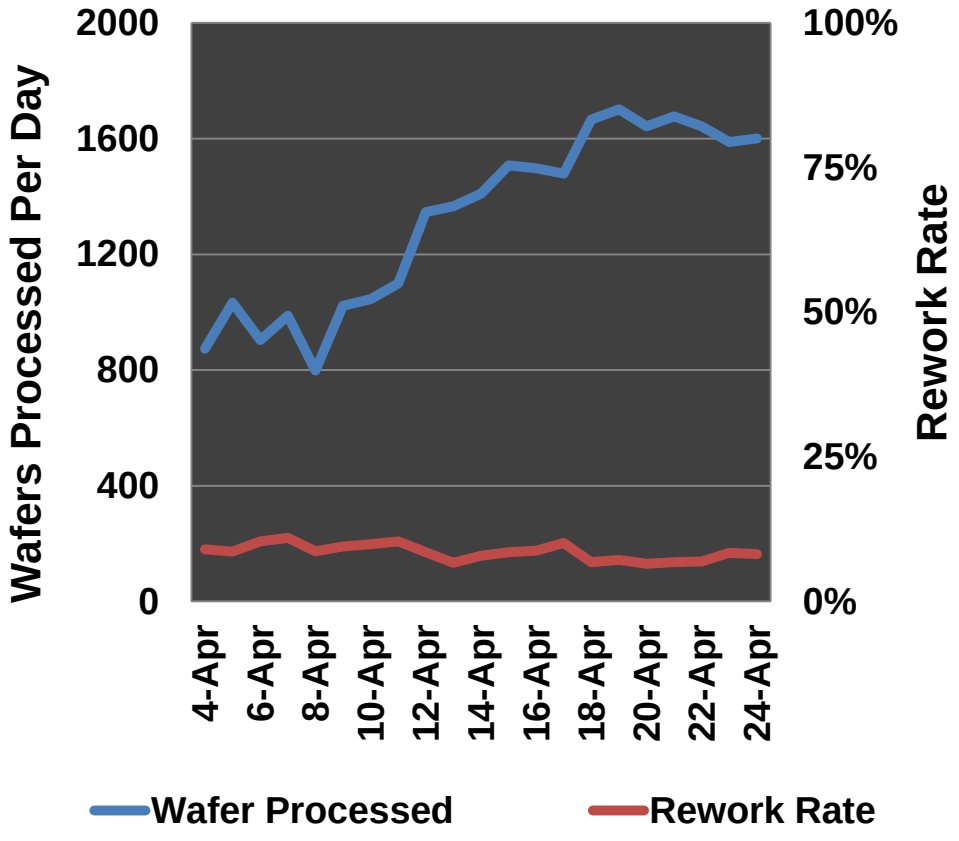

### Highlights

- Generates focus map of entire wafer before exposure
- Determines local tilt and applies corrections during exposure
- User can add, delete or move mapping points from the GUI




Grid Focus Alignment Illustration

# Technology and Economic Considerations
## (PSS Production)

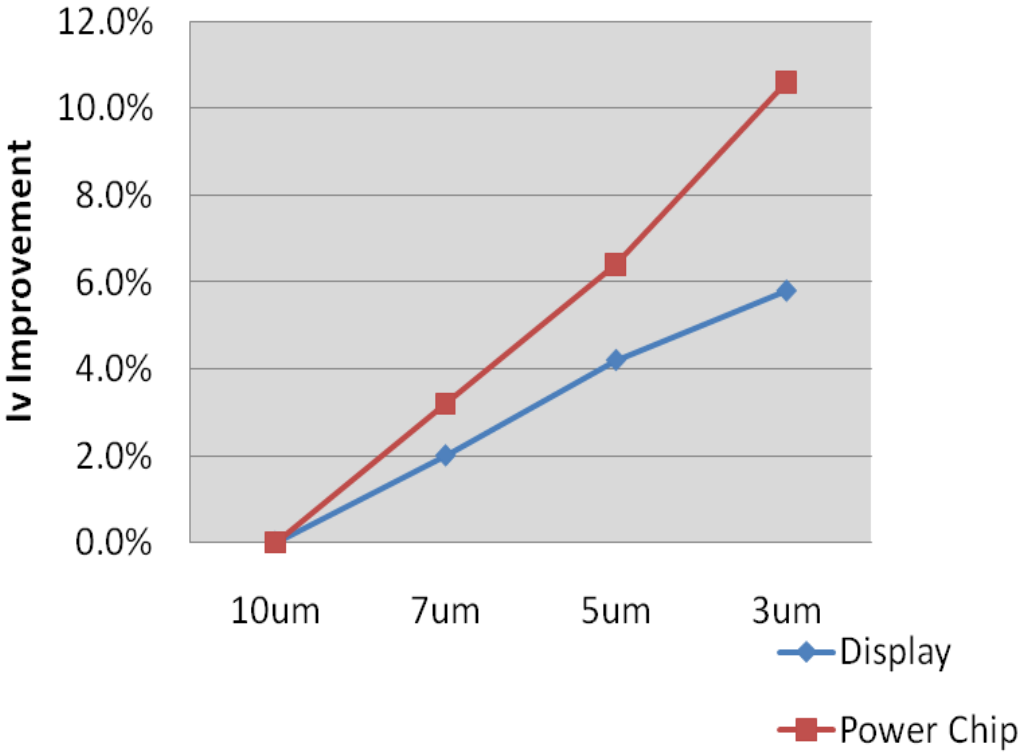



PSS Production Performance
(Feature Size: 2 x 1 micron)

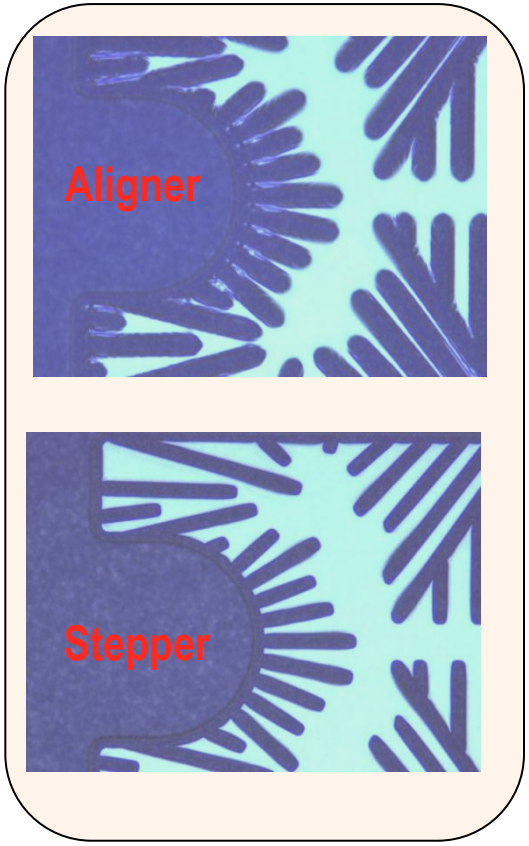
### Highlights

- Tools with Warped Wafer Handling Capabilities have demonstrated robust production performance for leading edge PSS geometry

# Technology and Economic Considerations
## (Chip Production)

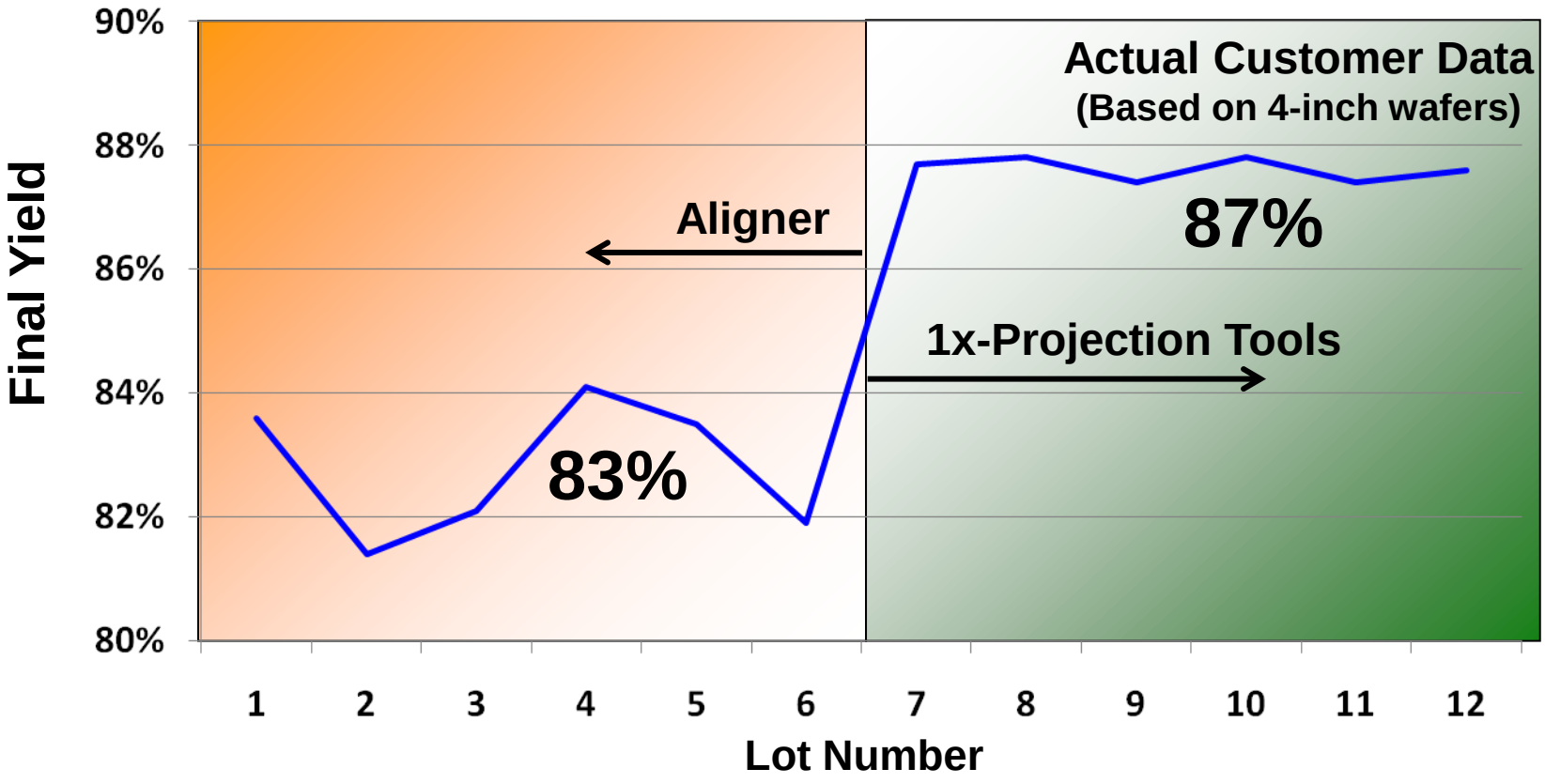



**Brightness Curve for Current Spreading Layer Width**



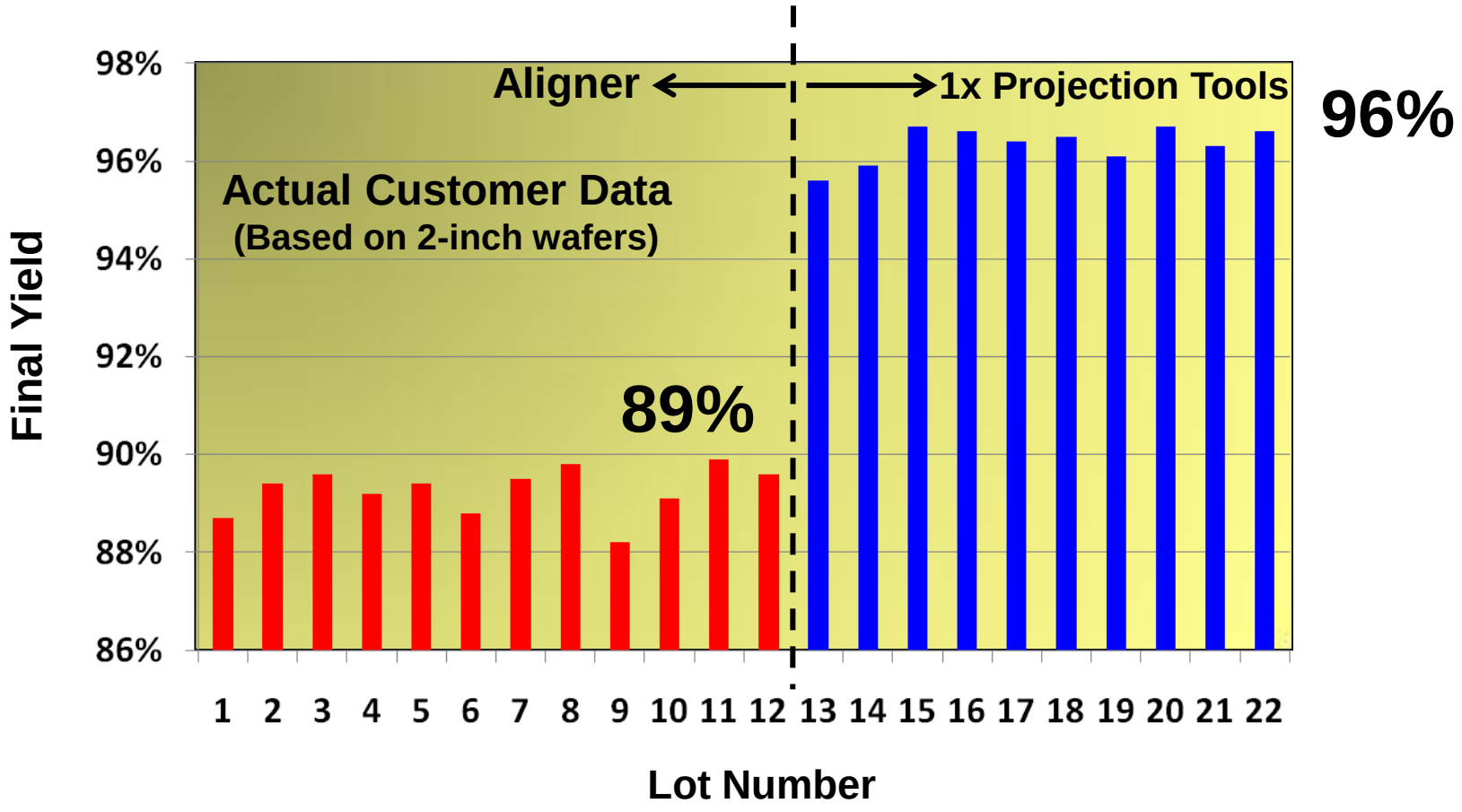

**Performance Comparison**

# Technology and Economic Considerations
## (Yield Comparison for Display Chips)

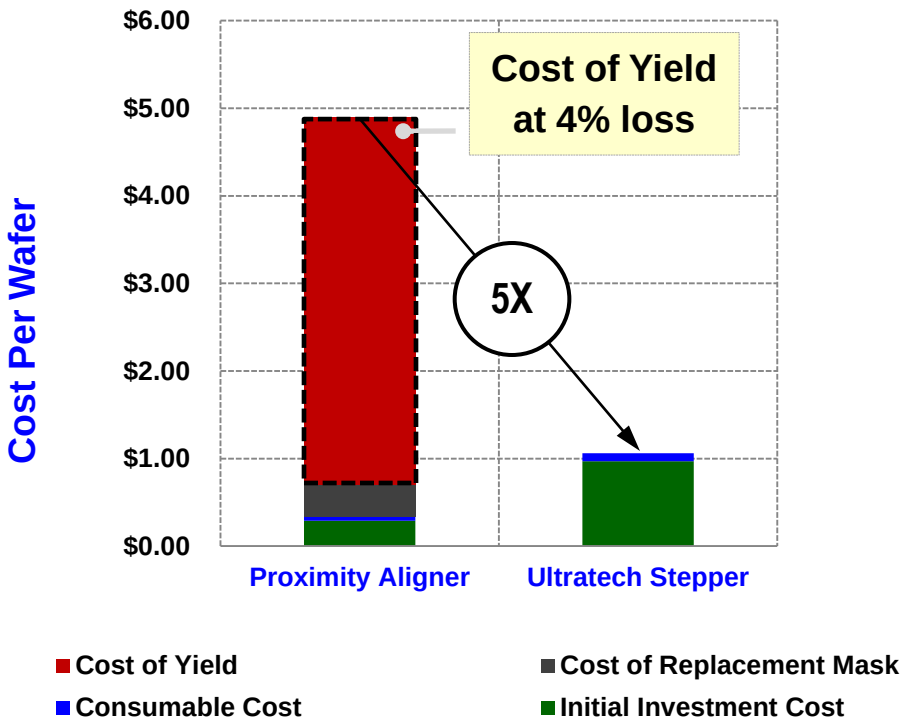


# Technology and Economic Considerations

## (Yield Comparison for Power Chips)



# Technology and Economic Considerations
## (Pay Back Period and Return on Investment)




### Highlights

- 1x Projection tools enable cost effective LED production and significant operational cost savings (>10M) over the useful life of equipment

### EVC Comparison

Significant yield savings result in a past pay back period (~20 weeks)*

# Economic Value Considerations

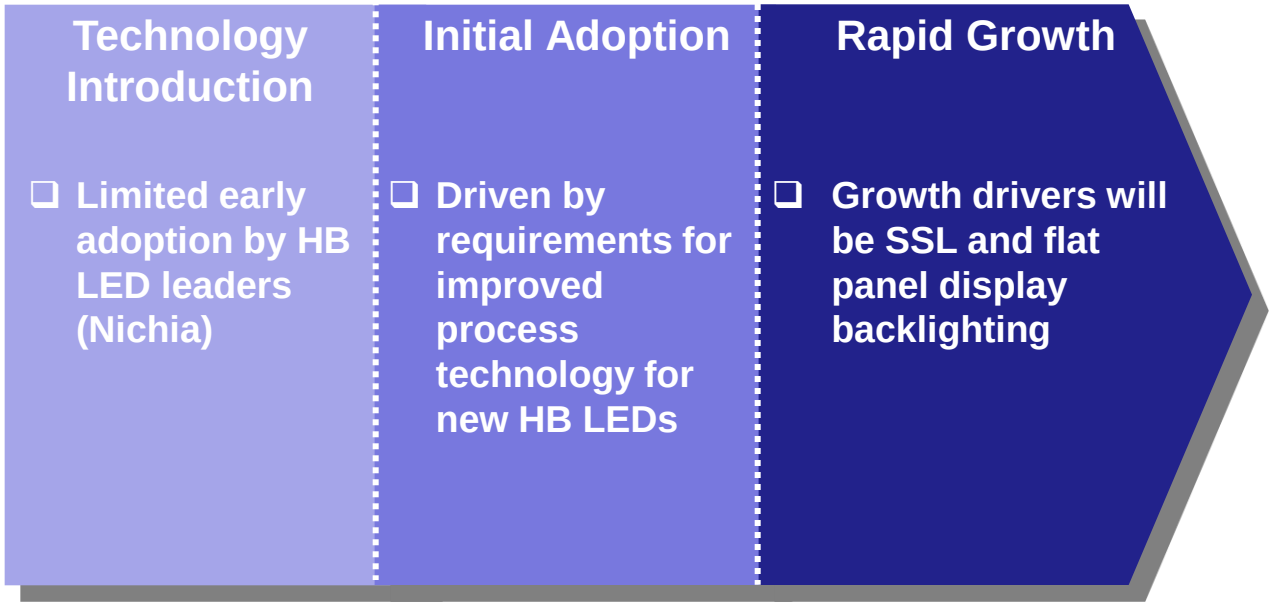
## (New Product Introduction Drives Superior COO)

### Highlights

- Ultratech offers a cost-effective, production proven, 1x projection tool with better alignment, better yields and better ROI
  - Recent LED adoption for backlighting has pushed customers towards stepper adoption
  - Significant momentum in Asia market after introduction of Sapphire product
    - Sapphire provides smallest footprint stepper with a cost effective technology upgrade solution


**Repositioning Legacy Product for HBLED Market Has Gained Considerable Momentum**

# Summary




HBLED Adoption Timeline

## Ultratech offers

- Market specific lens design for thick resist applications
- Technology readiness and volume production capability for current & future HBLED product offering