Process Development for Advanced Generation Crystalline Silicon Solar Cells

James Gee

Applied Materials, Santa Clara, CA

Northern California Chapter of the American Vacuum Society

Joint User Group Topical Conference

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Outline

- Roadmaps
  - Industry
  - Trends in High Efficiency
  - Applied Materials
- Process Development Examples:
  - Ion Implantation
  - Heterojunction
  - Screen Printing
  - Passivation
- Personal Observations

ITRPV March 2012 (2011 Roadmap)

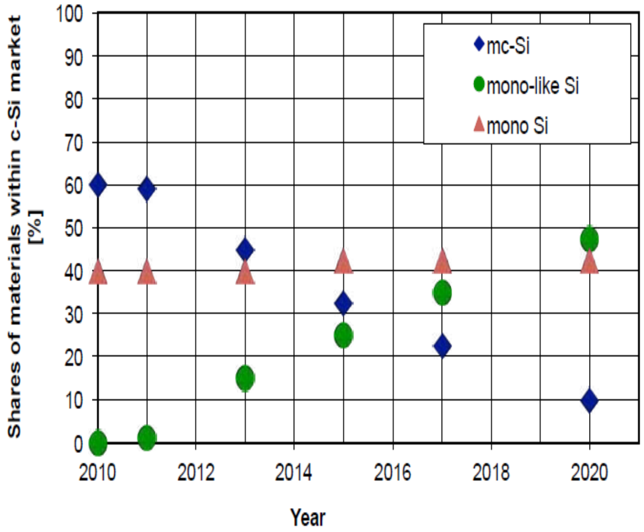


Fig. 26 Expected share of mc-Si, mono-Si and mono-like Si material.

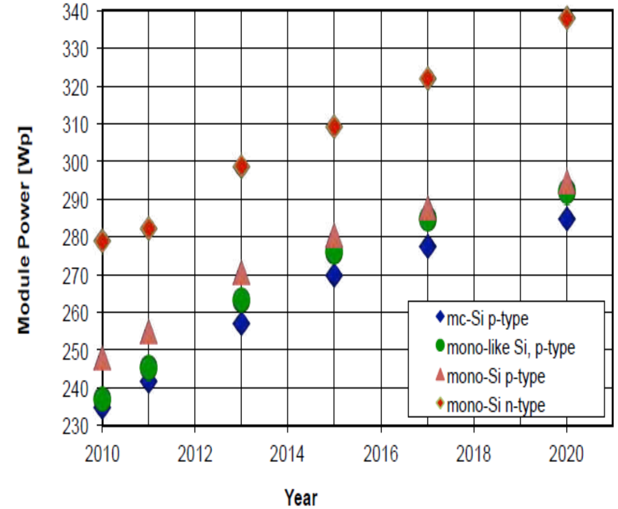


Fig. 29 Trend curve for mc-Si, mono-like and mono-Si module power.

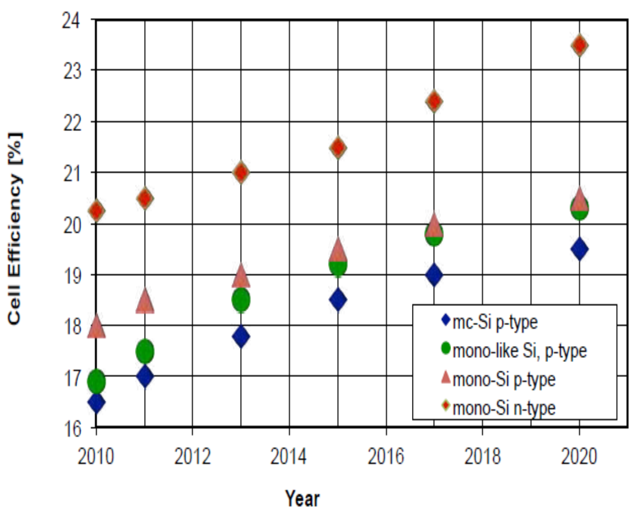


Fig. 28 Stabilized cell efficiency trend curve for mc-Si, mono-like and mono-Si.

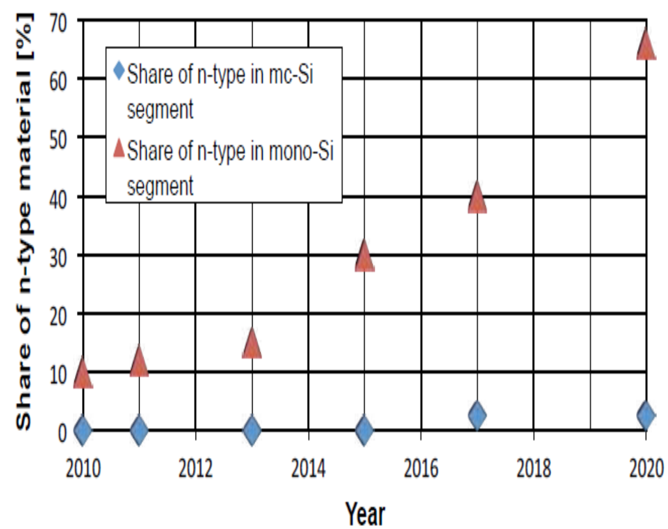


Fig. 27 Expected share of n-type material on world production of c-Si solar cells.

Industry Roadmap

- *Industry Roadmap*:
  - ITRPV provides a useful illustration of future trends
  - Does not have strong influence on individual company decisions
  - Each company has their own roadmap
- Reasons:
  - Past: Companies largely competed during rapid expansion of PV solar market by scale, value-chain cost optimization, and process optimization with largely similar process and products.
  - Semi industry serves a range of end markets, so cooperation for improvement of base technology does not impact individual company competitive positions. Products in end solar market is largely interchangeable, so strong tendency towards commoditization.
- Applied Roadmap
  - Based on analysis of emerging technology trends
  - Performance/cost analysis attempts to fully value efficiency, energy yield, etc. in end system

High Efficiency Structures in the News

Trinasolar
Honey

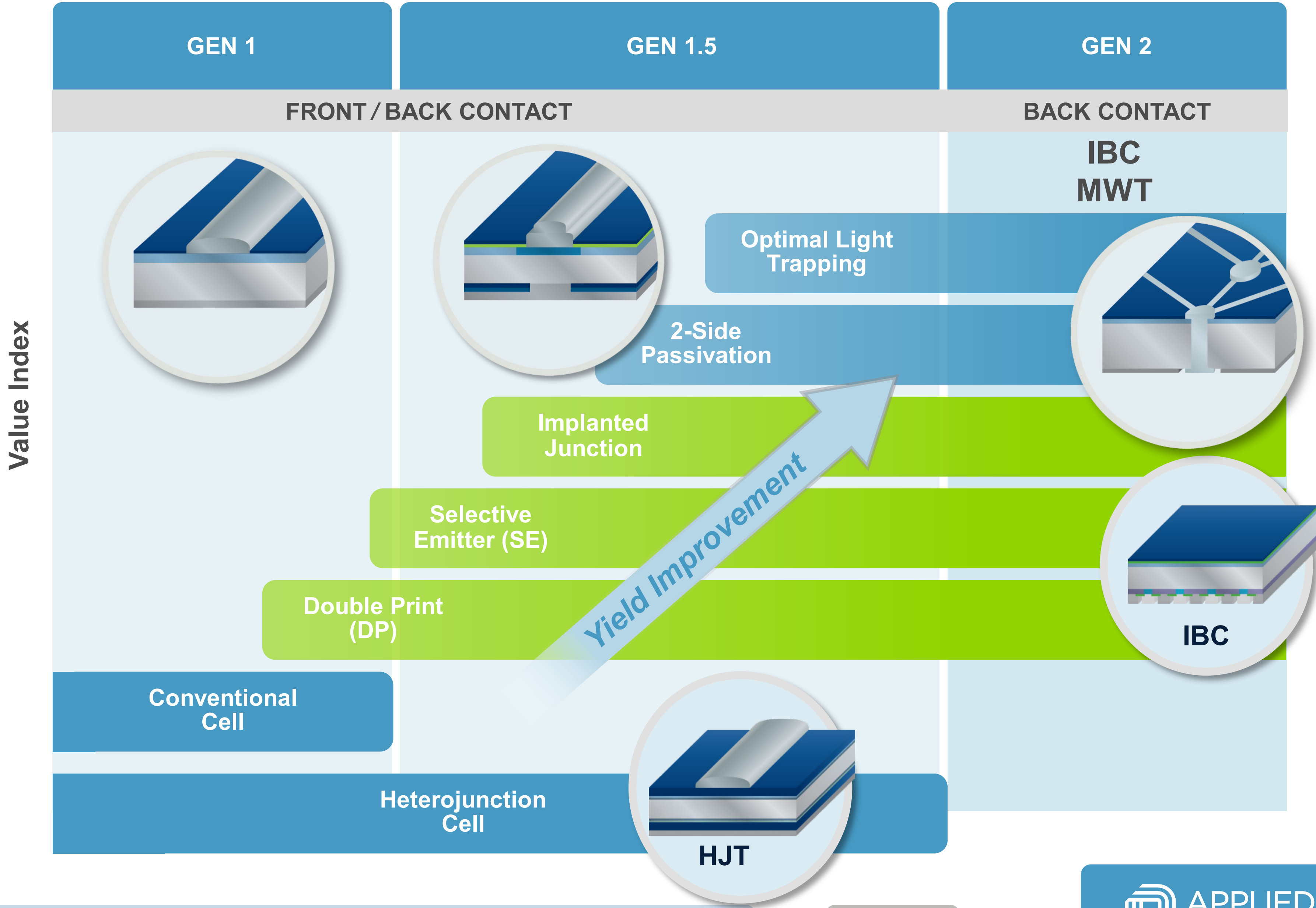
Panasonic
ideas for life
HIT®
Photovoltaic Module

YINGLI SOLAR
panda

SUNPOWER®
MAXEON™ CELL TECHNOLOGY

CanadianSolar
ELPS Cell Technology
Highest cell efficiency up to **21.1%**

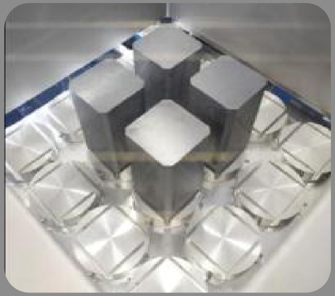
Applied Materials Powering the c-Si PV Roadmap



PV Manufacturing Solutions Leadership

SILICON → INGOT → WAFER → CELL → MODULE

PRECISION WAFERING SYSTEMS

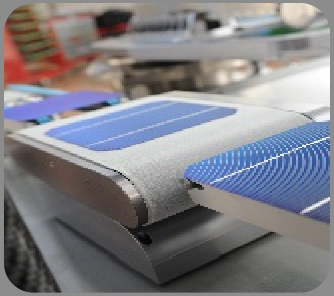


- Higher productivity
- Thinner wafers
- Consumables reduction

VARIAN ION IMPLANT SYSTEMS

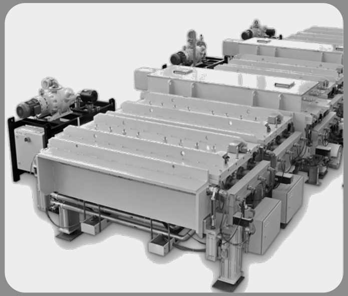
- Simplified process flow
- Improved yield
- Tight control of high efficiency cell distribution

BACCINI CELL SYSTEMS



- Increased cell efficiencies
- Low breakage
- Advanced automation

THIN FILMS DEPOSITION SYSTEMS



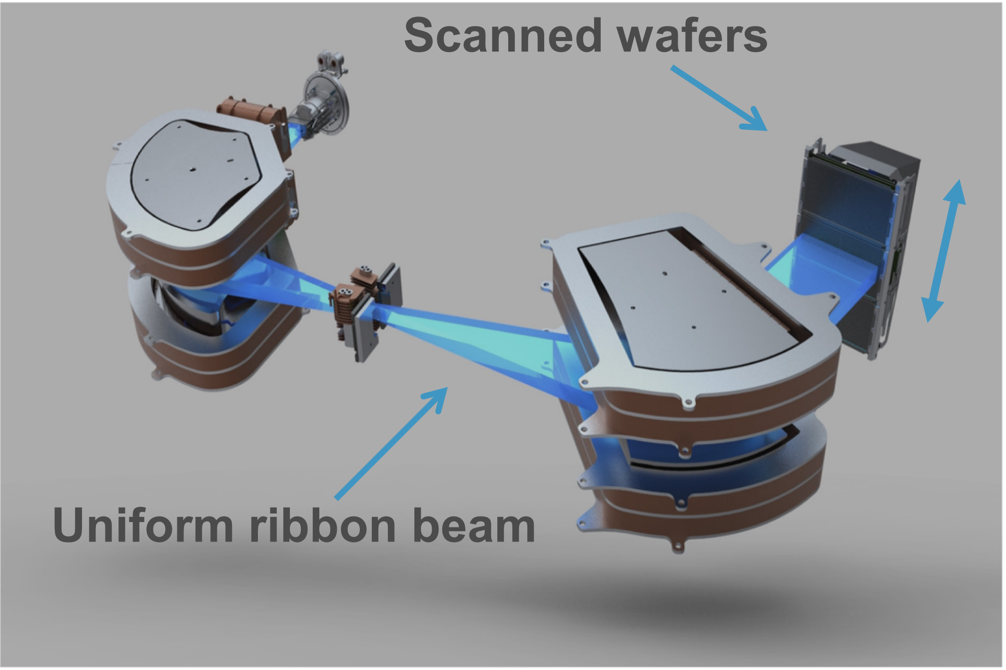
- High quality films
- Excellent thickness and uniformity control
- High productivity

External Use

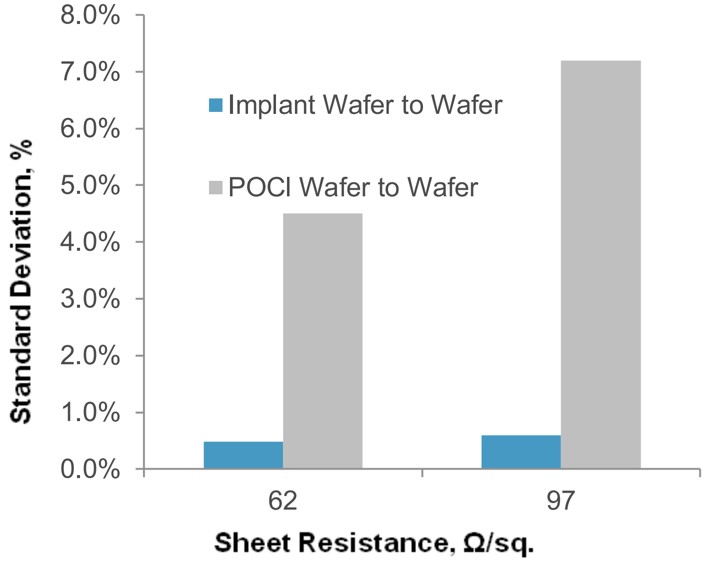
APPLIED MATERIALS®

Solion™: Exceptional Process Control

Doping Using Ion Implantation



Compatible with both p-type and n-type cSi processing



Excellent wafer uniformity – for high Rs emitters yields improved binning

Ribbon beam improves uniformity and binning performance

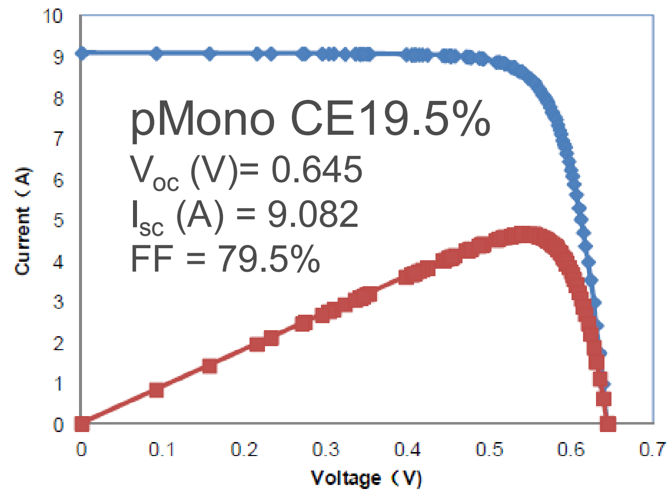
APPLIED MATERIALS®

High Quality Emitter = High Efficiency
Solion Device Performance and Yield

Device Performance

- Superior Emitter Junction Quality
  No dead layer - Better blue response
- Precise Uniform Doping- FF, J_{sc}
- No cost thermal oxide
  Improved passivation- V_{oc}

High Cell Efficiency



Yield

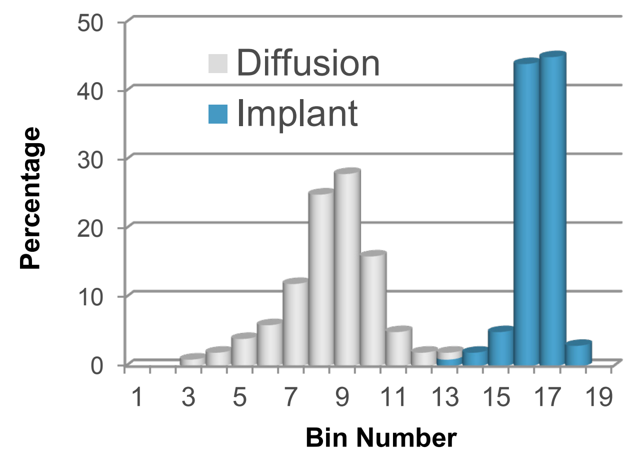
Process Simplification

- Eliminate PSG Clean
- Single sided doping – no edge isolation
- In situ patterning – SE

Precise Uniformity and Repeatability

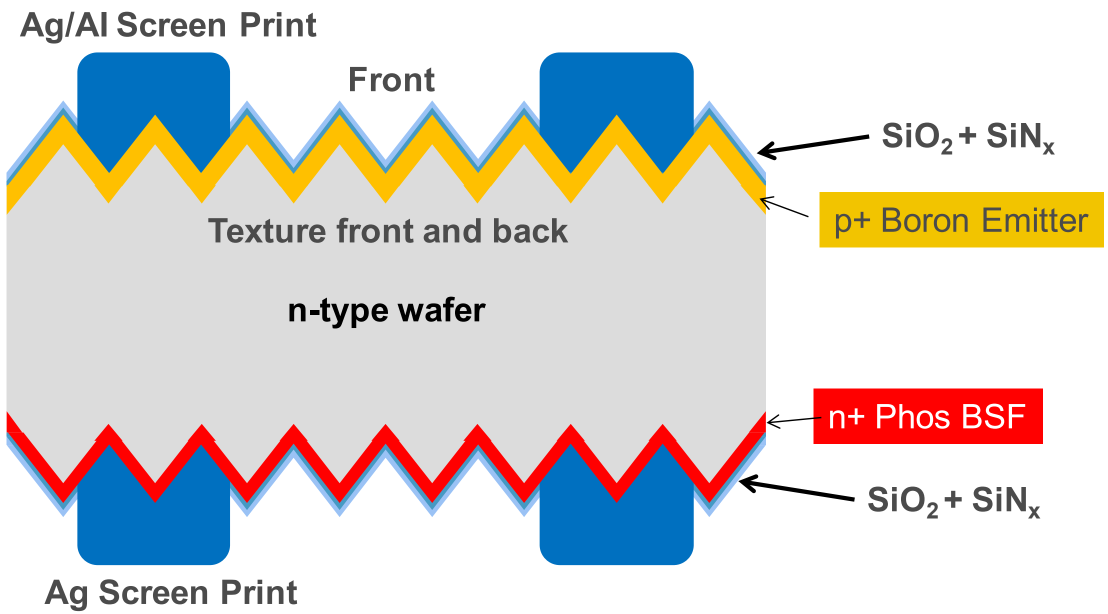
- Enables 2-3x fewer bins

Superior Binning



APPLIED MATERIALS®

Why n-type Cells?



Boron Front Emitter

- Efficiency entitlement exceeding 21% due to high bulk lifetime
- No Light Induced Degradation (LID)
- Passivation Options: SiO_2 / SiN_x or Al_2O_3 / SiN_x
- Metallization: Screen printed Grid, front and back
- Texturing: Single or Double side textured possible

Why Implant for n-type Cells?

N-type- Boron diffused front emitter

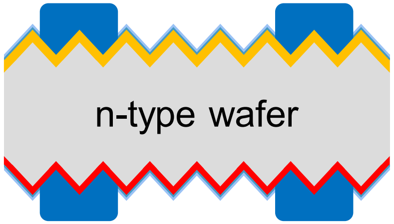
- SDE, KOH texture, clean
- Boron diffusion barrier-rear
- Boron diffusion (BBr_3/BCl_3)
- BRL and diffusion barrier etch
- Phos diffusion barrier-front
- Phos Diffusion
- PSG and diffusion barrier removal
- Thermal oxidation-front and rear
- SiN_x deposition-front
- SiN_x deposition-rear
- Metalization-front and rear
- Co-firing

12 steps

N-type boron implanted front emitter

- SDE, KOH texture, clean
- Boron implant-front
- Phos implant-rear
- Anneal/oxidation
- SiN_x deposition-front
- SiN_x deposition-rear
- Metalization-front and rear
- Co-firing

8 steps

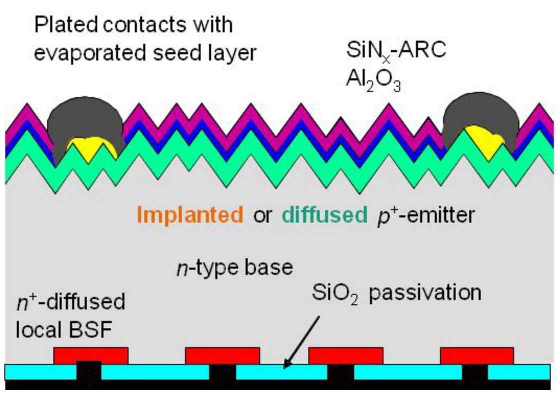


N-type cell process with implant significantly reduces process steps and complexity

n-type R&D → Customer

Early R&D

Fraunhofer ISE



Diffused Boron Emitter

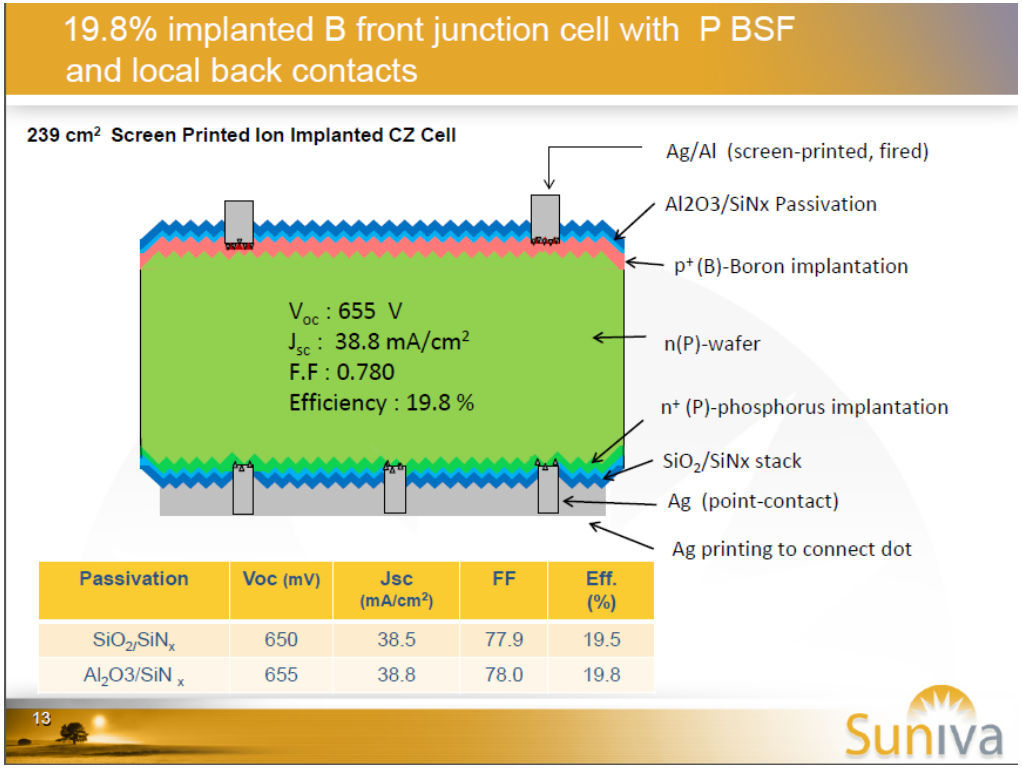
Mean value (#14)	669	39.3	79.1	20.8
Best cell	678	39.6	80.7	21.7

Implanted Boron Emitter

Mean value (#21)	659	39.6	78.8	20.6
Best cell	**679**	**40.0**	**80.0**	**21.7**

Cell area 2x2 cm² on 1 Ωcm FZ Silicon

Industrial


19.8% implanted B front junction cell with P BSF and local back contacts

239 cm² Screen Printed Ion Implanted CZ Cell

Passivation	Voc (mV)	Jsc (mA/cm²)	FF	Eff. (%)
SiO_2/SiN_x	650	38.5	77.9	19.5
Al_2O3/SiN_x	655	38.8	78.0	19.8

13 Suniva

- 19.8% CE with p+/n+ ion implantation
- Path to >21% CE

Hermle et al., 26th EUPVSC, p. 875, 2011

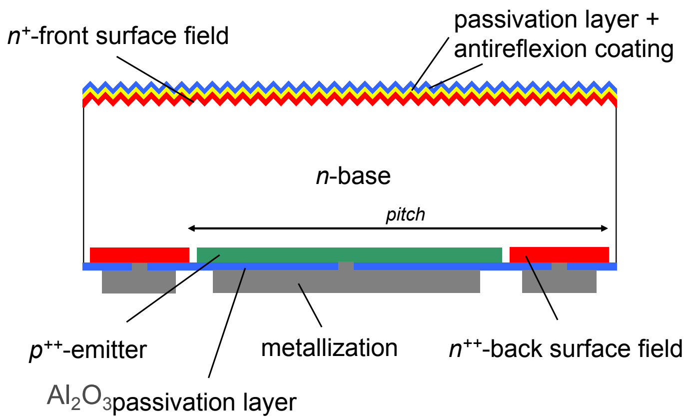
Rohatgi, nPV Workshop 2012

APPLIED MATERIALS ®

IBC R&D → Customer

Early R&D

Fraunhofer ISE



Rear Side Passivation	ρ (Ωcm)	V_{oc} (mV)	J_{sc} (mA/cm²)	*FF* (%)	*η* (%)
SiO_2	1	642.2	37.8	78.8	19.2
Al_2O_3	5	650.1	40.5	75.8	20.0

- >20% fully implanted POC

Bateman et al., 1st Silicon PV, p. 509, 2011

Industrial

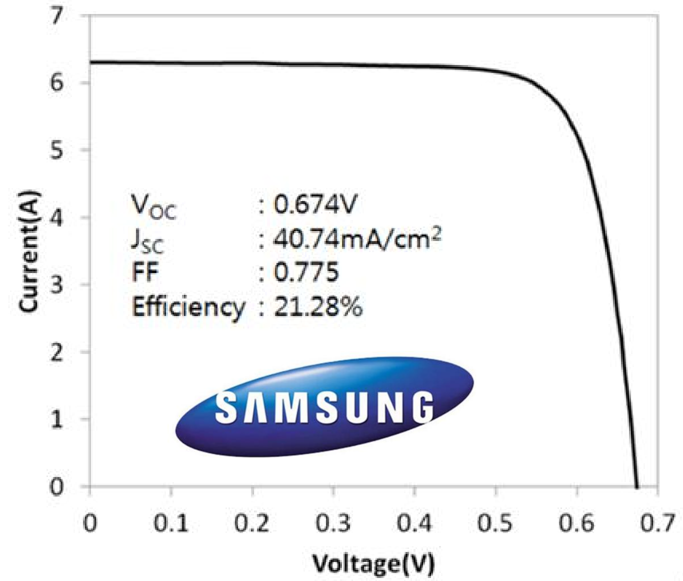


Fig. 3. I-V curve (at 25℃, 100mW/cm²) of IBC solar cell via ion implantation.

- **21.28% large-area IBC Solar Cell**
  - High J_{sc} (~41 mA/cm²)
- All doping through ion implantation with shadow masks

Mo et al., 27th EUPVSEC 2012,
“High Efficiency Back Contact Solar Cell via Ion Implantation“, 2CV.7.25

APPLIED MATERIALS®

Heterojunction

- Heterojunction cells offer high cell efficiency and low temperature process
- c-Si HJT cell performances

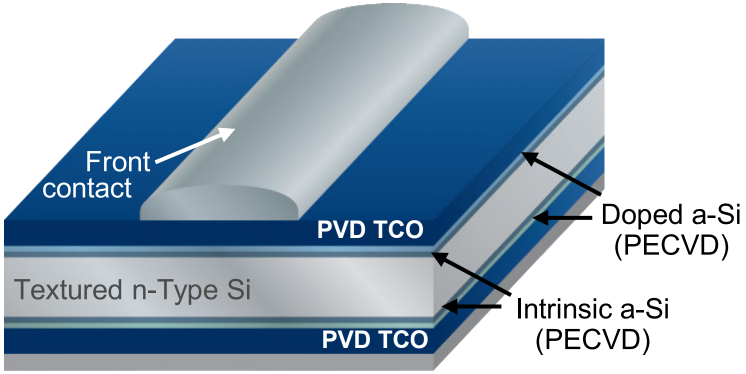
Panasonic HIT technology announcement:

R&D: 24.7%

Production: >20%

- Superior temperature coefficient and absence of PID & LID
- PECVD a-Si films best-in-class uniformity and lifetime; high productivity platforms
- High productivity PVD platform for TCO

Heterojunction Cell Structure



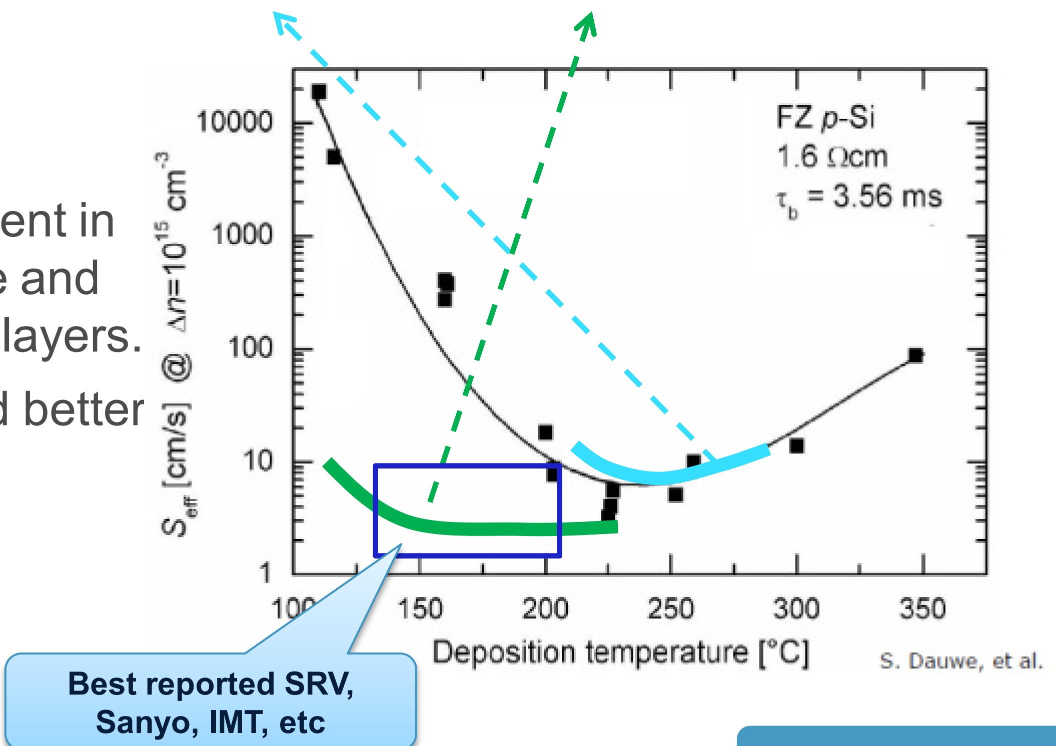
Heterojunction cell structures receiving greater interest

TCO: Transparent Conductive Oxide; PID: Potential induced degradation, LID: Light induced degradation

Improvement to Heterojunction Process

	Original RF Process	New VHF Process
RF Frequency	13.56 MHz	40 MHz
Substrate Temperature	225-300°C	120-250°C
Deposition Rate	>5Å/s for p, i, n layers	<2.5 Å/s for p, i, n layers
SRV	>10cm/s @ 50Å thickness	<5cm/s @ 50Å thickness

- New VHF-PECVD hardware and process have enabled improvement in the a-Si passivation performance and the development of novel doped layers.
- Reduced deposition rate enabled better thickness control and process repeatability.



Shuran et. al. 27th EU PVSEC (2012)

APPLIED MATERIALS

Applied Solutions for Heterojunction Cells

Production Proven PECVD Options for R&D and HVM

AKT Gen3.5 and Gen6 Platforms

High Throughput PVD System to Address Multiple Applications

ATON 1600 PVD Platform

Reliable and Proven Printing and Drying Solutions for Unique Heterojunction Requirements

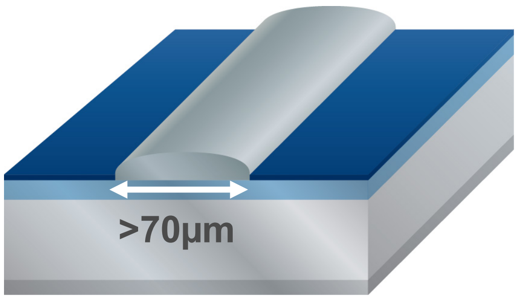
Baccini Metallization

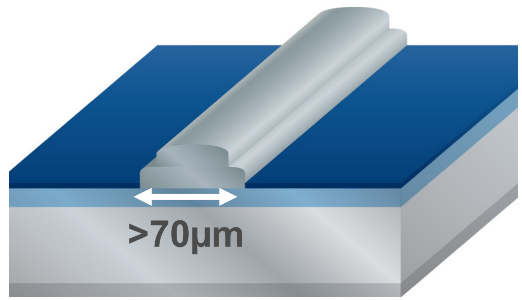
Production Proven Solutions for Emerging Technologies

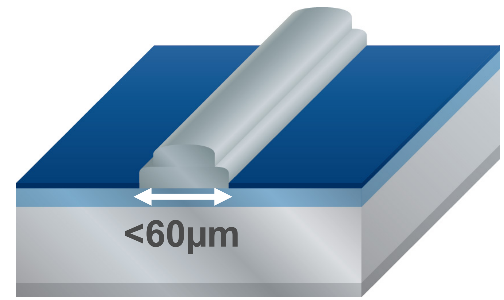
Screen Printing
Double Print
MWT

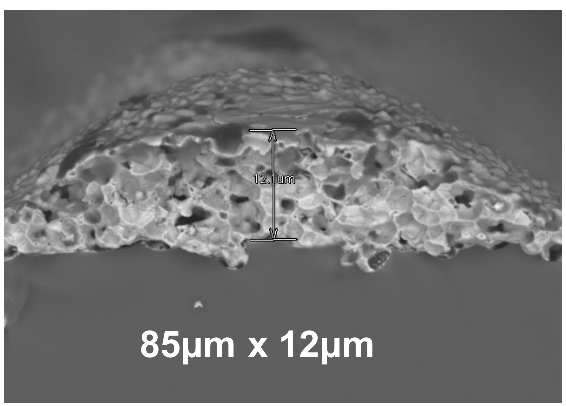
Double Print Structures

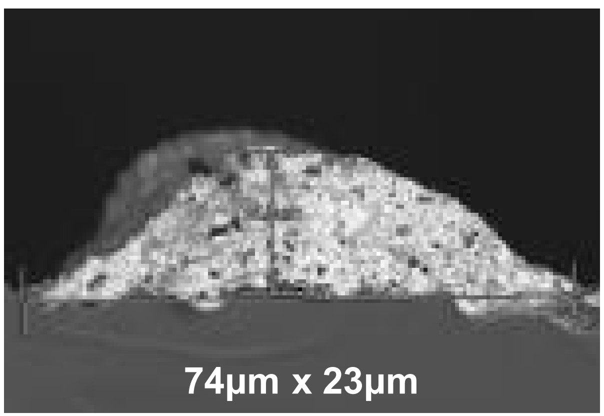
Single Print	Double Print	Fine Line Double Print™

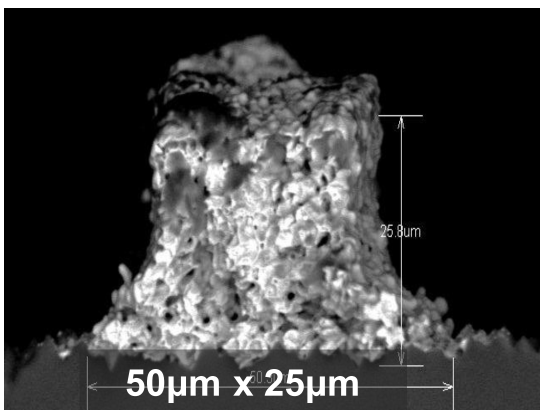








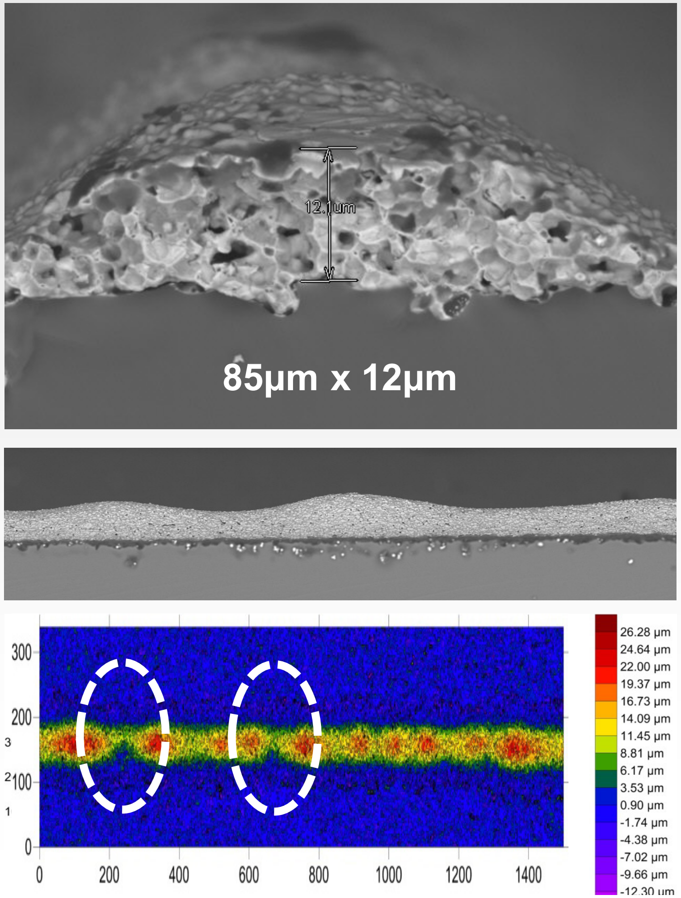




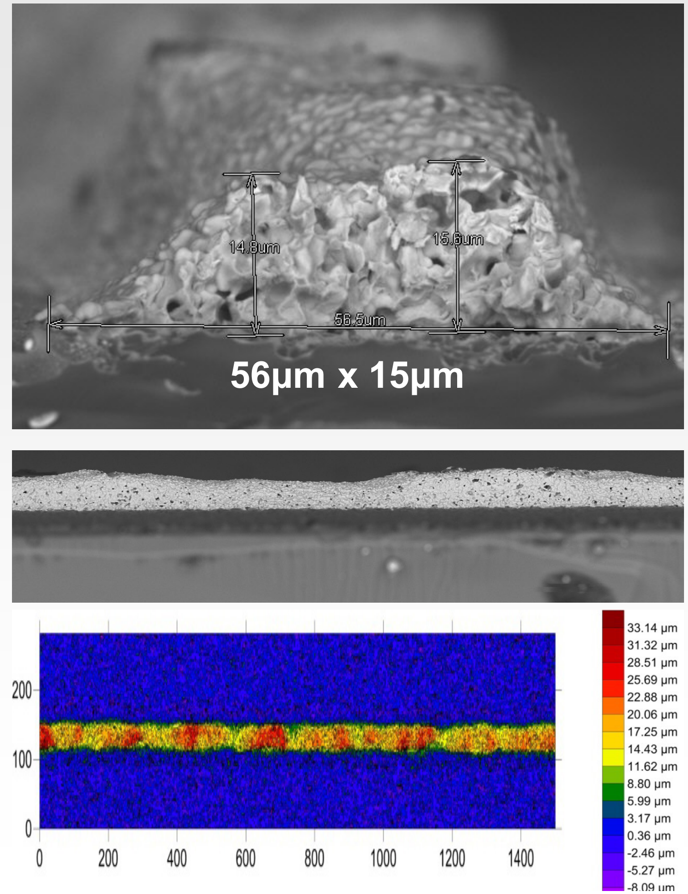
Fine Line Double Print enables 0.2% CE gain over single print and 20% Ag paste reduction

FLDP™ Morphology Comparison

Single Print



Fine Line Double Print™



Better morphology and fewer interrupts with Fine Line Double Print

Driving Force for FLDP™

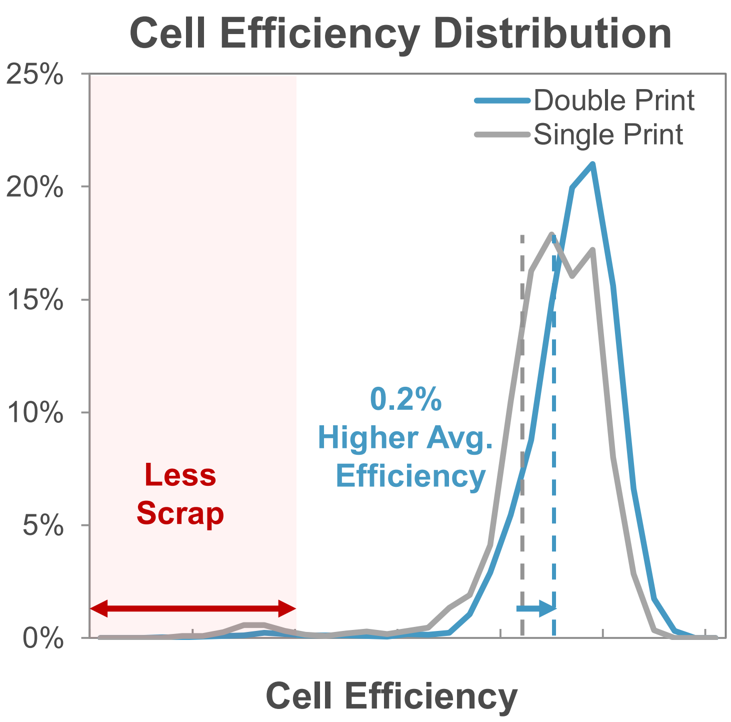
Increasing Revenues, Reducing Costs with Double Print

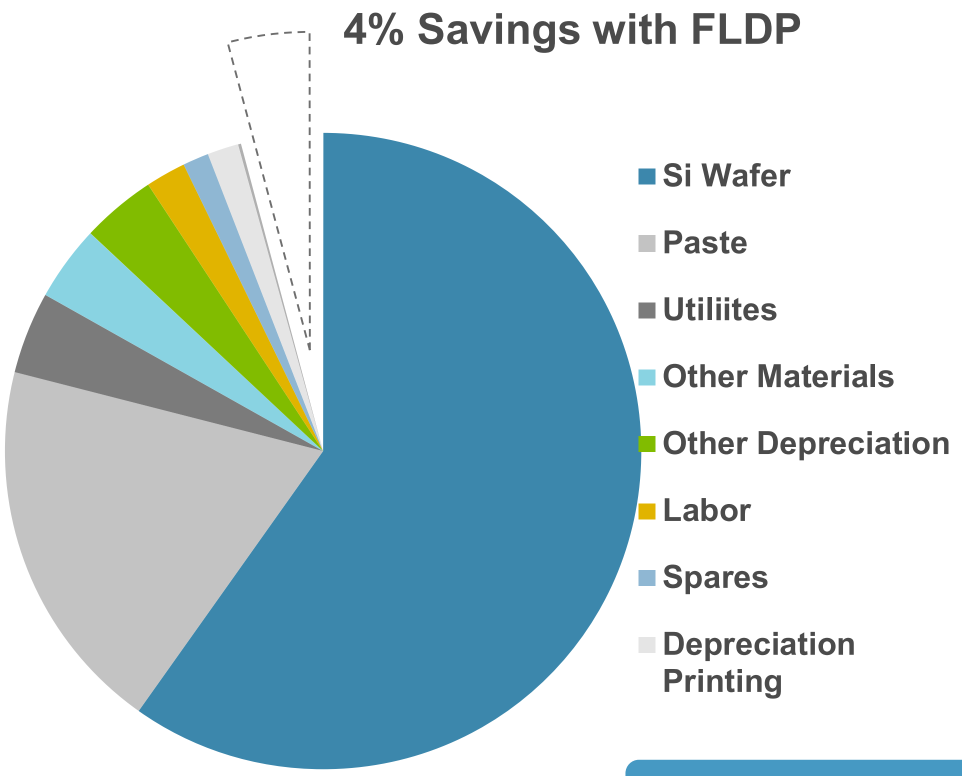
More Watts produced

- 0.2% absolute higher efficiency
- Scrap rate reduced

Reduced cell processing costs

- Reduce paste usage by 20%
- All costs reduced with higher efficiency





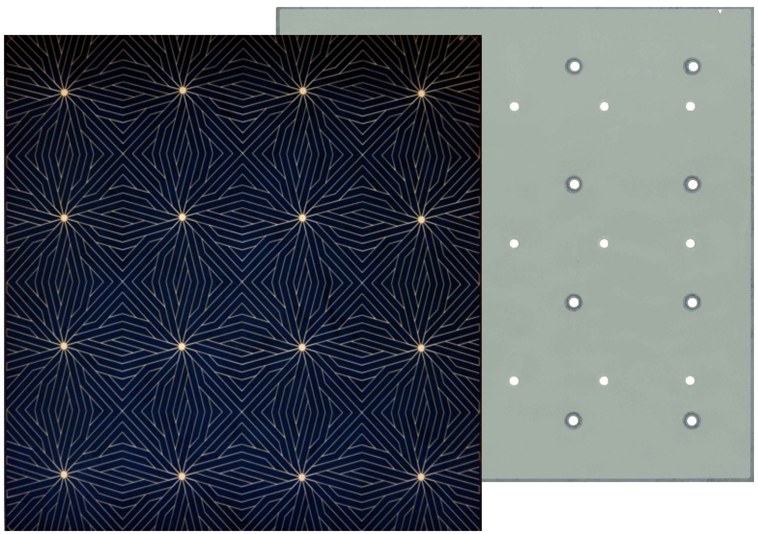
APPLIED MATERIALS®

Metal Wrap Through (MWT) Benefits

- No busbar on the front side
- Less paste deposit (up to 30% saving)
- Electrical contact only on the back side
- Higher short-circuit current density
- Higher V_{oc} (recombination current is reduced by lower metallized area)

- Busbar shading 2%
- Finger shading 5%

MWT Cell Front



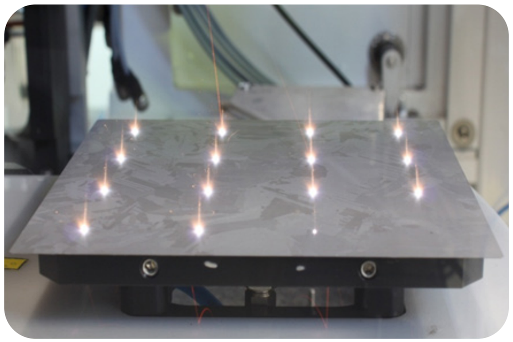
Conventional Front

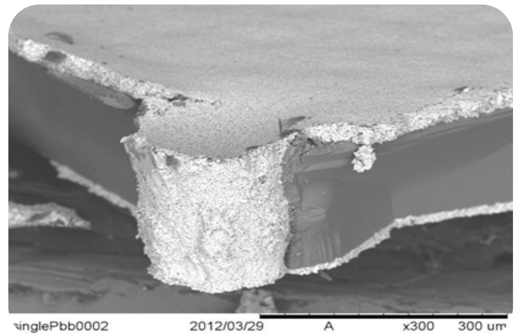
Efficiency gain of 0.3-0.5% absolute is observed
≥ 1% Efficiency gain at module level

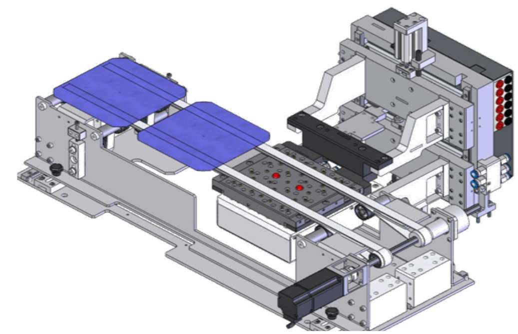
Source: S.W. Glunz, Advances in OptoElectronics Volume 2007, Article ID 97370

Applied Baccini MWT Distinctive Solutions

Laser Holes Drilling	p and n-contacts Metallization	I-V Testing

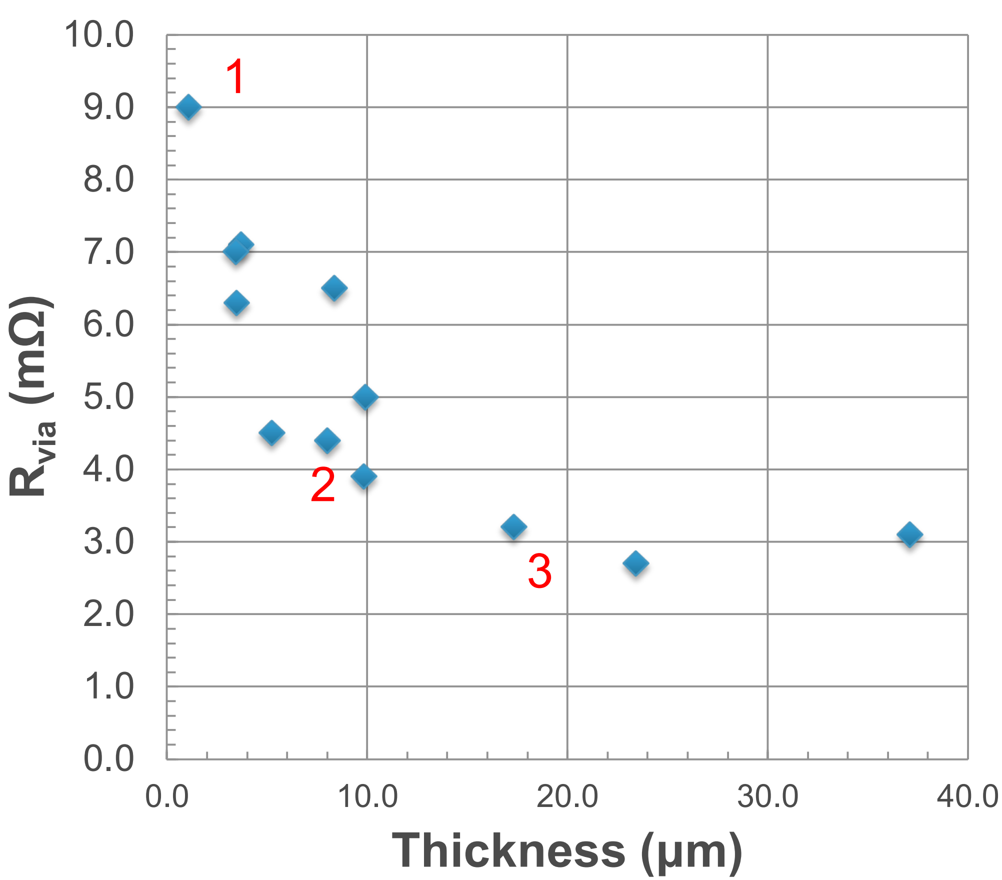




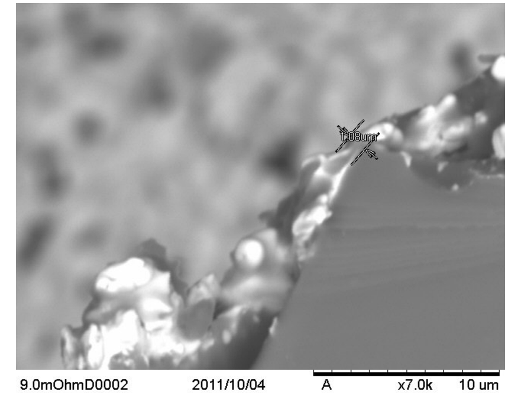


Unique Galvo head plus Rotary table	**Proven metallization**	**Proven back contact probing**
▪ Proprietary Closed Loop Control guarantees high accuracy and drift compensation	▪ Full control of the vias filling ▪ Prevention of the cell contaminations ▪ No need for paper on nest	▪ Best IV measurement repeatability

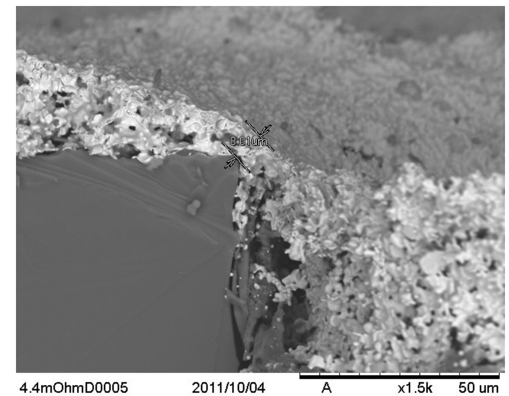
Via Printing



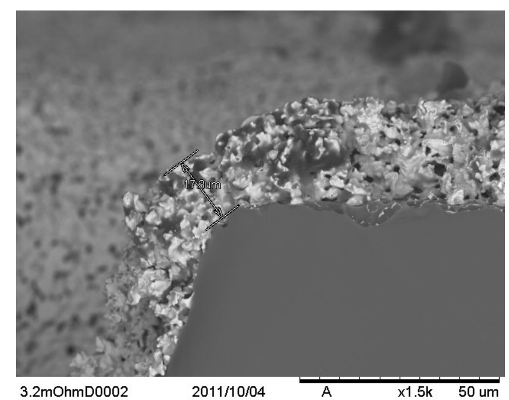
1
overlay
1µm



2
overlay
8µm



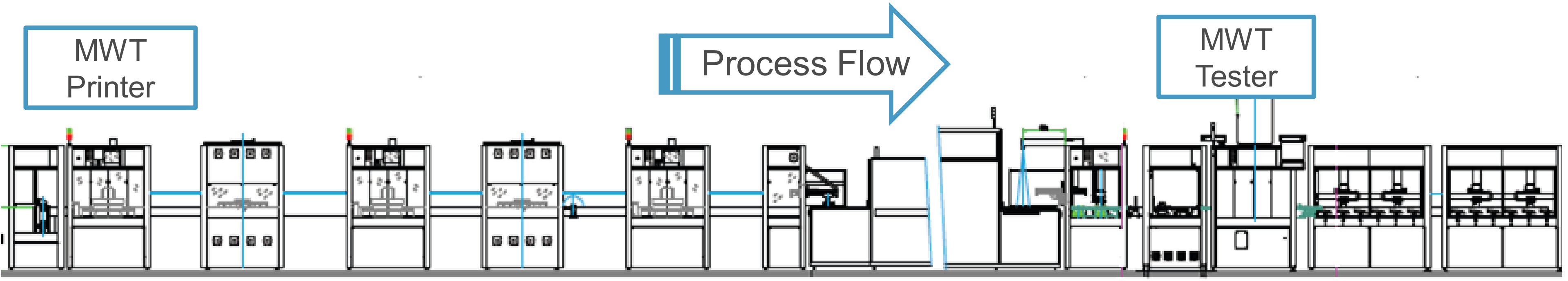
3
overlay
17µm

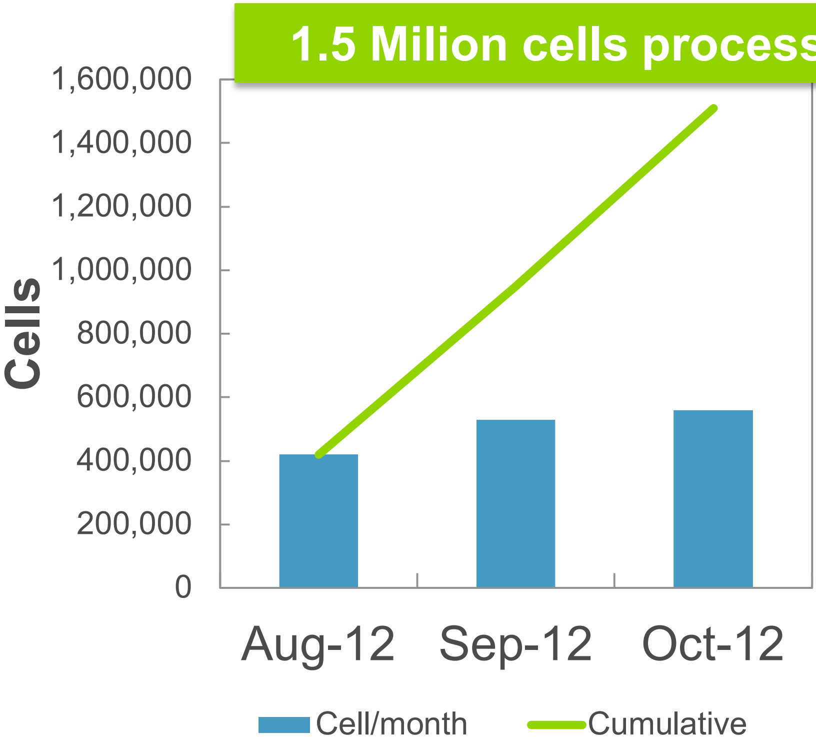


- Filling vs. via resistance
- Corner overlay drives the via resistance
- Optimized cell efficiency

F. Clement, et al., Sol. Energy Mater. Sol. Cells, 94 (2010) 51-56

Today: HVM

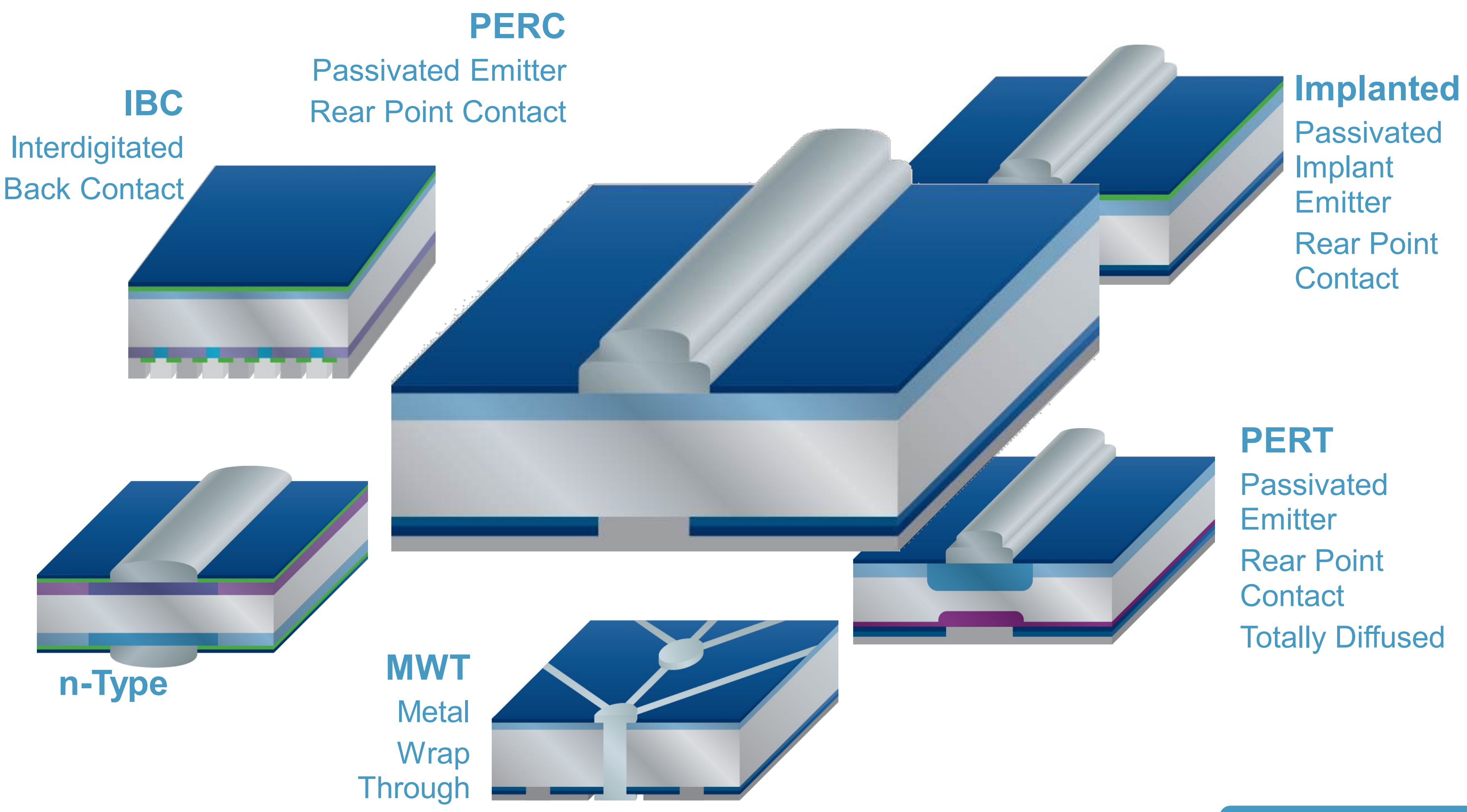




- Same Breakage rate of standard cell
- Via Filling ratio > 98%
- Average Efficiency repeteability ± 0.05% absolute (dynamic mode)

Advanced Passivation

Advanced Cell Structures For High Efficiency Need 2-Side Passivation Solutions



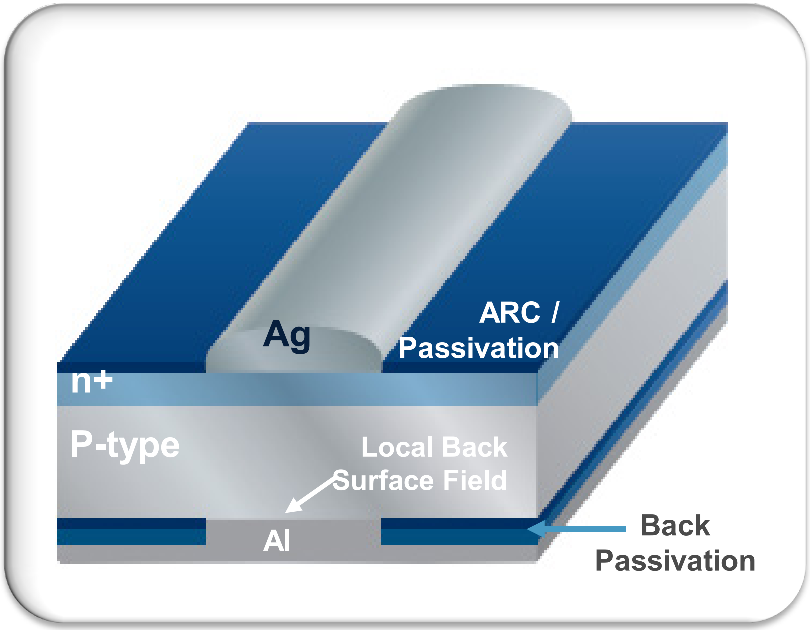
Two-Side Passivation

PERC Structure

- Reduces backside recombination losses
  - Contribute to ~ 45 % of efficiency gain
  - Low surface recombination velocity
  - Negative fixed charge Al_2O_3 film repels electrons

- Improves backside reflection
  - Contributes to ~ 55% of efficiency gain
  - High back surface reflection of AlO/SiN (~90%) vs Al (65%)

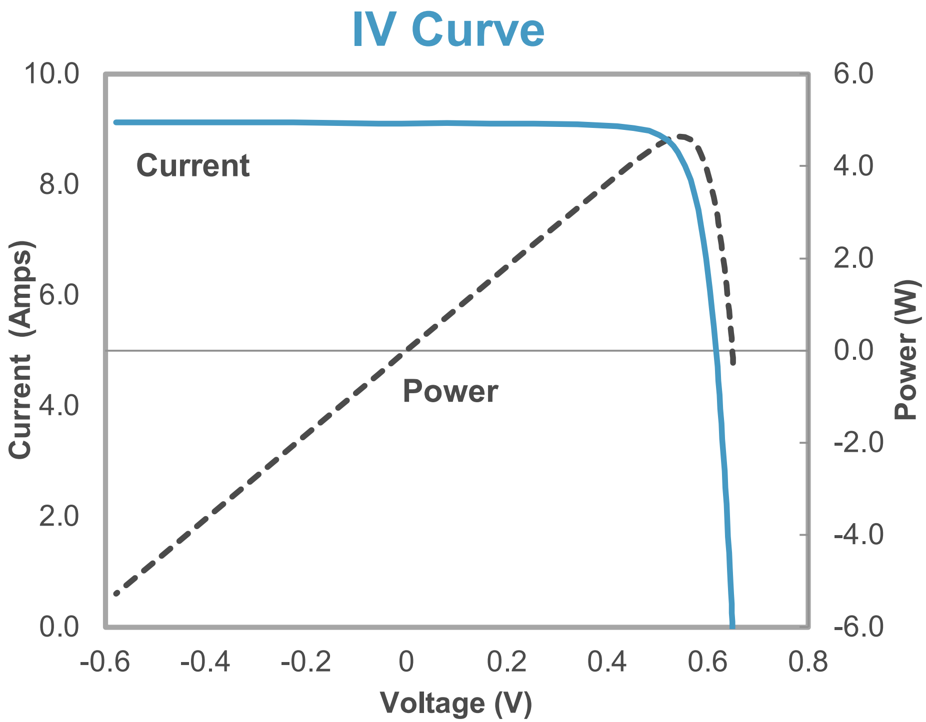
2 Side Passivated Cell (PERC)

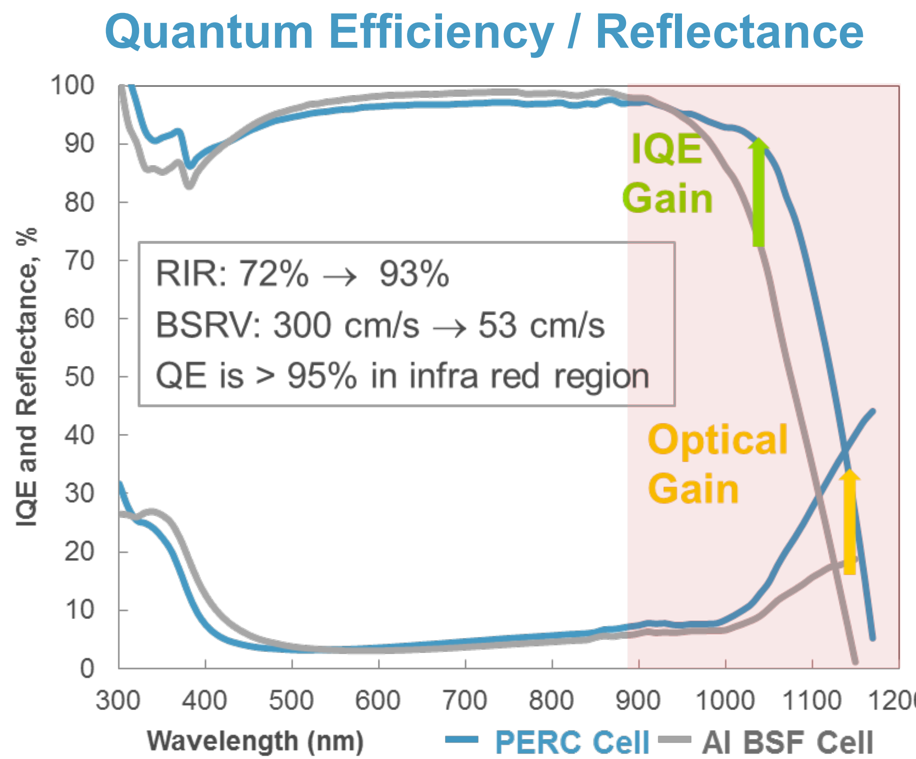


Cell Efficiency Gains from Backside Passivation
(Longer wavelength light capture)

P Type Mono-Si PERC

Device Performance





Champion pMono Cell	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	Eta (%)
Ref Cell	37.1	638	79.5	18.83
PERC	38.5	648	78.7	19.62

- Red response benefit from lowered recombination and higher reflection
- Significant enhancements in IR response with backside passivation
- Long wavelength gains transfers to module

Demonstrates >0.6 efficiency gain with backside passivation on p-type mono cSi

Wijekoon et.al. 27th EU PVSEC (2012)

Concluding Personal Observations

- End market continues to grow
- PV cell/module producers are becoming more sophisticated in valuing technology improvements
- A relentless drive to improve baseline technology *(another 5W or go home!*)
- Improved baseline technology and reduced costs raises the bar for disruptive technologies, but…
  – Technology and brand differentiation will become larger component of many company business plans
  – Cost structure of baseline technology will be migrated to the high-efficiency potential of n-type material