Process Development for Advanced Generation Crystalline Silicon Solar Cells

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Northern California Chapter of the American Vacuum Society
Joint User Group Topical Conference
February 21, 2011
Outline

- Roadmaps
  - Industry
  - Trends in High Efficiency
  - Applied Materials
- Process Development Examples:
  - Ion Implantation
  - Heterojunction
  - Screen Printing
  - Passivation
- Personal Observations
ITRPV March 2012 (2011 Roadmap)

Fig. 26 Expected share of mc-Si, mono-Si and mono-like Si material.

Fig. 28 Stabilized cell efficiency trend curve for mc-Si, mono-like and mono-Si.

Fig. 29 Trend curve for mc-Si, mono-like and mono-Si module power.

Fig. 27 Expected share of n-type material on world production of c-Si solar cells.
Industry Roadmap

- **Industry Roadmap:**
  - ITRPV provides a useful illustration of future trends
  - Does not have strong influence on individual company decisions
  - Each company has their own roadmap

- **Reasons:**
  - Past: Companies largely competed during rapid expansion of PV solar market by scale, value-chain cost optimization, and process optimization with largely similar process and products.
  - Semi industry serves a range of end markets, so cooperation for improvement of base technology does not impact individual company competitive positions. Products in end solar market is largely interchangeable, so strong tendency towards commoditization.

- **Applied Roadmap**
  - Based on analysis of emerging technology trends
  - Performance/cost analysis attempts to fully value efficiency, energy yield, etc. in end system
High Efficiency Structures in the News

- Trina Solar
- Panasonic
- Yingli Solar
- panda
- Canadian Solar
  ELPS Cell Technology
  Highest cell efficiency up to 21.1%
- SunPower
  MAXEON™ Cell Technology
  Photovoltaic Module
## Applied Materials Powering the c-Si PV Roadmap

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<th>GEN 1</th>
<th>GEN 1.5</th>
<th>GEN 2</th>
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<td>FRONT / BACK CONTACT</td>
<td>FRONT / BACK CONTACT</td>
<td>BACK CONTACT</td>
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<td>IBC MWT</td>
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<td>Conventional Cell</td>
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<td>Heterojunction Cell</td>
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<td>IBC</td>
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<td>Double Print (DP)</td>
<td>Implanted Junction</td>
<td>Optimal Light Trapping</td>
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<td>Selective Emitter (SE)</td>
<td>2-Side Passivation</td>
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<tr>
<td>Optimal Light Trapping</td>
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</table>

**Diagram Notes:**
- GEN 1: Conventional Cell
- GEN 1.5: Implanted Junction
- GEN 2: IBC MWT
- IBC: Heterojunction
- HJT: Heterojunction
- Selective Emitter (SE): Heterojunction
- 2-Side Passivation: Heterojunction
- Optimal Light Trapping: Heterojunction
- Double Print (DP): Heterojunction

**Yield Improvement:**

Applied Materials Powering the c-Si PV Roadmap

**Diagram Description:**
- The diagram illustrates the progression of solar cell technology from GEN 1 (Conventional Cell) to GEN 2 (IBC MWT) via GEN 1.5 (Implanted Junction).
- Each technology stage is associated with specific features, such as Double Print (DP), Implanted Junction, Selective Emitter (SE), 2-Side Passivation, and Optimal Light Trapping.
- The yield improvement is indicated across the different cell types, highlighting advancements in efficiency and performance.
PV Manufacturing Solutions Leadership

- **SILICON**
  - Higher productivity
  - Thinner wafers
  - Consumables reduction

- **INGOT**
  - Simplified process flow
  - Improved yield
  - Tight control of high efficiency cell distribution

- **WAFER**
  - Increased cell efficiencies
  - Low breakage
  - Advanced automation

- **CELL**
  - High quality films
  - Excellent thickness and uniformity control
  - High productivity

- **MODULE**

**PRECISION WAFERING SYSTEMS**

**VARIAN ION IMPLANT SYSTEMS**

**BACCINI CELL SYSTEMS**

**THIN FILMS DEPOSITION SYSTEMS**
Solion™: Exceptional Process Control

Doping Using Ion Implantation

- Scanned wafers
- Uniform ribbon beam
- Compatible with both p-type and n-type cSi processing

Excellent wafer uniformity – for high Rs emitters yields improved binning

Ribbon beam improves uniformity and binning performance
High Quality Emitter = High Efficiency
Solion Device Performance and Yield

Device Performance
- Superior Emitter Junction Quality
  - No dead layer - Better blue response
- Precise Uniform Doping - FF, \( J_{sc} \)
- No cost thermal oxide
  - Improved passivation - \( V_{oc} \)

Yield

Process Simplification
- Eliminate PSG Clean
- Single sided doping – no edge isolation
- In situ patterning – SE

Precise Uniformity and Repeatability
- Enables 2-3x fewer bins

High Cell Efficiency
pMono CE19.5%
\( V_{oc} \) (V) = 0.645
\( I_{sc} \) (A) = 9.082
FF = 79.5%

Superior Binning

Diffusion
Implant
Why n-type Cells?

- Efficiency entitlement exceeding 21% due to high bulk lifetime
- No Light Induced Degradation (LID)
- Passivation Options: SiO$_2$ / SiN$_x$ or Al$_2$O$_3$ / SiN$_x$
- Metallization: Screen printed Grid, front and back
- Texturing: Single or Double side textured possible

**Boron Front Emitter**
Why Implant for n-type Cells?

<table>
<thead>
<tr>
<th>N-type- Boron diffused front emitter</th>
<th>N-type boron implanted front emitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDE, KOH texture, clean</td>
<td>SDE, KOH texture, clean</td>
</tr>
<tr>
<td>Boron diffusion barrier-rear</td>
<td>Boron implant-front</td>
</tr>
<tr>
<td>Boron diffusion (BBr₃/BCl₃)</td>
<td>Phos implant-rear</td>
</tr>
<tr>
<td>BRL and diffusion barrier etch</td>
<td>Anneal/oxidation</td>
</tr>
<tr>
<td>Phos diffusion barrier-front</td>
<td>SiNₓ deposition-front</td>
</tr>
<tr>
<td>Phos Diffusion</td>
<td>SiNₓ deposition-rear</td>
</tr>
<tr>
<td>PSG and diffusion barrier removal</td>
<td>Metalization-front and rear</td>
</tr>
<tr>
<td>Thermal oxidation-front and rear</td>
<td>Co-firing</td>
</tr>
<tr>
<td>SiNₓ deposition-front</td>
<td>8 steps</td>
</tr>
<tr>
<td>SiNₓ deposition-rear</td>
<td></td>
</tr>
<tr>
<td>Metalization-front and rear</td>
<td></td>
</tr>
<tr>
<td>Co-firing</td>
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</tbody>
</table>

N-type cell process with implant significantly reduces process steps and complexity
n-type R&D → Customer

**Early R&D**

Plated contacts with evaporated seed layer

SIN$_x$-ARC

Al$_2$O$_3$

*Implanted or diffused* p*-emitter*

n*-diffused local BSF

SiO$_2$ passivation

**Diffused Boron Emitter**

Mean value (#14) 669 39.3 79.1 20.8

Best cell 678 39.6 80.7 21.7

**Implanted Boron Emitter**

Mean value (#21) 659 39.6 78.8 20.6

Best cell 679 40.0 80.0 21.7

Cell area 2x2 cm$^2$ on 1 Ωcm FZ Silicon

**Industrial**

19.8% implanted B front junction cell with P BSF and local back contacts

239 cm$^2$ Screen Printed Ion Implanted CZ Cell

- $V_{oc}$: 655 V
- $J_{sc}$: 38.8 mA/cm$^2$
- F.F.: 0.780
- Efficiency: 19.8%

**Passivation**

<table>
<thead>
<tr>
<th>Passivation</th>
<th>Voc (mV)</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>F.F.</th>
<th>Eff. (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$/SiN$_x$</td>
<td>650</td>
<td>38.5</td>
<td>77.9</td>
<td>19.5</td>
</tr>
<tr>
<td>Al$_2$O$_3$/SiN$_x$</td>
<td>655</td>
<td>38.8</td>
<td>78.0</td>
<td>19.8</td>
</tr>
</tbody>
</table>

- 19.8% CE with p+/n+ ion implantation
- Path to >21% CE

Hermle et al., 26th EUPVSC, p. 875, 2011

Rohatgi, nPV Workshop 2012
IBC R&D → Customer

**Early R&D**

- 21.28% large-area IBC Solar Cell
  - High $J_{SC}$ (~41 mA/cm²)
  - All doping through ion implantation with shadow masks

**Industrial**

<table>
<thead>
<tr>
<th>Rear Side Passivation</th>
<th>$\rho$ (Ω·cm)</th>
<th>$V_{oc}$ (mV)</th>
<th>$J_{sc}$ (mA/cm²)</th>
<th>FF (%)</th>
<th>η (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>1</td>
<td>642.2</td>
<td>37.8</td>
<td>78.8</td>
<td>19.2</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>5</td>
<td>650.1</td>
<td>40.5</td>
<td>75.8</td>
<td>20.0</td>
</tr>
</tbody>
</table>

- >20% fully implanted POC

Mo et al., 27th EUPVSEC 2012, “High Efficiency Back Contact Solar Cell via Ion Implantation”, 2CV.7.25
Heterojunction

- Heterojunction cells offer high cell efficiency and low temperature process
- c-Si HJT cell performances
  Panasonic HIT technology announcement:
  R&D: 24.7%
  Production: >20%
- Superior temperature coefficient and absence of PID & LID
- PECVD a-Si films best-in-class uniformity and lifetime; high productivity platforms
- High productivity PVD platform for TCO

Heterojunction cell structures receiving greater interest

TCO: Transparent Conductive Oxide; PID: Potential induced degradation, LID: Light induced degradation
Improvement to Heterojunction Process

- New VHF-PECVD hardware and process have enabled improvement in the a-Si passivation performance and the development of novel doped layers.
- Reduced deposition rate enabled better thickness control and process repeatability.

<table>
<thead>
<tr>
<th></th>
<th>Original RF Process</th>
<th>New VHF Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Frequency</td>
<td>13.56 MHz</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Substrate Temperature</td>
<td>225-300°C</td>
<td>120-250°C</td>
</tr>
<tr>
<td>Deposition Rate</td>
<td>&gt;5Å/s for p, i, n layers</td>
<td>&lt;2.5 Å/s for p, i, n layers</td>
</tr>
<tr>
<td>SRV</td>
<td>&gt;10cm/s @ 50Å thickness</td>
<td>&lt;5cm/s @ 50Å thickness</td>
</tr>
</tbody>
</table>

Shuran et. al. 27th EU PVSEC (2012)
Applied Solutions for Heterojunction Cells

Production Proven PECVD Options for R&D and HVM

AKT Gen3.5 and Gen6 Platforms

High Throughput PVD System to Address Multiple Applications

ATON 1600 PVD Platform

Baccini Metallization

Reliable and Proven Printing and Drying Solutions for Unique Heterojunction Requirements

Production Proven Solutions for Emerging Technologies
Screen Printing
Double Print
MWT
Double Print Structures

Single Print

Double Print

Fine Line Double Print™

Fine Line Double Print enables 0.2% CE gain over single print and 20% Ag paste reduction
FLDP™ Morphology Comparison

Better morphology and fewer interrupts with Fine Line Double Print™
Driving Force for FLDP™
Increasing Revenues, Reducing Costs with Double Print

More Watts produced
- 0.2% absolute higher efficiency
- Scrap rate reduced

Reduced cell processing costs
- Reduce paste usage by 20%
- All costs reduced with higher efficiency

Cell Efficiency Distribution
- Double Print
- Single Print

0.2% Higher Avg. Efficiency

Less Scrap

4% Savings with FLDP

- Si Wafer
- Paste
- Utilities
- Other Materials
- Other Depreciation
- Labor
- Spares
- Depreciation Printing
Metal Wrap Through (MWT) Benefits

- No busbar on the front side
- Less paste deposit (up to 30% saving)
- Electrical contact only on the back side
- Higher short-circuit current density
- Higher $V_{oc}$ (recombination current is reduced by lower metallized area)

Busbar shading 2%
Finger shading 5%

Efficiency gain of 0.3-0.5% absolute is observed
≥ 1% Efficiency gain at module level

Source: S.W. Glunz, Advances in OptoElectronics Volume 2007, Article ID 97370
# Applied Baccini MWT Distinctive Solutions

<table>
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<th>Laser Holes Drilling</th>
<th>p and n-contacts Metallization</th>
<th>I-V Testing</th>
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## Laser Holes Drilling
- [Image]

## p and n-contacts Metallization
- [Image]
- **Unique Galvo head plus Rotary table**
  - Proprietary Closed Loop Control guarantees high accuracy and drift compensation
- **Proven metallization**
  - Full control of the vias filling
  - Prevention of the cell contaminations
  - No need for paper on nest
- **Proven back contact probing**
  - Best IV measurement repeatability

## I-V Testing
- [Image]
Via Printing

- Filling vs. via resistance
- Corner overlay drives the via resistance
- Optimized cell efficiency

Today: HVM

- Same Breakage rate of standard cell
- Via Filling ratio > 98%
- Average Efficiency repeatability ± 0.05% absolute (dynamic mode)

1.5 Million cells processed

Cell/month  Cumulative

Aug-12  Sep-12  Oct-12
Advanced Passivation
Advanced Cell Structures For High Efficiency
Need 2-Side Passivation Solutions

**IBC**
Interdigitated Rear Point Contact

**PERC**
Passivated Emitter Rear Point Contact

**Implanted**
Passivated Implant Rear Point Contact

**n-Type**
Metal Wrap Through

**PERT**
Passivated Emitter Rear Point Contact

**Totally Diffused**
Two-Side Passivation

**PERC Structure**

- Reduces backside recombination losses
  - Contribute to ~ 45% of efficiency gain
  - Low surface recombination velocity
  - Negative fixed charge Al$_2$O$_3$ film repels electrons

- Improves backside reflection
  - Contributes to ~ 55% of efficiency gain
  - High back surface reflection of AlO/SiN (~90%) vs Al (65%)

**Cell Efficiency Gains from Backside Passivation**

*(Longer wavelength light capture)*
P Type Mono-Si PERC

Device Performance

**IV Curve**

- **Champion pMono Cell**
  - $J_{SC}$ (mA/cm²): 37.1
  - $V_{OC}$ (mV): 638
  - FF (%): 79.5
  - Eta (%): 18.83
- **Ref Cell**
  - $J_{SC}$ (mA/cm²): 37.1
  - $V_{OC}$ (mV): 638
  - FF (%): 79.5
  - Eta (%): 18.83
- **PERC**
  - $J_{SC}$ (mA/cm²): 38.5
  - $V_{OC}$ (mV): 648
  - FF (%): 78.7
  - Eta (%): 19.62

**Quantum Efficiency / Reflectance**

- Red response benefit from lowered recombination and higher reflection
- Significant enhancements in IR response with backside passivation
- Long wavelength gains transfers to module

**Demonstrates >0.6 efficiency gain with backside passivation on p-type mono cSi**

Wijekoon et.al. 27th EU PVSEC (2012)
Concluding Personal Observations

- End market continues to grow
- PV cell/module producers are becoming more sophisticated in valuing technology improvements
- A relentless drive to improve baseline technology (*another 5W or go home!*)
- Improved baseline technology and reduced costs raises the bar for disruptive technologies, but…
  - Technology and brand differentiation will become larger component of many company business plans
  - Cost structure of baseline technology will be migrated to the high-efficiency potential of n-type material