Process Integration for 2.5D/3D – A Few Steps from the Summit

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Event:
Date: June, 2012
Presentation Outline

- Early Engagements to Industry Adoption
  - Years in perspective, 2008-12

- 2.5D/3D TSV Process Flow / Integration
  - Via-Middle process integration
  - Technology extendibility to smaller TSVs
  - Interposer TSV oxide liner and fill window
  - Via-Reveal process integration
  - Making TSVs affordable

- 2.5D Interposer Copper Interconnect
  - Dual damascene wiring segment/solutions
  - Leverage hardware/processes

- Summary

End Markets: Mobile, Network/Telecom, Gaming/Computing
**TSV Process Flows**

**Via-Middle / Via-Reveal**
- TSV Etch
- CVD Oxide Liner
- PVD Barrier/Seed
- Copper Plating
- CMP Cu
- Edge Trim
- Temporary Bond
- Grind
- CMP Si
- Dry Recess Etch
- CVD Nitride/Oxide
- CMP Oxide

**Up to 400°C Processes**

**Interposer**
- TSV Etch
- CVD Oxide Liner
- PVD Barrier/Seed
- Copper Plating
- CMP Cu
- Edge Trim
- Temporary Bond
- Grind
- CMP Si
- Dry Recess Etch
- CVD Nitride/Oxide
- CMP Oxide

**Below 200°C Processes**

**Via-Last**
- Edge Trim
- Temporary Bond
- Grind
- CMP Si
- CVD Nitride/Oxide
- TSV Etch
- CVD Oxide Liner
- Oxide Bottom Etch
- PVD Barrier/Seed
- Copper Plating
- CMP Cu
TSV Via-Middle Characterized Within Integrated Framework

**CMP Cu**
- Low ILD loss (<10nm)
- Accurate end point and profile control
- Good post-CMP topography

**Etch**
- TSV profile, low scallop
- Depth uniformity
- High ER / selectivity

**CVD Liner**
- High step-coverage, film quality inside TSV
- E-test properties, low leakage ($V_{bd}$), reliability (TDDB), Cu outdiffusion

**ECD Cu**
- Void-free fill, rate, stability
- Low overburden
- Low Cu pumping- Chem., Grain

**PVD CuBS**
- Hi step-coverage (Ta, Ti, Cu)
- Gap-fill co-optimization

Via-Middle integration achieved at customer sites, challenges remain with narrow TSVs

*All SEMs Source: Applied Materials*
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- **Summary**
Conformal Oxide Liner and Wide ECD Fill Window (10x100um)

Invia Liner (2.5kA)

Iso TSV (Pitch~80um)

Dense TSV (Pitch~20um)

Wafer Center

Wafer Edge

Step Coverage ~105%

Conformal liner and good fill achieved on wide inspection range

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Via-Reveal Process Integration Framework

(a) CMP Si
- Improves WIW TTV and WTW repeatability
- Metrology & EP control
- Advanced clean
- Stress relief

(b) Si Recess Etch
- Selectivity, reduced defects
- Etch rate
- Predictive TTV control

(c) CVD Passivation (180°C)
- Stress tuning, Bow
- Seam-free, interfacial adhesion

(d) CMP SiOx
- End-point control
- Tunable topography
- Mechanical integrity of exposed TSVs with dielectric insulation

Optimize clean process for improved CVD film interface

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Leverage via-middle/Via-reveal processes and hardware for Interposer TSV and dual-damascene fabrication
Summary

- TSV feature size converging near 5x50um at Logic/Foundry/Memory for via-middle and 10x100um for Interposer

- Via-middle/via-reveal integration characterized within integrated framework and collaboration with industry eco-system

- Developments show promise to extend oxide liner, barrier/seed and ECD to smaller size ~2x40um TSVs

- Driving multiple approaches for Interposer interconnect fabrication while leveraging common TSV hardware platform
Turning innovations into industries.